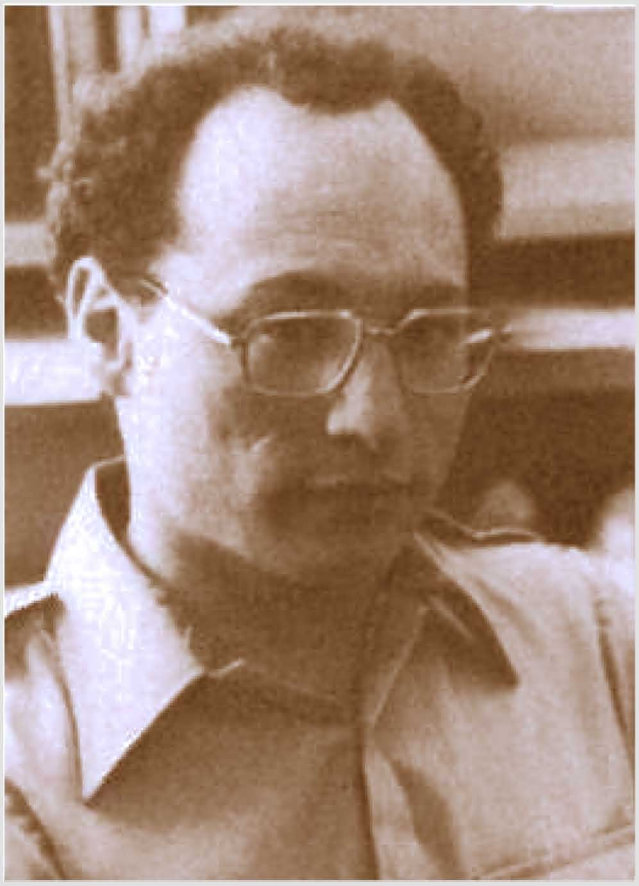
A Tribute to Jim Williams

National Semiconductor Corporation
Application Notes



Circuitry for Inexpensive Relative Humidity Measurement

National Semiconductor
Application Note 256
August 1981

Of all common environmental parameters, humidity is perhaps the least understood and most difficult to measure. The most common electronic humidity detection methods, albeit highly accurate, are not obvious and tend to be expensive and complex (See Box). Accurate humidity measurement is vital to a number of diverse areas, including food processing, paper and lumber production, pollution monitoring and chemical manufacturing. Despite these and other applications, little design oriented material has appeared on circuitry to measure humidity. This is primarily due to the small number of transducers available and a generally accepted notion that they are difficult and expensive to signal condition.

Although not as accurate as other methods, the sensor described by the response curve (*Figure 1*) is inexpensive and provides a direct readout of relative humidity. The curve reveals a close exponential relationship between the sensor and relative humidity spanning almost 4 decades of resistance. Linearization of this curve may be accomplished by taking the logarithm of the resistance value and utilizing breakpoint approximation techniques to minimize the residual non-linearities. A further consideration in signal conditioning is that the manufacturer specifies that no significant DC current component may pass through the sensor. This device must be excited with an unbiased AC waveform to preclude detrimental electrochemical migration. In addition, it has a 0.36 RH unit/°C positive temperature coefficient. The sensor is a chemically treated styrene copolymer which has a surface layer whose resistivity varies with relative humidity. Because the humidity sensitive portion of the sensor is at its surface, time response is reasonably rapid and is on the order of seconds.

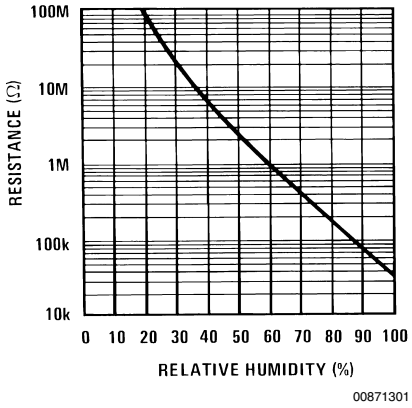


FIGURE 1. Phys-Chemical Research Corp. Model PCRC-55 Humidity Sensor

A block diagram of the concept chosen to instrument the sensor appears in *Figure 2*. An amplitude stabilized square wave which is symmetrical about zero volts is used to provide a precision alternating current through the sensor, satisfying the requirement for a zero DC component drive. The current through the sensor is fed into a current sensitive (e.g. the input is at virtual ground) logarithmic amplifier, which linearizes sensor response. The output of the logarithmic amplifier is scaled, rectified and filtered to provide a DC output which represents relative humidity. Residual non-linearity due to the sensors non-logarithmic response below RH = 40% is compensated by breakpoint techniques in this final stage.

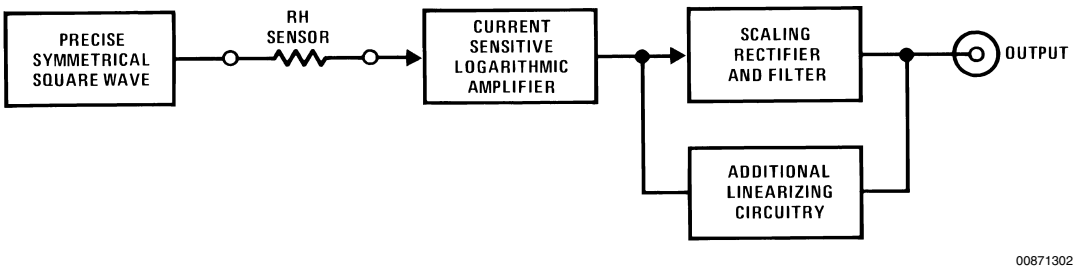
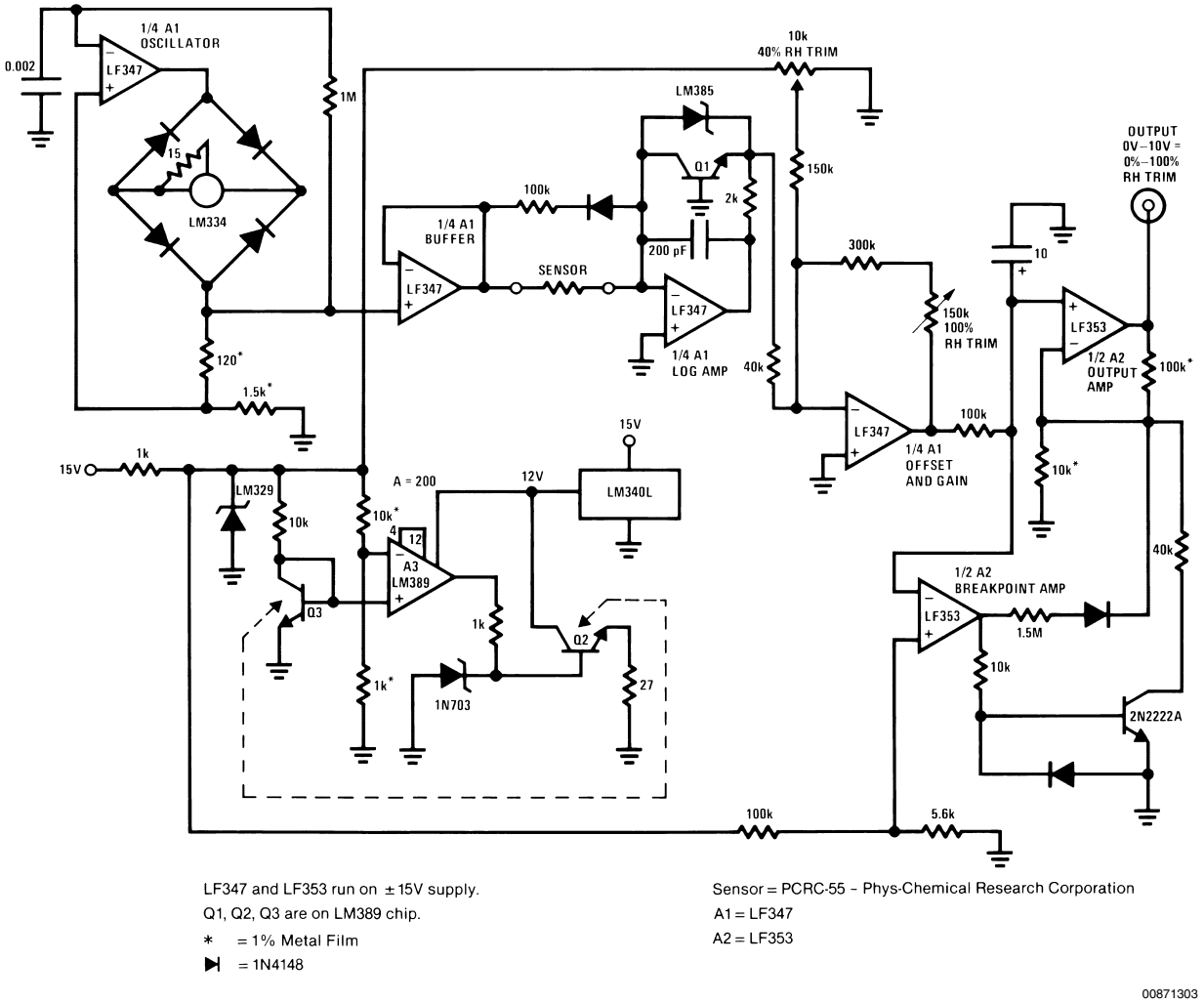


FIGURE 2.

The detailed circuitry appears in *Figure 3*. It is worth noting that the entire function described in *Figure 2* requires a small number of inexpensive ICs. This is accomplished by novel circuitry approaches, especially in the design of the logarithmic amplifier. The stabilized symmetrical square wave is generated by A1, ¼ of an LF347 quad amplifier. A1 is set up in a positive feedback configuration, causing it to oscillate. The output of A1 is current limited and clamped to ground for either polarity output by the LM334 current source diode bridge combination. The LM334 is programmed by the 15Ω resistor to current limit at about 5 mA. This forces the voltage across the 120Ω–1.5 kΩ resistor string to stabilize at about ±8V. Each time A1's output changes state the charging current into the 0.002 µF capacitor reverses, causing the amplifier to switch again when the capacitor reaches a threshold established by the 120Ω–1.5 kΩ divider (waveforms, *Figure 4*). This circuit's output is buffered by the A1 follower. The amplitude stability of the waveform is dependent upon the +0.33%/°C temperature coefficient of the LM334. This T.C. has been intentionally designed into the LM334 so that it may be used in temperature sensing and compensation applications. Here, the negative 0.3%/°C tem-

perature dependence of the humidity sensor is reduced by more than an order of magnitude by the LM334's T.C. and thermally induced inaccuracy in the humidity sensor's response drops out as an error term. In practice, the LM334 should be mounted in proximity to the humidity sensor. The residual −0.03%/˚C temperature coefficient is negligibly small compared to the sensors ±1% accuracy specification.

The output square wave is used to drive current through the sensor and into the summing junction of another ¼ of A1, which is connected as a logarithmic amplifier. On negative cycles of the input waveform the transistor (Q1) in the feedback loop provides logarithmic response, due to the well known relationship between V_{BE} and collector current in transistors. During positive excursions of the input waveform the diode provides feedback to the amplifier's summing junction. In this manner the summing junction always remains at virtual ground while the input current is expressed in logarithmic form by the negative going square wave at the transistor emitter. Since the summing junction is always at ground potential the sensor sees the required symmetrical drive (waveforms, *Figure 5*).



LF347 and LF353 run on ±15V supply.
Q1, Q2, Q3 are on LM389 chip.
* = 1% Metal Film
▶| = 1N4148

Sensor = PCRC-55 - Phys-Chemical Research Corporation
A1 = LF347
A2 = LF353

00871303

FIGURE 3.

The output of this stage is fed to another ¼ of A1. This amplifier is used to sum in the 40% RH trim and provide adjustable gain to set the 100% RH trim. The output is filtered to DC and routed to one half of A2, an LF353, which unloads the filter and provides additional gain and the final output.

The other ½ of A2 is used to compensate the sensor departure from logarithmic conformity below 40% RH (*Figure 1*). This is accomplished by changing the gain of the output amplifier for RH readings below 40%. The input to the output amplifier is sensed by the breakpoint amplifier. When this input goes below RH = 40% (about 0.36V at the output amplifiers "+" terminal) the breakpoint amplifier swings positive. This turns on the 2N2222A, causing the required gain change to occur at the output amplifier. For RH values above 40% the transistor is off and the circuits linearizing function is determined solely by the logarithmic amplifier.

In logarithmic configurations such as this, Q1's DC operating point will vary wildly with temperature and the circuit normally requires careful attention to temperature compensation, resulting in the expense associated with logarithmic amplifiers. Here, A3, an LM389 audio amplifier IC which also contains three discrete transistors, is used in an unorthodox configuration to eliminate all temperature compensation re-

quirements. In addition, the cost of the log function is reduced by an order of magnitude compared to available ICs and modules. Q3 functions as a chip temperature sensor while Q2 serves as a heater. The amplifier senses the temperature dependent V_{BE} of Q3 and drives Q2 to servo the chip temperature to the set-point established by the 10 kΩ–1 kΩ divider string. The LM329 reference ensures power supply independence of the temperature control. Q1 operates in this tightly controlled thermal environment (typically 50˚C) and is immune to ambient temperature shifts. The LM340L 12V regulator ensures safe operation of the LM389, a 12V device. The zener at the base of Q2 prevents servo lock-up during circuit start-up. Because of the small size of the chip, warm-up is quick and power consumption low. *Figure 6* shows the thermal servo's performance for a step function of 7˚C change in set-point. The step is shown in trace A while the LM389 output appears in trace B. The output responds almost instantaneously and complete settling to the new set-point occurs within 100 ms.

To adjust this circuit, ground the base of Q2, apply circuit power and measure the collector potential of Q3, at known room temperature. Next, calculate what Q3's collector potential will be at 50˚C, allowing –2.2 mV/˚C. Select the 1k value to yield a voltage close to the calculated 50˚C potential at the LM389's negative input. This can be a fairly loose trim, as the exact chip temperature is unimportant so long as it is stable. Finally, unground Q2's base and the circuit will servo. This may be functionally checked by reading Q3's collector voltage and noting stability within 100 µV (0.05˚C) while blowing on A3.

To calibrate the circuit for RH, place a 35 kΩ resistor in the sensor position and trim the 150 kΩ pot for an output of 10V. Next, substitute an 8 MΩ resistor for the sensor and trim the 10k potentiometer for an output of 4V. Repeat this procedure until the adjustments do not interfere with each other. Finally, substitute a 60 MΩ resistor for the sensor and select the nominal 40 kΩ value in the breakpoint amplifier for a reading of RH = 24%. It may be necessary to select the 1.5 MΩ value to minimize "hop" at the circuit output when the breakpoint is activated. The circuit is now calibrated and will read ambient relative humidity when the PCRC-55 sensor is connected.

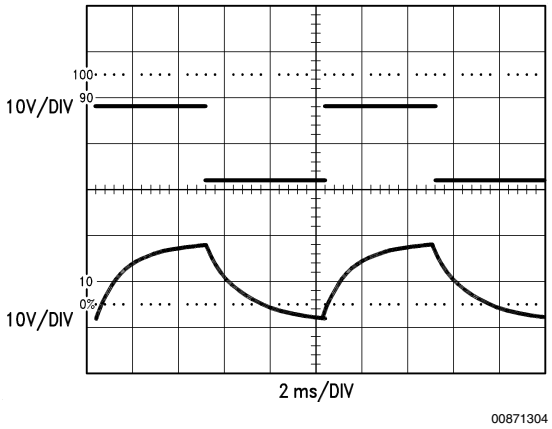


FIGURE 4.

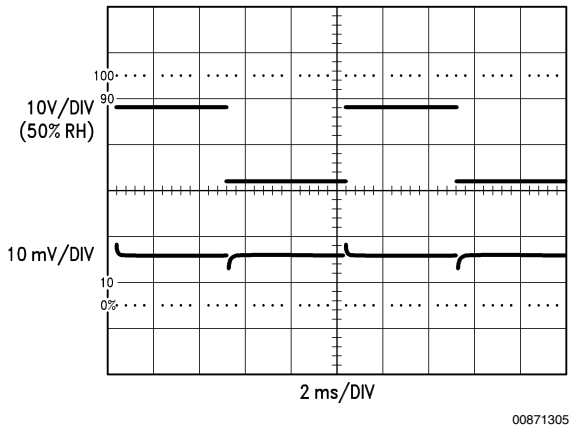


FIGURE 5.

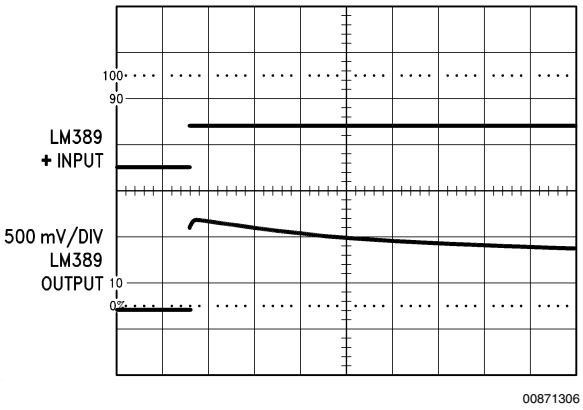


FIGURE 6.

Humidity

Humidity is simply water gas. In air the humidity may vary from zero percent for 90˚F dry air to as much as 4.5 percent for heavily water laden air at 90˚F. The amount of water air will hold is dependent upon temperature. *Relative* humidity is an expression denoting the ratio of water vapor in the air to the amount possible in saturated air at the same temperature.

Some of the more common ways of expressing humidity related information include wet bulb temperature, dew point and frost point. Wet bulb temperature refers to the minimum temperature reached by a wetted thermometer bulb in a stream of air. The dew point is the point at which water saturation occurs in air. It is evidenced by water condensation. When temperatures below 0˚C are required to produce this phenomenon it is called the frost point.

Other measurements and ways of expressing humidity exist and are useful in a variety of applications. For additional information consult the bibliography.

Bibliography

1. "Humidity Sensors"—brochure describing Models PCRC-11 and PCRC-55 Relative Humidity Sensors. Phys-Chemical Research Corp.; New York.
2. "Humidity Measurement"—*Instrumentation Technology*; reprint P. R. Wiederhold. Available from General Eastern Corp.; Watertown, Mass.
3. "Handbook of Transducers for Electronic Measuring Systems"—Norton, Harry N.; Prentice Hall, Inc.; 1969.
4. "Electric Hygrometers"—Wexler, A.; NBS Circular 586; NBS Washington, D.C. 1957.
5. "An elegant 6-IC circuit gauges relative humidity"—Williams, James M.; *EDN Magazine*, June 5, 1980.

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A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter

National Semiconductor
Application Note 260
January 1981

By combining an ''inferior'', 20 year old A/D conversion technique with a microprocessor, a developmental A/D converter achieves 1 part-per-million (20-bit) linearity. The absolute accuracy of the converter is primarily limited by the voltage reference available. The precision achieved by the unlikely combination of technologies surpasses conventional approaches by more than an order of magnitude. The approach used points the way towards a generation of ''smart'' converters, which would feature medium to high resolution (12 bits and above) with high accuracy over extended temperature range. The conversion technique employed, while slow speed, suits transducer based measurement systems which require high resolution over widely varying conditions of time and temperature. In addition, extensions of the basic converter have achieved 15-bit digitization of signal inputs of only 30 mV full-scale with no sacrifice in linearity or stability. This offers the prospect of an ''instrumentation converter'' which could interface directly with low level analog signals.

One of the many A/D techniques utilized in the late 50's and early 60's was the single-slope-integrating converter. One form of this circuit compares a linear reference ramp to the unknown voltage input (see About Integrating Converters and Capacitors). When the ramp potential crosses the unknown input voltage a comparator changes state. The length of time between the start of the ramp and the comparator changing state is proportional to the input voltage. This length of time is measured digitally and presented as the converter output. The inherent strengths of this type of converter are simplicity and high linearity. Although single-slope-integrators were used in early A/Ds and voltmeters their dependence on an integrating capacitor for stability was considered an intolerable weakness. The advent of the dual-slope converter (see About Integrating Converters and Capacitors) solved the problem of integrating capacitor drift with time and temperature by error cancellation techniques. In a dual-slope converter the output represents the ratio of the time required to integrate the unknown voltage for a fixed time and then, using a reference voltage of opposing polarity, measures the amount of time required to get back to the original starting point (see About Integrating Converters and Capacitors). The technique eliminates capacitor drift as an error term.

Limitations of Dual-Slope Converters

The dual-slope converter, and variants on it, have been refined to a point where 16 and 17-bit resolution units are available. A primary detriment to linearity in these converters is a parasitic effect in capacitors called dielectric absorption. Dielectric absorption can be conceptualized as a slight hysteresis of response by the capacitor to charging and discharging. It is influenced by the recent history of current flow in the capacitor, including the magnitude, duration and direction of current flow (see About Integrating Converters and Capacitors).

The nature of operation of dual-slope and related converters requires the instantaneous reversal of current in the integrating capacitor. This puts a substantial burden on the dielectric absorption characteristics of the capacitor. Although dual-slope and related techniques go far to cancel zero and full-scale drifts, residual non-linearity exists due to the effects of dielectric absorption. In addition to non-linearity, dielectric absorption can also cause the converter to give different outputs with a fixed input as the conversion rate is varied over any significant range. Various compensation arrangements are employed to partially offset these effects in present converters. What is really needed for high precision, however, is a conversion scheme which inherently acts to cancel the effects of dielectric absorption, while simultaneously correcting for zero and full-scale drifts.

Overcoming Dual-Slope Limitations

Figure 1 diagrams a converter which meets the requirement noted previously. In this arrangement a microprocessor is used to sequentially switch zero, full-scale reference and EX signals into one input of a comparator. The other comparator input is driven from the ramp output of an operational amplifier integrator. With no convert command applied to the microprocessor, the circuit is at quiescence. In this state the microprocessor sends a continuous, regularly spaced signal to the integrator reset switch. This results in a relatively fixed frequency, period and height ramp at the amplifier's output. This relationship never changes, regardless of the converter's operating state. In addition, the time between ramps is lengthy, resulting in an effective and repeatable reset for the capacitor. When a convert command is applied, the microprocessor switches the comparator input to the zero position, waits for the next available ramp and then measures the amount of time required for the ramp to cross zero volts. This information is stored in memory. The microprocessor then repeats this procedure for the full-scale reference and EX switch positions. With all this information, and the assumption that the integrator ramps are highly linear, the absolute value of EX is determined by the processor according to the following equation.

$$EX = \frac{[C_{EX} - C_{ZERO}]}{[C_{FULL\text{-}SCALE} - C_{ZERO}]} \times K\ \mu V$$

where C = count obtained

and K = a constant, typically 10^7

After this equation is solved and the answer presented as the converter's output, the conversion is complete and the microprocessor is ready to receive the next convert command.

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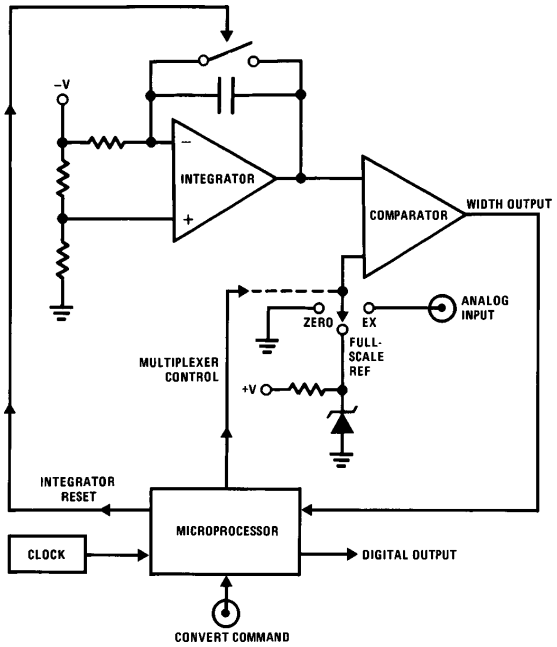

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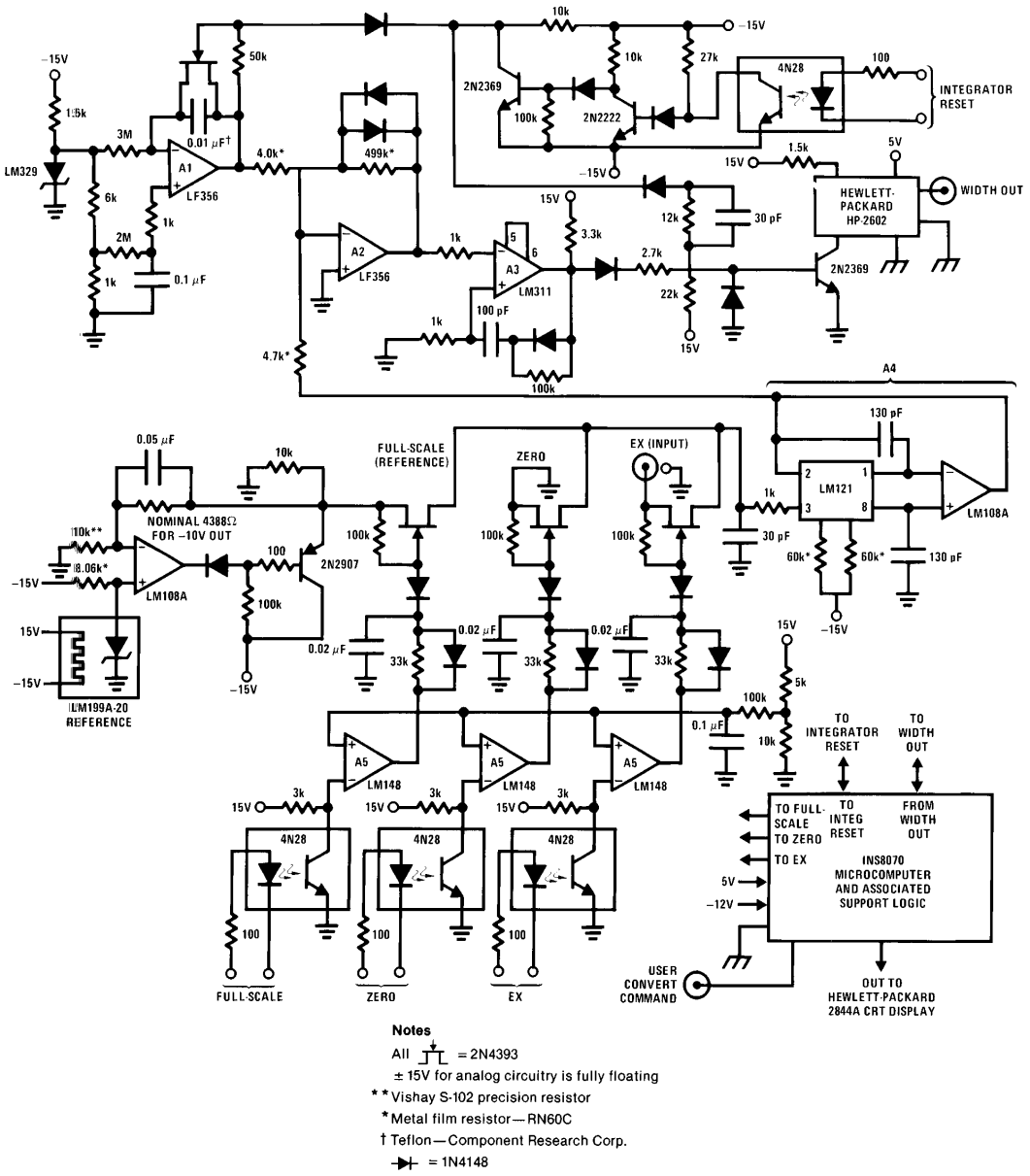
FIGURE 1

The converter arrangement shares many of the characteristics of a dual-slope type and also provides some significant advantages. The key operating features are as follows:

1. It continuously corrects for zero and full-scale drift in all components in the A/D circuit, regardless of changes in time or temperature. The primary limitation on accuracy is the stability of the full-scale reference. The zero signal is derived through conventional high quality grounding technique. These features are similar to a dual-slope converter.
2. Because the integrating capacitor is always charged in a continuous pattern and in the same direction, the dielectric absorption induced error will be relatively small, constant, and will appear as an offset term. This offset term will be removed during the microprocessor's calibration cycle. This feature is unique to this converter and is the key to high linearity.
3. The comparator always sees the ramp voltage approaching the trip point from the same direction and at the same slew rate, regardless of operating conditions. This helps maintain repeatability at the trip point in the face of noise and gain-bandwidth limitations in the comparator.
3. Unlike a dual-slope, this converter has no inherent noise rejection capability. The EX input signal is directly coupled to the comparator input with no filtering. This is a decided disadvantage because most ''real world'' signals require some smoothing. If a filter was placed at the input substantial time lag due to settling requirements would occur. This is unacceptable because the converter relies on short time intervals between multiplexer states to effectively cancel drift. The solution is to use the microprocessor to filter the signal digitally, using averaging techniques.

Filling Out the Blocks

The detailed schematic diagram of the prototype 20-bit linear A/D conveter is shown in *Figure 2*. For clarity, the details of the INS8070 microprocessor and its associated logic are shown in block from. Note that the entire analog section of the converter is fully floating from the digital section to eliminate noise due to digital current spiking and clock noise. The analog and digital circuits communicate via opto-isolators. The full-scale reference for the converter is provided by the LM199A-20-LM108A combination. This circuit, using the components specified, will typically deliver 0.25 ppm/°C performance with drift of several ppm per year. The accuracy to which this reference can be maintained is the primary limitation on absolute accuracy in this converter. The output of this reference is fed to an FET-switched multiplexer which also receives the EX and zero signals. Because all these sources are at low impedance, and only one is switched on at a time, the leakage and ON resistances do not contribute significant error. The A4 combination provides a low bias current unity gain follower with greater than 1,000,00:1 (120 dB) of CMRR, preserving converter linearity. Drifts in this follower are not significant because they will be cancelled out by the microprocessor's calibration cycle. The microprocessor's digital commands to the FET switches are received by the 4N28 opto-isolators. The LM148 quad op-amp (A5) is used to generate the voltage swing necessary to control the FET switches. The discrete components at each amplifier output are used to generate one-way time delays to give the FET switches break-before-make action. This prevents cross talk between the zero, full-scale reference and EX sources.



Notes

All ⊣⊢ = 2N4393

± 15V for analog circuitry is fully floating

** Vishay S-102 precision resistor

* Metal film resistor—RN60C

† Teflon—Component Research Corp.

⊣▶⊢ = 1N4148

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FIGURE 2

Another FET is used to reset the integrator and is biased by a "brute-force" level shifting-edge speed-up network formed by the 2N2222-2N2369 pair. A 4N28 opto-isolator biases this network when it receives the reset signal from the INS8070 processor. A1, an LF356, has its "+" input biased at about negative 1V, ensuring that the ramp will start far enough below ground to determine a true zero signal.

The requirement for a comparator with 1 ppm (1 LSB at 20 bits = 1 ppm) of trip point noise cannot be met by any standard device. At 10V full-scale this is only a 10 μV LSB. The 50 ms-10V ramp's relatively slow slew rate means that the gain-bandwidth and noise characteristics of a standard differential input comparator will cause considerable uncertainty at the trip point. Also, as the common-mode voltage at which the ramp vs EX crossing occurs changes, the trip point of the comparator will shift, introducing overall non-linearity.

These problems are addressed by the A2-A3 configuration, which forms a high precision comparator. A4's negative output is resistively summed with the positive output of the A1 ramp at A2. A2 normally operates at a low gain due to the diode bounding in its feedback loop. When the currents produced by the ramp potential and A4's output very nearly balance the potential at A2's summing junction will go low enough so that A2 comes out of bound and operates at a gain determined by the 499k feedback resistor (about 100). A2 remains in this high-gain state as long as the ramp and A4 output caused currents are nearly equal. As the ramp continues in its positive going direction the current into A2's summing junction will go to zero and then move positive until the A2 output bounds negative. The output of A2 drives A3, an LM311 comparator which is set up as a zero crossing detector. The components in the positive feedback path at A3 insure a sharp transition. *Figure 3* shows the waveforms of operation. The ramp (a) is shown in highly expanded form. The A2 output (b) can be seen to come cleanly out of diode-bound just before the ramp balances A4's output and then return to bound after the crossing occurs. Waveform (c) is A3's output. The A2 pre-amplifier makes the A3 comparator's job much easier in a number of ways. It amplifies the voltage difference of the two signals to be compared by a factor of 100. This knocks down the effect of A3's input uncertainties. It also produces an apparent 100 fold increase in the ramp slew rate at the trip point. This means A3 spends that much less time with its inputs nearly balanced in an uncertain and noise sensitive condition. Finally, A2 presents the difference signal as a single ended zero crossing signal. This eliminates errors due to changing common-mode voltages that a differential comparator's input would face. Such errors would manifest themselves as overall converter non-linearity.

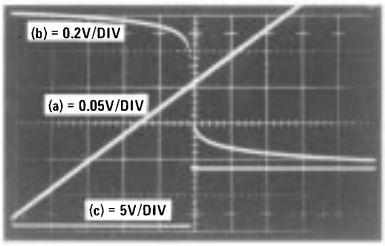

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FIGURE 3

The output of the A3 comparator feeds a 2N2369 transistor, which functions as a level shifter-gate. This transistor gates out that portion of the width output pulse which would be due to the length of the integrator reset pulse. The 2N2369, a low storage capacitance device, provides high speed, even in the relatively slow common emitter configuration. The HP-2602 high speed opto-coupler transmits the width information to the digital circuitry.

Converter Performance and Testing

Figure 4 shows the convert at work. A complete conversion cycle is captured in the photograph. Waveform (a) is the integrator reset out of the INS8070. (b) is the ramp at A1's output. Waveform (c) is the multiplexer output at A4, showing the zero, full-scale reference and EX states. For each state ample time is allowed before the ramp begins. The width output is shown in waveform (d).

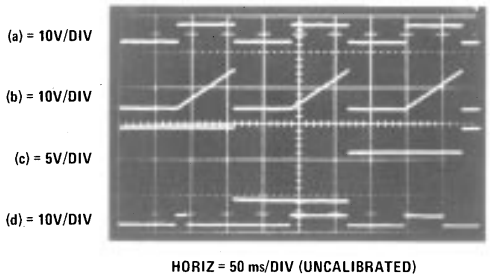

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FIGURE 4

The converter was tested with the arrangement shown in *Figure 5*. The Kelvin-Varley voltage divider, a primary standard type, has a guaranteed linearity of within 1 ppm. The LM11 op amp provides a low bias current, low drift follower to unload the Kelvin divider's output impedance. Because the LM11 gives greater than 120 dB common-mode rejection, its voltage output should track the linearity of the Kelvin divider. To test this the LM11 was adjusted for offset null and a battery-powered μV meter connected between its inputs. 20-bit linear (1 ppm) transfer characteristics were verified by running the Kelvin divider through its range and noting less than 10 μV (1 LSB at 10V full-scale) shift under all conditions. Then, the converter reference was used to drive the Kelvin divider input and the LM11 output to the EX input of the A/D converter.

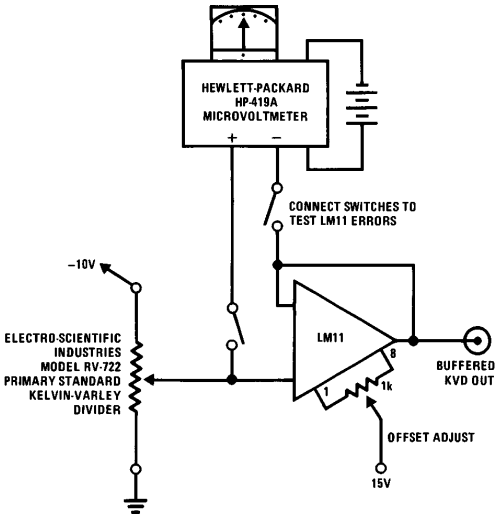

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FIGURE 5

A typical output on the Hewlett-Packard 2644A CRT terminal display is shown in *Figure 6*. For each convert command to the INS8070 the number of counts of zero, full-scale reference and EX are shown along with the final computed answer. Note that the final count is computed to one part in ten million and the last digit is insignificant. Note also that the 4 final counts are all within ± 1 ppm . . . despite the fact that they were individually spaced almost 1 hour apart in a varying thermal environment. Linearity of the converter over a 10V range was verified at 10 points by varying the MSB of the Kelvin divider. Although the prototype converter takes 300 ms to complete a cycle, faster speed is attainable by increasing the 20 MHz clock rate. Perhaps more practically, higher conversion speeds at lower resolutions are easily attainable by simply shortening the ramp time. The converter output word length and conversion time may be varied over a wide dynamic range by juggling clock speed and ramp time.

TL/H/5625–6

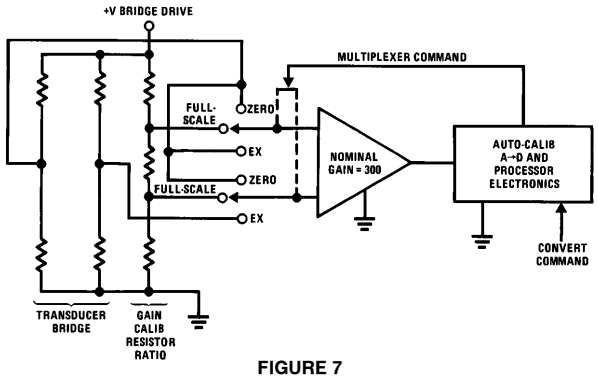
FIGURE 6

Although demonstrating a 20-bit converter is useful, there are other applications which do not require this degree of precision. The basic technique is readily adaptable to the practical solution of common transducer and other low-level interface problems. *Figure 7* shows the block diagram of the converter used to generate a 15-bit output directly from a 30 mV full-scale input. In this application the converter input is a differential input amplifier with a nominal gain of 300. Note that the amplifier's offset and gain drift will be cancelled by the microprocessor's calibration loop. The EX signal is the output of the transducer bridge. The full-scale reference signal is derived by measuring across the middle resistor of a string which has the same voltage across it as the nominal bridge output for a given bridge drive level. In this manner, even if the bridge drive varies, the gain of the system remains calibrated by ratiometric error cancellation. The zero signal is derived by shorting both amplifier inputs to the common-mode voltage at the bridge output. This system has been built and has maintained 15-bit accuracy over a 75°F temperature range.

Prospective constructors of this converter are advised that construction technique is extremely critical. In order for the converter to operate properly, the greatest care must be taken in grounding, guarding and shielding techniques. Useful sources of information are listed in the References

References

1. ''Grounding and Shielding Techniques in Instrumentation'', R. Morrison; Wiley Interscience.
2. ''Designing Sensitive Circuits? Don't Take Grounds for Granted!'', A. P. Brokaw; EDN, October 5, 1975.
3. ''Input Connection Practices for Differential Amplifiers'', J. H. Hueckel; Neff Inst. Corp.
4. ''Prevent Low Level Amplifier Problems'', J. Williams; Electronic Design, February 15, 1975.
5. ''Signal Conditioning'', Gould Inc., Brush Insts. Div., Cleveland, Ohio.
6. ''On Computing Errors of an Integrator'', T. Miura, et. al; Proc. 2nd ALCA Conf. Strasbourg, France. 1958. Presses Academiques Europeennes, Brussels.
7. ''Comparator I.C. Forms 10-Bit A/D Converter'', J. Williams: Electronics, April 17, 1975.
8. ''Low Cost, Linear A/D Conversion Uses Single-Slope Techniques'', J. Williams: EDN, August 5, 1978.
9. Component Research Corp.—Catalog JB.
10. ''The Secret Life of Capacitors'', ECD Corp., Cambridge, Massachusetts.
11. ''An Analysis of Errors in Single Slope Integrators'', R. A. Eckhardt; S. B. Thesis, M.I.T., 1974.
12. ''Characterization, Measurement and Compensation of Errors in Capacitors . . . a compendium of study, hacks, some good stuff and a few pearls'', J. Williams; Massachusetts Institute of Technology, Cambridge, Massachusetts, 1975.
13. ''Operating and Service Manual — HP3440 D.V.M.''; Hewlett-Packard Co., 1961.



TL/H/5625–7

FIGURE 7

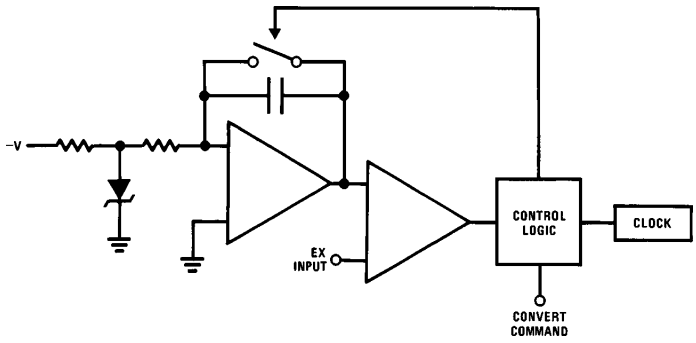
About Integrating Converters and Capacitors

The simplest form of integrating converter is the single-slope type (*Figure A*). In the single-slope unit shown, a linear reference ramp is compared against the unknown input, EX. When the switch across the integrator capacitor is opened, the ramp begins. The time interval between the opening of the integrator reset switch and the comparator changing state (when $E_{RAMP} = EX$) is directly proportional to the value of EX. This converter requires that the integrating capacitor and the clock used to measure the time interval be stable over time and temperature . . . a significant drawback under normal circumstances.

The dual-slope integrator (*Figure B*) overcomes these problems by effectively normalizing the capacitor value and clock rate each time a conversion is made. It does this by integrating the EX input for a pre-determined time. Then, the voltage reference is switched to the integrator input which proceeds to integrate in a negative going direction from the EX slope. The length of time the reference slope requires to get back to zero is proportionate to the EX signal value. These slopes are both established with the same integrating capacitor and measured with the same clock, so both parameters need only be stable over one conversion cycle.

Both of these converters are dependent to varying degrees on capacitor characteristics. The single-slope type requires stability in the capacitor over time and temperature while the dual-slope gets around this limitation. The effects of a phenomenon in capacitors called dielectric absorption, however, have direct impact on dual-slope performance. Dielectric absorption is due to the capacitor dielectric's unwillingness to accept or give up charge instantaneously. It is commonly and simply modeled as a parasitic series RC (*Figure C*) across the terminals of the main capacitor.

If a charged capacitor is discharged, even through a dead short, some degree of time will be required to remove all of the charge in the parasitic capacitance due to the parasitic series resistance. Conversely, some amount of charge will be absorbed by the parasitic capacitor after a charging of the main capacitor has ceased unless the charge source is maintained for many parasitic RC time constants. Various dielectrics offer differing performance with respect to dielectric absorption. Teflon, polystyrene and polypropylene are quite good, while paper, mylar and glass are relatively poor. Electrolytics are by far the worst offenders. Anyone who has received a shock after discharging a high voltage electrolytic in a television set has experienced the effect of dielectric absorption.



TL/H/5625–9

FIGURE A

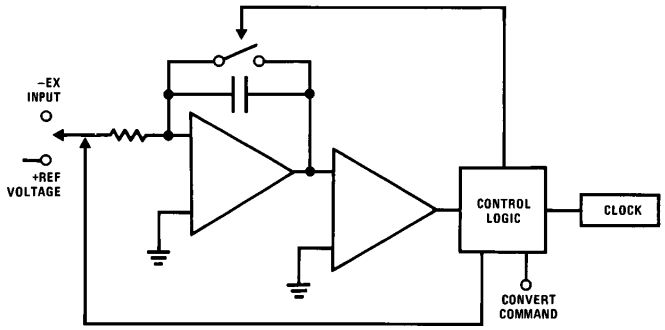
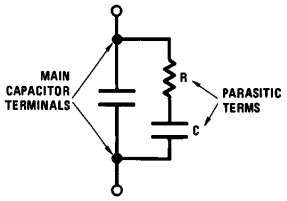


FIGURE B



TL/H/5625–8

FIGURE C

Applying Dual and Quad FET Op Amps

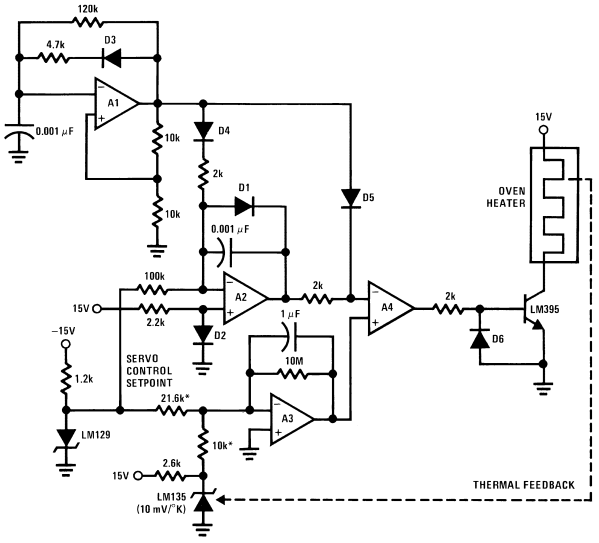
National Semiconductor
Application Note 262
May 1981

The availability of dual and quad packaged FET op amps offers the designer all the traditional capabilities of FET op amps, including low bias current and speed, and some additional advantages. The cost-per-amplifier is lower because of reduced package costs. This means that more amplifiers are available to implement a function at a given cost, making design easier. At the same time, the availability of more amplifiers-per-dollar means that relatively self contained and sophisticated functions can be designed around a single FET dual or quad package. In addition, duals and quads require less board space, fewer bypass capacitors and less power supply bussing. An inventive designer can capitalize on all of these advantages to produce complex circuit functions at low cost. An example is shown in *Figure 1*.

High Efficiency Precision Oven Temperature Controller

In this circuit, a complete, high efficiency pulse width modulating temperature controller is built around a single LF347 package. In *Figure 1*, A1 functions as an oscillator whose output (Trace A, *Figure 2*) periodically resets the A2 integrator output (Trace B, *Figure 2*) back to zero volts. Each time A1's output goes high, a large positive current is forced into A2's summing junction, overcoming the negative current that flows through the 100 kΩ resistor into the LM129 reference. This forces A2's output to head in a negative-going direction ultimately limited by the diode feedback-bound. Another diode provides bias at A2's "+" input to compensate the bound diode and A2's output settles very near zero volts. When the positive output pulse from A1 ends, the positive current into A2's summing junction ceases and A2's output ramps linearly until the next reset pulse.

A3 functions as a current summing servo-amplifier which compares the currents derived from the LM135 temperature sensor and the LM129 reference. In this example A3 operates at a gain of 1000 with a 1 µF capacitor providing 0.1 Hz servo response. A3's output represents the amplified difference between the LM135's temperature and the desired control setpoint, which may be varied by altering the 21.6k value. In this circuit the 21.6k resistor provides a setpoint of 49˚C. A3's output is compared to the ramp output of A2 and A4, which is set up as a comparator. A4's output will only be high during the time A3's output is greater than the ramp voltage. The ramp reset pulse is diode-summed with the ramp output (Trace C, *Figure 2*) at A4 to prevent A4's output from going high during the period of the reset pulse. A4's output biases the LM395 power transistor which switches power to the heater (Trace D, *Figure 2*). If the LM135 sensor is tightly coupled to the heater and the oven is well insulated, this controller will easily hold 0.05˚C over wide excursions of ambient temperature.



01258701

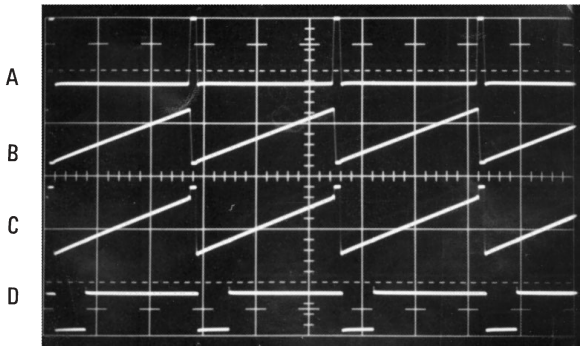
All diodes = 1N4148

* = Low TC, metal-film types

A1-A4 = LF347 quad

FIGURE 1. Connecting appropriate components to an LF347 quad FET op amp IC produces a high efficiency precision oven temperature controller. This design can hold a temperature within 0.05˚C despite wide ambient temperature fluctuations.

High Efficiency Precision Oven Temperature Controller (Continued)



01258702

Trace	Vertical	Horizontal
A	20V/Div	50 µs/Div
B	10V/Div	
C	10V/Div	
D	20V/Div	

FIGURE 2. Oven-controller waveforms from *Figure 1* circuit show A1's oscillator output (Trace A) and A2's integrator output (B) as the latter resets periodically to 0V. Trace C displays A4's ramp input, and (D) indicates the LM395's power input to the oven heater.

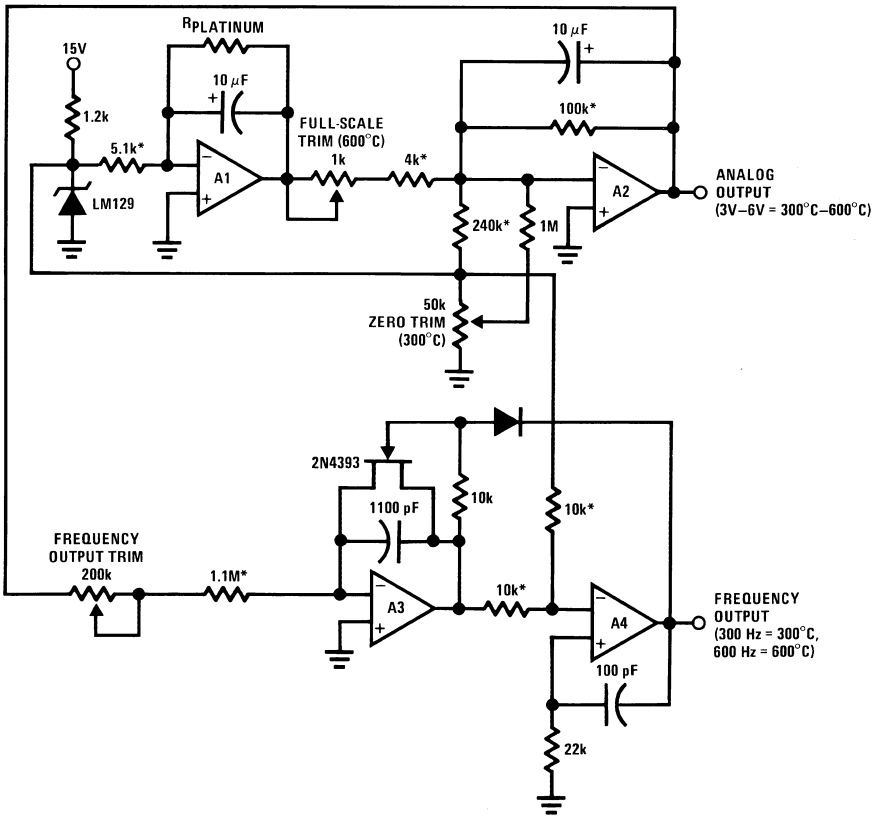
Platinum RTD High Temperature Thermometer with Analog and Digital Outputs

Another temperature related circuit appears in *Figure 3* . In this circuit an LF347 is used to signal condition a Platinum RTD and provide simultaneous analog and frequency outputs. These outputs are accurate to ±1˚C over a range of 300˚C–600˚C (572˚F–1112˚F). Although the circuit maintains linearity over a much wider range the non-linear response of the RTD over wide range is the limitation to accurate, wide range operation (see graph, *Figure 4*).

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LM129 and the 5.1k resistor provide the current reference. Because A1 operates at negative gain the voltage across the sensor is extremely low and self-heating induced errors are eliminated. A1's output potential, which varies with the platinum sensor's temperature, is fed to A2. A2 provides scaled gain and offsetting so that its output will swing from 3.00V to 6.00V for a 300˚C to 600˚C temperature swing at the platinum sensor.

A3 and A4 form a voltage-to-frequency converter which generates a 300 Hz to 600 Hz output from A2's 3V to 6V analog output. A3 integrates in a negative-going direction at a slope which is linearly dependent upon A2's output voltage. A4 compares A3's negative ramp to the LM129's positive reference voltage by current summing in the 10 kΩ resistors. When the negative value of the ramp just exceeds the LM129 voltage A4's output goes positive, turning on the 2N4393 FET and resetting the A3 integrator. AC feedback at A4 causes it to "hang up" in the positive state long enough to completely discharge the integrator capacitor.

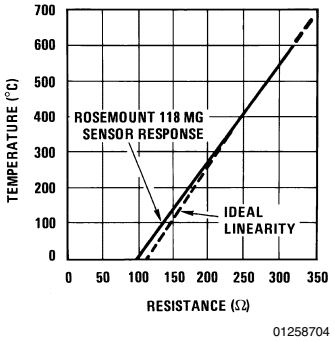
Platinum RTD High Temperature Thermometer with Analog and Digital Outputs (Continued)



RPLATINUM = Rosemount 118 MG
= 214.2Ω at 300˚C (572˚F)
= 318.2Ω at 600˚C (1112˚F)
All diodes = 1N4148
A1-A4 = LF347 quad
* = Low TC, metal-film types

FIGURE 3. Generate simultaneous analog level and frequency outputs using one LF347 package by signal-conditioning a platinum RTD sensor. You can calibrate this high temperature (300˚C to 600˚C) measuring circuit to ±1˚C by using three trimming pots.

Platinum RTD High Temperature Thermometer with Analog and Digital Outputs (Continued)



Temperature(˚C)	Resistance(Ω)
600	318.2
500	284.7
400	249.8
300	219.2
200	177.3
100	139.2
0	100.0

FIGURE 4. A platinum RTD sensor's resistance decreases linearly from 600˚C to 300˚C. Then, from 300˚C to 0˚C, the sensor's resistance deviates from a straight line slope and degrades the *Figure 3* circuit's accuracy beyond ±1˚C.

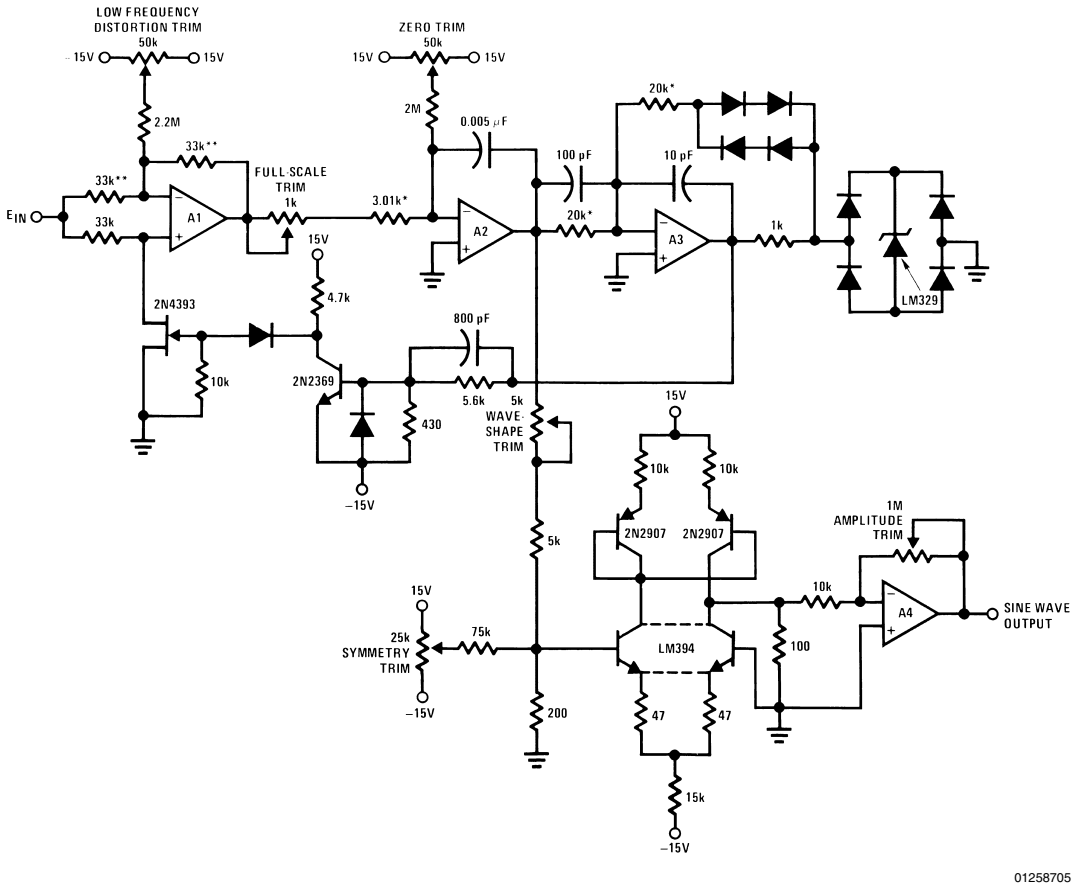
To calibrate this circuit, substitute a high quality decade box (e.g., General Radio #1432-K) for the sensor. Alternately adjust the zero (300˚C) and full-scale (600˚C) potentiometers for the resistance values noted in *Figure 4* until A2's output is calibrated. Next, adjust the 200 kΩ frequency output trim so the frequency output corresponds to the analog value at A2's output.

Voltage Controlled Sine Wave Oscillator

Figure 5 diagrams a very high performance voltage controlled sine wave oscillator which uses a single LF347 package. For a 0V–10V input the circuit produces sine wave outputs of 1 Hz to 20 kHz with better than 0.2% linearity. In addition, distortion is about 0.4% and the sine wave output frequency and amplitude settle instantaneously to a step input change. The circuit's sine wave output is achieved by non-linearly shaping the triangle wave output of a voltage-to-frequency converter.

Assume the 2N4393 FET is on and A1's output has just gone low. With the FET on, A1's "+" input is grounded and A1 functions as a unity gain inverter. In this state its output will be equal to $-E_{IN}$ (Trace A, *Figure 6*). This negative voltage is applied to the A2 integrator which responds by ramping in a positive direction (Trade B, *Figure 6*). This positive-going ramp is compared by A3 to the LM329 7V reference which is contained within its symmetrically bounded positive feedback loop. The paralleled diodes compensate the diodes in the bridge. When the positive-going ramp voltage just nulls out the –7V produced by the LM329, diode bound A3's output goes positive (Trace D, *Figure 6*). The 100 pF capacitor provides a frequency adaptive trim to A3's trip point, aiding V/F linearity at high frequencies by compensating A3's relatively slow response time when used as a comparator. The 10 pF capacitor provides AC positive feedback to A3's positive input (Trace C, *Figure 6*). The positive output of A3 is inverted by the 2N2369 transistor which also has the effect of further shortening A3's response time. It does this by using a heavy feed-forward capacitor in its base drive line. This allows the transistor to complete switching just barely after the A3 output has begun to move! (Trace E, *Figure 6*). The 2N2369's negative output turns off the 2N4393 FET. This lifts A1's "+" input from ground and causes A1 to become a unity gain follower. This forces A1's output to immediately slew to the value of E_{IN}. This causes the A2 integrator to reverse in direction, forming a triangle wave. When A2 ramps far enough negative A3 will again switch and the entire cycle will repeat. The triangle output at A2 is fed to the discrete transistors which form a sine shaper. This configuration uses the logarithmic relationship between collector current and V_{BE} in transistors to smooth the triangle wave. The last amplifier in the quad package provides gain and buffering and furnishes the sine wave output (Trace F, *Figure 6*).

Voltage Controlled Sine Wave Oscillator (Continued)



* = 1% metal-film resistors

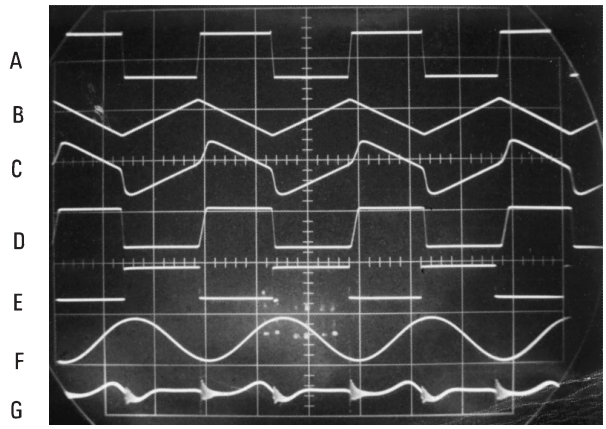
** = Match to 0.1%

All diodes = 1N4148

A1–A4 = LF347 quad

FIGURE 5. An LF347-based voltage-controlled sine wave oscillator combines high performance with versatility. For 0V to 10V inputs, this circuit generates 1 Hz to 20 kHz outputs with better than 0.2% linearity and only 0.4% distortion.

Voltage Controlled Sine Wave Oscillator (Continued)



Trace	Vertical	Horizontal
A	20V/Div	
B	20V/Div	
C	10V/Div	
D	20V/Div	20 µs/Div
E	50V/Div	
F	2V/Div	
G	0.2VDiv	

FIGURE 6. Waveforms from the oscillator shown in *Figure 5* show that upon receiving A1's negative voltage (Trace A), A2 ramps in a positive direction (B). This ramp joins the AC feedback delivered to A3's positive input (C); Trace D depicts A3's positive-going output. This output in turn is inverted by the 2N2369 transistor (E), which turns off the 2N4393 and drives A1's positive input above ground. A2's triangle output also connects to four sine-shaper transistors and A4 and finally emerges as the circuit's sine wave output (F). A distortion analyzer's output (G) shows the circuit's minimum distortion products after trimming.

To calibrate the circuit apply 10V to the input and adjust the wave shape trim and symmetry trim for minimum distortion on a distortion analyzer. Next, adjust the input voltage for an output frequency of 10 Hz and trim the low frequency distortion potentiometer for minimum indication on the distortion analyzer. Finally, alternately adjust the zero and full-scale potentiometers so that inputs of 500 µV and 10V yield respective outputs of 1 Hz and 20 kHz. Distortion products are shown in Trace G, *Figure 6*.

This circuit provides an unusually clean and wide ranging response to rapidly changing inputs, something most sine wave oscillators cannot do. *Figure 7* shows the circuit's response to a 10V ramp applied to the input. The output is singularly clean, with no untoward dynamics, even during or following the high speed reset of the ramp.

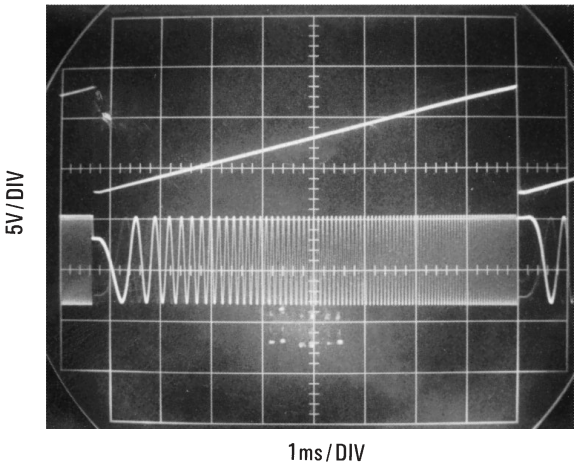


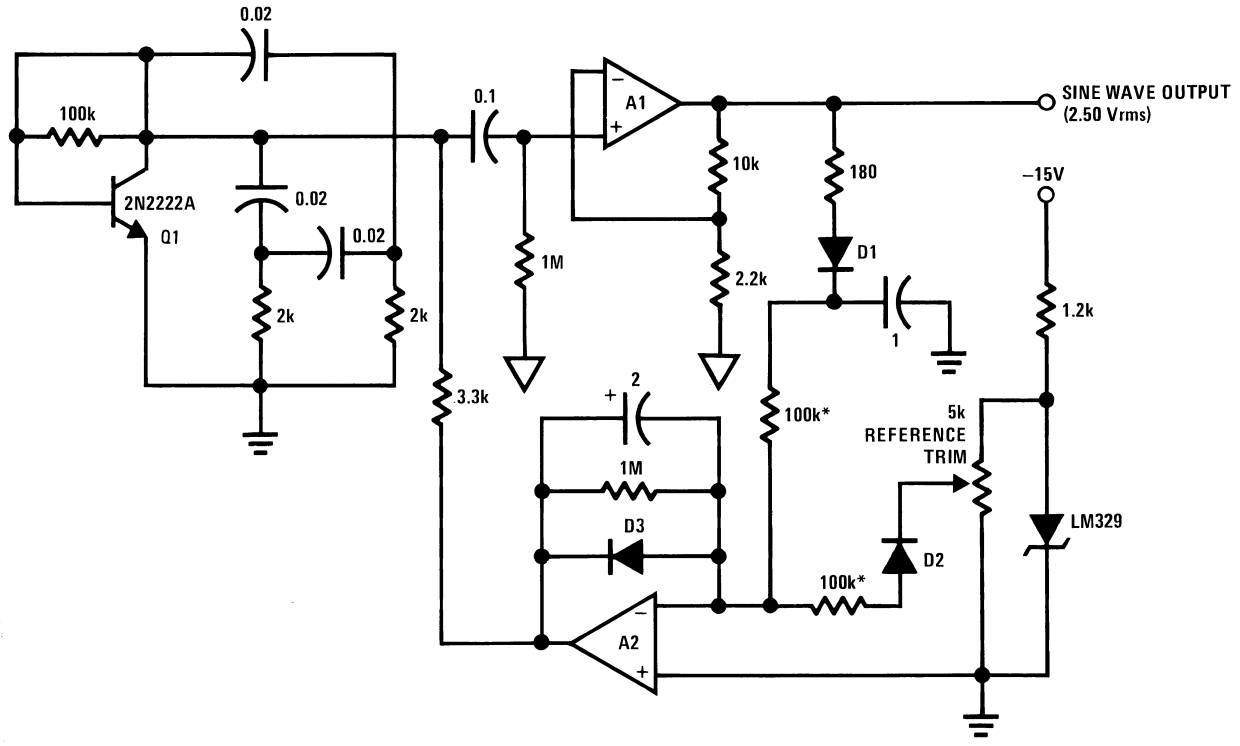
FIGURE 7. Applying a 10V ramp input (top trace) to the *Figure 5* circuit's input produces an extremely clean output (bottom trace) with no glitches, ringing or overshoot, even during or after the ramp's high speed reset.

Sine Wave Voltage Reference

Figure 8 depicts a simple and economical sine wave circuit which provides a fixed 1 kHz output with a precise 2.50 Vrms amplitude. The circuit may be used as inexpensive AC calibration source or anywhere an amplitude stabilized AC source is required. Q1 is set up in a phase shift oscillator configuration and oscillates at 1 kHz. The sine wave at Q1's collector is AC coupled to A1, which has a closed loop gain of about 5. A1's output, which is the circuit's output, is half-wave rectified by the diode and a DC potential appears across the 1 µF capacitor.

This positive voltage is compared by A2 to a voltage derived from the LM329 reference. The diode in the potentiometer wiper arm compensates the rectifying diode. The diode in A2's feedback loop prevents negative voltages from being applied to Q1 (and the feedback capacitor, an electrolytic) on start-up. A2 amplifies the difference of the reference and output signals at a gain of 10. The output of A2 is used to provide collector bias for Q1, completing an amplitude stabilizing feedback loop around the oscillator. The 2 µF electrolytic provides stable loop compensation. The 5 kΩ potentiometer is adjusted so that the circuit output is exactly 2.50V. This output will show less than 1 mV shift for ±5V variation in either supply. Drift is typically 250 µV/°C and distortion is inside 1%.

Sine Wave Voltage Reference (Continued)



All diodes = 1N4148

All capacitors in µF

* = 1% metal-film types

A1, A2 = LF353 dual

FIGURE 8. Reduce parts count and save money by basing this precision sine wave voltage reference on an LF353 dual FET op amp IC. This circuit generates a 1 kHz sine wave at 2.50 Vrms. The 2N2222A transistor functions as a phase-shift oscillator. The A1, A2 combination amplifies and amplitude stabilizes the circuit's sine wave output.

Analog-to-Digital Converter

An extremely versatile integrating analog-to-digital converter appears in *Figure 9*. A single LF347 quad implements the A/D converter which can be either internally or externally triggered. As shown, the converter provides a 10-bit serial output word with a 10 ms full-scale conversion time.

To understand this circuit assume the mode select switch is in the "free run with delay" position and the 2N4393 FET has just been turned off. The A2 integrator, biased from the LM129 reference, begins to ramp in a negative-going direction (Trace B, *Figure 10*). The 2N2222A transistor provides a −0.6V or a +7V feedback output bound for A4, keeping its output from saturating and aiding high speed response. AC positive feedback assures clean transitions. A3 is set up as a 100 kHz oscillator. The LM329 and the diodes provide a temperature compensated bipolar switching threshold reference for the oscillator. During the time A4 is low the pulses from A3's output are passed by the 2N3904 transistor. When A4 goes high the 2N3904 is biased on and no more pulses appear (Trace D, *Figure 10*). Since A2's output ramp is linear the length of time A4 spends low is directly proportional to the value of E_{IN}. The number of pulses at the 2N3904 output provides a digital indication of this information. A2's ramp continues to run after A4 goes high and the actual conversion ends. When the time constant associated with the "free run with delay" mode charges to 2V A1's output goes high (Trace A, *Figure 10*), turning on the 2N4393 FET, which resets the integrator. A1 stays high until the AC feedback provided by the 150 pF capacitor decays below 2V. At this point A1 goes low, A2 begins to ramp and a new conversion cycle starts. False data at the converter output is prevented during the time A1 is high by resistor diode gating at the 2N3904 base.

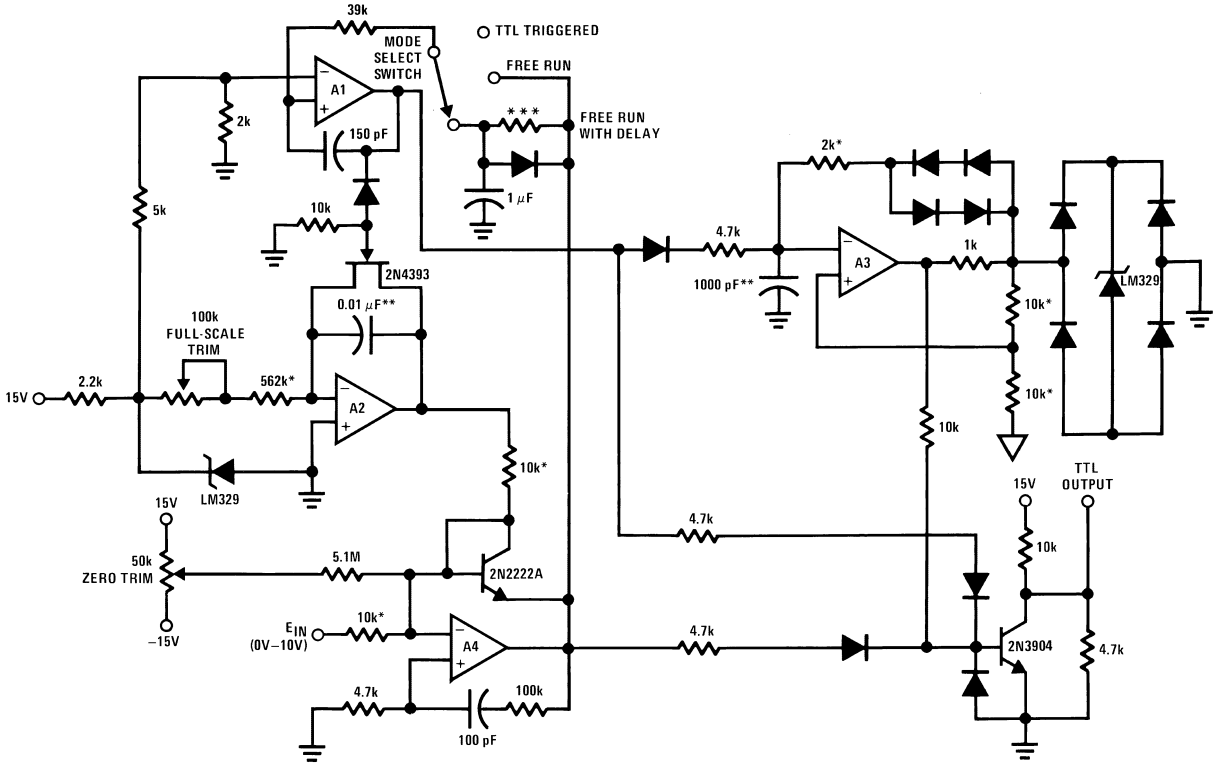
Normally, a ±1 count uncertainty at the output will be introduced because the 100 kHz clock runs asynchronously with the conversion cycle. This problem is eliminated by the diode and 4.7k resistor which run between A1's output and the A3 negative input. These components force the oscillator to synchronize to the conversion cycle at each falling edge of A1's output. The length of time between conversions in the "free run with delay" mode is adjustable by varying the RC combination associated with this switch position. The converter may be triggered externally by any source with a greater than 2V amplitude. In the "free run" mode the converter self triggers immediately after A4 goes high. Thus, the conversion time will vary with the input voltage.

This is graphically illustrated in the photo of *Figure 11*. Here, a positive biased sine wave (Trace B, *Figure 11*) is fed into

Analog-to-Digital Converter

(Continued)

the A/D input. Because the A/D resets and self triggers immediately after converting, the A2 ramp output shapes a ramp constructed envelope of the input signal (Trace C, *Figure 11*). Trace A shows this in time expanded form. Note that the −120 ppm/˚C temperature coefficients of the Polystyrene capacitors in the integrator and oscillator will tend to track, aiding drift performance in this circuit. From 15˚C to 35˚C this circuit achieves 10-bit absolute accuracy. To calibrate this circuit apply 10.00V to the input and adjust the FS trim for 1000 pulses out per conversion. Next, apply 0.05V and adjust zero trim for 5 pulses out per conversion. Repeat this procedure until the adjustments converge.



All diodes = 1N4148

*** = 2 kΩ to 20 MΩ typ for delays up to 20 sec

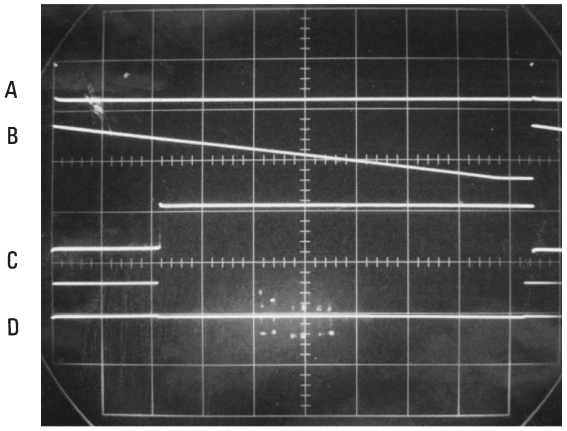
** = Polystyrene types

* = Metal-film types A1–A4 = LF347 quad

FIGURE 9. Three mode select switch positions offer a choice of internal or external trigger conditions for this integrating A/D converter. Over 15˚C to 35˚C, this trimmable converter provides a 10-bit serial output, converts in 10 ms and accepts 0V to 10V inputs.

Analog-to-Digital Converter

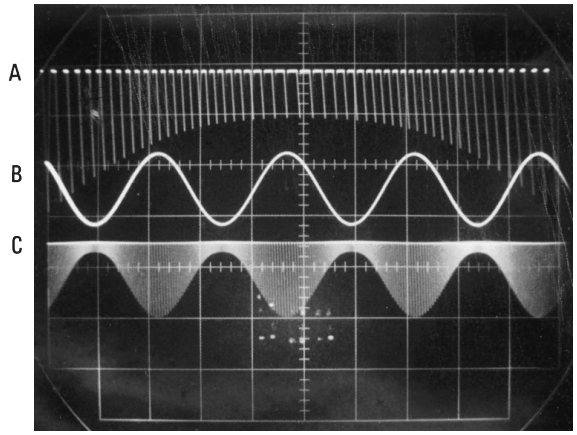
(Continued)



01258710

Trace	Vertical	Horizontal
A	5V/Div	
B	10V/Div	1 ms/Div
C	10V/Div	
D	5V/Div	

FIGURE 10. Depicting the operation of *Figure 9* A/D circuit in "free run with delay" mode, Trace A shows A1's output low. In this state, integrator A2 starts to ramp in a negative-going direction (Trace B). When A2's ramp potential barely exceeds the input voltage's negative value, A4's output goes high (C). This transition turns on the 2N3904 transistor, which shuts off the TTL output pulse train (D).



01258711

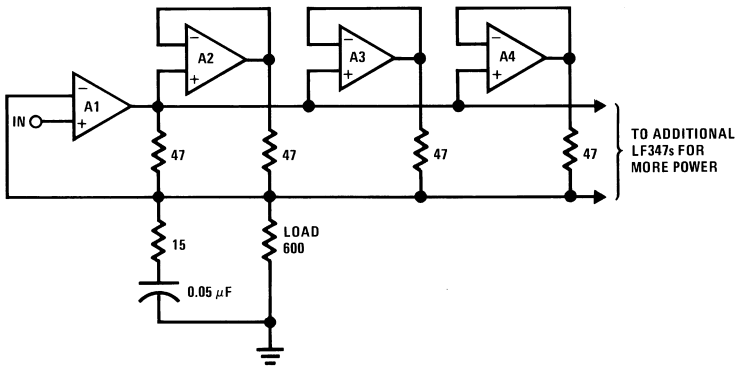
Trace	Vertical	Horizontal
A	1V/Div	2 ms/Div
B	5V/Div	20 ms/Div
C	5V/Div	20 ms/Div

FIGURE 11. Illustrating the A/D converter's operation in the "free run" mode, Trace B shows a positively biased sine wave input. Because reset and self trigger occur instantly after conversion. A2's output produces a ramp-constructed envelope of the input (Trace C). Trace A shows a time expanded form of the envelope waveform.

High Output Current Amplifier

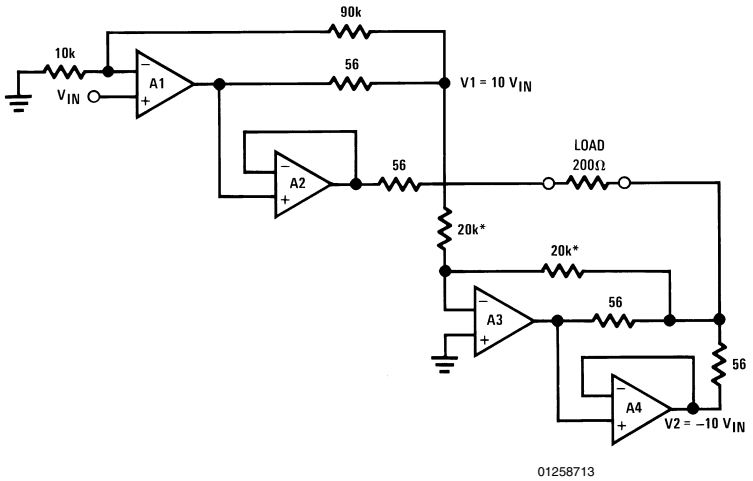
Figure 12 shows a scheme for obtaining high output current into a load by using all 4 amplifiers in an LF347 to supply output power. It operates on the principle that all the amplifiers have to supply the same current as A1, whether that current is plus, minus or zero. A single LF347 can be used to drive a 600Ω load to ±11V in this fashion. Two LF347 packages permit ±40 mA of output current. The series RC damper prevents oscillations. The circuit of *Figure 13* is similar but features a gain of 10 and output to a floating load. A1 amplifies the signal and A2 helps it drive the load. A3 operates as a unity gain inverter and A4 helps it to drive the load. This circuit will easily drive a 2000Ω floating load to ±20V.

High Output Current Amplifier (Continued)



A1–A4 = LF347 quad

FIGURE 12. Utilizing current-amplifying capabilities, one LF347 can drive a 600Ω load to ±11V. For additional power, two LF347's can supply an output current of ±40 mA.



*= 1% types

A1–A4 = LF347 quad

FIGURE 13. Configured as a high output current amplifier with a gain of 10, this LF347 circuit can drive a 200Ω floating load to ±20V.

Sine Wave Generation Techniques

National Semiconductor
Application Note 263
October 1999

Producing and manipulating the sine wave function is a common problem encountered by circuit designers. Sine wave circuits pose a significant design challenge because they represent a constantly controlled linear oscillator. Sine wave circuitry is required in a number of diverse areas, including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications.

A number of techniques utilizing both analog and digital approaches are available for a variety of applications. Each individual circuit approach has inherent strengths and weaknesses which must be matched against any given application (see table).

Phase Shift Oscillator

A simple inexpensive amplitude stabilized phase shift sine wave oscillator which requires one IC package, three transistors and runs off a single supply appears in *Figure 1*. Q2, in combination with the RC network comprises a phase shift configuration and oscillates at about 12 kHz. The remaining circuitry provides amplitude stability. The high impedance output at Q2's collector is fed to the input of the LM386 via the 10 µF-1M series network. The 1M resistor in combination with the internal 50 kΩ unit in the LM386 divides Q2's output by 20. This is necessary because the LM386 has a fixed gain of 20. In this manner the amplifier functions as a unity gain current buffer which will drive an 8Ω load. The positive peaks at the amplifier output are rectified and stored in the 5 µF capacitor. This potential is fed to the base of Q3. Q3's collector current will vary with the difference between its base and emitter voltages. Since the emitter voltage is fixed by the LM313 1.2V reference, Q3 performs a comparison function and its collector current modulates Q1's base voltage. Q1, an emitter follower, provides servo controlled drive to the Q2 oscillator. If the emitter of Q2 is opened up and driven by a control voltage, the amplitude of the circuit output may be varied. The LM386 output will drive 5V (1.75 Vrms) peak-to-peak into 8Ω with about 2% distortion. A ±3V power supply variation causes less than ±0.1 dB amplitude shift at the output.

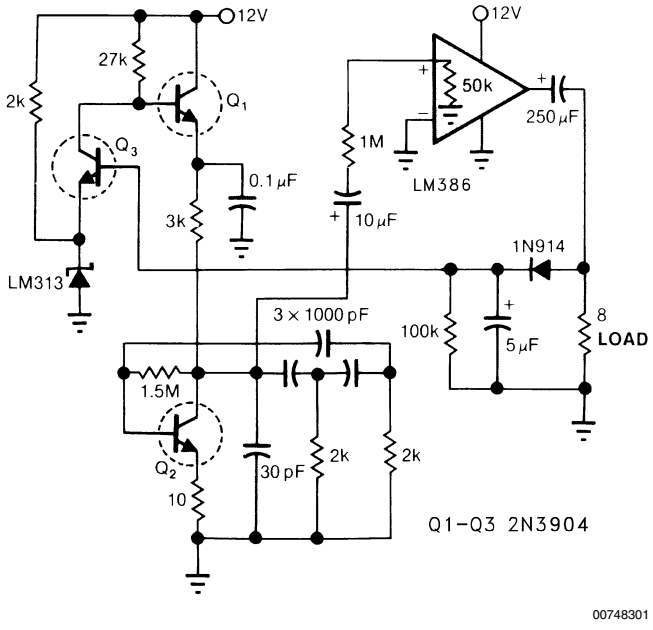


FIGURE 1. Phase-shift sine wave oscillators combine simplicity with versatility. This 12 kHz design can deliver 5 Vp-p to the 8Ω load with about 2% distortion.

Sine-Wave-Generation Techniques

Type	Typical Frequency Range	Typical Distortion (%)	Typical Amplitude Stability (%)	Comments
Phase Shift	10 Hz–1 MHz	1–3	3 (Tighter with Servo Control)	Simple, inexpensive technique. Easily amplitude servo controlled. Resistively tunable over 2:1 range with little trouble. Good choice for cost-sensitive, moderate-performance applications. Quick starting and settling.
Wein Bridge	1 Hz–1 MHz	0.01	1	Extremely low distortion. Excellent for high-grade instrumentation and audio applications. Relatively difficult to tune — requires dual variable resistor with good tracking. Take considerable time to settle after a step change in frequency or amplitude.
LC Negative Resistance	1 kHz–10 MHz	1–3	3	Difficult to tune over wide ranges. Higher Q than RC types. Quick starting and easy to operate in high frequency ranges.
Tuning Fork	60 Hz–3 kHz	0.25	0.01	Frequency-stable over wide ranges of temperature and supply voltage. Relatively unaffected by severe shock or vibration. Basically untunable.
Crystal	30 kHz–200 MHz	0.1	1	Highest frequency stability. Only slight (ppm) tuning possible. Fragile.
Triangle-Driven Break-Point Shaper	< 1 Hz–500 kHz	1–2	1	Wide tuning range possible with quick settling to new frequency or amplitude.
Triangle-Driven Logarithmic Shaper	< 1 Hz–500 kHz	0.3	0.25	Wide tuning range possible with quick settling to new frequency or amplitude. Triangle and square wave also available. Excellent choice for general-purpose requirements needing frequency-sweep capability with low-distortion output.
DAC-Driven Logarithmic Shaper	<1 Hz–500 kHz	0.3	0.25	Similar to above but DAC-generated triangle wave generally easier to amplitude-stabilize or vary. Also, DAC can be addressed by counters synchronized to a master system clock.
ROM-Driven DAC	1 Hz–20 MHz	0.1	0.01	Powerful digital technique that yields fast amplitude and frequency slewing with little dynamic error. Chief detriments are requirements for high-speed clock (e.g., 8-bit DAC requires a clock that is 256 x output sine wave frequency) and DAC glitching and settling, which will introduce significant distortion as output frequency increases.

Low Distortion Oscillation

In many applications the distortion levels of a phase shift oscillator are unacceptable. Very low distortion levels are provided by Wein bridge techniques. In a Wein bridge stable oscillation can only occur if the loop gain is maintained at unity at the oscillation frequency. In *Figure 2a* this is achieved by using the positive temperature coefficient of a small lamp to regulate gain as the output attempts to vary. This is a classic technique and has been used by numerous circuit designers* to achieve low distortion. The smooth limiting action of the positive temperature coefficient bulb in combination with the near ideal characteristics of the Wein network allow very high performance. The photo of *Figure 3* shows the output of the circuit of *Figure 2a*. The upper trace is the oscillator output. The middle trace is the downward slope of the waveform shown greatly expanded. The slight aberration is due to crossover distortion in the FET-input LF155. This crossover distortion is almost totally responsible for the sum of the measured 0.01% distortion in this oscillator. The output of the distortion analyzer is shown in the bottom trace. In the circuit of *Figure 2b*, an electronic equivalent of the light bulb is used to control loop gain. The zener diode determines the output amplitude and the loop time constant is set by the 1M-2.2 µF combination.

Low Distortion Oscillation (Continued)

The 2N3819 FET, biased by the voltage across the 2.2 µF capacitor, is used to control the AC loop gain by shunting the feedback path. This circuit is more complex than *Figure 2a* but offers a way to control the loop time constant while maintaining distortion performance almost as good as in *Figure 2*.

Note: * Including William Hewlett and David Packard who built a few of these type circuits in a Palo Alto garage about forty years ago.

High Voltage AC Calibrator

Another dimension in sine wave oscillator design is stable control of amplitude. In this circuit, not only is the amplitude stabilized by servo control but voltage gain is included within the servo loop.

A 100 Vrms output stabilized to 0.025% is achieved by the circuit of *Figure 4*. Although complex in appearance this circuit requires just 3 IC packages. Here, a transformer is used to provide voltage gain within a tightly controlled servo loop. The LM3900 Norton amplifiers comprise a 1 kHz amplitude controllable oscillator. The LH0002 buffer provides low impedance drive to the LS-52 audio transformer. A voltage gain of 100 is achieved by driving the secondary of the transformer and taking the output from the primary. A current-sensitive negative absolute value amplifier composed of two amplifiers of an LF347 quad generates a negative rectified feedback signal. This is compared to the LM329 DC reference at the third LF347 which amplifies the difference at a gain of 100. The 10 µF feedback capacitor is used to set the frequency response of the loop. The output of this amplifier controls the amplitude of the LM3900 oscillator thereby closing the loop. As shown the circuit oscillates at 1 kHz with under 0.1% distortion for a 100 Vrms (285 Vp-p) output. If the summing resistors from the LM329 are replaced with a potentiometer the loop is stable for output settings ranging from 3 Vrms to 190 Vrms (542 Vp-p!) with no change in frequency. If the DAC1280 D/A converter shown in dashed lines replaces the LM329 reference, the AC output voltage can be controlled by the digital code input with 3 digit calibrated accuracy.

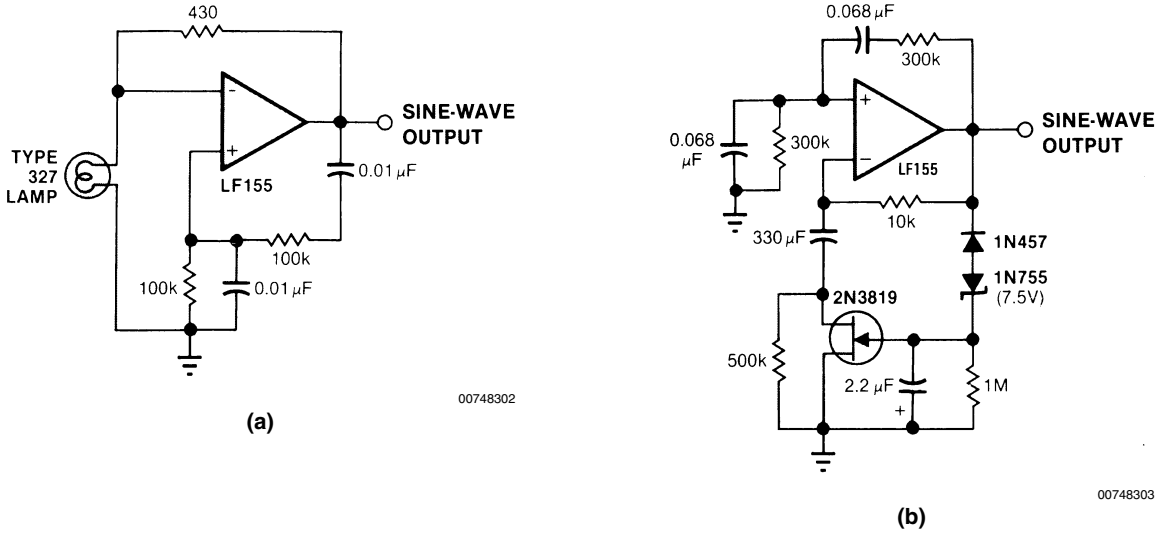
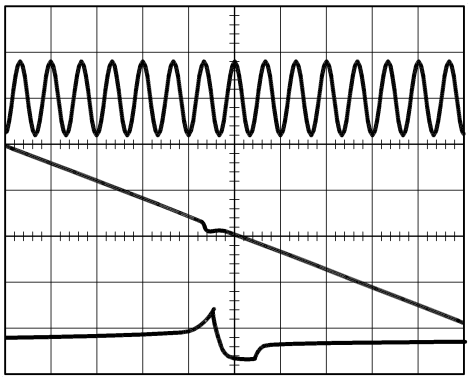


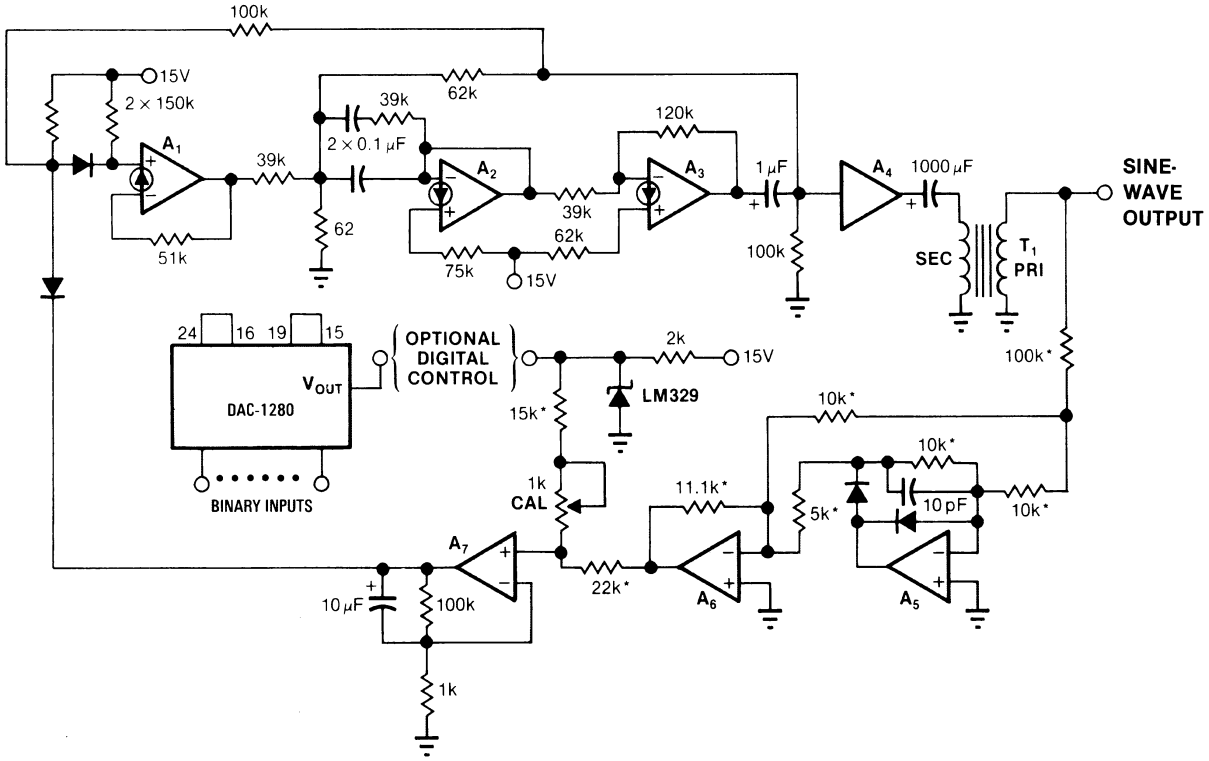
FIGURE 2. A basic Wein bridge design (a) employs a lamp's positive temperature coefficient to achieve amplitude stability. A more complex version (b) provides the same feature with the additional advantage of loop time-constant control.

High Voltage AC Calibrator (Continued)



Trace	Vertical	Horizontal
Top	10V/DIV	10 ms/DIV
Middle	1V/DIV	500 ns/DIV
Bottom	0.5V/DIV	500 ns/DIV

FIGURE 3. Low-distortion output (top trace) is a Wein bridge oscillator feature. The very low crossover distortion level (middle) results from the LF155's output stage. A distortion analyzer's output signal (bottom) indicates this design's 0.01% distortion level.



A1–A3 = ¼ LM3900
A4 = LH0002
A5–A7 = ¼ LF347
T1 = UTC LS-52
All diodes = 1N914
* = low-TC, metal-film types

FIGURE 4. Generate high-voltage sine waves using IC-based circuits by driving a transformer in a step-up mode. You can realize digital amplitude control by replacing the LM329 voltage reference with the DAC1287.

Negative Resistance Oscillator

All of the preceding circuits rely on RC time constants to achieve resonance. LC combinations can also be used and offer good frequency stability, high Q and fast starting.

In *Figure 5* a negative resistance configuration is used to generate the sine wave. The Q1-Q2 pair provides a 15 µA current source. Q2's collector current sets Q3's peak collector current. The 300 kΩ resistor and the Q4-Q5 LM394 matched pair accomplish a voltage-to-current conversion that decreases Q3's base current when its collector voltage rises. This negative resistance characteristic permits oscillation. The frequency of operation is determined by the LC in the Q3-Q5 collector line. The LF353 FET amplifier provides gain and buffering. Power supply dependence is eliminated by the zener diode and the LF353 unity gain follower. This circuit starts quickly and distortion is inside 1.5%.

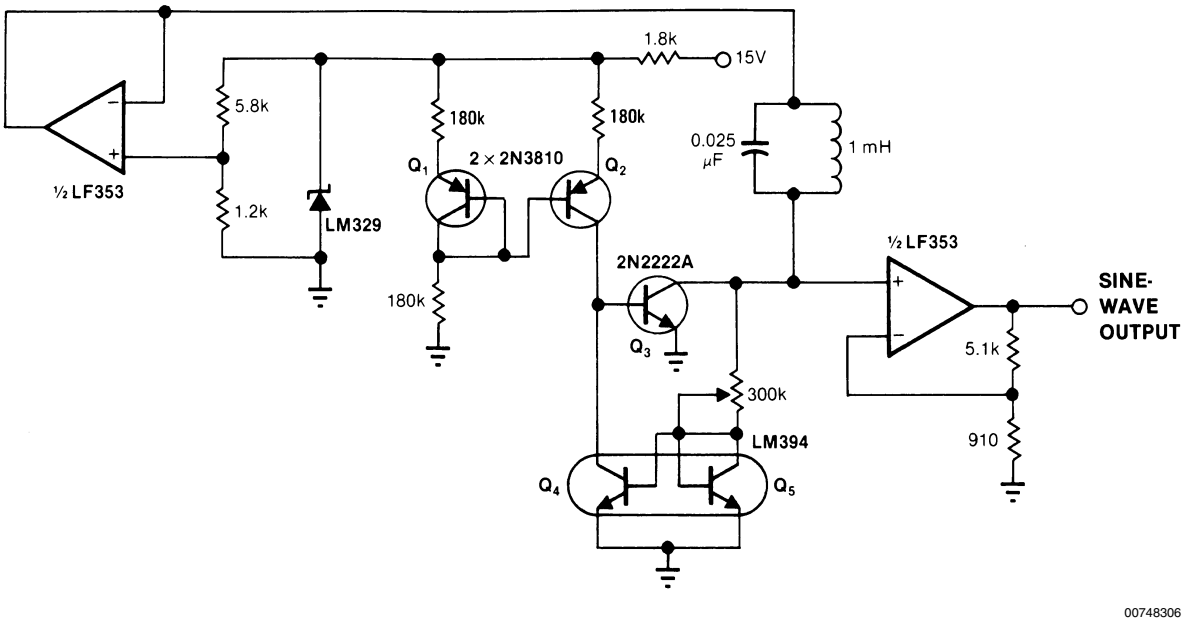


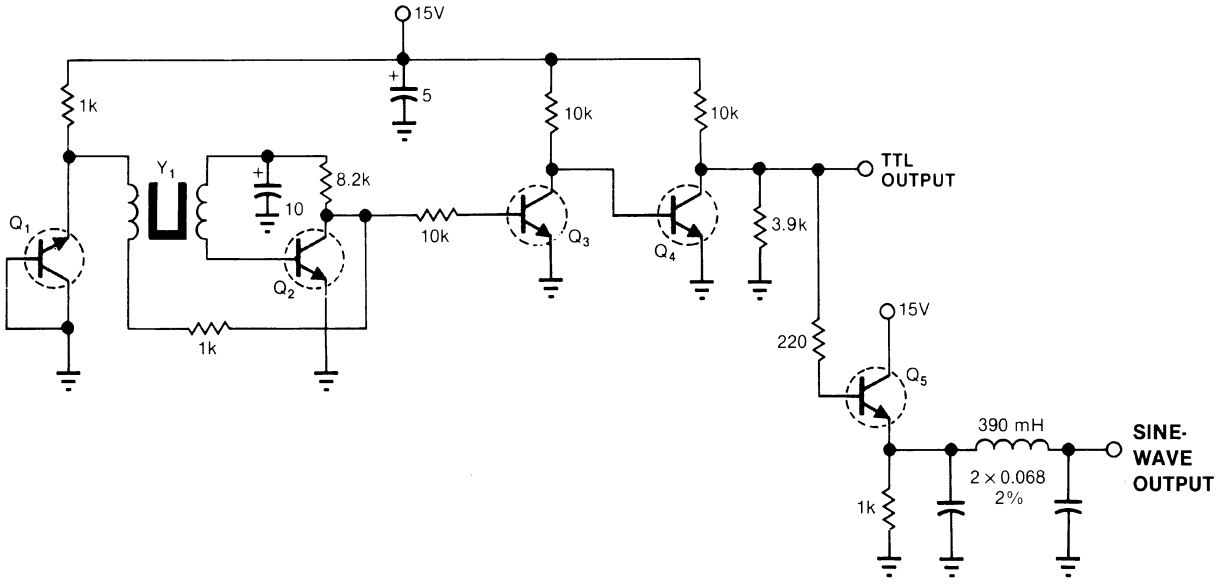
FIGURE 5. LC sine wave sources offer high stability and reasonable distortion levels. Transistors Q1 through Q5 implement a negative-resistance amplifier. The LM329, LF353 combination eliminates power-supply dependence.

Resonant Element Oscillator—Tuning Fork

All of the above oscillators rely on combinations of passive components to achieve resonance at the oscillation frequency. Some circuits utilize inherently resonant elements to achieve very high frequency stability. In *Figure 6* a tuning fork is used in a feedback loop to achieve a stable 1 kHz output. Tuning fork oscillators will generate stable low frequency sine outputs under high mechanical shock conditions which would fracture a quartz crystal.

Because of their excellent frequency stability, small size and low power requirements, they have been used in airborne applications, remote instrumentation and even watches. The low frequencies achievable with tuning forks are not available from crystals. In *Figure 6*, a 1 kHz fork is used in a feedback configuration with Q2, one transistor of an LM3045 array. Q1 provides zener drive to the oscillator circuit. The need for amplitude stabilization is eliminated by allowing the oscillator to go into limit. This is a conventional technique in fork oscillator design. Q3 and Q4 provide edge speed-up and a 5V output for TTL compatibility. Emitter follower Q5 is used to drive an LC filter which provides a sine wave output. *Figure 7*, trace A shows the square wave output while trace B depicts the sine wave output. The 0.7% distortion in the sine wave output is shown in trace C, which is the output of a distortion analyzer.

Resonant Element Oscillator—Tuning Fork (Continued)

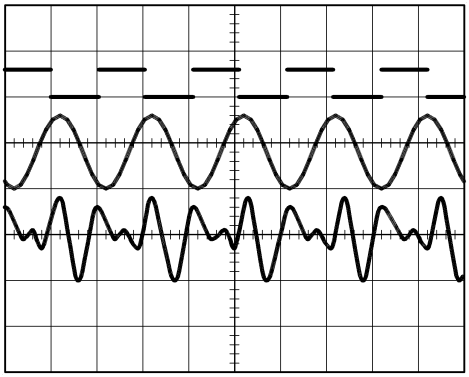


Q1–Q5 = LM3045 array

Y1 = 1 kHz tuning fork, Fork Standards Inc.

All capacitors in µF

FIGURE 6. Tuning fork based oscillators don't inherently produce sinusoidal outputs. But when you do use them for this purpose, you achieve maximum stability when the oscillator stage (Q1, Q2) limits. Q3 and Q4 provide a TTL compatible signal, which Q5 then converts to a sine wave.



Trace	Vertical	Horizontal
Top	5V/DIV	
Middle	50V/DIV	500 µs/DIV
Bottom	0.2V/DIV	

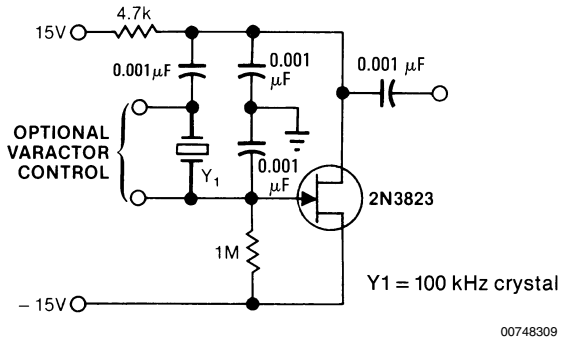
FIGURE 7. Various output levels are provided by the tuning fork oscillator shown in *Figure 6*. This design easily produces a TTL compatible signal (top trace) because the oscillator is allowed to limit. Low-pass filtering this square wave generates a sine wave (middle). The oscillator's 0.7% distortion level is indicated (bottom) by an analyzer's output.

Resonant Element Oscillator—Quartz Crystal

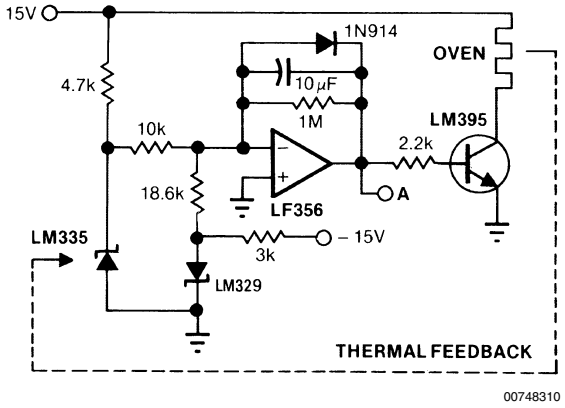
Quartz crystals allow high frequency stability in the face of changing power supply and temperature parameters. *Figure 8a* shows a simple 100 kHz crystal oscillator. This Colpitts class circuit uses a JFET for low loading of the crystal, aiding stability. Regulation will eliminate the small effects (~ 5 ppm for 20% shift) that supply variation has on this circuit. Shunting the crystal with a small amount of capacitance allows very fine trimming of frequency. Crystals typically drift less than 1 ppm/°C and temperature controlled ovens can be used to eliminate this term (*Figure 8b*). The RC feedback values will depend upon the thermal time constants of the oven used. The values shown are typical. The temperature of the oven should be set so that it coincides with the crystal's zero temperature coefficient or "turning point" temperature which is manufacturer specified. An alternative to temperature control uses a varactor diode placed across the crystal. The varactor is biased by a temperature dependent voltage from a circuit which could be very similar to *Figure 8b* without the output transistor. As ambient temperature varies the circuit changes the voltage across the varactor, which in turn changes its capacitance. This shift in capacitance trims the oscillator frequency.

Approximation Methods

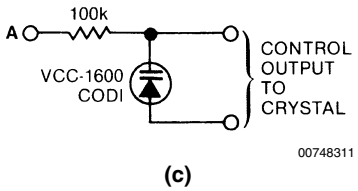
All of the preceding circuits are *inherent* sine wave generators. Their normal mode of operation supports and maintains a sinusoidal characteristic. Another class of oscillator is made up of circuits which *approximate* the sine function through a variety of techniques. This approach is usually more complex but offers increased flexibility in controlling amplitude and frequency of oscillation. The capability of this type of circuit for a digitally controlled interface has markedly increased the popularity of the approach.



(a)



(b)

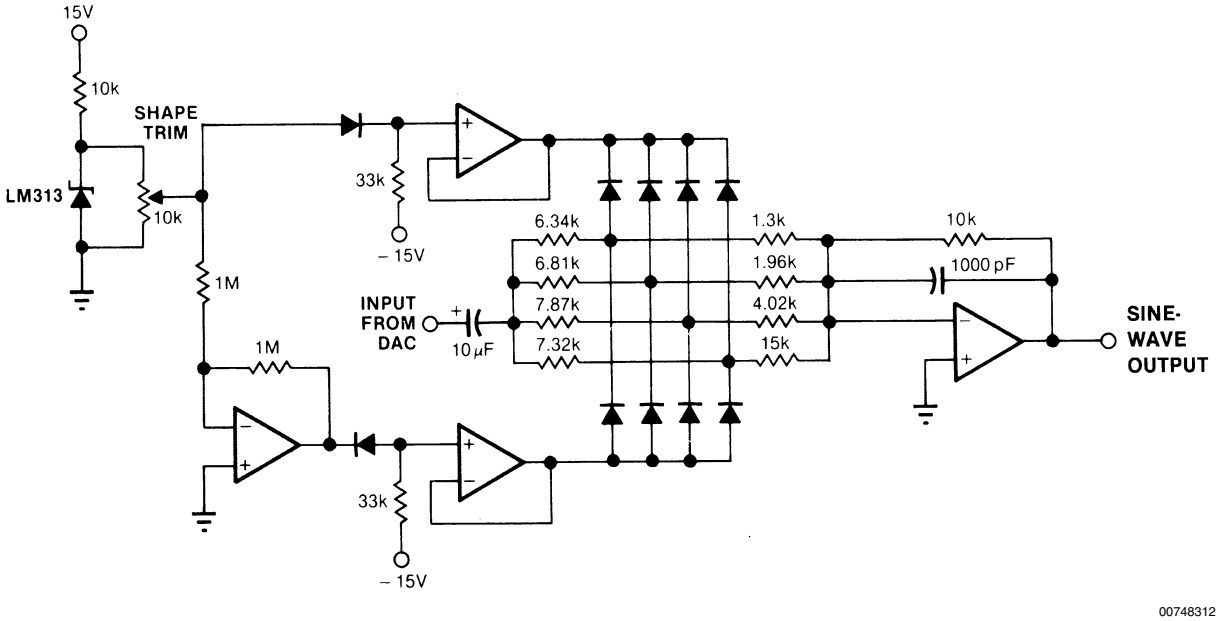


(c)

FIGURE 8. Stable quartz-crystal oscillators can operate with a single active device (a). You can achieve maximum frequency stability by mounting the oscillator in an oven and using a temperature-controlling circuit (b). A varactor network (c) can also accomplish crystal fine tuning. Here, the varactor replaces the oven and retunes the crystal by changing its load capacitances.

Sine Approximation—Breakpoint Shaper

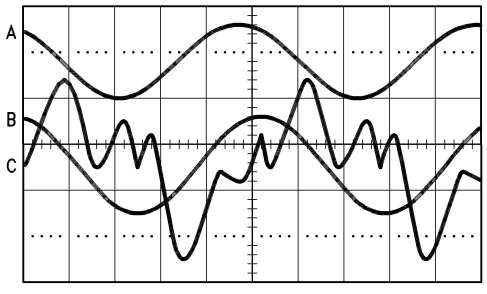
Figure 9 diagrams a circuit which will "shape" a 20 Vp-p wave input into a sine wave output. The amplifiers serve to establish stable bias potentials for the diode shaping network. The shaper operates by having individual diodes turn on or off depending upon the amplitude of the input triangle. This changes the gain of the output amplifier and gives the circuit its characteristic non-linear, shaped output response. The values of the resistors associated with the diodes determine the shaped waveform's appearance. Individual diodes in the DC bias circuitry provide first order temperature compensation for the shaper diodes. *Figure 10* shows the circuit's performance. Trace A is the filtered output (note 1000 pF capacitor across the output amplifier). Trace B shows the waveform with no filtering (1000 pF capacitor removed) and trace C is the output of a distortion analyzer. In trace B the breakpoint action is just detectable at the top and bottom of the waveform, but all the breakpoints are clearly identifiable in the distortion analyzer output of trace C. In this circuit, if the amplitude or symmetry of the input triangle wave shifts, the output waveform will degrade badly. Typically, a D/A converter will be used to provide input drive. Distortion in this circuit is less than 1.5% for a filtered output. If no filter is used, this figure rises to about 2.7%.



All diodes = 1N4148

All op amps = ¼ LF347

FIGURE 9. Breakpoint shaping networks employ diodes that conduct in direct proportion to an input triangle wave's amplitude. This action changes the output amplifier's gain to produce the sine function.

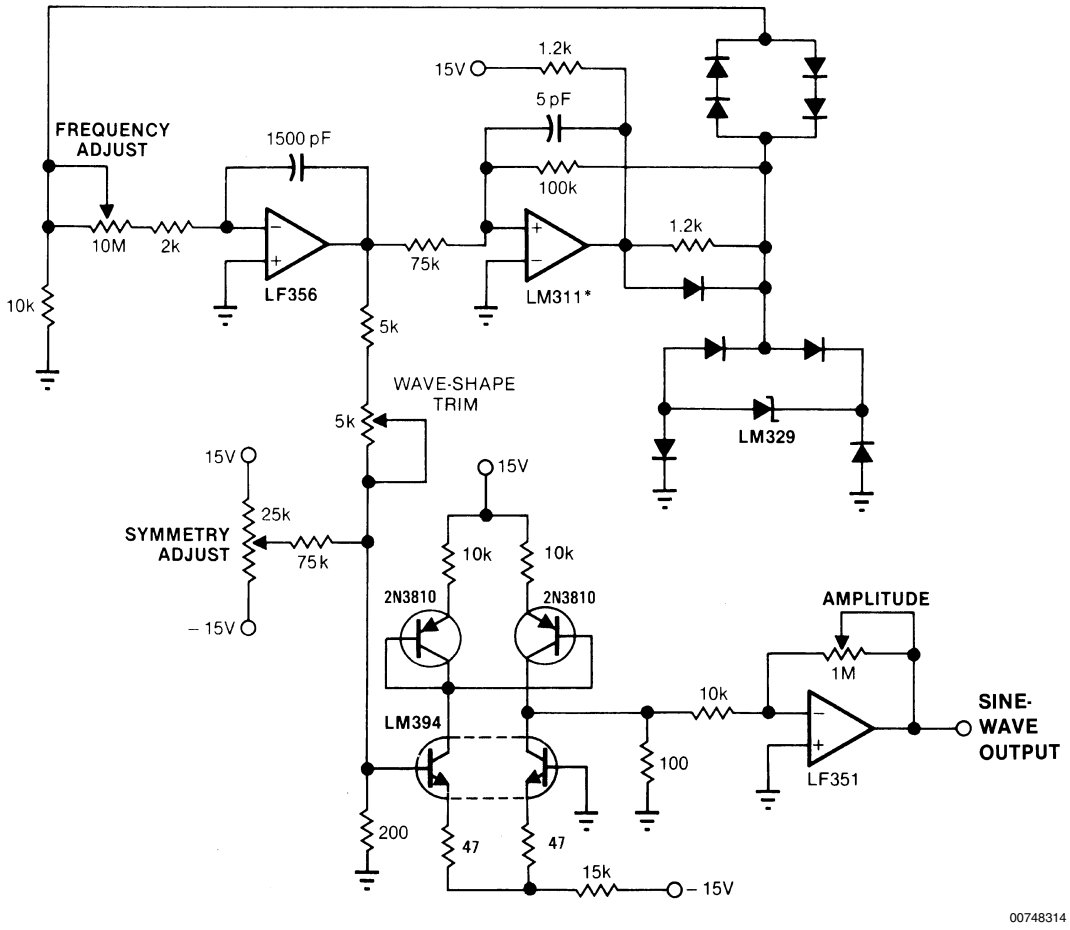


Trace	Vertical	Horizontal
A	5V/DIV	20 µs/DIV
B	5V/DIV	
C	0.5V/DIV	

FIGURE 10. A clean sine wave results (trace A) when *Figure 9* circuit's output includes a 1000 pF capacitor. When the capacitor isn't used, the diode network's breakpoint action becomes apparent (trace B). The distortion analyzer's output (trace C) clearly shows all the breakpoints.

Sine Approximation—Logarithmic Shaping

Figure 11 shows a complete sine wave oscillator which may be tuned from 1 Hz to 10 kHz with a single variable resistor. Amplitude stability is inside 0.02%/°C and distortion is 0.35%. In addition, desired frequency shifts occur instantaneously because no control loop time constants are employed. The circuit works by placing an integrator inside the positive feedback loop of a comparator. The LM311 drives symmetrical, temperature-compensated clamp arrangement. The output of the clamp biases the LF356 integrator. The LF356 integrates this current into a linear ramp at its output. This ramp is summed with the clamp output at the LM311 input. When the ramp voltage nulls out the bound voltage, the comparator changes state and the integrator output reverses. The resultant, repetitive triangle waveform is applied to the sine shaper configuration. The sine shaper utilizes the non-linear, logarithmic relationship between V_{be} and collector current in transistors to smooth the triangle wave. The LM394 dual transistor is used to generate the actual shaping while the 2N3810 provides current drive. The LF351 allows adjustable, low impedance, output amplitude control. Waveforms of operation are shown in *Figure 14*.



All diodes = 1N4148

Adjust symmetry and wave-shape controls for minimum distortion

* LM311 Ground Pin (Pin 1) at –15V

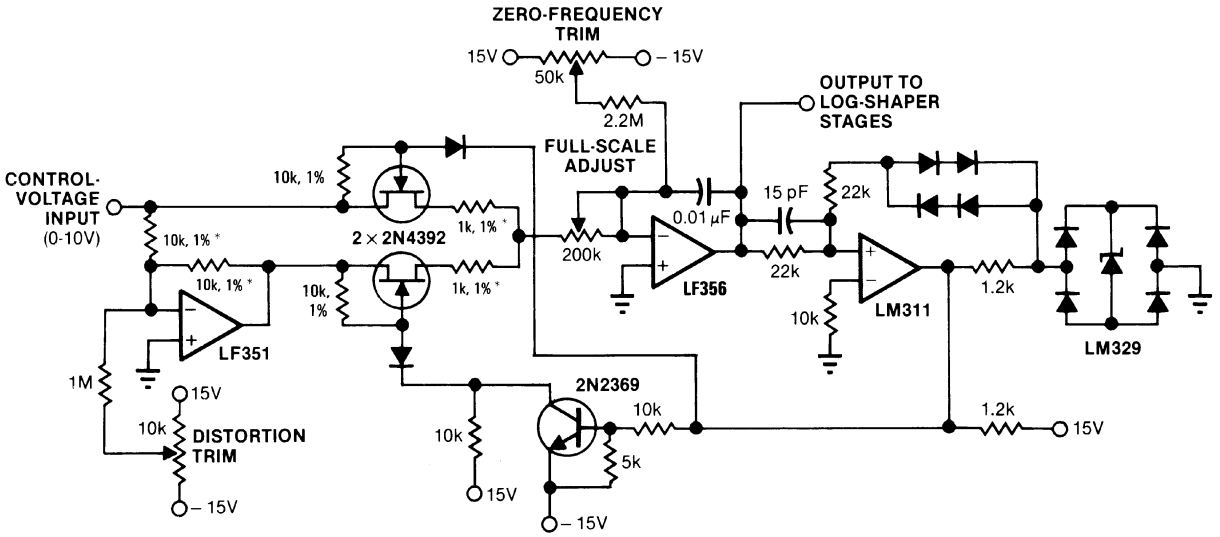
FIGURE 11. Logarithmic shaping schemes produce a sine wave oscillator that you can tune from 1 Hz to 10 kHz with a single control. Additionally, you can shift frequencies rapidly because the circuit contains no control-loop time constants.

Sine Approximation—Voltage Controlled Sine Oscillator

Figure 12 details a modified but extremely powerful version of *Figure 11*. Here, the input voltage to the LF356 integrator is furnished from a control voltage input instead of the zener diode bridge. The control input is inverted by the LF351. The two complementary voltages are each gated by the 2N4393 FET switches, which are controlled by the LM311 output. The frequency of oscillation will now vary in direct proportion to the control input. In addition, because the amplitude of this circuit is controlled by limiting, rather than a servo loop, response to a control step or ramp input is almost instantaneous. For a 0V–10V input the output will run over 1 Hz to 30

Sine Approximation—Voltage Controlled Sine Oscillator (Continued)

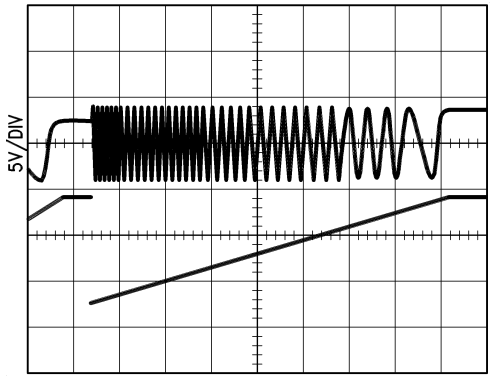
kHz with less than 0.4% distortion. In addition, linearity of control voltage vs output frequency will be within 0.25%. *Figure 13* shows the response of this circuit (waveform B) to a 10V ramp (waveform A).



00748315

Adjust distortion for
minimum at 1 Hz to 10 Hz
Adjust full-scale for 30 kHz
at 10V input
All diodes = 1N4148
* Match to 0.1%

FIGURE 12. A voltage-tunable oscillator results when *Figure 11's* design is modified to include signal-level-controlled feedback. Here, FETs switch the integrator's input so that the resulting summing-junction current is a function of the input control voltage. This scheme realizes a frequency range of 1 Hz to 30 kHz for a 0V to 10V input.

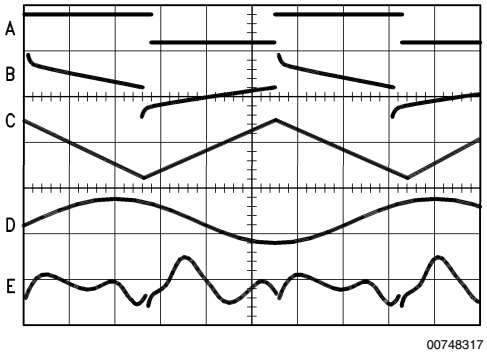


00748316

FIGURE 13. Rapid frequency sweeping is an inherent feature of *Figure 12's* voltage-controlled sine wave oscillator. You can sweep this VCO from 1 Hz to 30 kHz with a 10V input signal; the output settles quickly.

Sine Approximation—Digital Methods

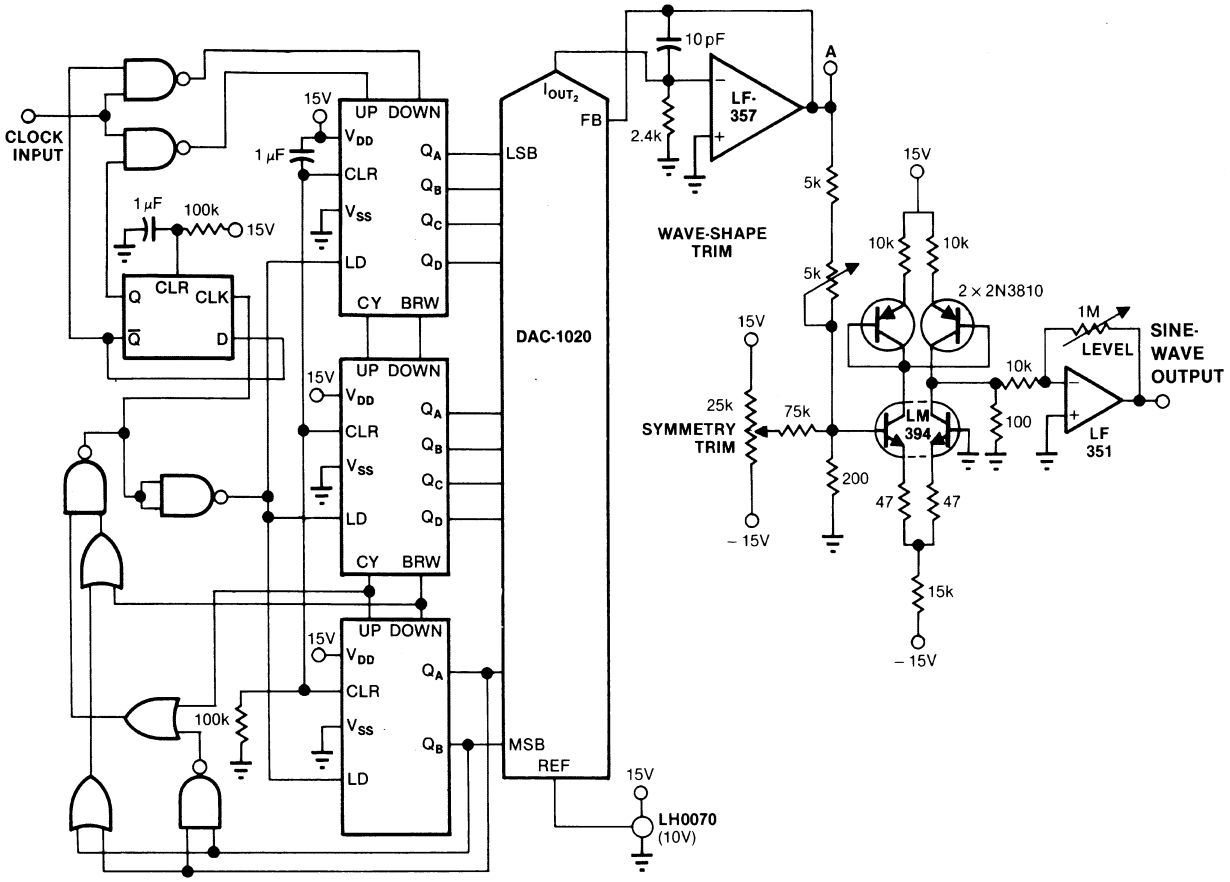
Digital methods may be used to approximate sine wave operation and offer the greatest flexibility at some increase in complexity. *Figure 15* shows a 10-bit IC D/A converter driven from up/down counters to produce an amplitude-stable triangle current into the LF357 FET amplifier. The LF357 is used to drive a shaper circuit of the type shown in *Figure 11*. The output amplitude of the sine wave is stable and the frequency is solely dependent on the clock used to drive the counters. If the clock is crystal controlled, the output sine wave will reflect the high frequency stability of the crystal. In this example, 10 binary bits are used to drive the DAC so the output frequency will be 1/1024 of the clock frequency. If a sine coded read-only-memory is placed between the counter outputs and the DAC, the sine shaper may be eliminated and the sine wave output taken directly from the LF357. This constitutes an extremely powerful digital technique for generating sine waves. The amplitude may be voltage controlled by driving the reference terminal of the DAC. The frequency is again established by the clock speed used and both may be varied at high rates of speed without introducing significant lag or distortion. Distortion is low and is related to the number of bits of resolution used. At the 8-bit level only 0.5% distortion is seen (waveforms, *Figure 16*; graph, *Figure 17*) and filtering will drop this below 0.1%. In the photo of *Figure 16* the ROM directed steps are clearly visible in the sine waveform and the DAC levels and glitching show up in the distortion analyzer output. Filtering at the output amplifier does an effective job of reducing distortion by taking out these high frequency components.



Trace	Vertical	Horizontal
A	20V/DIV	
B	20V/DIV	20 µs/DIV
C	10V/DIV	
D	10V/DIV	
E	0.5V/DIV	

FIGURE 14. Logarithmic shapers can utilize a variety of circuit waveforms. The input to the LF356 integrator (*Figure 11*) appears here as trace A. The LM311's input (trace B) is the summed result of the integrator's triangle output (C) and the LM329's clamped waveform. After passing through the 2N3810/LM394 shaper stage, the resulting sine wave is amplified by the LF351 (D). A distortion analyzer's output (E) represents a 0.35% total harmonic distortion.

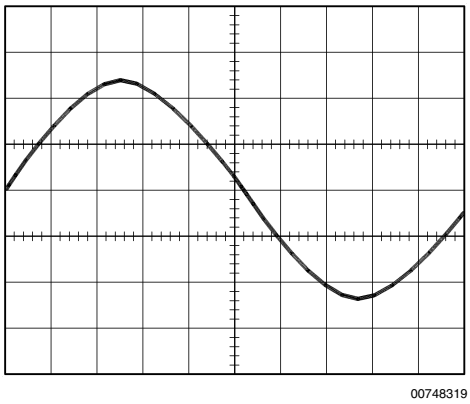
Sine Approximation—Digital Methods (Continued)



MM74C00 = NAND
MM74C32 = OR
MM74C74 = D flip-flop
MM74193 = counters

FIGURE 15. Digital techniques produce triangular waveforms that methods employed in *Figure 11* can then easily convert to sine waves. This digital approach divides the input clock frequency by 1024 and uses the resultant 10 bits to drive a DAC. The DAC's triangular output—amplified by the LF357—drives the log shaper stage. You could also eliminate the log shaper and place a sine-coded ROM between the counters' outputs and the DAC, then recover the sine wave at point A.

Sine Approximation—Digital Methods (Continued)



Trace	Vertical	Horizontal
Sine Wave	1V/DIV	200 µs/DIV
Analyzer	0.2V/DIV	

FIGURE 16. An 8-bit sine coded ROM version of *Figure 15's* circuit produces a distortion level less than 0.5%. Filtering the sine output—shown here with a distortion analyzer's trace—can reduce the distortion to below 0.1%.

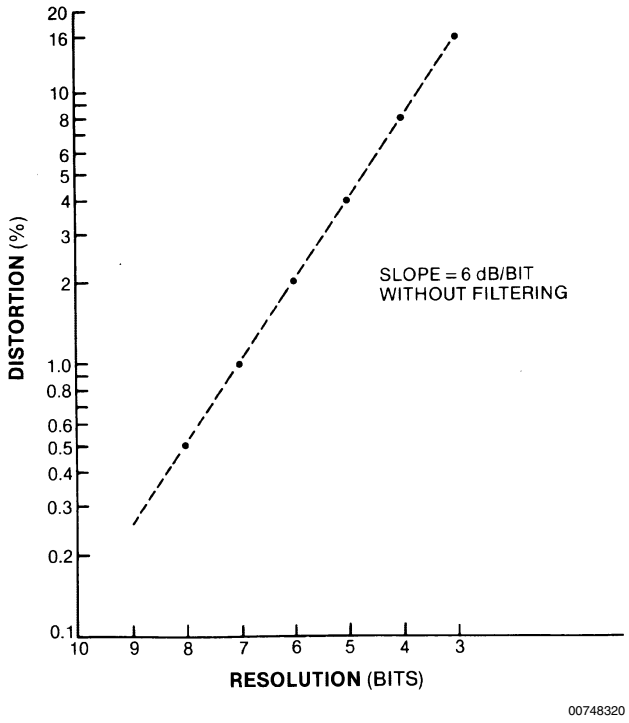


FIGURE 17. Distortion levels decrease with increasing digital word length. Although additional filtering can considerably improve the distortion levels (to 0.1% from 0.5% for the 8-bit case), you're better off using a long digital word.

Sine Wave Generation Techniques

National Semiconductor
Application Note 263
Rereleased May 26, 2009
October 21, 1999

Producing and manipulating the sine wave function is a common problem encountered by circuit designers. Sine wave circuits pose a significant design challenge because they represent a constantly controlled linear oscillator. Sine wave circuitry is required in a number of diverse areas, including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications.

A number of techniques utilizing both analog and digital approaches are available for a variety of applications. Each individual circuit approach has inherent strengths and weaknesses which must be matched against any given application (see table).

Phase Shift Oscillator

A simple inexpensive amplitude stabilized phase shift sine wave oscillator which requires one IC package, three transistors and runs off a single supply appears in *Figure 1*. Q2, in combination with the RC network comprises a phase shift configuration and oscillates at about 12 kHz. The remaining circuitry provides amplitude stability. The high impedance output at Q2's collector is fed to the input of the LM386 via the 10 µF-1M series network. The 1M resistor in combination with the internal 50 kΩ unit in the LM386 divides Q2's output by 20. This is necessary because the LM386 has a fixed gain of 20. In this manner the amplifier functions as a unity gain current buffer which will drive an 8Ω load. The positive peaks at the amplifier output are rectified and stored in the 5 µF capacitor. This potential is fed to the base of Q3. Q3's collector current will vary with the difference between its base and emitter voltages. Since the emitter voltage is fixed by the LM313 1.2V reference, Q3 performs a comparison function and its collector current modulates Q1's base voltage. Q1, an emitter follower, provides servo controlled drive to the Q2 oscillator. If the emitter of Q2 is opened up and driven by a control voltage, the amplitude of the circuit output may be varied. The LM386 output will drive 5V (1.75 Vrms) peak-to-peak into 8Ω with about 2% distortion. A ±3V power supply variation causes less than ±0.1 dB amplitude shift at the output.

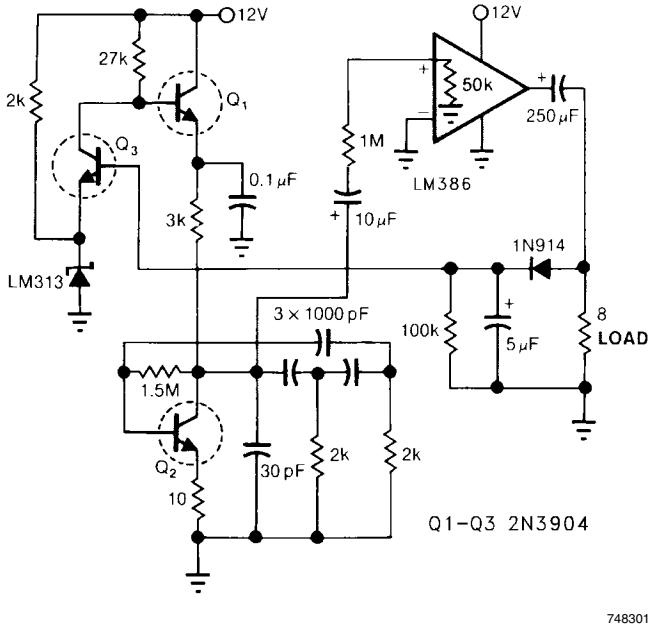


FIGURE 1. Phase-shift sine wave oscillators combine simplicity with versatility. This 12 kHz design can deliver 5 Vp-p to the 8Ω load with about 2% distortion.

Sine-Wave-Generation Techniques

Type	Typical Frequency Range	Typical Distortion (%)	Typical Amplitude Stability (%)	Comments
Phase Shift	10 Hz–1 MHz	1–3	3 (Tighter with Servo Control)	Simple, inexpensive technique. Easily amplitude servo controlled. Resistively tunable over 2:1 range with little trouble. Good choice for cost-sensitive, moderate-performance applications. Quick starting and settling.
Wein Bridge	1 Hz–1 MHz	0.01	1	Extremely low distortion. Excellent for high-grade instrumentation and audio applications. Relatively difficult to tune—requires dual variable resistor with good tracking. Take considerable time to settle after a step change in frequency or amplitude.
LC Negative Resistance	1 kHz–10 MHz	1–3	3	Difficult to tune over wide ranges. Higher Q than RC types. Quick starting and easy to operate in high frequency ranges.
Tuning Fork	60 Hz–3 kHz	0.25	0.01	Frequency-stable over wide ranges of temperature and supply voltage. Relatively unaffected by severe shock or vibration. Basically untunable.
Crystal	30 kHz–200 MHz	0.1	1	Highest frequency stability. Only slight (ppm) tuning possible. Fragile.
Triangle-Driven Break-Point Shaper	< 1 Hz–500 kHz	1–2	1	Wide tuning range possible with quick settling to new frequency or amplitude.
Triangle-Driven Logarithmic Shaper	< 1 Hz–500 kHz	0.3	0.25	Wide tuning range possible with quick settling to new frequency or amplitude. Triangle and square wave also available. Excellent choice for general-purpose requirements needing frequency-sweep capability with low-distortion output.
DAC-Driven Logarithmic Shaper	<1 Hz–500 kHz	0.3	0.25	Similar to above but DAC-generated triangle wave generally easier to amplitude-stabilize or vary. Also, DAC can be addressed by counters synchronized to a master system clock.
ROM-Driven DAC	1 Hz–20 MHz	0.1	0.01	Powerful digital technique that yields fast amplitude and frequency slewing with little dynamic error. Chief detriments are requirements for high-speed clock (e.g., 8-bit DAC requires a clock that is 256 × output sine wave frequency) and DAC glitching and settling, which will introduce significant distortion as output frequency increases.

Low Distortion Oscillation

In many applications the distortion levels of a phase shift oscillator are unacceptable. Very low distortion levels are provided by Wein bridge techniques. In a Wein bridge stable oscillation can only occur if the loop gain is maintained at unity at the oscillation frequency. In *Figure 2a* this is achieved by using the positive temperature coefficient of a small lamp to regulate gain as the output attempts to vary. This is a classic technique and has been used by numerous circuit designers* to achieve low distortion. The smooth limiting action of the positive temperature coefficient bulb in combination with the near ideal characteristics of the Wein network allow very high performance. The photo of *Figure 3* shows the output of the circuit of *Figure 2a*. The upper trace is the oscillator output. The middle trace is the downward slope of the waveform shown greatly expanded. The slight aberration is due to crossover distortion in the FET-input LF155. This crossover distortion is almost totally responsible for the sum of the measured 0.01% distortion in this oscillator. The output of the distortion analyzer is shown in the bottom trace. In the circuit of *Figure 2b*, an electronic equivalent of the light bulb is used to control loop gain. The zener diode determines the output amplitude and the loop time constant is set by the 1M-2.2 µF combination.

The 2N3819 FET, biased by the voltage across the 2.2 µF capacitor, is used to control the AC loop gain by shunting the feedback path. This circuit is more complex than *Figure 2a* but offers a way to control the loop time constant while maintaining distortion performance almost as good as in *Figure 2*.

Note: * Including William Hewlett and David Packard who built a few of these type circuits in a Palo Alto garage about forty years ago.

High Voltage AC Calibrator

Another dimension in sine wave oscillator design is stable control of amplitude. In this circuit, not only is the amplitude stabilized by servo control but voltage gain is included within the servo loop.

A 100 Vrms output stabilized to 0.025% is achieved by the circuit of *Figure 4*. Although complex in appearance this circuit requires just 3 IC packages. Here, a transformer is used to provide voltage gain within a tightly controlled servo loop. The LM3900 Norton amplifiers comprise a 1 kHz amplitude controllable oscillator. The LH0002 buffer provides low impedance drive to the LS-52 audio transformer. A voltage gain of 100 is achieved by driving the secondary of the transformer and taking the output from the primary. A current-sensitive negative absolute value amplifier composed of two amplifiers of an LF347 quad generates a negative rectified feedback signal. This is compared to the LM329 DC reference at the third LF347 which amplifies the difference at a gain of 100. The 10 µF feedback capacitor is used to set the frequency response of the loop. The output of this amplifier controls the amplitude of the LM3900 oscillator thereby closing the loop. As shown the circuit oscillates at 1 kHz with under 0.1% distortion for a 100 Vrms (285 Vp-p) output. If the summing resistors from the LM329 are replaced with a potentiometer the loop is stable for output settings ranging from 3 Vrms to 190 Vrms (542 Vp-p!) with no change in frequency. If the DAC1280 D/A converter shown in dashed lines replaces the LM329 reference, the AC output voltage can be controlled by the digital code input with 3 digit calibrated accuracy.

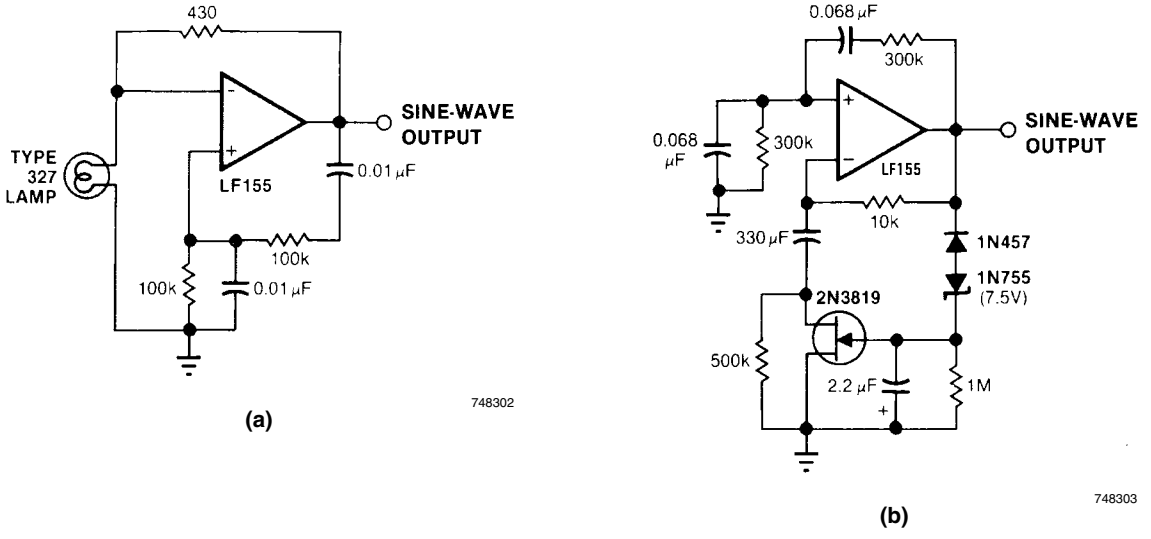
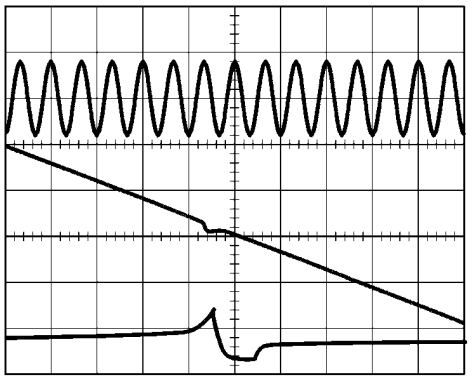


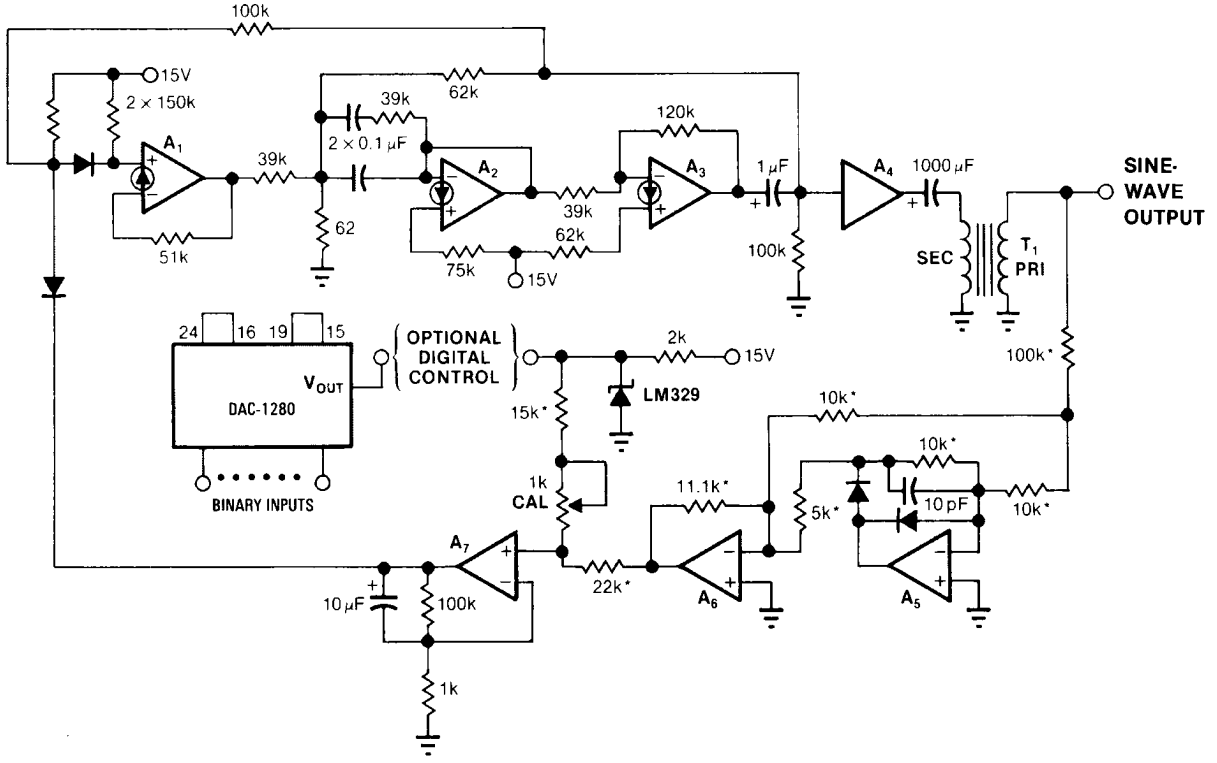
FIGURE 2. A basic Wein bridge design (a) employs a lamp's positive temperature coefficient to achieve amplitude stability. A more complex version (b) provides the same feature with the additional advantage of loop time-constant control.



Trace	Vertical	Horizontal
Top	10V/DIV	10 ms/DIV
Middle	1V/DIV	500 ns/DIV
Bottom	0.5V/DIV	500 ns/DIV

748304

FIGURE 3. Low-distortion output (top trace) is a Wein bridge oscillator feature. The very low crossover distortion level (middle) results from the LF155's output stage. A distortion analyzer's output signal (bottom) indicates this design's 0.01% distortion level.



748305

A1–A3 = ¼ LM3900
A4 = LH0002
A5–A7 = ¼ LF347
T1 = UTC LS-52
All diodes = 1N914
* = low-TC, metal-film types

FIGURE 4. Generate high-voltage sine waves using IC-based circuits by driving a transformer in a step-up mode. You can realize digital amplitude control by replacing the LM329 voltage reference with the DAC1287.

Negative Resistance Oscillator

All of the preceding circuits rely on RC time constants to achieve resonance. LC combinations can also be used and offer good frequency stability, high Q and fast starting.

In *Figure 5* a negative resistance configuration is used to generate the sine wave. The Q1-Q2 pair provides a 15 µA current source. Q2's collector current sets Q3's peak collector current. The 300 kΩ resistor and the Q4-Q5 LM394 matched pair accomplish a voltage-to-current conversion that decreases Q3's base current when its collector voltage rises. This negative resistance characteristic permits oscillation. The frequency of operation is determined by the LC in the Q3-Q5 collector line. The LF353 FET amplifier provides gain and buffering. Power supply dependence is eliminated by the zener diode and the LF353 unity gain follower. This circuit starts quickly and distortion is inside 1.5%.

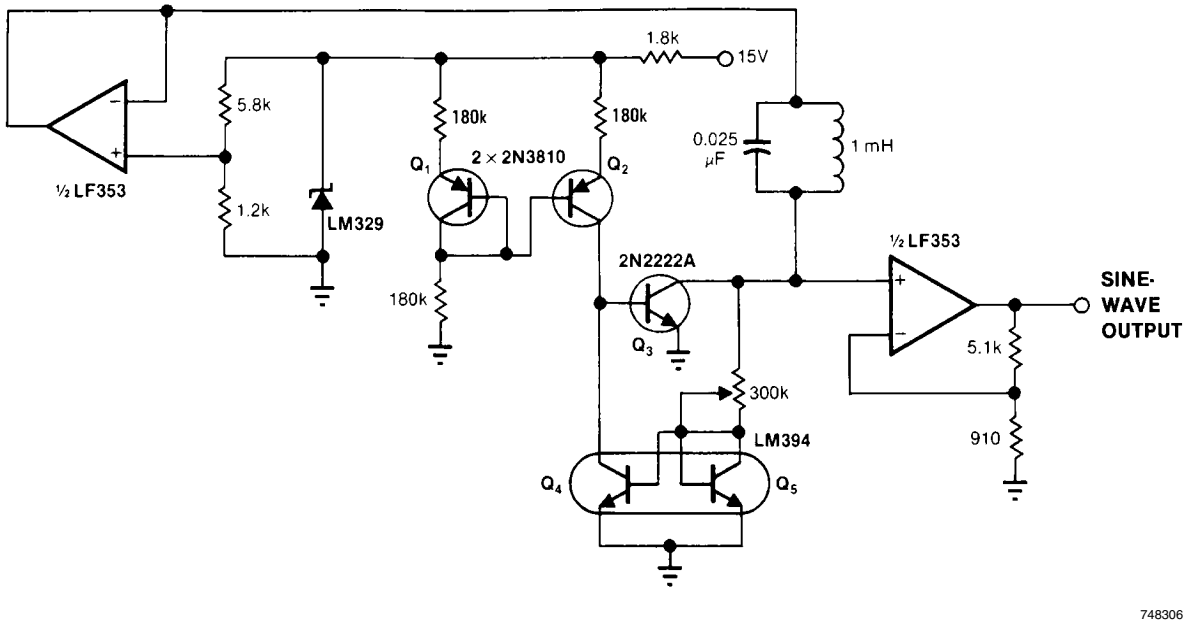
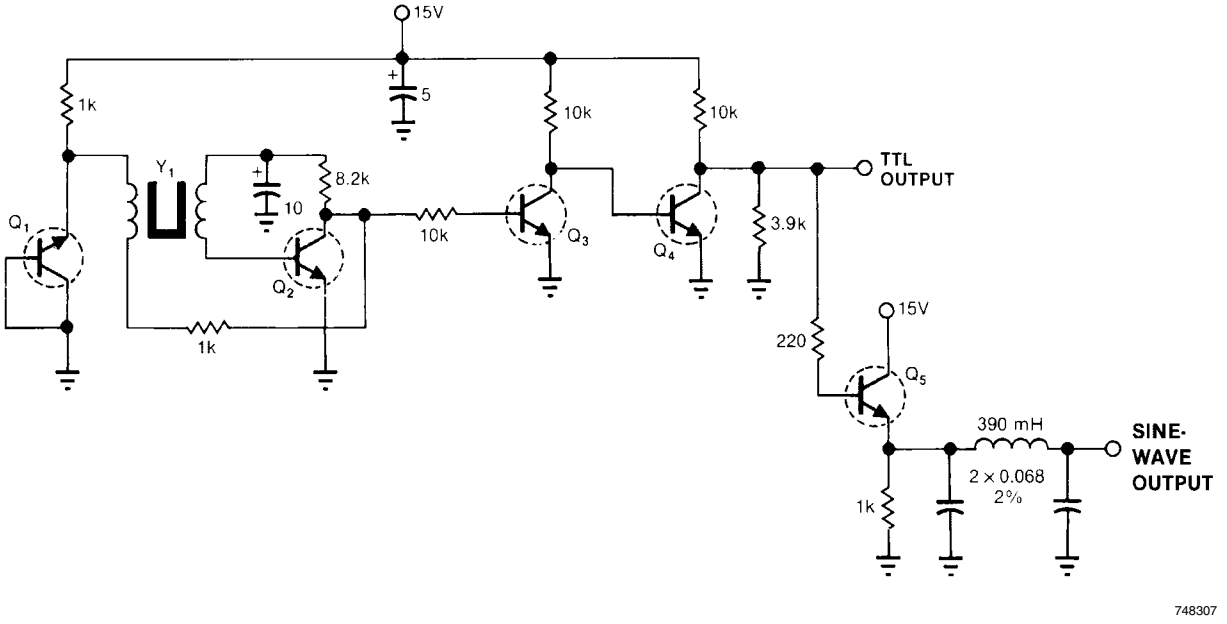


FIGURE 5. LC sine wave sources offer high stability and reasonable distortion levels. Transistors Q1 through Q5 implement a negative-resistance amplifier. The LM329, LF353 combination eliminates power-supply dependence.

Resonant Element Oscillator—Tuning Fork

All of the above oscillators rely on combinations of passive components to achieve resonance at the oscillation frequency. Some circuits utilize inherently resonant elements to achieve very high frequency stability. In *Figure 6* a tuning fork is used in a feedback loop to achieve a stable 1 kHz output. Tuning fork oscillators will generate stable low frequency sine outputs under high mechanical shock conditions which would fracture a quartz crystal.

Because of their excellent frequency stability, small size and low power requirements, they have been used in airborne applications, remote instrumentation and even watches. The low frequencies achievable with tuning forks are not available from crystals. In *Figure 6*, a 1 kHz fork is used in a feedback configuration with Q2, one transistor of an LM3045 array. Q1 provides zener drive to the oscillator circuit. The need for amplitude stabilization is eliminated by allowing the oscillator to go into limit. This is a conventional technique in fork oscillator design. Q3 and Q4 provide edge speed-up and a 5V output for TTL compatibility. Emitter follower Q5 is used to drive an LC filter which provides a sine wave output. *Figure 7*, trace A shows the square wave output while trace B depicts the sine wave output. The 0.7% distortion in the sine wave output is shown in trace C, which is the output of a distortion analyzer.

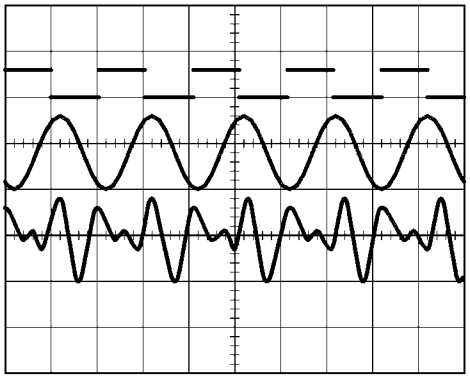


Q1–Q5 = LM3045 array

Y1 = 1 kHz tuning fork, Fork Standards Inc.

All capacitors in µF

FIGURE 6. Tuning fork based oscillators don't inherently produce sinusoidal outputs. But when you do use them for this purpose, you achieve maximum stability when the oscillator stage (Q1, Q2) limits. Q3 and Q4 provide a TTL compatible signal, which Q5 then converts to a sine wave.



748308

Trace	Vertical	Horizontal
Top	5V/DIV	500 µs/DIV
Middle	50V/DIV	
Bottom	0.2V/DIV	

FIGURE 7. Various output levels are provided by the tuning fork oscillator shown in *Figure 6*. This design easily produces a TTL compatible signal (top trace) because the oscillator is allowed to limit. Low-pass filtering this square wave generates a sine wave (middle). The oscillator's 0.7% distortion level is indicated (bottom) by an analyzer's output.

Resonant Element Oscillator—Quartz Crystal

Quartz crystals allow high frequency stability in the face of changing power supply and temperature parameters. *Figure 8a* shows a simple 100 kHz crystal oscillator. This Colpitts class circuit uses a JFET for low loading of the crystal, aiding stability. Regulation will eliminate the small effects (~ 5 ppm for 20% shift) that supply variation has on this circuit. Shunting the crystal with a small amount of capacitance allows very fine trimming of frequency. Crystals typically drift less than 1 ppm/°C and temperature controlled ovens can be used to eliminate this term (*Figure 8b*). The RC feedback values will depend upon the thermal time constants of the oven used. The values shown are typical. The temperature of the oven should be set so that it coincides with the crystal's zero temperature coefficient or "turning point" temperature which is manufacturer specified. An alternative to temperature control uses a varactor diode placed across the crystal. The varactor is biased by a temperature dependent voltage from a circuit which could be very similar to *Figure 8b* without the output transistor. As ambient temperature varies the circuit changes the voltage across the varactor, which in turn changes its capacitance. This shift in capacitance trims the oscillator frequency.

Approximation Methods

All of the preceding circuits are *inherent* sine wave generators. Their normal mode of operation supports and maintains a sinusoidal characteristic. Another class of oscillator is made up of circuits which *approximate* the sine function through a variety of techniques. This approach is usually more complex but offers increased flexibility in controlling amplitude and frequency of oscillation. The capability of this type of circuit for a digitally controlled interface has markedly increased the popularity of the approach.

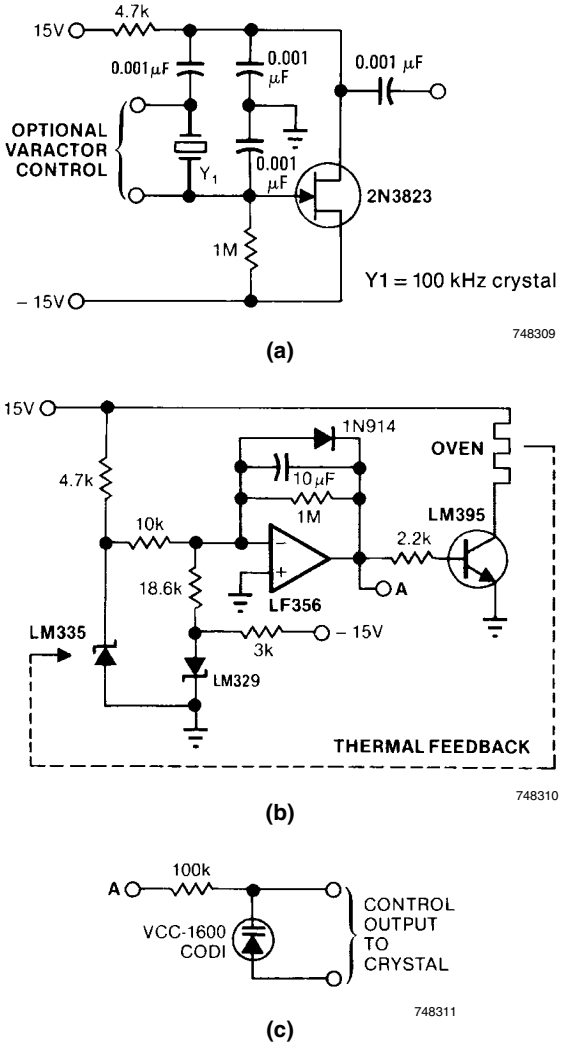
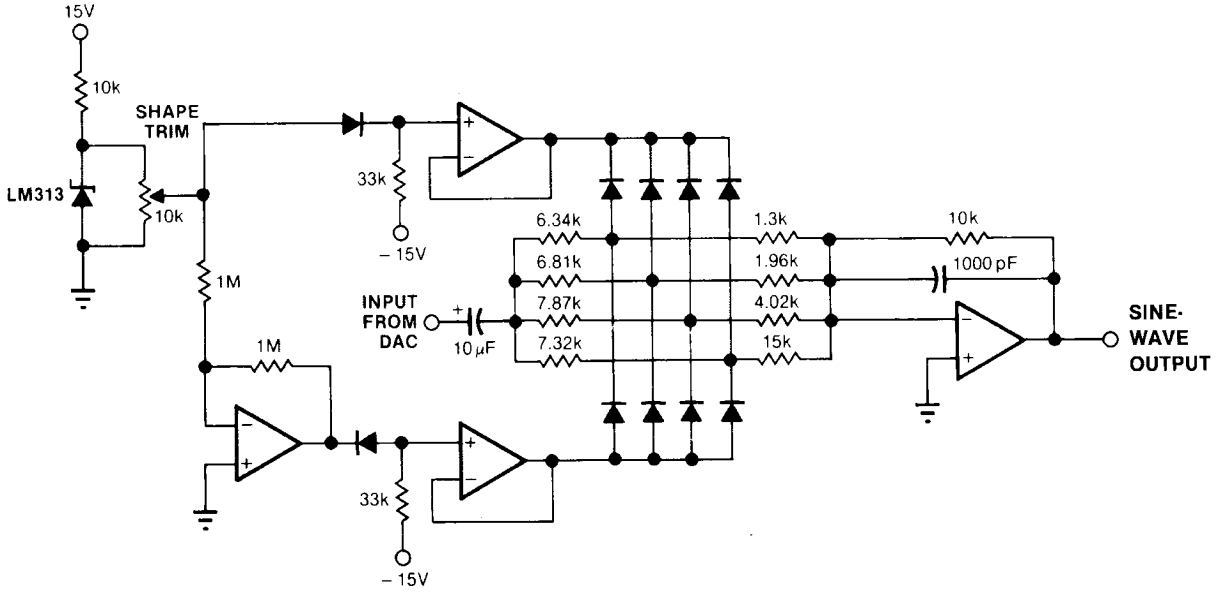


FIGURE 8. Stable quartz-crystal oscillators can operate with a single active device (a). You can achieve maximum frequency stability by mounting the oscillator in an oven and using a temperature-controlling circuit (b). A varactor network (c) can also accomplish crystal fine tuning. Here, the varactor replaces the oven and retunes the crystal by changing its load capacitances.

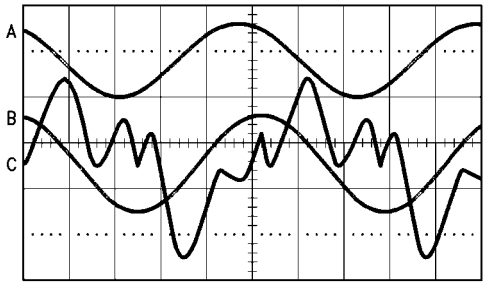
Sine Approximation—Breakpoint Shaper

Figure 9 diagrams a circuit which will "shape" a 20 Vp-p wave input into a sine wave output. The amplifiers serve to establish stable bias potentials for the diode shaping network. The shaper operates by having individual diodes turn on or off depending upon the amplitude of the input triangle. This changes the gain of the output amplifier and gives the circuit its characteristic non-linear, shaped output response. The values of the resistors associated with the diodes determine the shaped waveform's appearance. Individual diodes in the DC bias circuitry provide first order temperature compensation for the shaper diodes. *Figure 10* shows the circuit's performance. Trace A is the filtered output (note 1000 pF capacitor across the output amplifier). Trace B shows the waveform with no filtering (1000 pF capacitor removed) and trace C is the output of a distortion analyzer. In trace B the breakpoint action is just detectable at the top and bottom of the waveform, but all the breakpoints are clearly identifiable in the distortion analyzer output of trace C. In this circuit, if the amplitude or symmetry of the input triangle wave shifts, the output waveform will degrade badly. Typically, a D/A converter will be used to provide input drive. Distortion in this circuit is less than 1.5% for a filtered output. If no filter is used, this figure rises to about 2.7%.



All diodes = 1N4148
All op amps = ¼ LF347

FIGURE 9. Breakpoint shaping networks employ diodes that conduct in direct proportion to an input triangle wave's amplitude. This action changes the output amplifier's gain to produce the sine function.



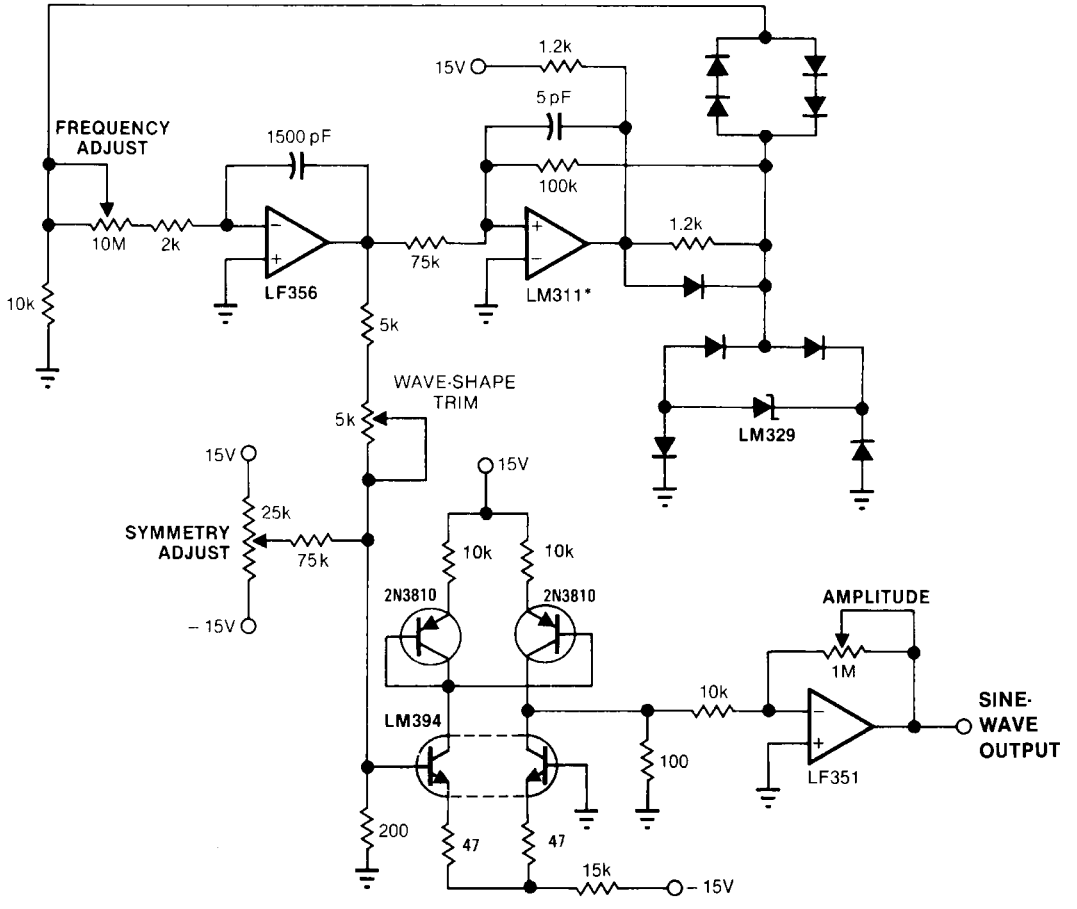
748313

Trace	Vertical	Horizontal
A	5V/DIV	20 µs/DIV
B	5V/DIV	
C	0.5V/DIV	

FIGURE 10. A clean sine wave results (trace A) when *Figure 9* circuit's output includes a 1000 pF capacitor. When the capacitor isn't used, the diode network's breakpoint action becomes apparent (trace B). The distortion analyzer's output (trace C) clearly shows all the breakpoints.

Sine Approximation—Logarithmic Shaping

Figure 11 shows a complete sine wave oscillator which may be tuned from 1 Hz to 10 kHz with a single variable resistor. Amplitude stability is inside 0.02%/°C and distortion is 0.35%. In addition, desired frequency shifts occur instantaneously because no control loop time constants are employed. The circuit works by placing an integrator inside the positive feedback loop of a comparator. The LM311 drives symmetrical, temperature-compensated clamp arrangement. The output of the clamp biases the LF356 integrator. The LF356 integrates this current into a linear ramp at its output. This ramp is summed with the clamp output at the LM311 input. When the ramp voltage nulls out the bound voltage, the comparator changes state and the integrator output reverses. The resultant, repetitive triangle waveform is applied to the sine shaper configuration. The sine shaper utilizes the non-linear, logarithmic relationship between V_{be} and collector current in transistors to smooth the triangle wave. The LM394 dual transistor is used to generate the actual shaping while the 2N3810 provides current drive. The LF351 allows adjustable, low impedance, output amplitude control. Waveforms of operation are shown in *Figure 14*.

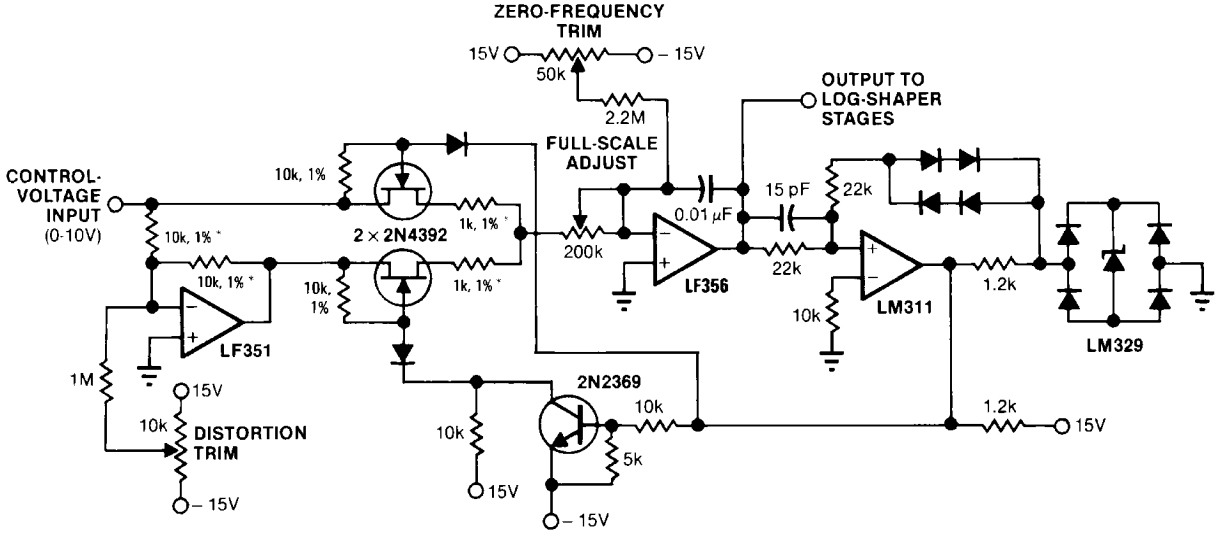


All diodes = 1N4148
Adjust symmetry and wave-shape controls for minimum distortion
* LM311 Ground Pin (Pin 1) at –15V

FIGURE 11. Logarithmic shaping schemes produce a sine wave oscillator that you can tune from 1 Hz to 10 kHz with a single control. Additionally, you can shift frequencies rapidly because the circuit contains no control-loop time constants.

Sine Approximation—Voltage Controlled Sine Oscillator

Figure 12 details a modified but extremely powerful version of *Figure 11*. Here, the input voltage to the LF356 integrator is furnished from a control voltage input instead of the zener diode bridge. The control input is inverted by the LF351. The two complementary voltages are each gated by the 2N4393 FET switches, which are controlled by the LM311 output. The frequency of oscillation will now vary in direct proportion to the control input. In addition, because the amplitude of this circuit is controlled by limiting, rather than a servo loop, response to a control step or ramp input is almost instantaneous. For a 0V–10V input the output will run over 1 Hz to 30 kHz with less than 0.4% distortion. In addition, linearity of control voltage vs output frequency will be within 0.25%. *Figure 13* shows the response of this circuit (waveform B) to a 10V ramp (waveform A).



Adjust distortion for minimum at 1 Hz to 10 Hz
Adjust full-scale for 30 kHz at 10V input
All diodes = 1N4148
* Match to 0.1%

FIGURE 12. A voltage-tunable oscillator results when *Figure 11's* design is modified to include signal-level-controlled feedback. Here, FETs switch the integrator's input so that the resulting summing-junction current is a function of the input control voltage. This scheme realizes a frequency range of 1 Hz to 30 kHz for a 0V to 10V input.

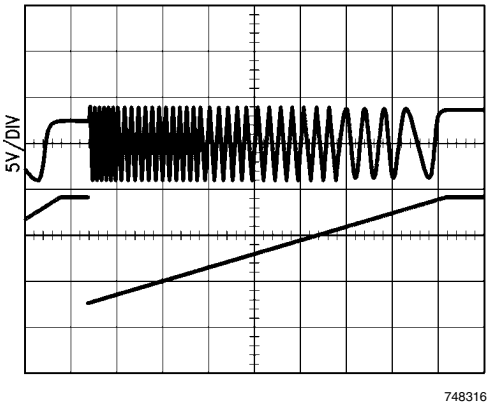
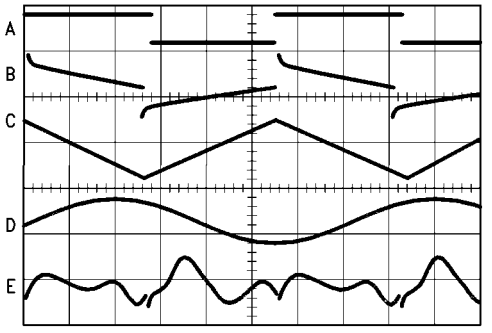


FIGURE 13. Rapid frequency sweeping is an inherent feature of *Figure 12's* voltage-controlled sine wave oscillator. You can sweep this VCO from 1 Hz to 30 kHz with a 10V input signal; the output settles quickly.

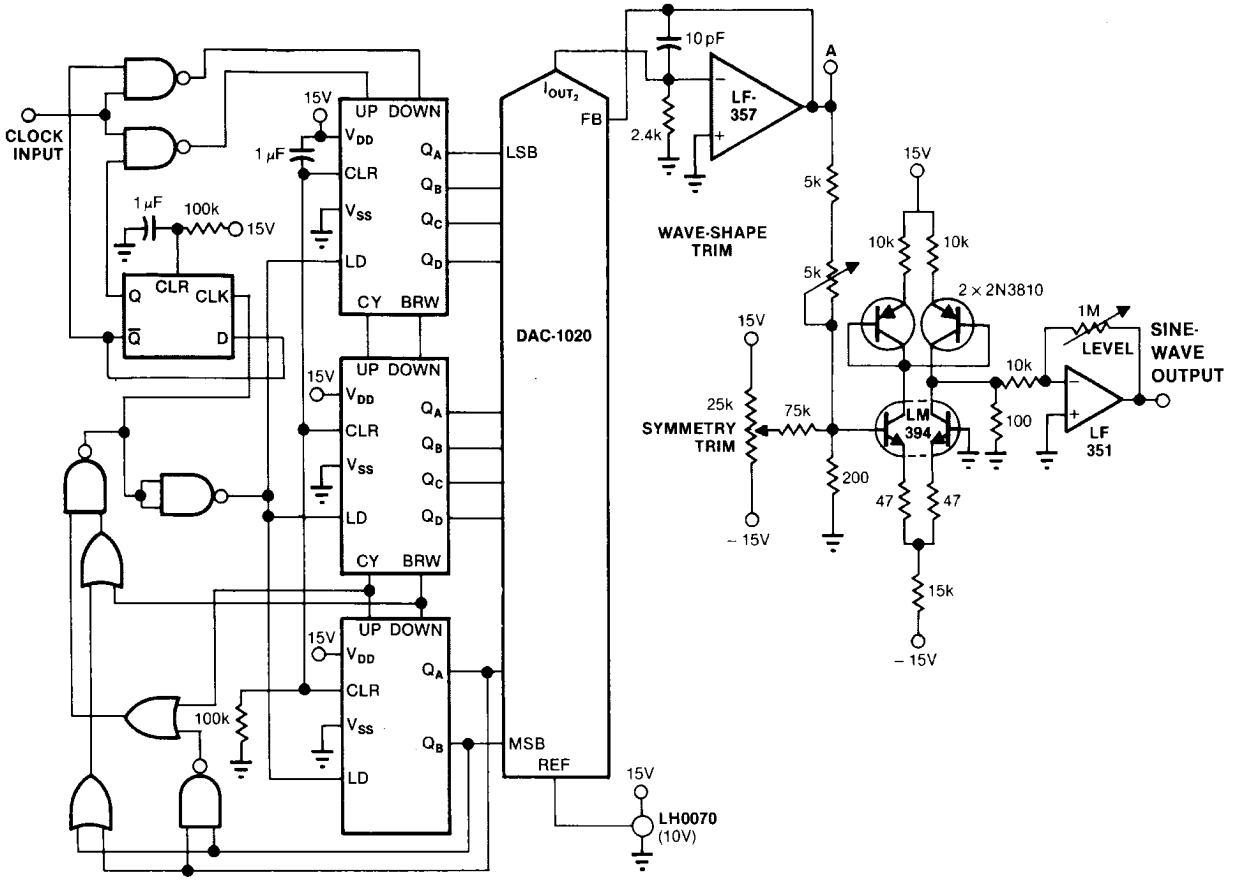
Sine Approximation—Digital Methods

Digital methods may be used to approximate sine wave operation and offer the greatest flexibility at some increase in complexity. *Figure 15* shows a 10-bit IC D/A converter driven from up/down counters to produce an amplitude-stable triangle current into the LF357 FET amplifier. The LF357 is used to drive a shaper circuit of the type shown in *Figure 11*. The output amplitude of the sine wave is stable and the frequency is solely dependent on the clock used to drive the counters. If the clock is crystal controlled, the output sine wave will reflect the high frequency stability of the crystal. In this example, 10 binary bits are used to drive the DAC so the output frequency will be 1/1024 of the clock frequency. If a sine coded read-only-memory is placed between the counter outputs and the DAC, the sine shaper may be eliminated and the sine wave output taken directly from the LF357. This constitutes an extremely powerful digital technique for generating sine waves. The amplitude may be voltage controlled by driving the reference terminal of the DAC. The frequency is again established by the clock speed used and both may be varied at high rates of speed without introducing significant lag or distortion. Distortion is low and is related to the number of bits of resolution used. At the 8-bit level only 0.5% distortion is seen (waveforms, *Figure 16*; graph, *Figure 17*) and filtering will drop this below 0.1%. In the photo of *Figure 16* the ROM directed steps are clearly visible in the sine waveform and the DAC levels and glitching show up in the distortion analyzer output. Filtering at the output amplifier does an effective job of reducing distortion by taking out these high frequency components.



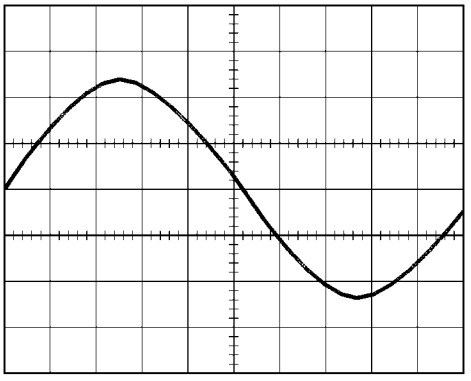
Trace	Vertical	Horizontal
A	20V/DIV	20 µs/DIV
B	20V/DIV	
C	10V/DIV	
D	10V/DIV	
E	0.5V/DIV	

FIGURE 14. Logarithmic shapers can utilize a variety of circuit waveforms. The input to the LF356 integrator (*Figure 11*) appears here as trace A. The LM311's input (trace B) is the summed result of the integrator's triangle output (C) and the LM329's clamped waveform. After passing through the 2N3810/LM394 shaper stage, the resulting sine wave is amplified by the LF351 (D). A distortion analyzer's output (E) represents a 0.35% total harmonic distortion.



MM74C00 = NAND
MM74C32 = OR
MM74C74 = D flip-flop
MM74193 = counters

FIGURE 15. Digital techniques produce triangular waveforms that methods employed in *Figure 11* can then easily convert to sine waves. This digital approach divides the input clock frequency by 1024 and uses the resultant 10 bits to drive a DAC. The DAC's triangular output—amplified by the LF357—drives the log shaper stage. You could also eliminate the log shaper and place a sine-coded ROM between the counters' outputs and the DAC, then recover the sine wave at point A.



Trace	Vertical	Horizontal
Sine Wave	1V/DIV	200 µs/DIV
Analyzer	0.2V/DIV	

FIGURE 16. An 8-bit sine coded ROM version of *Figure 15's* circuit produces a distortion level less than 0.5%. Filtering the sine output—shown here with a distortion analyzer's trace—can reduce the distortion to below 0.1%.

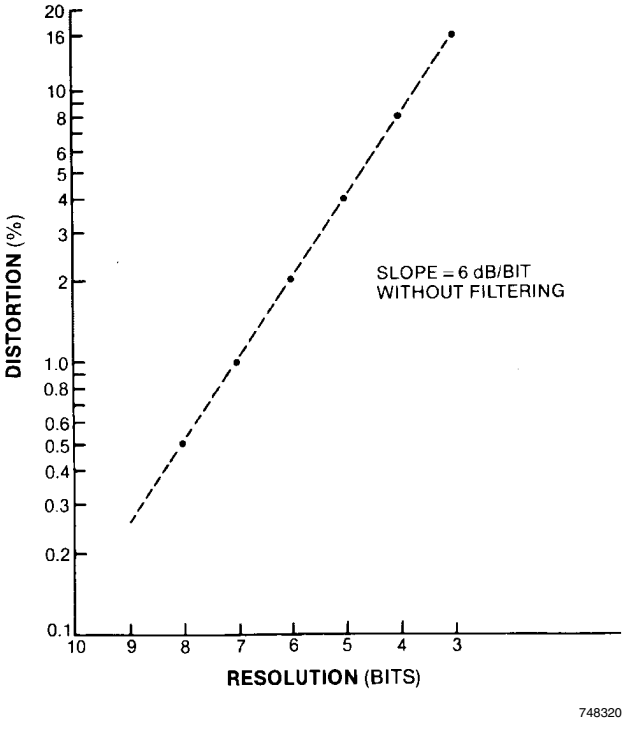


FIGURE 17. Distortion levels decrease with increasing digital word length. Although additional filtering can considerably improve the distortion levels (to 0.1% from 0.5% for the 8-bit case), you're better off using a long digital word.

Applications of Audio Amplifier—Transistor Array ICs

National Semiconductor
Application Note 264

The availability of extremely low cost audio amplifier ICs with on-chip transistor arrays allows designers a great deal of flexibility in designing audio circuits. The availability of the uncommitted transistors on the chip makes it easier and more economical to implement audio functions. One chip, the LM389, features a 250 mW audio amplifier and a 3 NPN transistor array (see "The LM389 Audio Amplifier—Transistor Array IC" drawing). The amplifier has differential inputs, separate pins for setting the gain via a resistor and runs from a single supply which may range from 4V to 15V. The 3 transistors have good beta over a wide range of collector currents and current handling capability of 25 mA. This combination of devices and features on a single, low priced chip suggests that application areas unrelated to audio can be served. A good example appears in *Figure 1*.

DC-DC CONVERTER

The circuit in *Figure 1* uses the LM389 to provide a fully isolated ±15V supply from a 5V line. This is useful in powering op amps and related circuitry in a primarily digital system. This circuit is intended for use in a digital system where it is necessary to supply ±15V power to a small, low power load. Although units are available which will do this, they are designed to supply much more power than is required for many applications and are quite expensive. In this circuit, the LM389 amplifier is set up to oscillate at 20 kHz (Trace

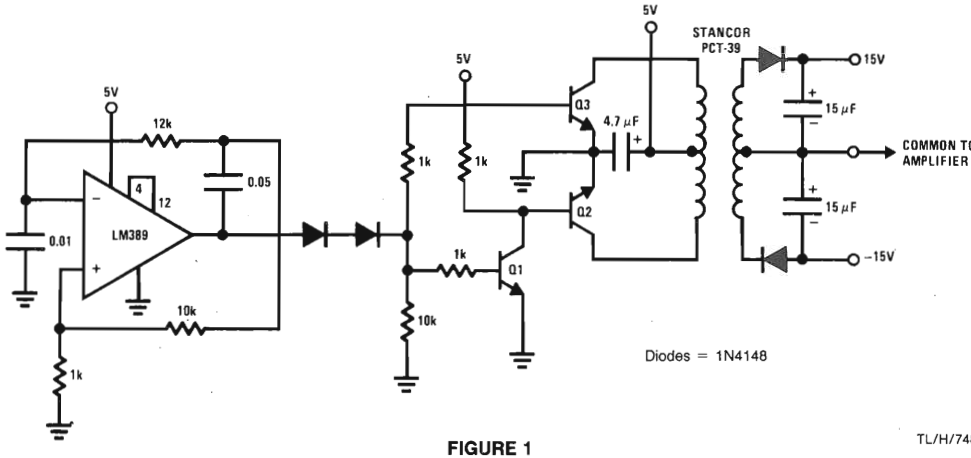
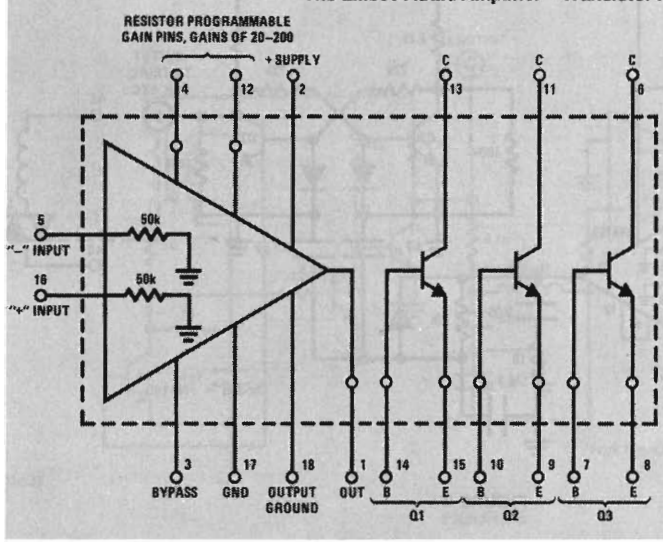


FIGURE 1

TL/H/7484–1

The LM389 Audio Amplifier—Transistor Array IC



- The gain pins allow resistive programming of gains from 20 to 200.
- The bypass pin may be connected to ground through a 10 μF capacitor for increased supply rejection.
- The three transistors have a minimum beta of 100 over a wide range of collector current. V_{CE} = 12V minimum.
- Output (high current) ground should be returned directly to power supply ground.

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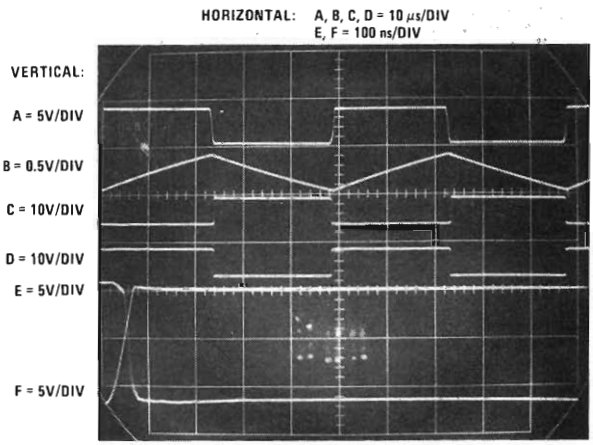
A, *Figure 2*). Each time the amplifier output changes state, the charging voltage supplied to the 0.01 μF capacitor reverses polarity, resulting in a triangle at the amplifier's negative input (Trace B, *Figure 2*). When the triangle potential crosses the voltage at the positive input, the output again changes state. The 20 kHz square wave output is fed to Q1 and Q3. The series diodes insure clean turn-off for Q1 and Q3. Q1's inverted output drives Q2 while Q3 is used to drive half the transformer primary (Trace C, *Figure 2*). Q2 drives the other half of the transformer primary out of phase because of Q1's inversion (Trace D, *Figure 2*). The saturated switching of Q3 and Q2 is fast and clean (Q2 = Trace E, *Figure 2*; Q3 = Trace F, *Figure 2*; note horizontal sweep speed change) and results in an efficient voltage step-up across the transformer. The transformer output is rectified and filtered to produce complementary voltages which may be used to power the required linear components. This circuit will deliver ±1.5 mA, enough to power an op amp or instrumentation amplifier in a signal conditioning application.

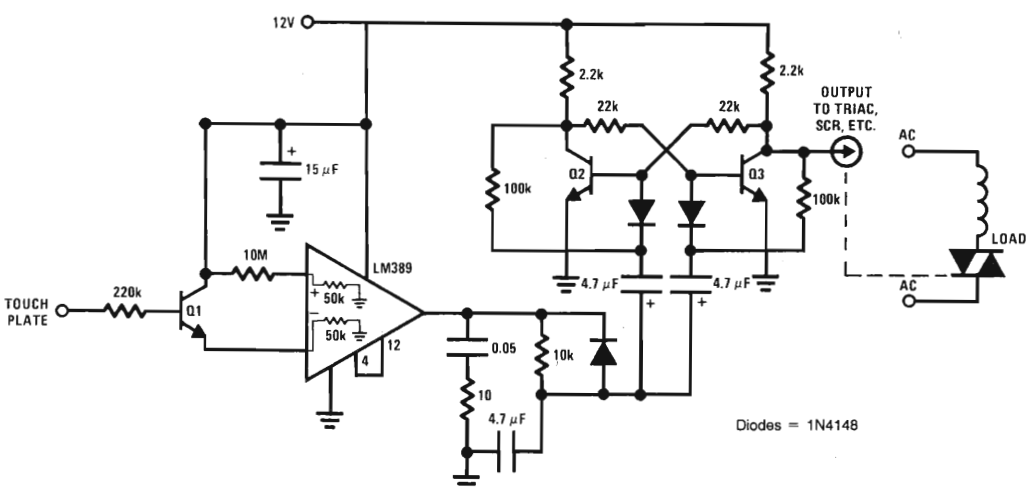
BI-STABLE TOUCH SWITCH

The circuit of *Figure 3* allows a 115 V_{AC} powered load to be controlled from a touch plate. The circuit's output is bi-stable and changes state each time the plate is touched. In operation, each time the touch plate is contacted the Q1 emitter follower conducts and its output is amplified by the LM389's amplifier, whose normally positive output (note the 10 MΩ bias resistor to "+" input) becomes a 60 Hz square wave. This causes the potential at the output of the 10 kΩ-4.7 μF filter to jump sharply negative and remain there as long as the plate is touched. This negative step triggers a toggling flip-flop comprised of the remaining Q2 and Q3 LM389 transistors. In this manner, each time the touch plate is contacted the output of the flip-flop changes state. The flip-flop output is used to control a Triac or SCR which switches AC power to the load.



TL/H/7484–3

FIGURE 2



TL/H/7484–4

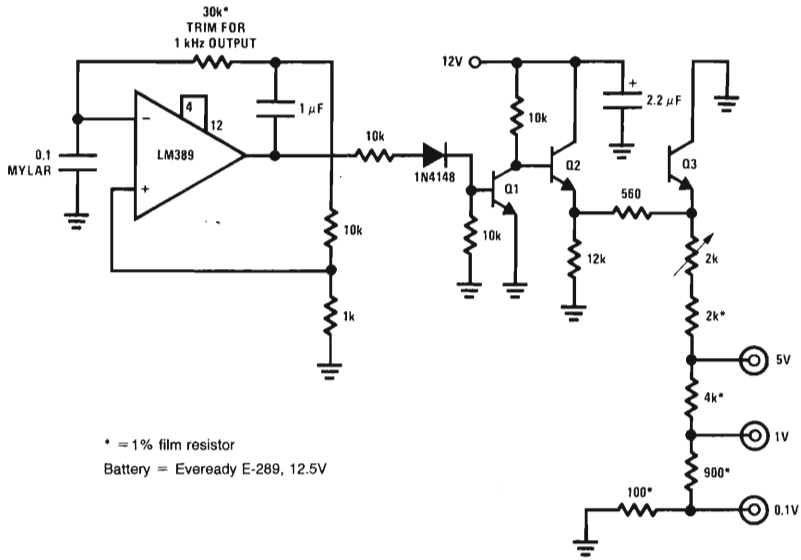
FIGURE 3

PORTABLE OSCILLOSCOPE CALIBRATOR

The circuit shown in *Figure 4* allows a quick check of an oscilloscope's time base and vertical calibration. It may be built into a small hand-held box and powered by a 12.5V battery, such as an Eveready type E-289. In this circuit the amplifier oscillates at 1 kHz. The 30 kΩ value should be trimmed for a precise (±5 Hz) 1 kHz output. The amplifier output drives Q1 which provides very fast edges at Q2's base. Q2, an emitter follower, is used to drive Q3, which is connected in inverse mode and functions as a zener diode. Q3's breakdown potential is scaled by the 2k potentiometer to provide a 5.00V high square wave at the 5V output tap. The remaining resistors in the string furnish the 1V and 0.1V outputs. The 1 MΩ oscilloscope impedance does not introduce any appreciable loading error.

TUNING FORK STABILIZED FREQUENCY STANDARD

Figure 5 shows a circuit which provides a low frequency tuning fork stabilized output. Both sine wave and TTL compatible outputs are available. The circuit runs from 5V, which could be battery derived, due to the low power consumption. The tuning fork provides a direct low frequency output with very high stability (typically 5 ppm/°C) with an initial accuracy of 0.01%. It will withstand vibration and shock which would fracture a quartz crystal. Q3 is set up in a feedback configuration which forces the tuning fork to oscillate at its resonant frequency. The signal at Q3's collector is squared up by Q1 and Q2, which provide a TTL compatible square wave at Q2's collector (Trace A, *Figure 6*). This square wave is also used to drive an LC filter whose output is a sine wave. The filter's output is unity gain amplified



TL/H/7484–5

FIGURE 4

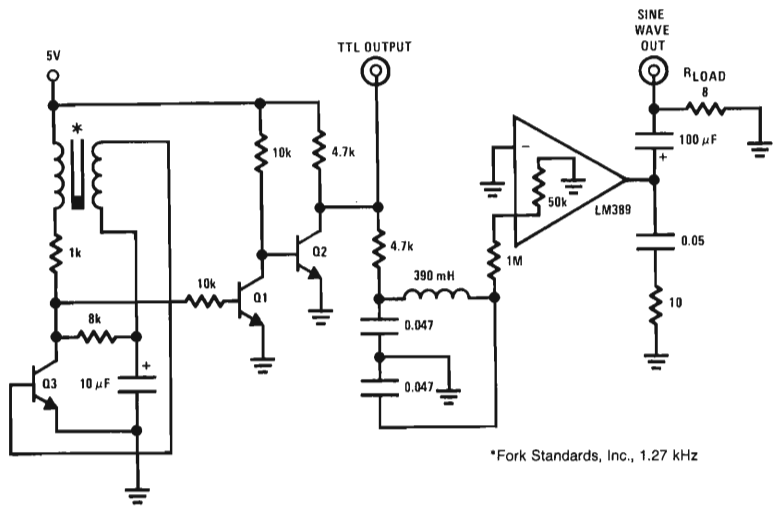


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FIGURE 5

by the amplifier to provide a low impedance output (Trace B, *Figure 6*). The amplifier, which has a minimum gain of 20, is made to achieve apparent unity gain by the voltage divider created between the internal 50 kΩ resistor and the 1 MΩ unit in series with the positive input. The circuit's sine wave output, which will drive an 8Ω load, has less than 1% distortion. Trace C, *Figure 6* shows the output of a distortion analyzer connected to the sine wave output.

LOW DISTORTION OSCILLATOR

In *Figure 7*, the LM389 is used to produce a low distortion sine wave and a synchronous in-phase wave output is also provided. The circuit's 1/4W output drive capability allows it to drive loads such as transducer bridges. In such applications, the in-phase square wave output can be used to drive synchronous demodulation switches. The oscillator's low distortion (0.2%) is directly traceable to the use of a light bulb which provides smooth amplitude limiting for the Wein bridge network at the amplifier. In this example, oscillation frequency is 1 kHz. The in-phase square wave output is provided by the three transistors. Q1, operating in the common base configuration, is based by the diode drop and the 100Ω potentiometer. The resultant square wave at Q1's collector is used to drive the Q2-Q3 common emitter stages which provide edge speed-up. The potentiometer is adjusted so that the edges of the output square wave precisely line up with the zero crossings of the sine wave.

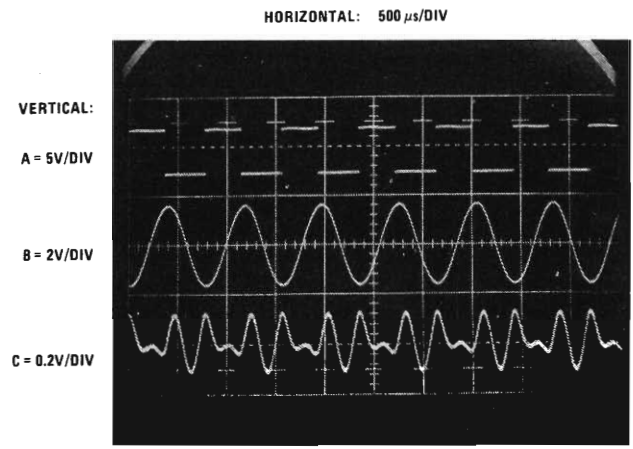

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FIGURE 6

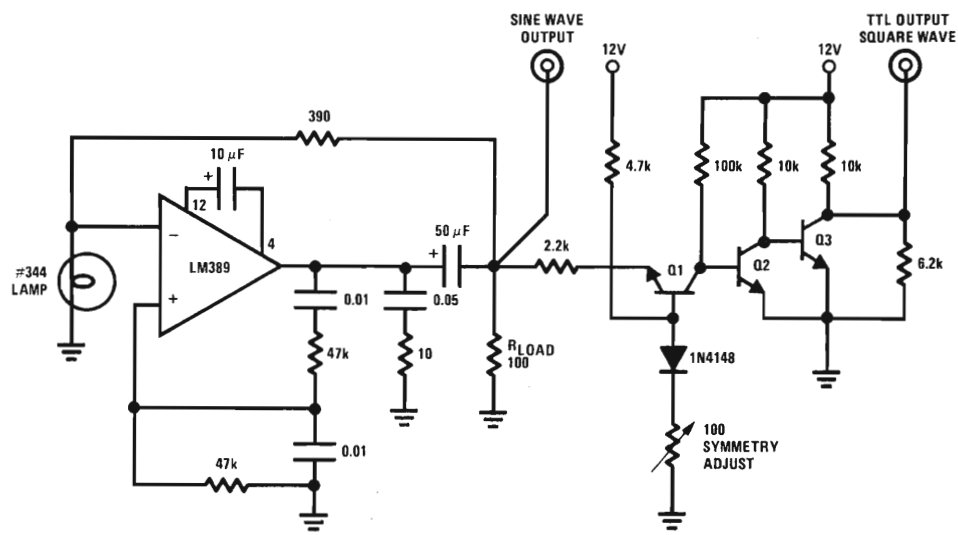

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FIGURE 7

LOGARITHMIC AMPLIFIER

In *Figure 8*, the LM389 is used in an unorthodox fashion to build a logarithmic amplifier which eliminates the usual complex and expensive temperature compensation associated with such circuits. This allows the cost of the logarithmic amplifier function to be reduced by an order of magnitude compared to conventional approaches. Q3 functions as a chip temperature sensor while Q2 serves as a heater. The amplifier senses the temperature dependent V_{BE} of Q3 and drives Q2 to servo the chip temperature to the set point established by the 10 kΩ-1 kΩ divider string. The LM329 reference insures power supply independence of the temperature control. Q1, the logging transistor, operates in this tightly controlled thermal environment (typically 50°C) and is immune to ambient temperature shifts. The LM340L 12V regulator insures safe operation of the LM389, a 12V device. When the circuit is first turn ON, the voltage Q2's emitter is about 3.3V resulting in a current flow of 120 mA. This forces Q2 to dissipate about 1.5W which raises the chip to operating temperature very rapidly. At this point the thermal servo takes control and backs the power down. The LM340L regulator has only 3V across it, so dissipation never exceeds more than about 0.3W. The zener at the base of Q2 prevents servo lock-up during circuit start-up. Because of the small size of the chip, warmup is quick and power consumption low.

To adjust this circuit, ground the base of Q2, apply circuit power and measure the collector potential of Q3 at known room temperature. Next, calculate what Q3's collector potential will be at 50°C, allowing −2.2 mV/°C. Select the 1k value to yield a voltage close to the calculated 50°C potential at the LM389's negative input. This can be a fairly loose trim, as the exact chip temperature is unimportant, so long as it is stable. Finally, unground Q2's base and the circuit will servo. This may be functionally checked by reading Q3's collector voltage and noting stability within 100 μV (0.05°C) while blowing on A3.

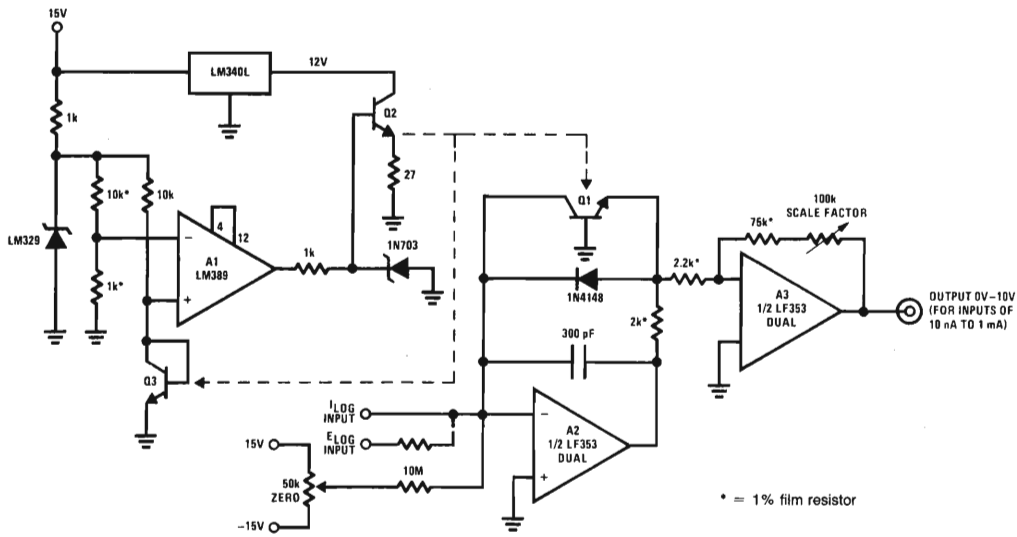

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FIGURE 8

An Electronic Watt-Watt-Hour Meter

National Semiconductor
Application Note 265
February 1984

The continued emphasis on energy conservation has forced designers to consider the power consumption and efficiency of their products. While equipment for the industrial market must be designed with attention towards these factors, the consumer area is even more critical. The high cost of electricity has promoted a great deal of interest in the expense of powering various appliances. The watt-watt-hour meter outlined in *Figure 1* allows the designer to easily determine power consumption of any 115V AC powered device. The extremely wide dynamic range of the design allows measurement of loads ranging from 0.1W to 2000W.

Conceptually, the instrument is quite straightforward (*Figure 1*). The device to be monitored is plugged into a standard 110V AC outlet which is mounted on the front panel of the instrument. The AC line voltage across the monitored load is divided down and fed via an op amp to one input of a 4-quadrant analog multiplier. The current through the load is determined by the voltage across a low resistance shunt. Even at 20A the shunt "steals" only 133 mV, eliminating the inaccuracies a high resistance current shunt would contribute. This single shunt is used for all ranges, eliminating the need to switch in high impedance shunts to obtain adequate signal levels on the high sensitivity scales.

This provision is made possible by low uncertainty in the current amplifier, whose output feeds the other multiplier input. Switchable gain at the current amplifier allows decade setting of instrument sensitivity. The instantaneous power product (E x I) drawn by the load is represented by the multiplier output. Because the multiplier is a 4-quadrant type, its output will be a true reflection of load power consumption, regardless of the phase relationship between voltage and current in the load. Because the multiplier and its associated amplifiers are connected directly to the AC line, they must be driven from a floating power supply. In addition, their outputs cannot be safely monitored with grounded test equipment, such as strip chart recorders. For this reason, the multiplier output drives an isolation amplifier which operates at unity gain but has no galvanic connection between its input and output terminals.

This feature is accomplished through pulse amplitude modulation techniques in conjunction with a small transformer, which provides isolation. The isolated amplifier output is ground referenced and may safely be connected to any piece of test equipment. This output is filtered to provide a strip chart output and drive the readout meter, both of which indicate load power consumption. The isolation amplifier output also biases a voltage-to-frequency converter which combines with digital counters to form a digital integrator. This allows power over time (watt-hours) to be integrated and displayed. Varying the divide ratio of the counters produces ranging of the watt-hour function.

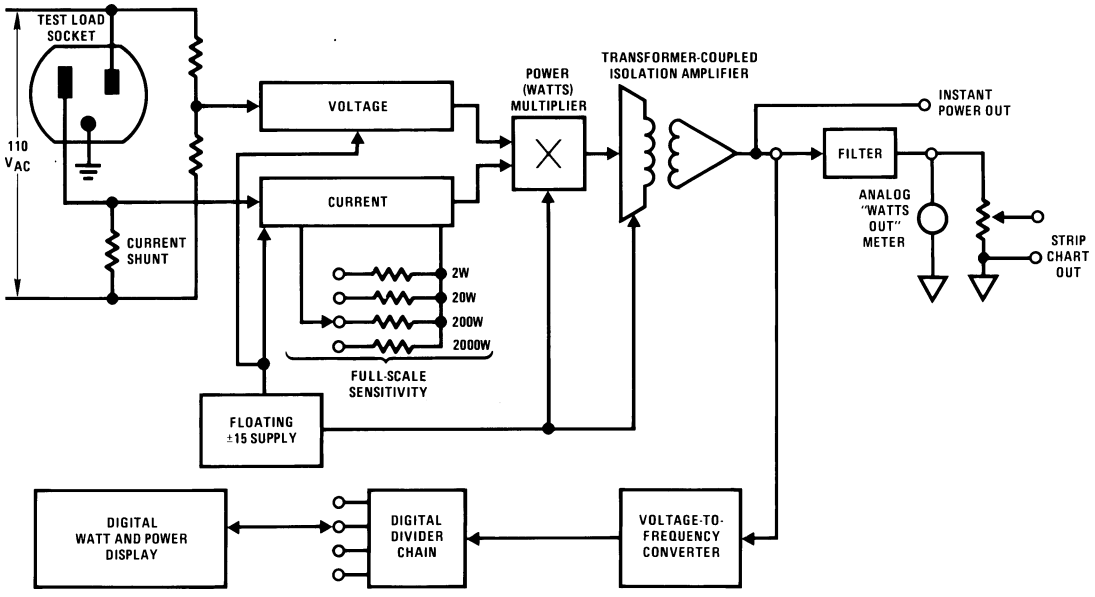
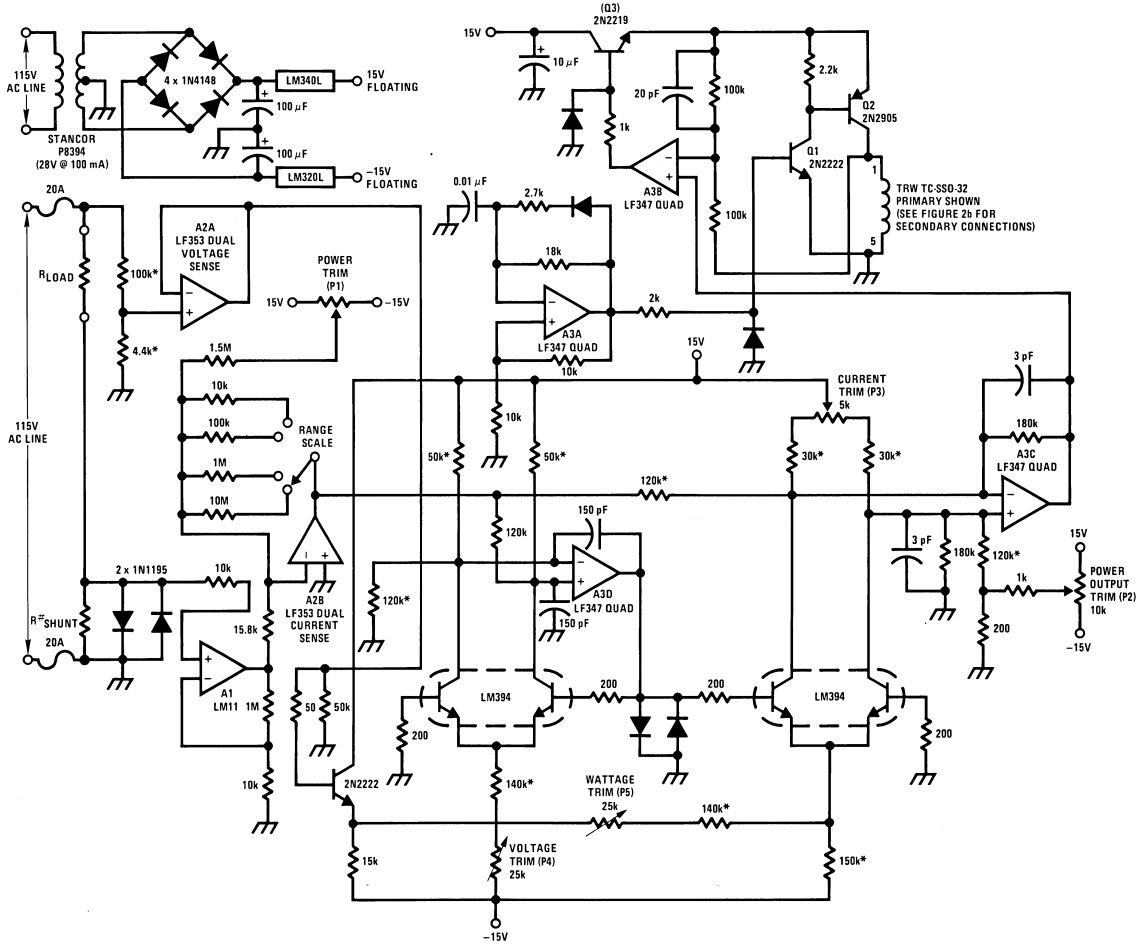


FIGURE 1.



00562602

Note 1: All diodes 1N4148.

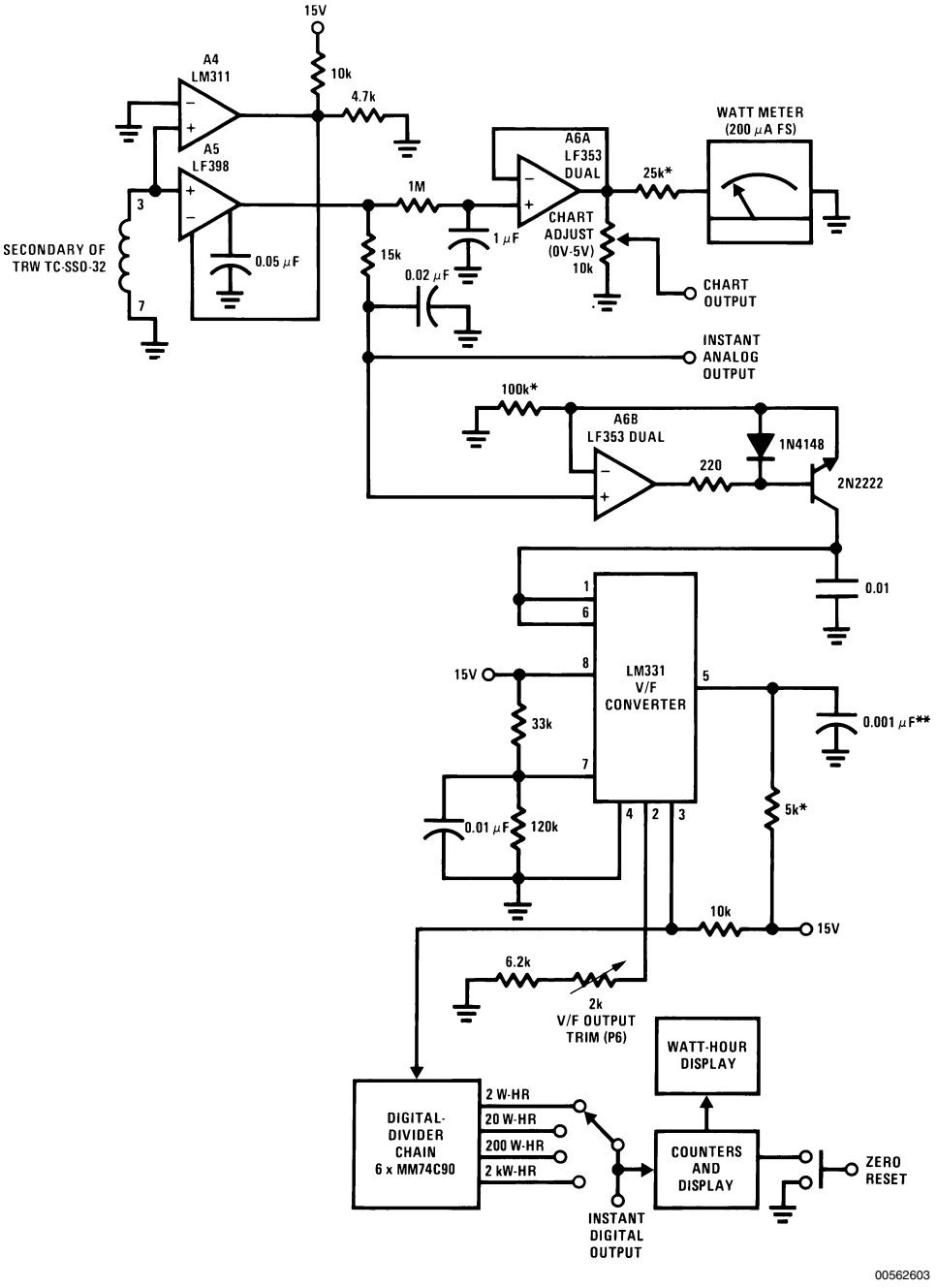
Note 2: ⏚ floating ground connected to neutral side of 110 VAC line.

Note 3: R#=G.E. current shunt 50−140034NDAA.

Note 4: Circuit power from ±15V floating supply shown in schematic.

Note 5: *Resistors are 1% metal film types.

FIGURE 2. Floating Half of Circuit is Connected Directly to the AC Line. Always Use Caution when Working with this Circuitry.



Note 6: *Resistors are 1% metal film types.

Note 7: **Polystyrene capacitor.

Note 8: DO NOT connect ( ) ground of this half of circuit to (C) ground of *Figure 2*.

Note 9: ±15V power must come from a source other than floating supply of *Figure 2*.

Note 10: *Figure 2* and *Figure 3* must be electrically isolated from each other.

FIGURE 3. Grounded Side of Circuit. This Circuit Can Safely Be Connected to a Chart Recorder or Computer Due to Isolation Provided by TRW Transformer.

Figure 2 and *Figure 3* show the detailed schematic, with *Figure 4* giving the waveforms of operation. The AC line is divided down by the 100 kΩ–4.4 kΩ resistor string. ½ of A2 (amplifier A) serves as a buffer and feeds one input of an analog multiplier configuration. A1 monitors the voltage across the current shunt at a fixed gain of 100. The other half of A2 (B) provides additional gain and calibrated switching of wattage sensitivities from 2W to 2000W full-scale over four decade ranges. The 1N1195 diodes and the 20A fuses protect A1 and the shunt in the event a short appears across the load test socket. The voltage and current signals are multiplied by a multiplier configuration comprised of amplifiers A3, C and D, and the LM394 dual transistors. The multiplier is of

the variable transconductance type and works by using one input to vary the gain of an amplifier whose output is the other input of the multiplier.

The output of the multiplier (*Figure 4*, Trace A) represents the instantaneous power consumed by the load. This information is used to bias a pulse amplitude modulating isolation amplifier. The isolation amplifier is made up of A3 (A and B) and the discrete transistors. The A3 (A) oscillator output (*Figure 4*, Trace B) biases the Q1-Q2 switch, which drives a pulse transformer. A3 (B) measures the amplitude of the pulses at the transformer and servo controls them to be the same amplitude as its "+" input, which is biased from the multiplier output. Q3 provides current drive capability and completes the feedback path for A3 (B). *Figure 4*, Trace D shows the pulses applied to the transformer. Note that the amplitude of the pulses applied to the transformer forms an envelope whose amplitude equals the multiplier output. *Figure 4*, Trace C shows Q3's emitter voltage changing to meet the requirements of the servo loop.

The amplitude modulated pulses appear at the transformer's secondary, which is referenced to instrument ground. The amplitude of each pulse is sampled by A5, a sample-hold amplifier. The sample command is generated by A4. The output of A5 is lightly filtered by the 15 kΩ–0.02 µF combination and represents a sampled version of the instantaneous power consumed in the load (*Figure 4*, Trace E). Heavy filtering by the 1 MΩ–1 µF time constant produces a smoothed version of the power signal, which drives the watts meter and the strip chart output via the A6 (A) buffer. The watt-hour time integration function is provided by an LM331 voltage-to-frequency converter and a digital divider chain which form a digital integrator. The lightly filtered A5 output is fed to A6 (B) which is used to bias the V/F converter. The V/F output drives a divider chain. The ratio of the divider chain sets the time constant of the integrator and is used to switch the scale factor of the watt-hours display. The additional counters and display provide the digital readout in watt-hours. A zero reset button allows display reset.

Instrument Calibration

To calibrate the instrument, pull the 20A fuses from their holders. Next, adjust P1 for 0.00V out at A2 (B) with the watts range switch in the 2 watt position. Then, disconnect both multiplier input lines and connect them to floating instrument ground. Adjust P2 for 0V out at A6 (A). Next, apply a 10 Vp-p 60 Hz waveform to the current input of the multiplier (leave the voltage input grounded) and adjust P3 for zero volts out at A6 (A). Then, reverse the state of the multiplier inputs and adjust P4 for zero volts out at A6 (A). Reconnect the multiplier input into the circuit. Read the AC line voltage with a digital voltmeter. Plug in a known load (e.g., 1% power resistor) to the test socket and adjust P5 until the meter reads what the wattage should be (wattage = line voltage^2/resistance of load). Finally, lift A6's (B's) "+" input line, apply 5.00V to it, and adjust P6 until the LM331V/F output (pin 3) runs at 27.77 kHz. Reconnect A6's (B's) input. This completes the calibration.

Applications

Once calibrated, the watt-watt-hour meter provides a powerful measurement capability. A few simple tests provide some surprising and enlightening results. The strip chart of *Figure 5* shows the measured power a home refrigerator draws over 3½ hours at a temperature set-point of 7˚C. Each time the compressor comes on, the unit draws about 260W. Actually, the strip chart clearly shows that as the compressor warms up over time, the amount of power drawn drops off a bit. The watt-hour display was used to record the total watt-hours consumed during this 3½ hour period. The data is summarized in the table provided. With the temperature control in the refrigerator set to maintain 5˚C, just 2˚C colder, it can be seen that the compressor duty cycle shifts appreciably (*Figure 6*), over 6%! This factor is directly reflected in the kW-H/cycle and yearly operating cost columns. If you want your milk 2˚C colder you will have to pay for it!

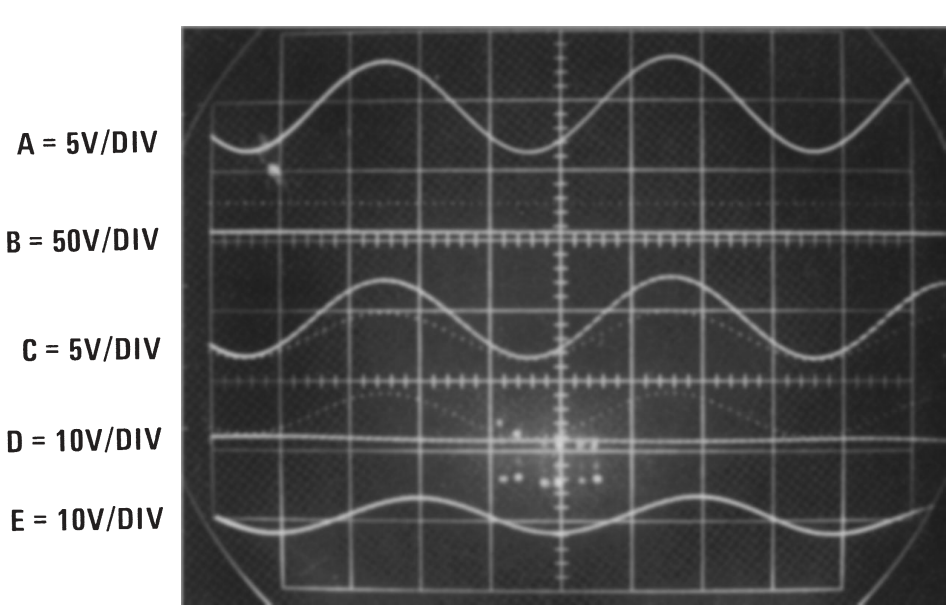
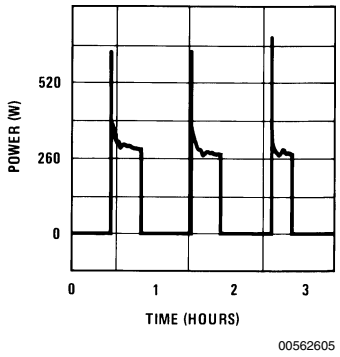


FIGURE 4.

Applications (Continued)



Temperature	Watts	Kilowatt-Hours/Cycle	Cost/Day	Cost/Year
5˚C	260	0.119	$0.1147	$41.89
7˚C	260	0.104	$0.0998	$36.44

FIGURE 5. Temperature=7.0˚C Compressor Duty Cycle=40%

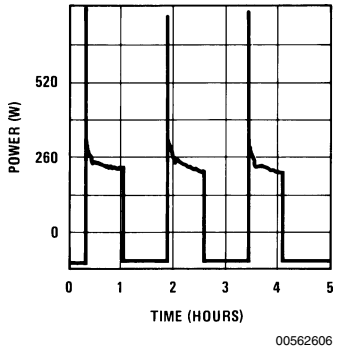
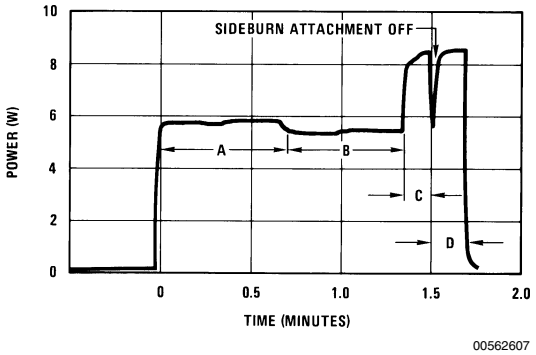


FIGURE 6. b. Temperature=5.0˚C Compressor Duty Cycle=46%

The strip chart of *Figure 7* is somewhat less depressing but no less informative. In this example, the watt-watt-hour meter was used to record power consumption during morning shaving with an electric razor. From the strip chart and the table it can be seen that various facial areas cost more to shave than others. The high power drawn by the sideburn attachment on the razor is somewhat compensated for by the relatively short period of time it is in use. A complete shave, including the 4 areas listed, costs 0.00692 cents/day or 8.68 cents per year. If this is too high, you can economize by growing a beard.



Facial Area	Power (W)	Watt-Hours	Cost (at 4¢ Kilowatt-Hours) Per Shave
Cheeks (“A”)	5.8	0.173	0.00692¢
Upper/Lower Lip (“B”)	5.4	0.123	0.00492¢
Right Sideburn (“C”)	8.4	0.063	0.00252¢
Left Sideburn (“D”)	8.4	0.061	0.00244¢

FIGURE 7.

LIFE SUPPORT POLICY

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Circuit Applications of Sample-Hold Amplifiers

National Semiconductor
Application Note 266
January 1981

Most designers are familiar with the sample-hold amplifier as a *system* component which is utilized in high speed data acquisition work. In these applications, the sample-hold amplifier is used to store analog data which is then digitized by a relatively slow A/D converter. In this fashion, high speed or multiplexed analog data can be digitized without resorting to complex and expensive ultra-high speed A/D converters.

The use of sample-hold amplifiers as *circuit* oriented components is not as common as the class of application described above. This is unfortunate, because sampling techniques allow circuit functions which are sophisticated, low cost and not easily achieved with other approaches. An excellent example is furnished by the fiber optic data link intrusion alarm of *Figure 1*.

Fiber Optic Data Link Intrusion Alarm

The circuit of *Figure 1* will detect an attempt to tap a fiber optic data link. It may be used with any fiber optic communication system which transmits data in pulse coded form. The circuit works by detecting any short-term change in the loss characteristics of the fiber optic line. Long term changes due to temperature and component aging do not affect the circuit. The amplitude of the pulses at the LH0082 fiber optic receiver IC (A6) will depend upon the characteristics of the photocomponents and the losses in the optical line. Any attempt to tap the fiber optic will necessitate removal of some amount of light energy. This will cause an instantaneous drop in the pulse amplitude at A6's output. The amplitude of each of A6's output pulses is sampled by the LF398 sample-hold amplifier (A3), A1 and A2 provide a delayed sample-hold control pulse to A3, which insures that A6's output is sampled well after its output has settled. Under normal conditions, the pulse-to-pulse amplitude variations at A6's output will be negligible, and the output of A3 will be at a DC level. A4 is AC coupled and its output will be zero. During an intrusion attempt, energy will be removed from the line and A6's output will shift, causing A3 to jump to a new DC level. This shift will be AC amplified by A4 and the A5 comparator will trip, activating the latch circuitry.

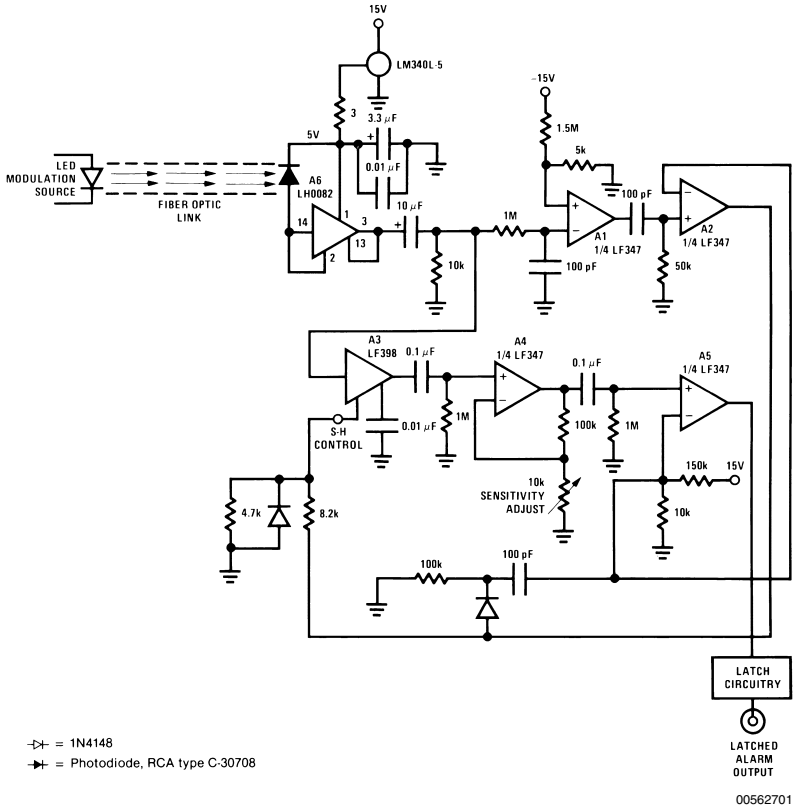
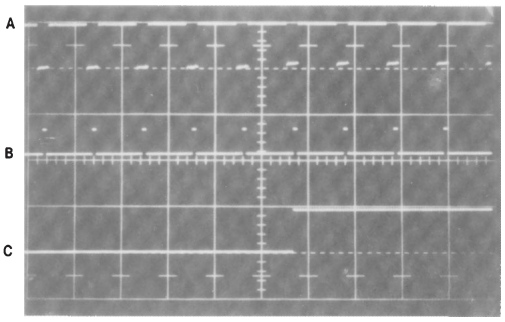


FIGURE 1. Fiber optic link eavesdropping attempts are immediately detected by this design. Working on a pulse-by-pulse comparison basis, A3 samples each input pulse and holds its output amplitude value at a DC level. Anything that disturbs the next input's amplitude causes a jump in this level; because A4 is an AC-coupled amplifier, the comparator and latch then activate.

Fiber Optic Data Link Intrusion Alarm (Continued)

Note that the circuit is not affected by slow drifts in circuit components over time and temperature because it is only sensitive to AC disturbances on the line. In addition, the frequency and pulse widths of the data may vary over wide ranges. The photo of *Figure 2* shows the circuit in operation. Trace A is A6's output. Trace B is the sample-hold control pin at A3 and Trace C is the latch-alarm output. In this figure, a disturbance on the fiber optic line has occurred just past the midpoint of the photo. This is reflected by the reduced amplitude of A6's output at this point. The latch-alarm output goes high just after the sample command rises, due to the sample-hold amplifier jumping to the new value at A6's output. In the photo, the disturbance has been made large (≃10%) for viewing purposes. In practice, the circuit will detect an energy removal as small as 0.1% from the line.



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TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	1 mSEC/DIV
C	10V/DIV	1 mSEC/DIV

FIGURE 2. An intrusion attempt occurring just past the midpoint of Trace A is immediately detected by *Figure 1*'s circuit. The photodetector's amplifier output (A) shows a slight amplitude drop. The next time the S-H amplifier samples this signal (B), the alarm latch sets (C).

Proportional Pulse Stretcher

The circuit of *Figure 3* allows high accuracy measurement of short width pulse durations. The pulses may be either repetitive or single-shot events. Using digital techniques, a 1% width measurement of a 1 µs event requires a 100 MHz clock. This circuit gets around this requirement by linearly amplifying the width of the input pulse with a time multiplying factor of 1000 or more. Thus, a 1 µs input event will yield a 1 ms output pulse which is easy to measure to 1%. This measurement capability is useful in high energy physics and nuclear instrumentation work, where short pulse width signals are common.

Figure 4, Trace A shows a 350 ns input pulse applied to the circuit of *Figure 3*. The A1 comparator output goes low (*Figure 4*, Trace B), triggering the DM74121 one shot, which resets the 100 pF capacitor to 0V via Q1 with a 50 ns pulse (Trace C). Concurrently, Q2 is turned off, allowing the A3 current source to charge the 100 pF capacitor in a linear fashion (*Figure 4*, Trace C). This charging continues until the circuit input pulse ends, causing A1's output to return high and cutting off the current source. The voltage across the 100 pF capacitor at this point in time is directly proportional to the width of the circuit input pulse. This voltage is sampled by the LF398 sample-hold amplifier (A2) which receives its sample-hold command from A3 (*Figure 4*, Trace E—note horizontal scale change at this point). A3 is fed from a delay network which is driven by A1's inverting output. The output of A2 is a DC voltage, which represents the width of the most recently applied pulse to the circuit's input. This DC potential is applied to A4, which along with A5 comprises a voltage controlled pulse width modulator. A5 ramps positive (*Figure 4*, Trace G) until it is reset by a pulse from A6, which goes high for a short period (*Figure 4*, Trace F) each time A3's output (*Figure 4*, Trace E) goes low. The ramps at A6's output are compared to A2's output voltage by A4, which goes high for a period linearly dependent on A2's output value (*Figure 4*, Trace H). This pulse is the circuit's output.

In this particular circuit, the time amplification factor is about 2000 with a 1 µs full-scale width giving a 1.4 ms output pulse. Absolute accuracy of the time expansion is 1% (10 ns) referred to input with resolution down to 2 ns. The 50 ns DM74121 reset pulse limits the minimum pulse width the circuit can measure.

Proportional Pulse Stretcher (Continued)

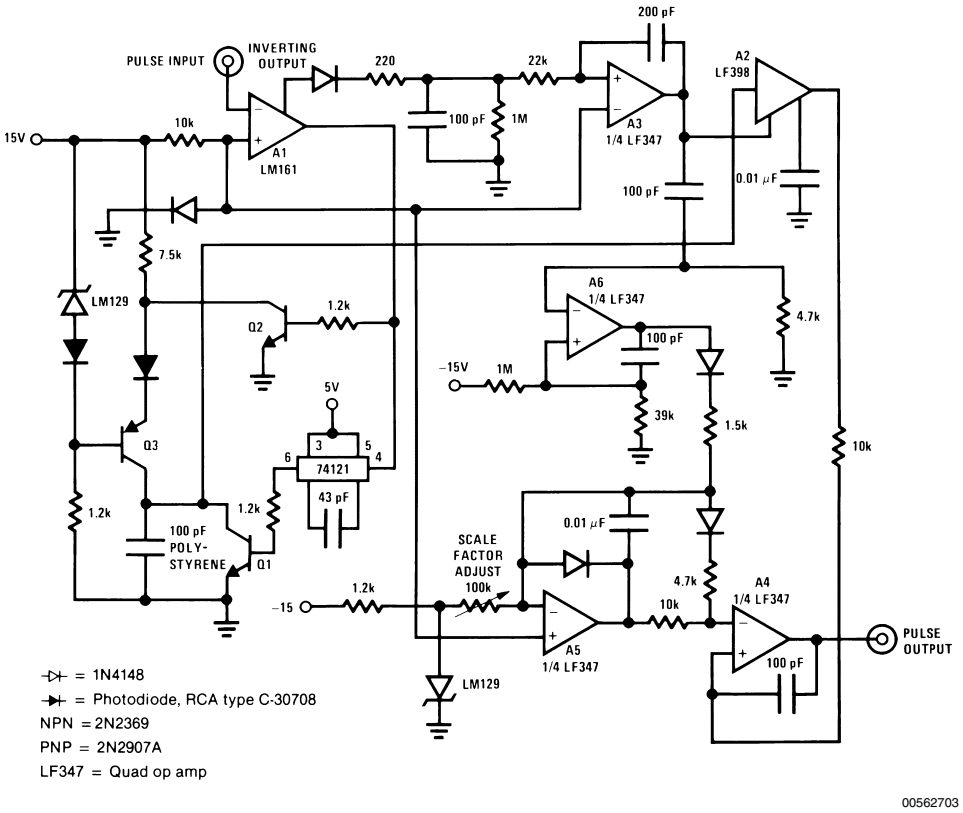
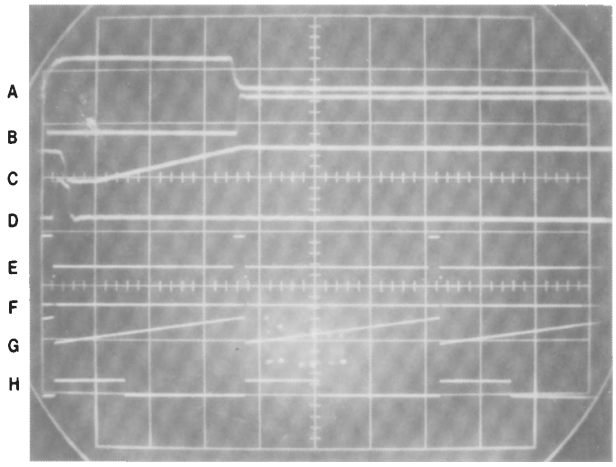


FIGURE 3. Pulse width measurement accuracy is enhanced by this pulse stretching circuit. A short input pulse triggers the 74121 one-shot and (via Q1) discharges the 100 pF capacitor while concurrently turning on the recharging current source, Q3. So long as the input pulse is present, the capacitor charges; when the pulse ends, the capacitor's voltage is proportional to the pulse's width. S-H amplifier A2 samples this voltage, and the resultant DC level controls the ON duration of the A4/A5 pulse width modulator.

Proportional Pulse Stretcher (Continued)



00562704

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 nSEC/DIV

TRACE	VERTICAL	HORIZONTAL
E	50V/DIV	500 µSEC/DIV
F	50V/DIV	500 µSEC/DIV
G	20V/DIV	500 µSEC/DIV
H	100V/DIV	500 µSEC/DIV

FIGURE 4. A sequence of events in *Figure 3*'s circuit stretches a 350 ns input pulse (A) by a factor of 2000. When triggered, comparator A1 goes low (B). This action starts the recharging of a capacitor (C) after its previously stored charge has been dumped (D). When the input pulse ends, the capacitor's voltage is sampled under control of a delayed pulse (E) derived from the input amplifier's inverting output (F). The sampled and held voltage then turns off a voltage controlled pulse width modulator (G), and a stretched output pulse results (H).

Controlled Amplitude Pulser

Figure 5 depicts a circuit which converts an input pulse train into an amplitude stabilized pulse output which will drive a 20Ω load. The output pulse amplitude is adjustable from 0V to 10V and is stable over time, temperature and load changes. This circuit function is useful in automatic test equipment and general laboratory applications.

The circuit works by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. Each time a pulse is applied at the circuit input, the Q2-Q3 combination turns on and drives the load.

Simultaneously, the A1 sample-hold amplifier is placed in the sample mode. When the pulse ends, A1's output is at a DC level equal to the amplitude of the output pulse. This level is compared to the amplitude set DC reference by A2, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the amplitude of the output pulse to be the same as the DC potential at the amplitude set potentiometer wiper, regardless of Q3 switch losses or loading. In *Figure 6*, Trace A is the circuit output. Traces B and C detail the rising and falling edges of the output (note horizontal sweep time change for B and C) with clean 50 ns transitions into the 20Ω load.

Controlled Amplitude Pulser (Continued)

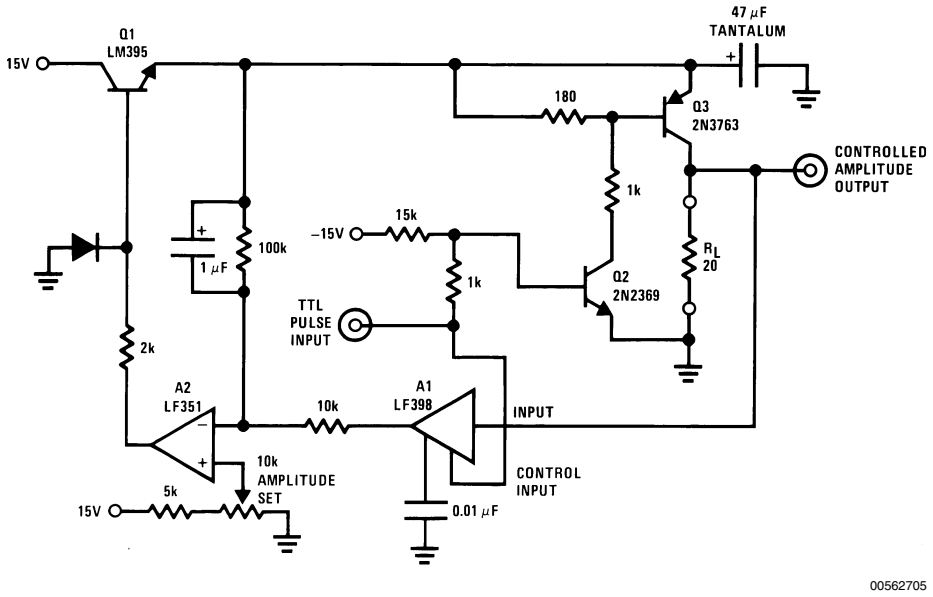
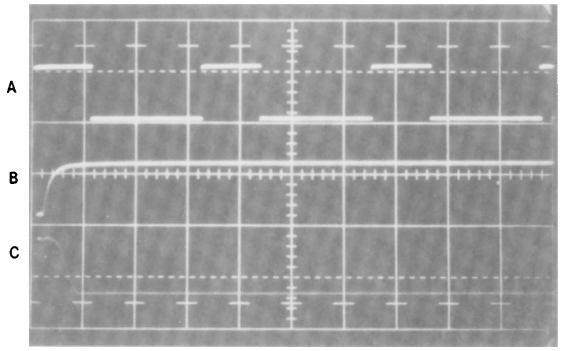


FIGURE 5. Pulse amplitude control results when this circuit samples an output pulse's amplitude and compares it with a preset reference level. When the output exceeds this reference, A2 readjusts switching transistor Q3's supply voltage to the correct level.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	10V/DIV	100 nSEC/DIV

FIGURE 6. A 10V, 0.5A pulse (A) is amplitude stabilized by the S-H technique depicted in *Figure 5*. Note the clean 50 ns rise (B) and fall (C) times.

Isolated Input Signal Conditioning Amplifier

Figure 7 is a logical and very powerful extension of the controlled amplitude pulser shown in *Figure 5*. This circuit permits measurement of a small amplitude signal, e.g., thermocouples, in the presence of common-mode noise or voltages as high as 500V. This is a common requirement in industrial control systems. Despite the fact that the input terminals are fully galvanically isolated from the output, a transfer accuracy of 0.1% may be expected. With the optional low-level pre-amplifier shown, inputs as low as 10 mV full-scale may be measured.

The circuit works by converting the input signal into a pulse train whose amplitude is linearly dependent on the input signal value. This pulse train drives a transformer which provides total galvanic isolation of the input circuitry from ground. The transformer output is then demodulated back to a DC level to provide the circuit's system ground referenced

Isolated Input Signal Conditioning Amplifier (Continued)

output. The amplitude of the pulse train which drives the transformer is controlled by a loop very similar to the one described in *Figure 5*. The amplitude set potentiometer has been deleted, and the servo amplifier's "+" input becomes the circuit input. A1, a low drift *X1000* amplifier, may be employed for boosting low-level inputs. The pulse train is supplied by A2, which is set up as an oscillator (A2 output shown in *Figure 8*, Trace A). The feedback to the pulse amplitude stabilizing loop is taken from an isolated secondary of the transformer, which insures high accuracy amplitude information transfer. The amplitude coded information at the transformer's secondary (*Figure 8*, Trace B) is demodulated back to a DC level by sample-hold amplifier, A7. A5 (output, *Figure 8*, Trace C) and A6 ("+" input, *Figure 8*, Trace D; output, *Figure 8*, Trace E) provide a delayed sample command to A7, ensuring accurate acquisition of the transformer's output pulse amplitude. A8 provides gain trimming and filtering capability.

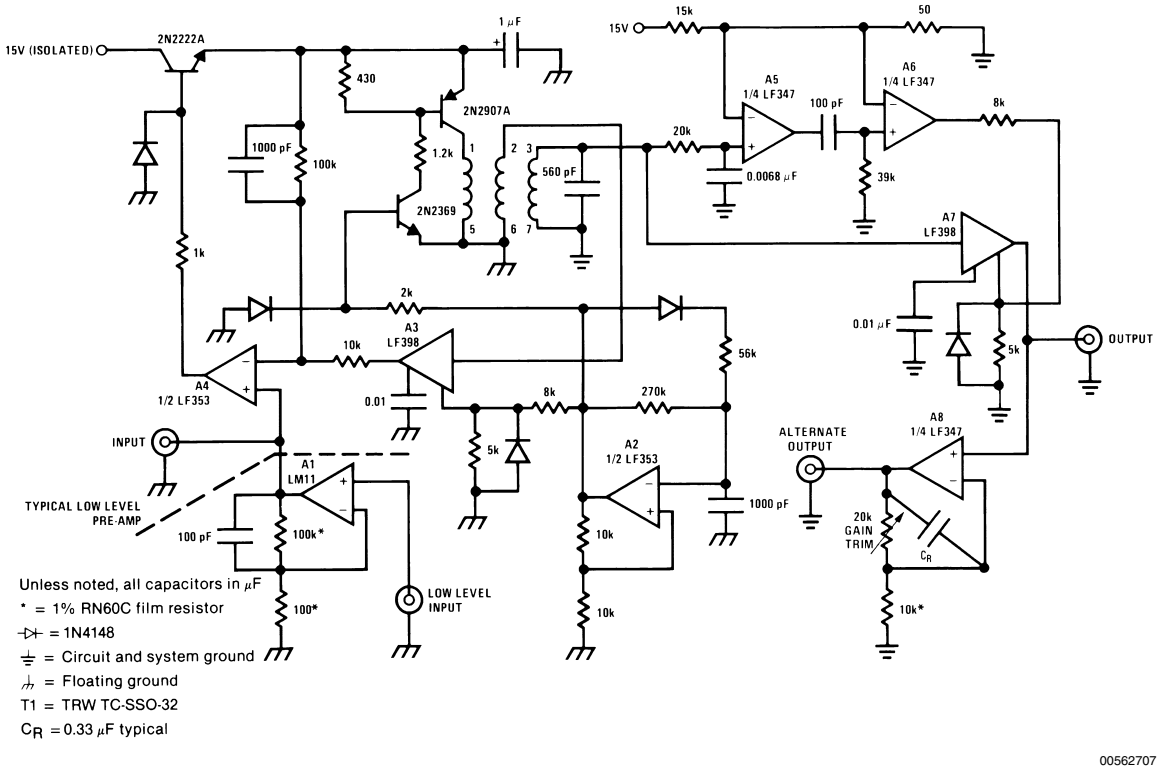
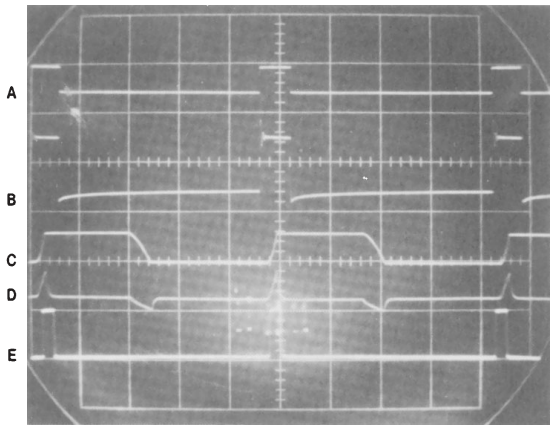


FIGURE 7. Obtain input signal isolation using this circuit's dual S-H scheme. Analog input signals amplitude modulate a pulse train using a technique similar to that employed in *Figure 5*'s design. This modulated data is transformer coupled, and thereby isolated, to a DC filter stage, where it is resampled and reconstructed.

Isolated Input Signal Conditioning Amplifier (Continued)



00562708

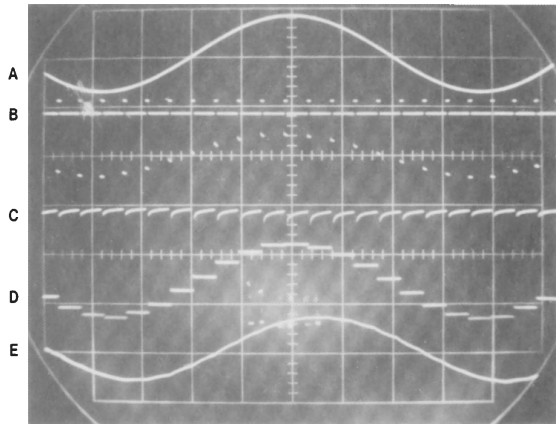
TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	100 µSEC/DIV
B	1V/DIV	100 µSEC/DIV
C	50V/DIV	100 µSEC/DIV
D	10V/DIV	100 µSEC/DIV
E	5V/DIV	100 µSEC/DIV

FIGURE 8. *Figure 7*'s in-circuit oscillator (A2) generates both the sampling pulse (A) and the switching transistor's drive. Modulated by the analog input signal, Q2's (and therefore T1's) output (B) is demodulated by S-H amplifier A7. A5's output (C) and A6's input (D) and output (E) provide a delayed sample command.

Figure 9 provides very graphic evidence of the circuit at work. Here, a DC biased sine wave (*Figure 9*, Trace A) is fed into the circuit input. Trace B is the clock from A2's output. Trace C is the transformer secondary (input of A7 sample-hold amplifier) and Trace D is A7's output. Trace E shows the filter's output at A8.

Precision, High Efficiency Temperature Controller

The sample-hold amplifier in *Figure 10* is used to provide very high stability in an oven temperature control circuit. In this circuit, the output signal of the pulse driven thermistor-bridge is ten times greater than the usual DC driven bridge. In thermistor-bridges, power dissipation in the resistors and thermistor is the limiting factor in how much DC bridge drive may be used. However, if the bridge drive is applied in the form of high voltage pulses at very low duty cycle, average power dissipation will be low and a high bridge output signal will result.



00562709

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	100V/DIV	
C	5V/DIV	
D	5V/DIV	
E	5V/DIV	

FIGURE 9. Completely input-to-output isolated, *Figure 7*'s circuit's analog input signal (A) is sampled by a clock pulse (B) and converted to a pulse amplitude modulated format (C). After filtering and resampling, the reconstructed signal (D) is available smoothed (E).

Precision, High Efficiency Temperature Controller (Continued)

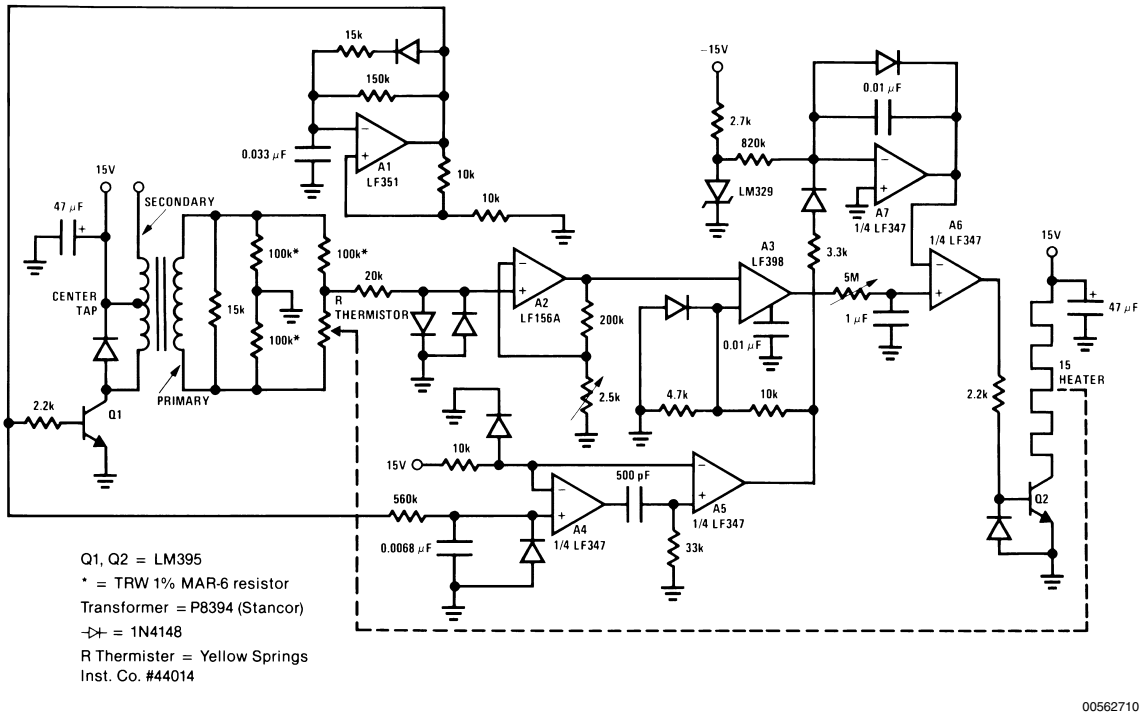


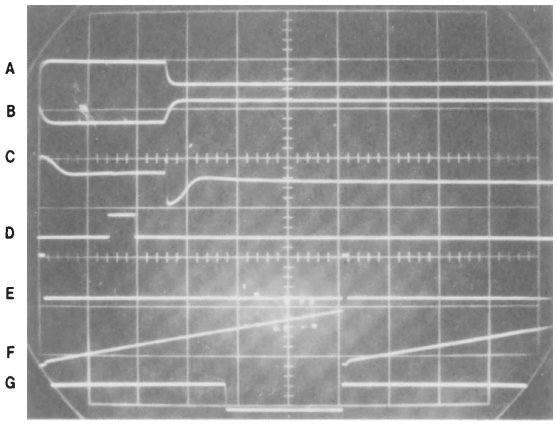
FIGURE 10. Tight temperature control results when high voltage pulses synchronously drive a thermistor-bridge—a trick that increases signal level—and are then sampled and used to control a pulse width modulated heater driver.

In *Figure 10*, this operation is implemented by having the A1 oscillator drive Q1 to energize a common 24V transformer used "backwards". The transformer's floated output is a 100V pulse which is applied directly across the thermistor-bridge. With one side of the bridge output grounded, the bridge drive with respect to ground appears as complementary 50V pulses (*Figure 11*, Traces A and B). A2 provides amplification of the bridge's pulsed output (*Figure 11*, Trace C). A3, a sample-hold amplifier, samples the middle of A2's output pulses and has a DC output equal to the amplitude of these pulses. Proper timing for A3's sample command (*Figure 11*, Trace D) is provided by the A4-A5 pair and their associated RC networks. The DC output of A3 is low-pass filtered and fed to A6, which combines with A7 to form a simple pulse width modulator. The output of A7 is a ramp (*Figure 11*, Trace F—note horizontal scale change) which is periodically reset by A5's output (*Figure 11*, Trace E). This ramp is compared at A6 to A3's output, and the resultant pulse at A6's output (*Figure 11*, Trace G) is used to drive the Q2 heater control switch. In this fashion, the ON time of the pulse applied to the heater will be proportional to the sensed offset at the thermistor-bridge. Thermal feedback from the heater to the thermistor completes a loop around the circuit. The 5 MΩ potentiometer is used to adjust the time constant of this loop, and the 2.5k potentiometer at A2 sets the gain.

In operation, with the thermistor and heater tightly coupled, the time constant of the loop is adjusted by applying small step changes in the temperature setpoint. This is done by alternately opening and closing a switch across a 100Ω resistor in series with one of the bridge resistors. For the thermistor shown, this represents a 0.02°C step. The response of the loop to these steps can be monitored at A3's output. With the loop time constant and gain properly adjusted, A3's output will settle in a minimum amount of time in

Precision, High Efficiency Temperature Controller (Continued)

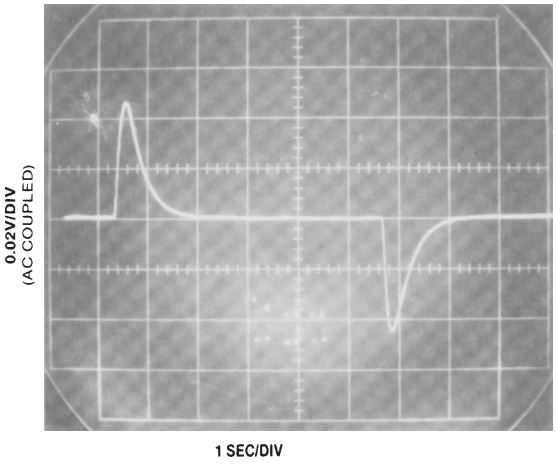
response to the steps. *Figure 12* shows settling for both "+" and "–" steps, with settling inside 2 seconds for either polarity step.



00562711

TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	200 µSEC/DIV
B	100V/DIV	200 µSEC/DIV
C	5V/DIV	200 µSEC/DIV
D	10V/DIV	200 µSEC/DIV
E	5V/DIV	1 mSEC/DIV
F	10V/DIV	1 mSEC/DIV
G	50V/DIV	1 mSEC/DIV

FIGURE 11. Driving a thermistor-bridge with complementary high voltage pulses (A and B) permits high gain amplification without drift problems (C). Driven by a delayed sample command (D), a S-H amplifier converts the bridge's error signal to a DC level (E) that controls a pulse width modulated heater driver (F and G).



00562712

FIGURE 12. Tight heater to thermistor coupling and careful calibration can provide rapid temperature restabilization. Here the controlled oven recovers within 2 seconds after ±0.002˚C steps.

Once adjusted, and driving a well insulated and designed oven, the circuit's control stability can be monitored. The high output signal levels from the bridge, in combination with the gain provided by A2, yield extremely good performance.

Sample-Hold Amplifier Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between hold command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the hold logic command.

Hold Step: The voltage step at the output of the sample-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is specified, usually 5V.

Sample-Hold Amplifier Terms (Continued)

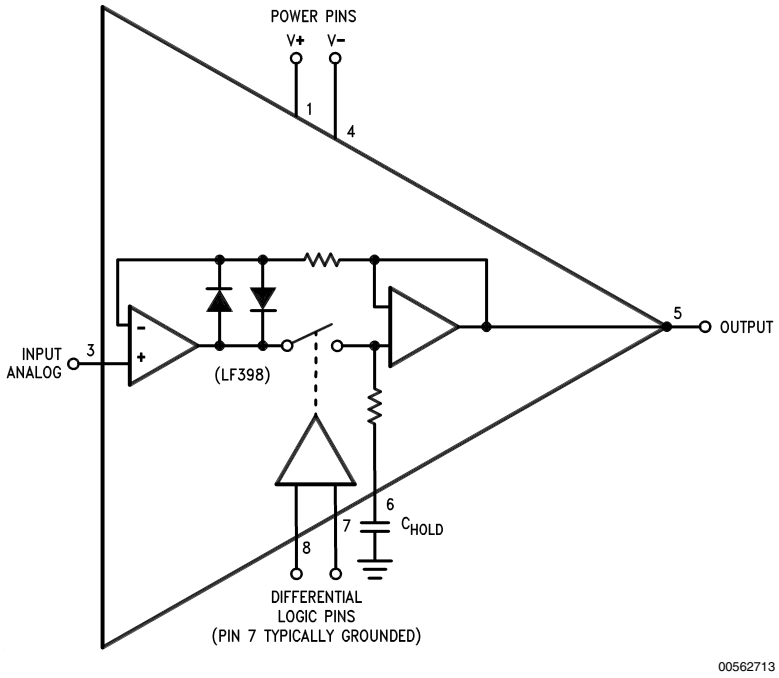


FIGURE 13. Typical Sample-Hold IC Amplifier

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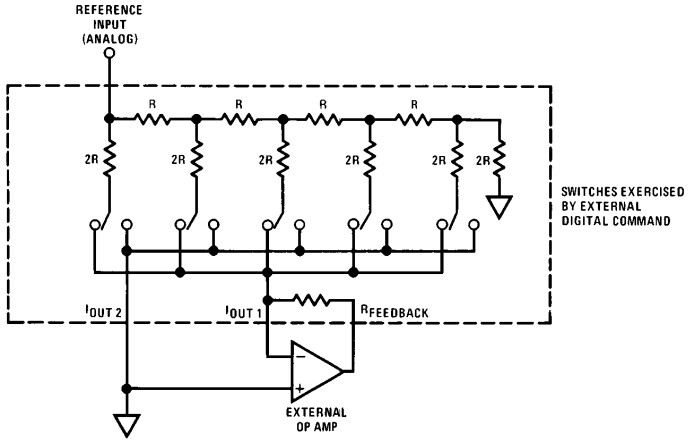
Circuit Applications of Multiplying CMOS D to A Converters

National Semiconductor
Application Note 269
September 1981

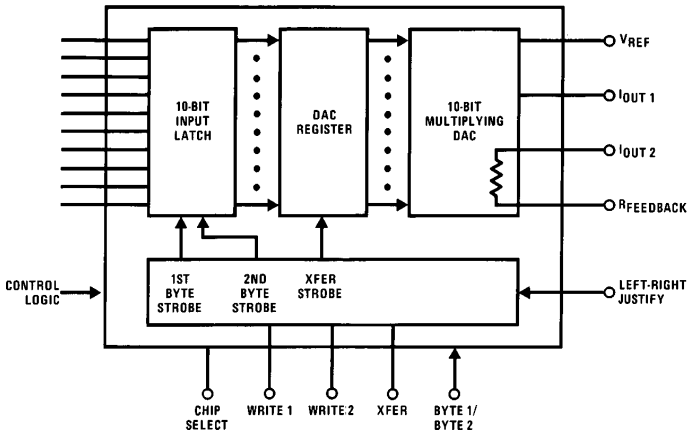
The 4-quadrant multiplying CMOS D to A converter (DAC) is among the most useful components available to the circuit designer. Because CMOS DACs allow a digital word to operate on an analog input, or vice versa, the output can represent a sophisticated function. Unlike most DAC units, CMOS types permit true bipolar analog signals to be applied to the reference input of the DAC (see shaded area for CMOS DAC details).

This feature is one of the keys to the CMOS DAC's versatility. Although D to A converters are usually thought of as system data converters, they can also be used as circuit elements to achieve complex functions. Some CMOS DACs contain internal logic which makes interface with microprocessors and digital systems easy. In circuit oriented applications, however, the ''bare bones'' DACs will usually suffice. As an example, *Figure 1* shows a 0 kHz–30 kHz variable frequency sine wave generator which has essentially instantaneous response to digital commands to change frequency. This capability is valuable in automatic test equipment and instrumentation applications and is not readily achievable with normal sine wave generation techniques. The linearity of output frequency to digital code input is within 0.1% for each of the 1024 discrete output frequencies the 10-bit DAC can generate.



Details (Simplified) of CMOS DAC1020—Last 5 Bits Shown

Other CMOS DACs are similar in the nature of operation but also include internal logic for ease of interface to microprocessor based systems. Typical is the DAC1000 shown below.



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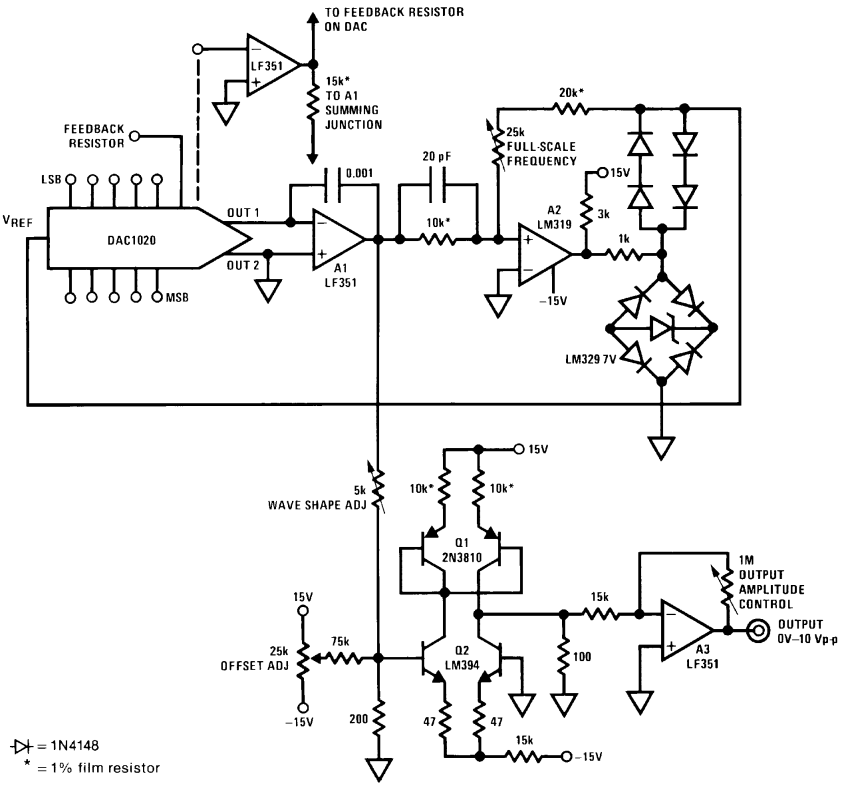

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FIGURE 1

To understand this circuit, assume A2's output is negative. This means that its zener bounded output applies −7V to the DAC's reference input. Under these conditions, the DAC pulls a current from A1's summing junction which is directly proportional to the digital code applied to the DAC. A1, an integrator, responds by ramping in the positive direction. When A1 ramps far enough so that the potential at A2's "+" input just goes positive, A2's output changes state and the potential at the DAC's reference input becomes +7V. The DAC output current reverses and the A1 integrator is forced to move in the negative direction. When the negative-going output of A1 becomes large enough to pull A2's "+" input slightly, negative A2's output changes state and the process repeats. The resultant amplitude stabilized triangle wave at A1's output will have a frequency which is dependent on the digital word at the DAC. The 20 pF capacitor provides a slight leading response at high operating frequencies to offset the 80 ns response time of A2, aiding overall circuit linearity. The triangle wave is applied to the Q1–Q2 shaper network, which furnishes a sine wave output. The shaper works by utilizing the well known logarithmic relationship between V_{BE} and collector current in a transistor to smooth the triangle wave.

To adjust this circuit, set all DAC digital inputs high and trim the 25k pot for 30 kHz output. Next, connect a distortion analyzer to the circuit output and adjust the 5k and 75k potentiometers associated with the shaper network for minimum distortion. The output amplifier may be adjusted with its potentiometer to provide the desired output amplitude.

This circuit permits rapid switching of output frequency which is not possible with other methods. *Figure 2* shows the clean, almost instantaneous response when the digital word is changed. Note that the output frequency shifts immediately by more than an order of magnitude with no untoward dynamics or delays. If operation over temperature is required, the absolute change in resistance in the DAC's internal ladder network may cause unacceptable errors. This can be corrected by reversing A2's inputs and inserting an amplifier (dashed lines in schematic) between the DAC and A1. Because this amplifier uses the DAC's internal feedback resistor, the temperature error in the ladder is cancelled and more stable operation results.

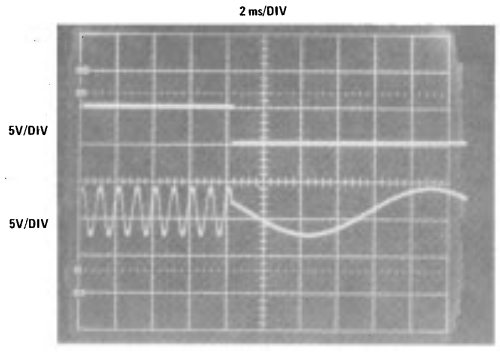

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FIGURE 2

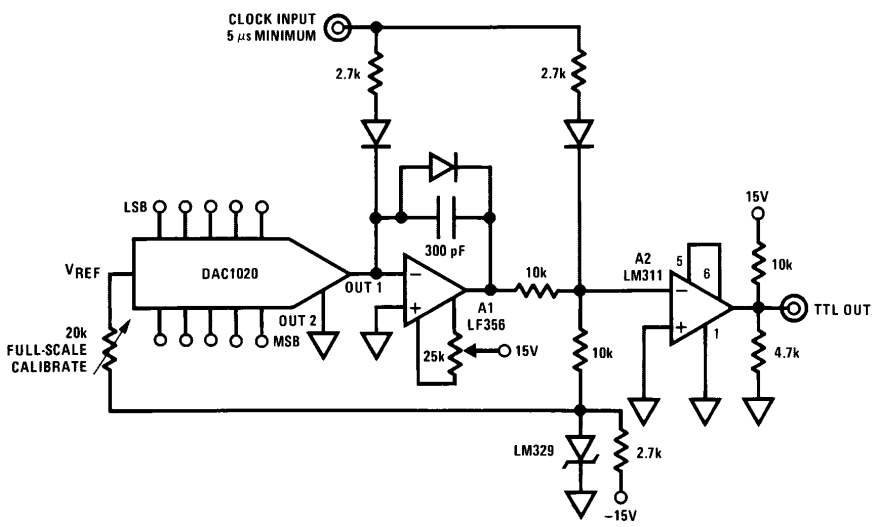

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FIGURE 3

Digitally Programmable Pulse Width Modulator

The circuit of *Figure 3* allows the DAC inputs to control a pulse width. This capability has been used in automatic testing of secondary breakdown limits in switching transistors. The high resolution of control the DAC exercises over the pulse width is useful anywhere wide range, precision pulse width modulation is necessary. In this circuit, the length of time the A1 integrator requires to charge to a reference level is determined by the current coming out of the DAC. The DAC output current is directly proportional to the digital input code. Both the DAC analog input and the reference trip point are derived from the LM329 voltage reference. During the time the integrator output (*Figure 4*, Trace A) is below the trip point, the A2 comparator output remains high (*Figure 4*, Trace B). When the trip point is exceeded, A2's output goes low. In this fashion, the DAC input code can vary the output pulse width over a range determined by the DAC resolution. Traces C, D and E show the fine detail of the resetting sequence (note expanded horizontal scale for these traces). Trace C is the 5 μs clock pulse. When this pulse rises, the A1 integrator output (Trace D) is forced negative until it bounds against the diode in its feedback loop. During the time the clock pulse is high, the current through the 2.7k diode path forces A2's output low. When the clock pulse goes low, A2's output goes high and remains high until the A1 integrator output amplitude exceeds the trip point. To calibrate this circuit set all DAC bits high and adjust the "full-scale calibrate" potentiometer for the desired full-scale pulse width. Next, set only the DAC LSB high and adjust the A1 offset potentiometer for the appropriate length pulse, e.g., 1/1024 of the full-scale value for a 10-bit DAC. If the 2.2mV/°C drift of the clamp diode in A1's feedback loop is objectionable it can be replaced with an FET switch.

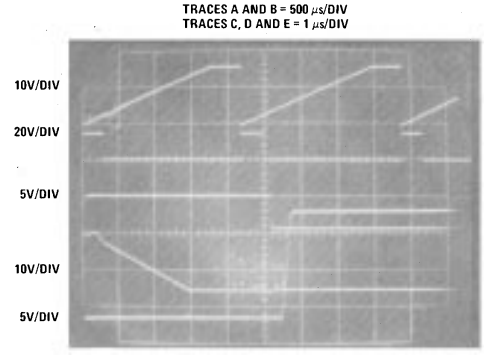

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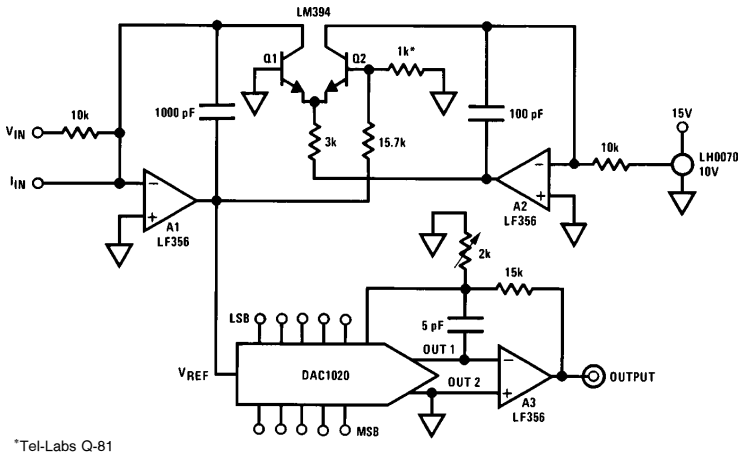
FIGURE 4

Digitally Controlled Scale Factor Logarithmic Amplifier

Wide dynamic measurement range is required in many applications, such as photometry. Logarithmic amplifiers are commonly employed in these applications to achieve wide measurement range. In such applications it is often required to be able to set the scale factor of the logarithmic amplifier. A DAC controlled circuit permits this to be done under digital control. *Figure 5* shows a typical logarithmic amplifier circuit. Q1 is the actual logarithmic converter transistor, while Q2 and the 1 kΩ resistor provide temperature compensation. The logarithmic amplifier output is taken at A3. The digital code applied to the DAC will determine the overall scale factor of the input voltage (or current) to output voltage ratio.

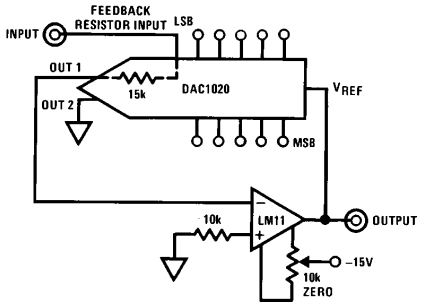
Digitally Programmable Gain Amplifier

Figure 6 shows how a CMOS DAC can be used to form a digitally programmable amplifier which will handle bipolar input signals. In this circuit, the input is applied to the amplifier via the DAC's feedback resistor. The digital code selected at the DAC determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback path. If no digital code (all zeros) is applied to the DAC, there will be no feedback and the amplifier output will saturate. If this condition is objectionable, a large value (e.g. 22 MΩ) resistor can be shunted across the DAC feedback path with minimal effect at lower gains. It is worth noting that the gain accuracy of this circuit is directly dependent on the open loop gain of the amplifier employed.



*Tel-Labs Q-81

FIGURE 5



TL/H/5628–7

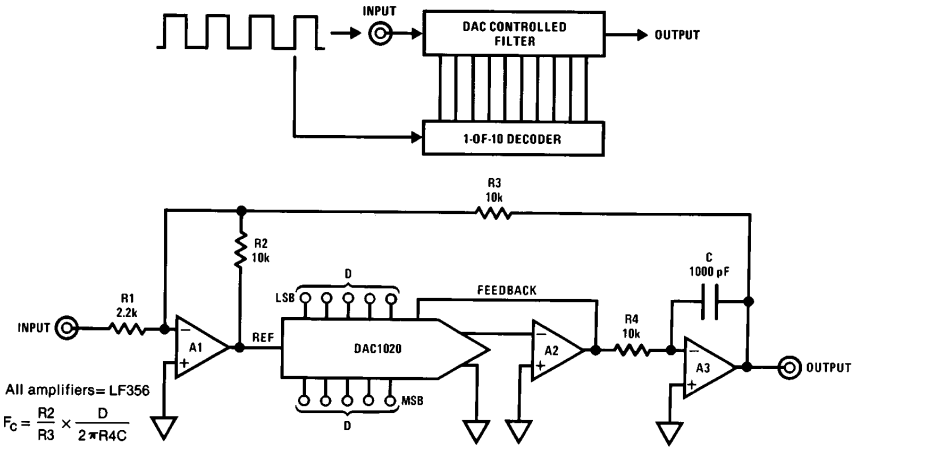
FIGURE 6

Digitally Controlled Filter

In *Figure 7* the DAC is used to control the cutoff frequency of a filter. The equation given in the figure governs the cutoff frequency of the circuit. In this circuit, the DAC allows high resolution digital control of frequency response by effectively varying the time constant of the A3 integrator. *Figure 8* dramatically demonstrates this. Here, the circuit is driven from the test circuit shown in *Figure 7*.

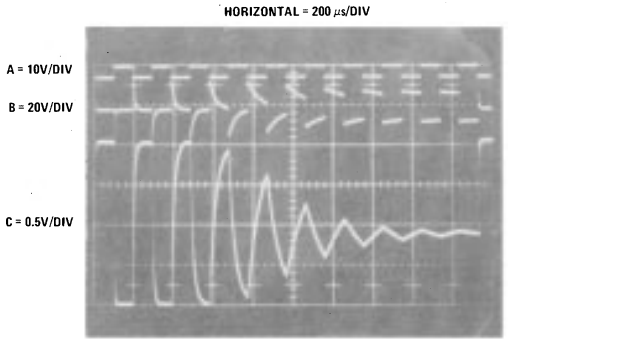
As each input square wave is presented to the filter the one-of-ten decoder sequentially shifts a ''one'' to the next DAC digital input line. Trace A is the input waveform, while Trace B is the waveform at A1's output (the reference input of the DAC). The circuit output at A3 appears as Trace C. It is clearly evident that as the decoder shifts the ''one'' towards the lower order DAC inputs the circuit's cutoff frequency decays rapidily.

Test Circuit



TL/H/5628–8

FIGURE 7



TL/H/5628–9

FIGURE 8

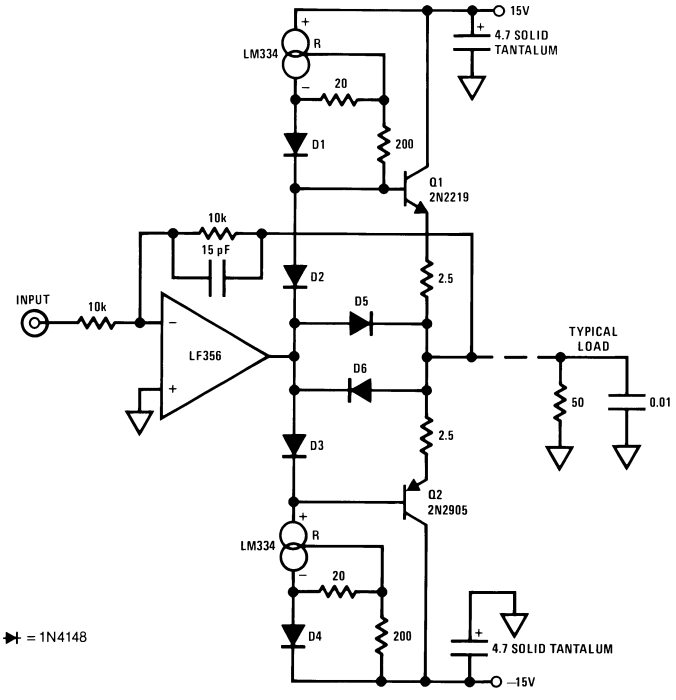
Op Amp Booster Designs

National Semiconductor
Application Note 272
September 1981

Although modern integrated circuit operational amplifiers ease linear circuit design, IC processing limits amplifier output power. Many applications, however, require substantially greater output voltage swing or current (or both) than IC amplifiers can deliver. In these situations an output "booster," or post amplifier, is required to achieve the needed voltage or current gain. Normally, this stage is placed within the feedback loop of the operational amplifier so that the low drift and stable gain characteristics of the amplifier are retained. Because the booster is a gain stage with its own inherent AC characteristics, the issues of phase shift, oscillation, and frequency response cannot be ignored if the booster and amplifier are to work well together. The design of booster stages which achieve power gain while maintaining good dynamic performance is a difficult challenge. The circuitry for boosters will change with the application's requirements, which can be very diverse. A typical current gain stage is shown in *Figure 1*.

200 mA Current Booster

The circuit of *Figure 1* boosts the LF356 unity gain inverter amplifier's output current to a ±200 mA level while maintaining a full ±12V output swing. The LM334 current sources are used to bias complementary emitter-followers. The 200Ω resistors and D1-D4 diodes associated with the LM334s provide temperature compensation for the current sources, while the 20Ω resistor sets the current value at 3.5 mA. Q1 provides drive for positive LF356 output swings, while Q2 sinks current for negative amplifier outputs. Crossover distortion is avoided by the D2-D3 diodes which compensate the V_{BE}s of Q1 and Q2. For best results, D2 and D3 would be thermally coupled to the TO-5 type heat sinks used for Q1 and Q2. Amplifier feedback is taken from the booster output and returned to the LF356 summing junction. D5 and D6 achieve short circuit protection for the output by shunting drive from Q1 or Q2 when output current exceeds about 275 mA. This value is derived from the output 2.5Ω resistors value divided by the 0.7V drop across the diodes. The 15 pF-10k feedback values provide a roll-off above 2 MHz. *Figure 2* shows the circuit at work driving a 100 kHz 20 Vp-p sine wave into a 50Ω load paralleled by 10,000 pF. Trace A is the input, while Trace B is the output. Despite the heavy load, response is clean below and quick with overall circuit distortion 0.05% (Trace C).

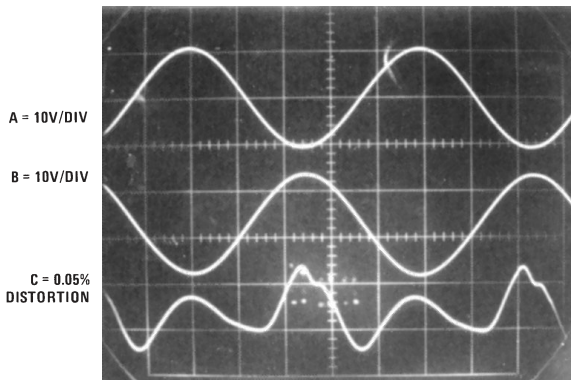


Use TO-5 heat sinks on transistors

All capacitor values in µF unless otherwise noted

FIGURE 1.

200 mA Current Booster (Continued)

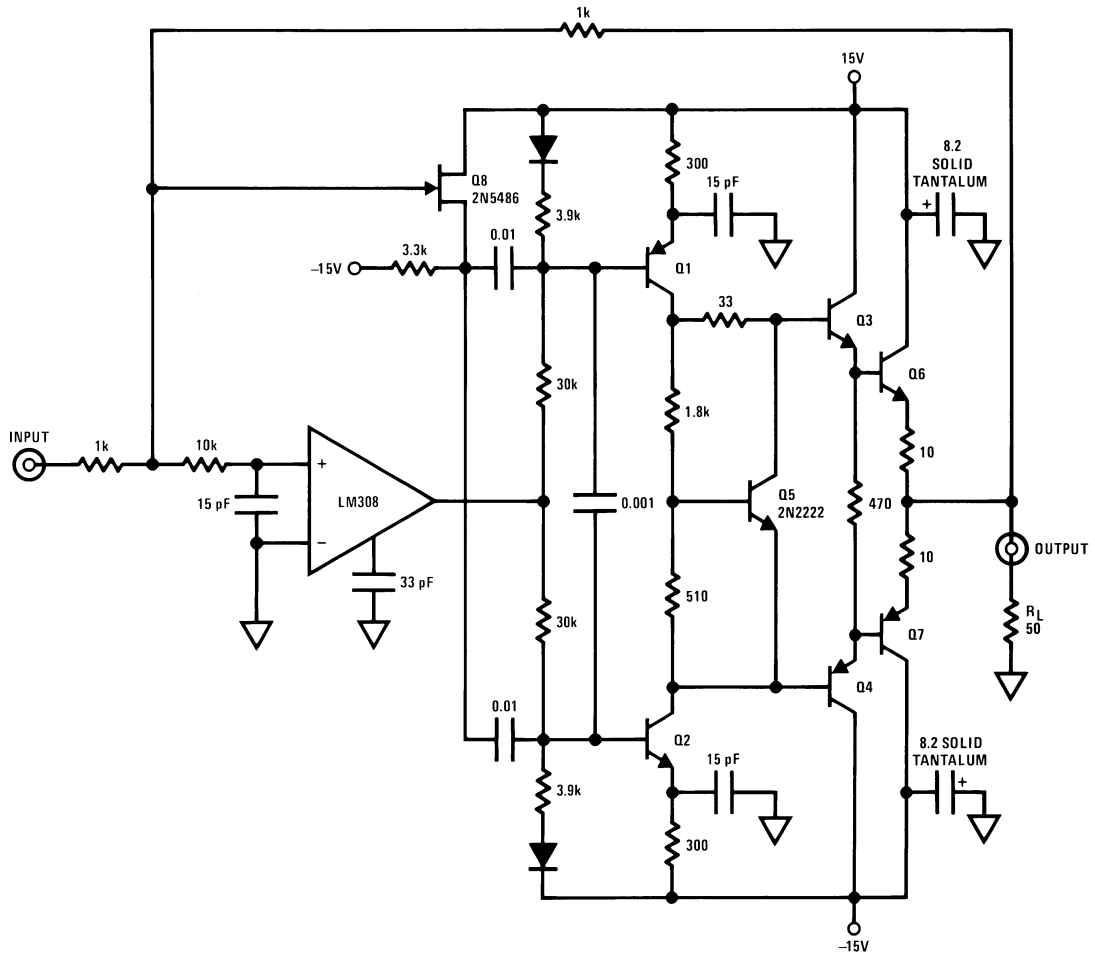


00563002

FIGURE 2.

Ultra High Speed Fed-Forward Current Booster

The schematic of *Figure 3* features the same output specifications as the previous current booster, but provides much greater speed. The speed of the booster in *Figure 1* is limited by the response of the op amp which drives it. Because that booster resides in the op amp's feedback loop, it cannot go any faster than the op amp, even though it has inherently greater bandwidth. In *Figure 3* we employ a feed-forward network which allows AC signals to bypass the LM308 op amp and directly drive a very high bandwidth current boost stage. At DC and low frequencies the LM308 provides the signal path to the booster. In this fashion, a very high speed, high current output is achieved without sacrificing the DC stability of the op amp. The output stage is made up of the Q1 and Q2 current sources which bias complementary emitter-followers, Q3-Q6 and Q4-Q7. Because the stage inverts, feedback is returned to the non-inverting input of the LM308. The actual summing junction for the circuit is the meeting point of the 1k resistors and the 10k unit at the LM308. The 10k-15 pF combination prevents the LM308 from seeing high frequency inputs. Instead, these inputs are source-followed by the Q8 FET and fed directly to the output stage via the two 0.01 µF capacitors. The LM308, therefore, is used to maintain loop stability only at DC and low frequencies. Although this arrangement is substantially more complex than *Figure 1*, the result is a breathtaking increase in speed. This boosted amplifier features a slew rate of 750V per microsecond, a full power bandwidth over 6 MHz and a 3 dB point beyond 11 MHz while retaining a ±12V, 200 mA output. *Figure 4* shows the amplifier-booster at work. Trace A is the input, while Trace B is the output. The booster drives a 10V pulse into 50Ω, with rise and fall times inside 15 ns and clean settling characteristics.



PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

FIGURE 3.

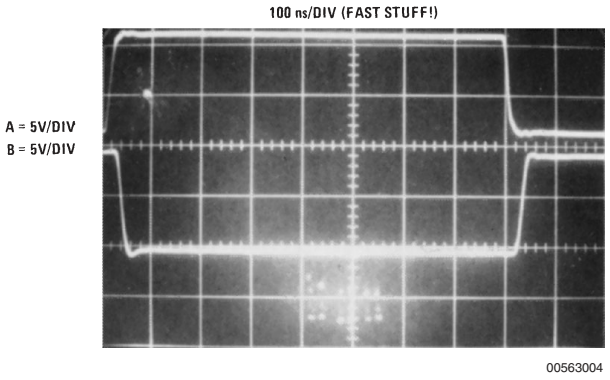


FIGURE 4.

Voltage-Current Booster

In many applications it is desirable to obtain voltage gain from a booster stage. Most monolithic amplifiers will only swing ±12V, although some types, such as the LM143, can swing ±35V. The circuit of *Figure 5* shows a simple way to effectively double the voltage swing across a load by stacking or "bridging" amplifier outputs. In the circuit shown, LF0002 current amplifiers are included in each LF412 output to provide current drive capability. Because one amplifier inverts and the other does not, the load sees 24V across it for ±12V swings from each amplifier. With the LH0002 current buffers, 24V can be placed across a 250Ω load. Although this circuit is simple and no high voltage supplies are needed, it requires that the load float with respect to ground.

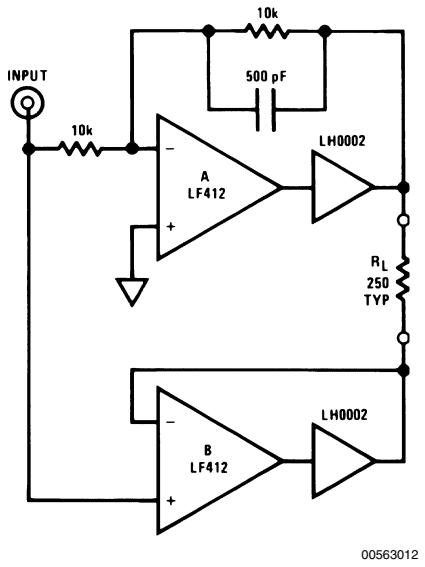
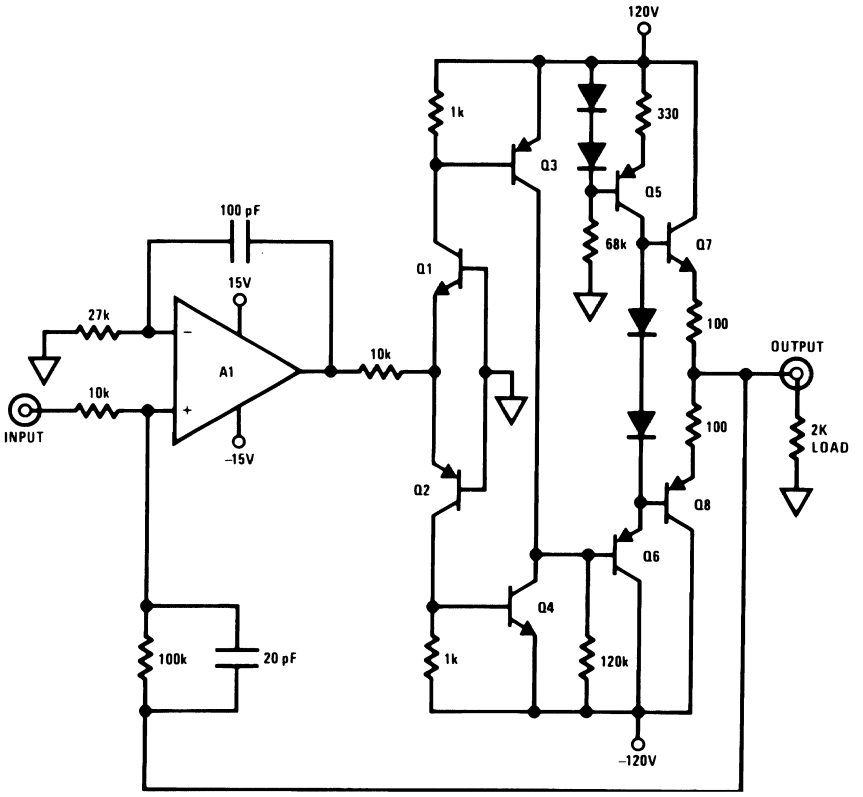


FIGURE 5.

±120V Swing Booster

In *Figure 7* the load does not have to float from ground to be driven at high voltage. This booster will drive a 2000Ω load to ±100V with good speed. In this circuit, voltage gain is obtained from the complementary common base stage, Q1-Q2. Q3 and Q4 provide additional gain to the Q7-Q8 complementary emitter-follower output stage. Q5 and Q6 provide bias, and crossover distortion is minimized by the diodes in Q5's collector line. For ±10V input signals, A1 must operate at a minimum gain of 10 to achieve a ±100V swing at the output. In this case, 10k-100k feedback values are used for a gain of ten, and the 20 pF capacitor provides loop roll-off. Because the booster contains an inverting stage (Q3-Q4), overall feedback is returned to A1's positive input. Local AC feedback at A1's negative input provides circuit dynamic stability. With its ±50 mA output, this booster yields currents as well as voltage gain. In many applications, such as CRT deflection plate driving, this current capability is not required. If this is the case, Q5 through Q8 and their associated components can be eliminated and the output and feedback taken directly from the Q3-Q4 collector line. Under these conditions, resistive output loading should not exceed 1 MΩ or significant crossover distortion will appear. Since deflection plates are a pure capacitive load, this is usually not a problem. *Figure 7* shows the boosted amplifier driving a ±100V square wave into a 2000Ω load at 30 kHz.

±120V Swing Booster (Continued)



A1 = LF357
PNP = 2N5415
NPN = 2N3440

FIGURE 6.

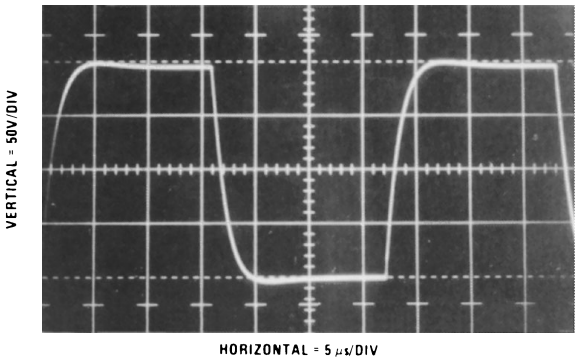
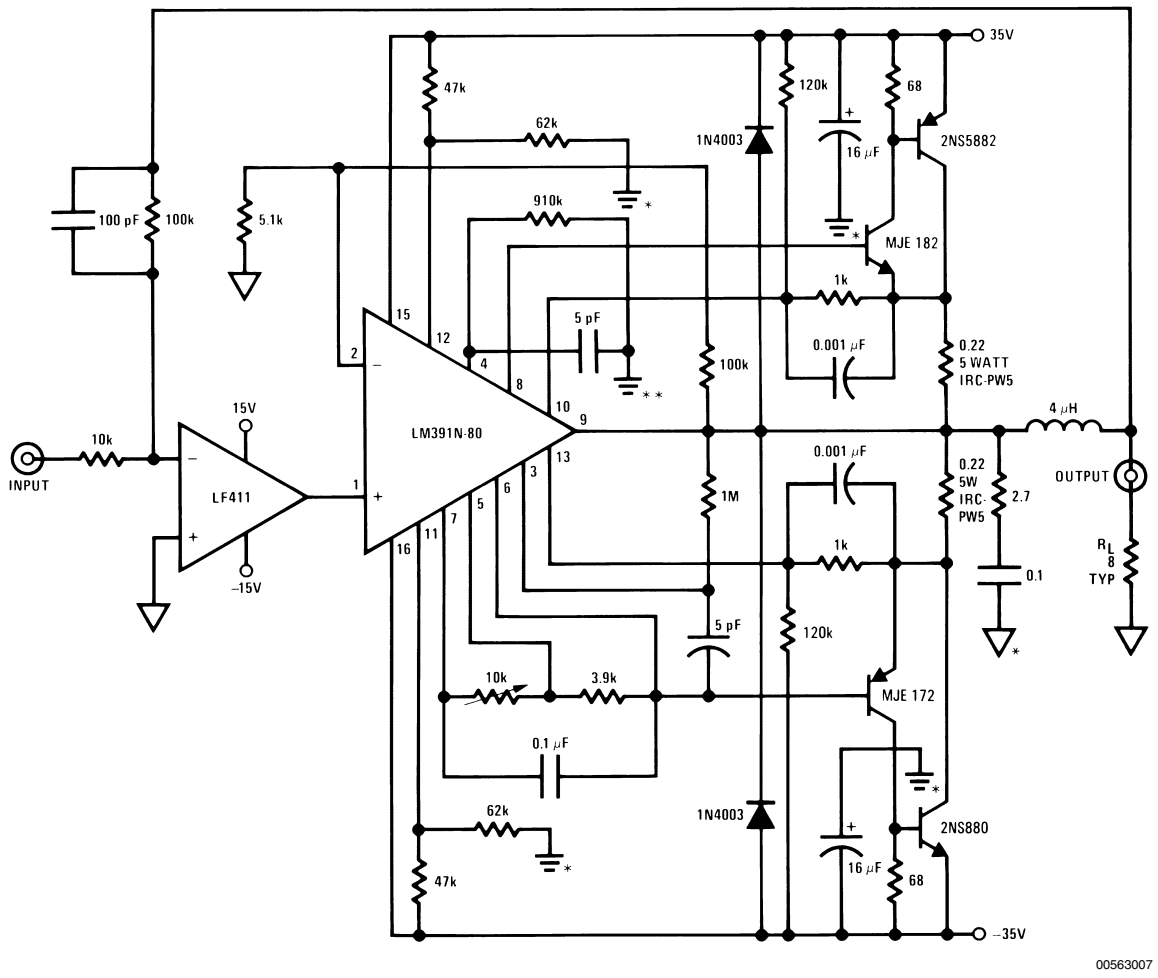


FIGURE 7.

High Current Booster

High current loads are well served by the booster circuit of *Figure 8*. While this circuit does provide voltage gain, its ability to drive 3A of current into an 8Ω load at 25V peak makes it useful as a current booster. In this circuit, the LM391-80 driver chip and its associated power transistors are placed inside the LF411's feedback loop. The 5 pF capacitor at pin 3 of the LM391-80 sets the booster bandwidth well past 250 kHz. The 100k-10k feedback resistors set a gain of ten, and the 100 pF feedback capacitor rolls off the loop gain at 100 kHz to insure stability for the amplifier-booster combination. The 2.7Ω-0.1 μF damper network and the 4 μH inductor prevent oscillations. The zero signal current of the output stage is set with the 10k potentiometer (pins 6-7 at the LM391) while a DVM is monitored for 10 mV across the 0.22Ω output resistors.

High Current Booster (Continued)



Adjust 10k pot
for 25 mA zero signal
current through the
0.22Ω resistors

* High frequency ground

** Input Ground

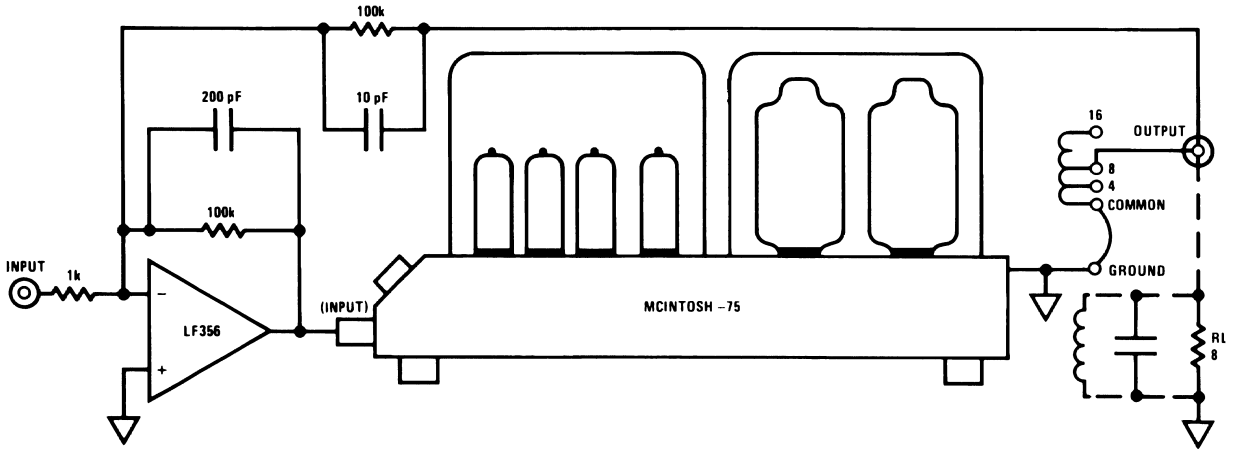
Note: All grounds should be tied together
only at power supply ground.
5.0˚ C/W heat sink on BD348 and BD349
3.0˚ C/W heat sink on BD360 and BD361

FIGURE 8.

Indestructible, Floating Output Booster

Figure 9 shows how a high quality audio amplifier can be used as a current-voltage booster for AC signals. The audio amplifier, specified as the booster, is a venerable favorite in research labs, due to its transformer isolated output and clean response. The LF356 op amp's loop is closed locally at a DC gain of 100, and rolled off at 50 kHz by the 200 pF capacitor. The audio amplifier booster's output is fed back via the 100k resistor for an overall AC gain of 100 with respect to the booster amplifier output. The arrangement is ideal for laboratory use because the vacuum tube driven transformer isolated output is extremely forgiving and almost indestructible. AC variable frequency power supplies, shaker table drives, motors and gyro drives, as well as other difficult inductive and active loads, can be powered by this booster. Power output is 75W into 4Ω-16Ω, although loads of 1Ω can be driven at reduced power output.

Indestructible, Floating Output Booster (Continued)



Phase Shift — Less than ±8° 20-20 kHz

Power Output — 75 watts RMS 16 Hz-60 kHz

Output Impedance — Less than 10% of rated output load Z.

Frequency Response — 10 Hz-100 kHz-1 dB.

16 Hz-40 kHz-0.1 dB.

16 Hz-60 kHz-0.5 dB.

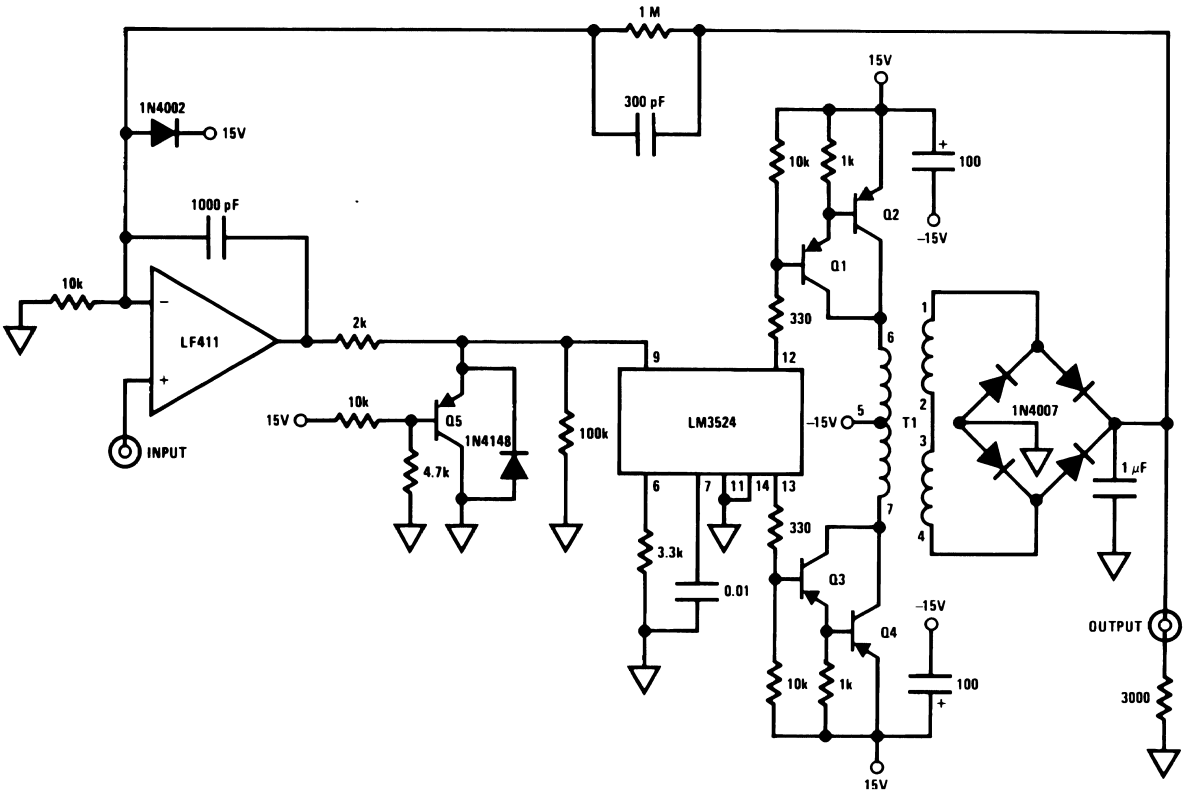
FIGURE 9.

1000V-300 mA Booster

Figure 10 diagrams a very high voltage, high current booster which will allow an op amp to control up to 300W for positive outputs up to a staggering 1000V. This performance is achieved without sacrificing efficiency because this booster, in contrast to all the others shown, operates in a switching mode. In addition, this booster runs off ±15V supplies and has the highly desirable property of *not* requiring a high voltage power supply to achieve its high potential outputs. The high voltage required for the output is directly generated by a switching DC-DC converter which forms an integral part of the booster. The LM3524 switching regulator chip is used to pulse width modulate the transistors which provide switched 20 kHz drive to the TY-85 step-up transformer. The transformer's rectified and filtered output is fed back to the LF411, which controls the input to the LM3524 switching regulator. In this manner, the high voltage booster, although operating switched mode, is controlled by the op amp's feedback action in a similar fashion to all the other designs. Q5 and the diode act as clamps to prevent the LF411's output swing from damaging the LM3524's 4V input on start-up. The diode at the LF411 swing junction prevents high voltage transients coupled through the feedback capacitor from destroying the amplifier. The 1 MΩ-10k feedback resistors set the gain of the amplifier at 100 so that a 10V input will give a 1000V output. Although the 20 kHz torroid switching rate places an upper limit on how fast information can be transmitted around the loop, the 1 µF filter capacitor at the circuit output restricts the bandwidth. For the design shown, full power sine wave output frequency is 55H. *Figure 11* shows the response of the boosted LF411 when a 10V pulse (Trace A) is applied to the circuit input. The output (Trace B) goes to 1000V in about 1 ms, while fall time is about 10 ms because of capacitor discharge time. During the output pulse's rise time the booster is slew rate limited and the switching action of the torroid is just visible in the leading edge of the pulse.

The reader is advised that the construction, testing and use of this circuit must be approached with the greatest care. The output potentials produced are many times above the level which will kill. Repeating, the output of this circuit is lethal.

1000V-300 mA Booster (Continued)

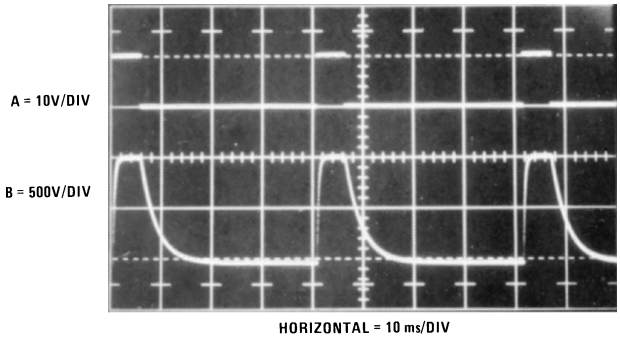


00563015

T1 = Triad TY-85
Q1, Q3 = 2N3468
Q2, Q4 = 2N4399
Q5 = 2N2907

CAUTION:
LETHAL OUTPUT POTENTIALS

FIGURE 10. Son of Godzilla Booster



00563009

FIGURE 11.

300V Output Booster

The circuit of *Figure 12* is another high voltage booster, but will only provide 10 mA of output current. This positive-output-only circuit will drive 350V into a 30k load, and is almost immune to load shorts and reverse voltages. A solid state output requires substantial protection against these conditions. Although the circuit shown has a 350V limit, tubes (remember them?) with higher plate voltage ratings can extend the output capacity to several kilovolts. In this circuit, our thermionic friends are arranged in a common cathode (V2B) loaded-cathode-follower (V2A) output, driven from a common cathode gain stage (V1). The booster output is fed back to the LF357 via the 1 MΩ resistor. Local feedback is used to stabilize the LF357, while the pF-1 MΩ pair rolls off the loop at 1 MHz. Because the V1 stage inverts, the feedback summing junction is placed at the LF357 positive input. The parallel diodes at the summing junction prevent

300V Output Booster (Continued)

high voltage from destroying the amplifier during circuit start-up and slew rate limiting. Tubes are inherently much more tolerant of load shorts and reverse voltages than transistors, and are much easier to protect. In this circuit, an LM335 temperature sensor is in contact with V2. This sensor's output is compared with another LM335 which senses ambient temperature. Under normal operating conditions, V2 operates about 45˚C above ambient and the "+" input of the LF311 is about −100 mV, causing its output to be low. When a load fault occurs, V2's plate dissipation increases, causing its associated LM335's output to rise with respect to ambient temperature. This forces the LF311's output high, which makes the LF357 output go low, shutting down the output stage. Adequate hysteresis is provided by the thermal time constant of V2 and the 10 MΩ-1 µF delay in the LF311 input line. *Figure 13* shows the response of this amplifier booster at a gain of about 25. With a 15V input pulse (Trace A), the output (Trace B) goes to 350V in 1 µs, and settles within 5 µs. The falling edge slews equally fast and settling occurs within 4 µs.

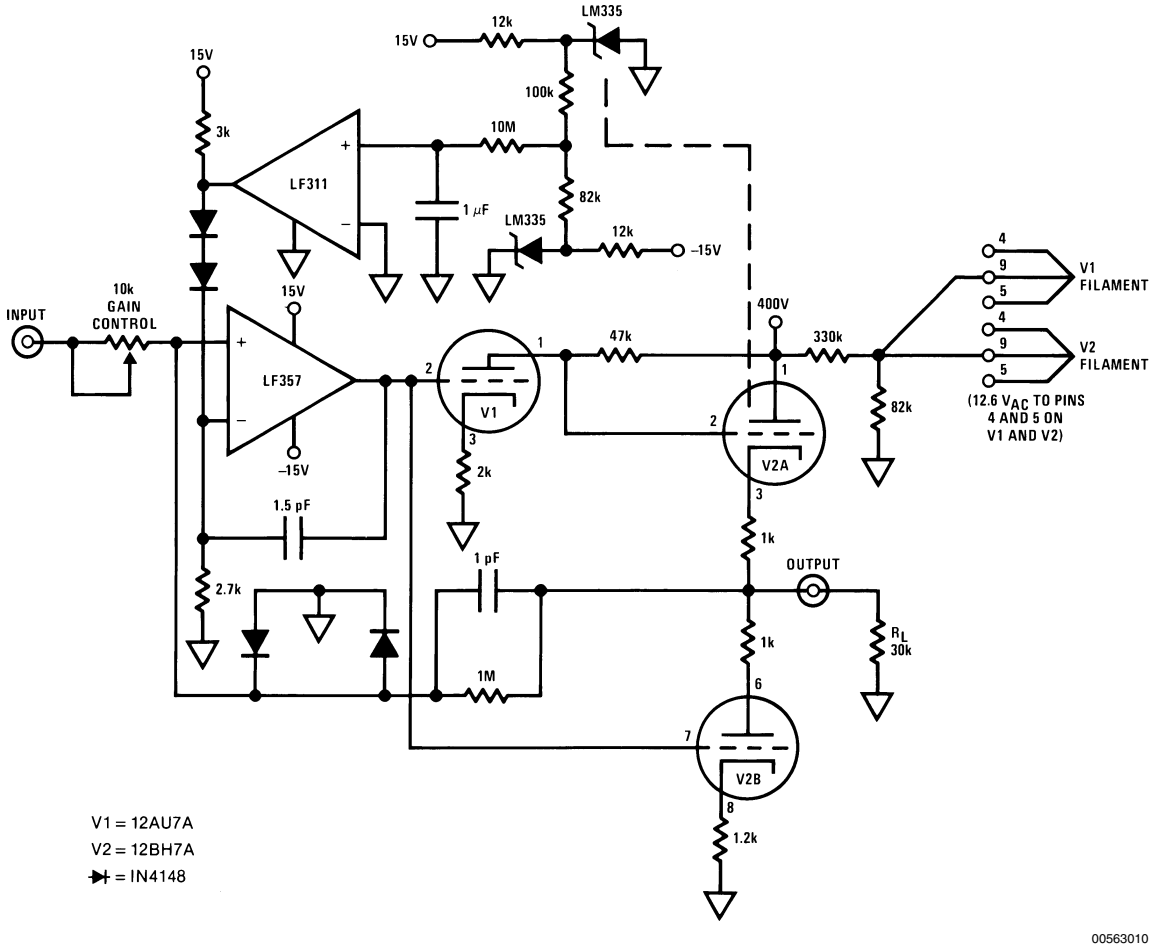


FIGURE 12.

300V Output Booster (Continued)

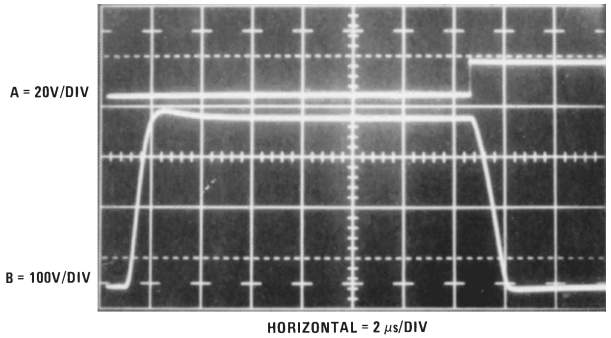


FIGURE 13.

Figure 14 is a table which summarizes the information in this article and will help you to pick the right booster for your particular application.

Figure	Voltage Gain	Current Gain	Bandwidth	Comments
1	No	Yes—200 mA	Depends on op amp. Typical 1 MHz	Full "+" and "–" output swing. Stable into 50Ω-10,000 pF load. Inverting or non-inverting operation. Simple.
3	No	Yes—200 mA	Full output to 5 MHz-3dB. Point at 11 MHz.	Ultra fast. 750V/μs. Full bipolar output. Inverting operation only.
5	Yes—24V swing	No	Depends on op amp.	Requires that load float from ground.
6	Yes—±100V	Yes—50 mA	50 kHz typical.	Full "+" and "–" output swing. Allows inverting or non-inverting operation. Simplified version ideal for CRT deflection plate driving. More complex version drives full 200V swing into 2 kΩ and 1000 pF.
8	Yes—±30V	Yes—3A	50 kHz	Full "+" and "–" output swing. Allows inverting or non-inverting operation.
9	Yes—70V swing	Yes—3A	100 kHz	Output extremely rugged. Well suited for driving difficult loads in lab. Set-ups. Full bipolar output. AC only.
10	Yes—1000V	Yes—300 mA	50 Hz	High voltage at high current. Switched mode operation allows operation from ±15V supplies with good efficiency. Limited bandwidth with asymmetrical slewing. Positive outputs only.
12	Yes—350V	No	500 kHz	Output very rugged. Good speed. Positive outputs only.

FIGURE 14.

An Acoustic Transformer Powered Super-High Isolation Amplifier

National Semiconductor
Application Note 285
October 1981

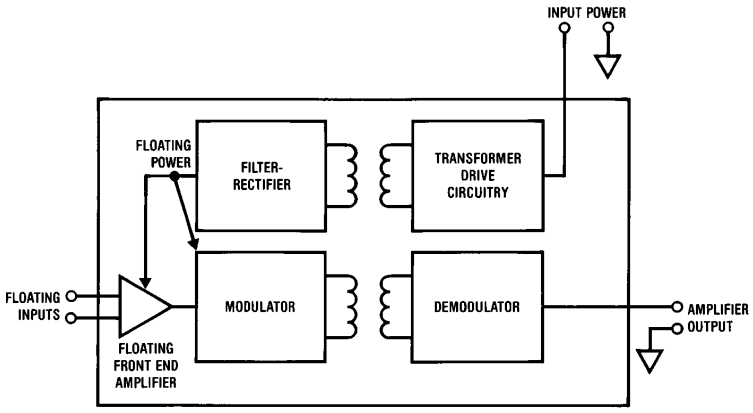
A number of measurements require an amplifier whose input terminals are galvanically isolated from its output and power terminals. Such devices, often called parametric or isolation amplifiers, are employed in situations that call for measurements in the presence of high common-mode voltages or require complete ground path isolation for safety reasons. Although commercial devices are available to meet these needs, the method of power transfer used to supply power to the floating input circuitry has limited the common-mode voltage capability to about 2500V. In addition, leakage currents can run as high as 2 μA.

Present devices (*Figure 1)* employ transformers to transmit power to the floating front end of the amplifier. The output of the floating amplifier is then modulated onto a carrier which is transmitted via a transformer or opto-isolator to the output of the amplifier. Modulation schemes employed include pulse width and pulse amplitude as well as frequency and light intensity coding. The limitation on common-mode voltage breakdown and leakage in this type of device is the breakdown rating of the transformers employed. Even when opto-isolators are used to transmit the modulated signal, the requirement for power to run the floating front end mandates the need for at least one transformer in the amplifier.

Although other methods of transmitting electrical energy with high isolation are available (e.g., microwaves, solar cells) they are expensive, inefficient and impractical. Batteries present and obvious choice but have drawbacks due to maintenance and reliability. What is really needed to achieve extremely high common-mode capability and low leakage is a method for transferring electrical energy which is relatively efficient, easy to implement and offers almost total input-to-input isolation.

ACOUSTIC TRANSFORMERS

A technique which satisfies the aforementioned requirements is available by taking advantage of the piezoelectric characteristics of certain ceramic materials. Although piezoelectric materials have long been recognized as electrical-to-acoustic or acoustic-to-electrical transducers (e.g., buzzers and microphones) their capability for electrical-to-acoustic-to-electrical energy conversion has not been employed. This technique, which capitalizes on the non-conducting nature of ceramic materials, is the key to a super-high isolation electrical transformer. In this device the conventional transformer's transmission medium of magnetic flux and conductive core material is replaced by acoustic waves and a



TL/H/5634–1

FIGURE 1

RRD-B30M125/Printed in U. S. A.

non-conducting piezoceramic core. *Figure 2* shows a photograph of typical acoustic transformers, fabricated by Channel Industries, Santa Barbara, California. Two physical configurations are shown, although many are possible. In each case the transformer is constructed by simply bonding a pair of leads to each end of the piezoceramic material. Insulation resistance exceeds $10^{12}\Omega$ and primary-to-secondary capacitance is typically a few pF. The nature of the piezoceramic material employed and the specific physical configuration determines the resonant frequency of the transformer. *Figure 3* shows a plot of the output of an acoustic transformer driven at resonance. From the data it can be seen that transfer efficiency can exceed 75%, depending upon loading conditions. Output short circuit current for the device tested was 35 mA.

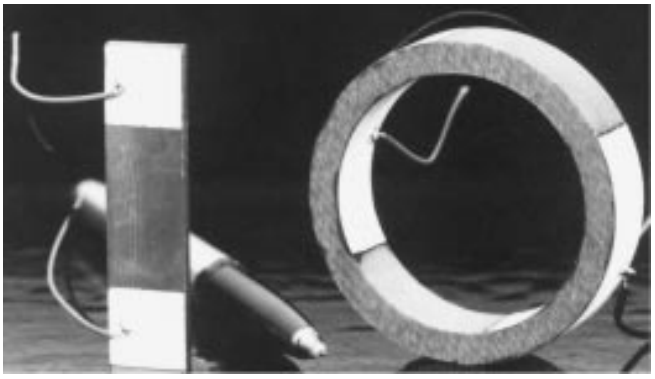
APPLYING THE TRANSFORMER—A 20,000V ISOLATION AMPLIFIER

Figure 4 shows a basic but working design for an isolation amplifier using the acoustic transformer. This design will easily stand off common-mode voltages of 20,000V and versions that operate at 100 kV potentials have been constructed. In this design the acoustic transformer's HI-Q characteristics are used to allow it to self resonate in a manner similar to a quartz crystal. This eliminates the requirement to drive the transformer with a stable oscillator.

The Q1 configuration provides excitation to the transformer primary, while the diodes and capacitor rectify and filter the secondary's output. *Figure 5* shows the collector waveform at Q1 (Trace A) while Trace B, *Figure 5* shows the secondary output. Despite the distorted drive waveform the transformer's secondary output is a clean sinusoid because of the extremely Hi-Q of the device. An LM331 V/F converter is used to convert the amplitude input to a frequency output. The V/F output drives an LED, whose output is coupled to a length of fiber-optic cable. Trace A, *Figure 6* shows the LM331's output, while Trace B indicates the current through the LED. Each time the LM331 output goes low, a short 20 mA current spike is passed through the LED via the 0.01 μF capacitor. Because the duty cycle is low, the average current out of the transformer's secondary is small and power requirements are minimized. At the amplifier output a photodiode is used to detect the light encoded signal and another LM331 serves as an F/V converter to demodulate the frequency encoded signal.

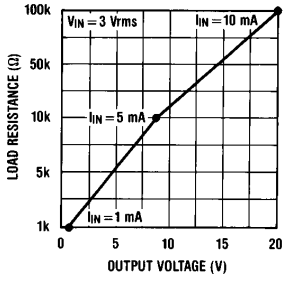
APPLICATIONS

An excellent application for the high isolation amplifier is shown in *Figure 7*. Here, the winding temperature of an electric utility transformer operating at 10,000V is monitored by the LM135 temperature transducer. The LM135 output biases the isolation amplifier input and the temperature information comes out at the amplifier output, safely referenced to ground.



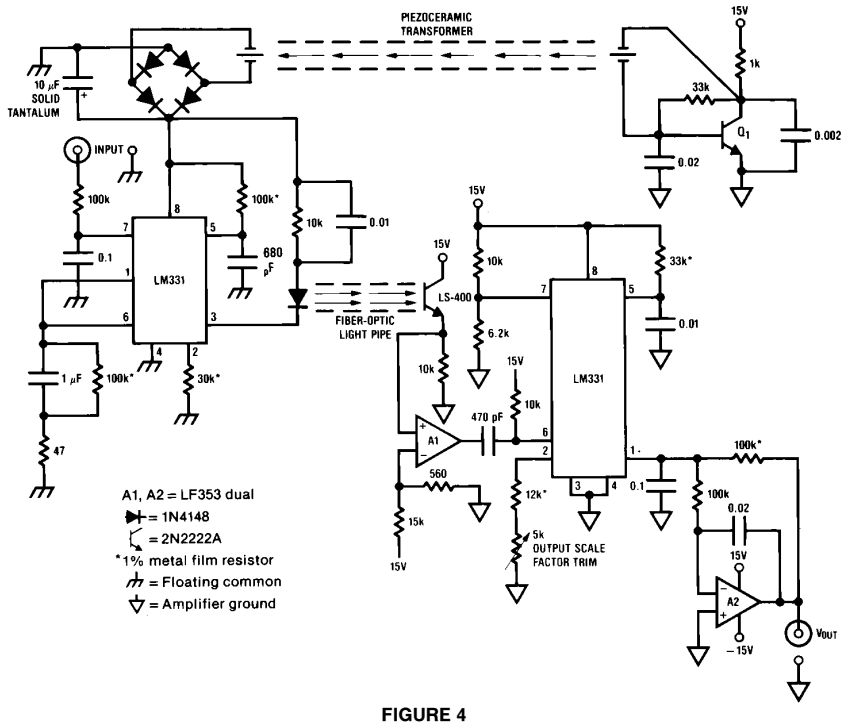
TL/H/5634–2

FIGURE 2



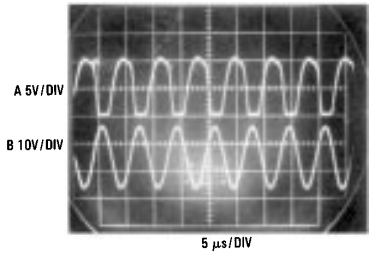
TL/H/5634–3

FIGURE 3



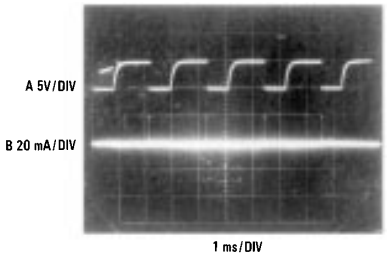
TL/H/5634–4

FIGURE 4



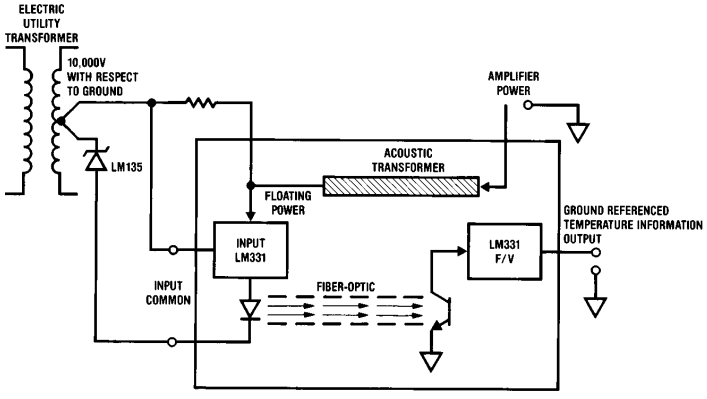
TL/H/5634–5

FIGURE 5



TL/H/5634–6

FIGURE 6



TL/H/5634–7

FIGURE 7

Figure 8 shows another application where the high common-mode voltage capability allows a 5000V regulated power supply to have a fully floating output. Here, a push-pull type DC-DC converter generates the 5 kV output. The piezo-isolation amplifier provides a ground referenced output feedback signal to A1, which controls the transformer drive, completing a feedback loop.

In *Figure 9,* the piezo-isolation amplifier is used to provide complete and fail-safe isolation for the inputs of a piece of test equipment to be connected into a CMOS IC production line. This capability prevents any possibility of static discharge damage, even when the equipment may have accumulated a substantial charge.

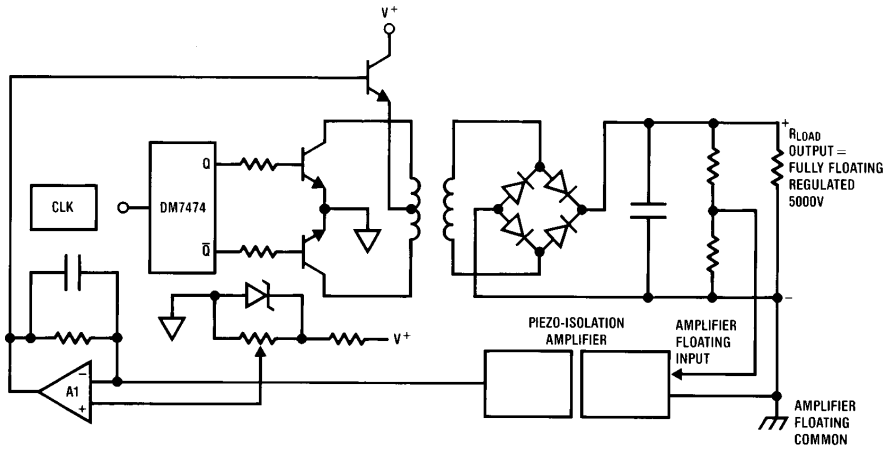
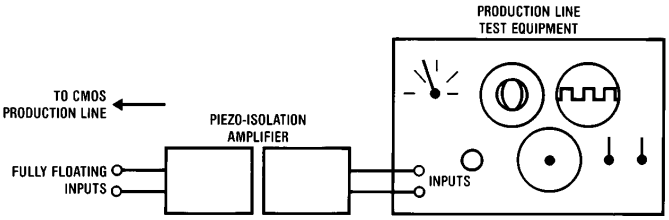


FIGURE 8



TL/H/5634–8

FIGURE 9

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Applications of the LM392 Comparator Op Amp IC

National Semiconductor
Application Note 286
September 1981

The LM339 quad comparator and the LM324 op amp are among the most widely used linear ICs today. The combination of low cost, single or dual supply operation and ease of use has contributed to the wide range of applications for these devices.

The LM392, a dual which contains a 324-type op amp and a 339-type comparator, is also available. This device shares all the operating features and economy of 339 and 324 types with the flexibility of both device types in a single 8-pin mini-DIP. This allows applications that are not readily implemented with other devices but retain simplicity and low cost. *Figure 2* provides an example.

Sample-Hold Circuit

The circuit of *Figure 2* is an unusual implementation of the sample-hold function. Although its input-to-output relationship is similar to standard configurations, its operating principle is different. Key advantages include simplicity, no hold step, essentially zero gain error and operation from a single 5V supply. In this circuit the sample-hold command pulse (Trace A, *Figure 1*) is applied to Q3, which turns on, causing current source transistor Q4's collector (Trace B, *Figure 1*) to go to ground potential. Amplifier A1 follows Q4's collector voltage and provides the circuit's output (Trace C, *Figure 1*). When the sample-hold command pulse falls, Q4's collector drives a constant current into the 0.01 µF capacitor. When the capacitor ramp voltage equals the circuit's input voltage, comparator C1 switches, causing Q2 to turn off the current source. At this point the collector voltage of Q4 sits at the circuit's input voltage. Q1 insures that the comparator will not self trigger if the input voltage increases during a "hold" interval. When a DC biased sine wave is applied to the circuit (Trace D, *Figure 1*) the sampled output (Trace E, *Figure 1*) is available at the circuit's output. The ramping action of the Q4 current source during the "sample" states is just visible in the output.

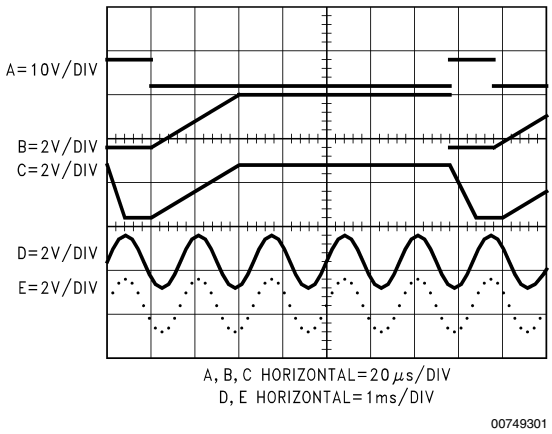
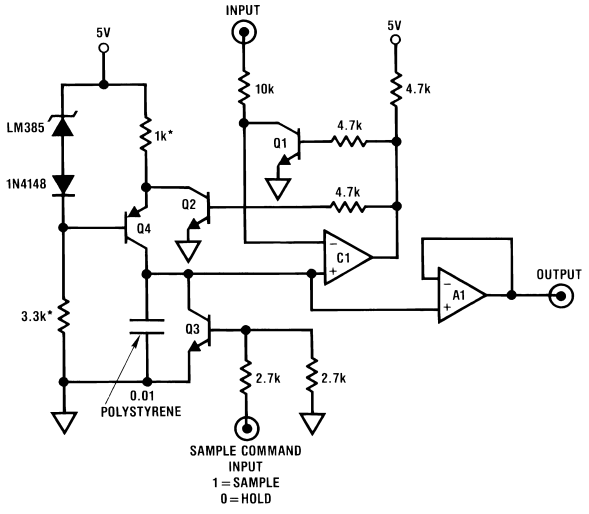


FIGURE 1.



Q1, Q2, Q3 = 2N2369

Q4 = 2N2907

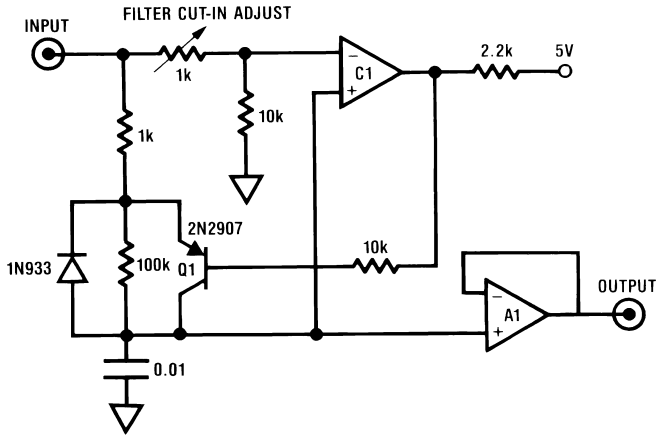
C1, A1 = LM392 amplifier-comparator dual

*1% metal film resistor

FIGURE 2.

"Fed-Forward" Low-Pass Filter

In *Figure 3* the LM392 implements a useful solution to a common filtering problem. This single supply circuit allows a signal to be rapidly acquired to final value but provides a long filtering constant. This characteristic is useful in multiplexed data acquisition systems and has been employed in electronic infant scales where fast, stable readings of infant weight are desired despite motion on the scale platform. When an input step (Trace A, *Figure 4*) is applied, C1's negative input will immediately rise to a voltage determined by the 1k pot-10 kΩ divider. C1's "+" input is biased through the 100 kΩ-0.01 µF time constant and phase lags the input. Under these conditions C1's output will go low, turning on Q1. This causes the capacitor (Waveform B, *Figure 1*) to charge rapidly towards the input value. When the voltage across the capacitor equals the voltage at C1's positive input, C1's output will go high, turning off Q1. Now, the capacitor can only charge through the 100k value and the time constant will be long. Waveform B clearly shows this. The point at which the filter switches from short to long time constant is adjustable with the 1 kΩ potentiometer. Normally, this is adjusted so that switching occurs at 90%–98% of final value, but the photo was taken at a 70% trip point so circuit operation is easily discernible. A1 provides a buffered output. When the input returns to zero the 1N933 diode, a low forward drop type, provides rapid discharge for the capacitor.



A1, C1 = LM392 amplifier-comparator dual

FIGURE 3.

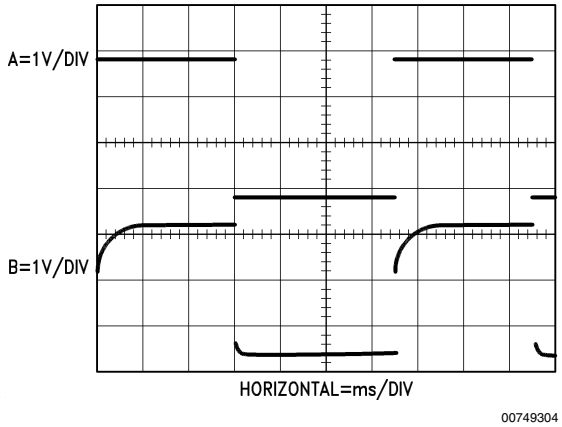


FIGURE 4.

Variable Ratio Digital Divider

In *Figure 5* the circuit allows a digital pulse input to be divided by any number from 1 to 100 with control provided by a single knob. This function is ideal for bench type work where the rapid set-up and flexibility of the division ratio is highly desirable. When the circuit input is low, Q1 and Q3 are off and Q2 is on. This causes the 100 pF capacitor to accumulate a quantity of charge (Q) equal to

$Q = CV$

where C = 100 pF

and V = the LM385 potential (1.2V) minus the $V_{CE(SAT)}$ of Q2.

When the input goes high (Trace A, *Figure 6*) Q2 goes off and Q1 turns on Q3. This causes Q3 to displace the 100 pF capacitor's charge into A1's summing junction. A1's output responds (Waveform B, *Figure 6*) by jumping to the required

Variable Ratio Digital Divider

(Continued)

value to maintain the summing junction at 0V. This sequence is repeated for every input pulse. During this time A1's output will form the staircase shape shown in Trace B as the 0.02 µFfeedback capacitor is pumped up by the charge dispensing action into A1's summing junction. When A1's output is great enough to just bias C1's "+" input below ground, C1's output (Trace C, *Figure 6*) goes low and resets A1 to 0V. Positive feedback to C1's "+" input (Trace D, *Figure 6*) comes through the 300 pF unit, insuring adequate reset time for A1. The 1 MΩ potentiometer, by setting the number of steps in the ramp required to trip C1, controls the circuit input-output division ratio. Traces E–G expand the scale to show circuit detail. When the input (Trace E) goes high, charge is deposited into A1's summing junction (Trace F) and the resultant staircase waveform (Trace G) takes a step.

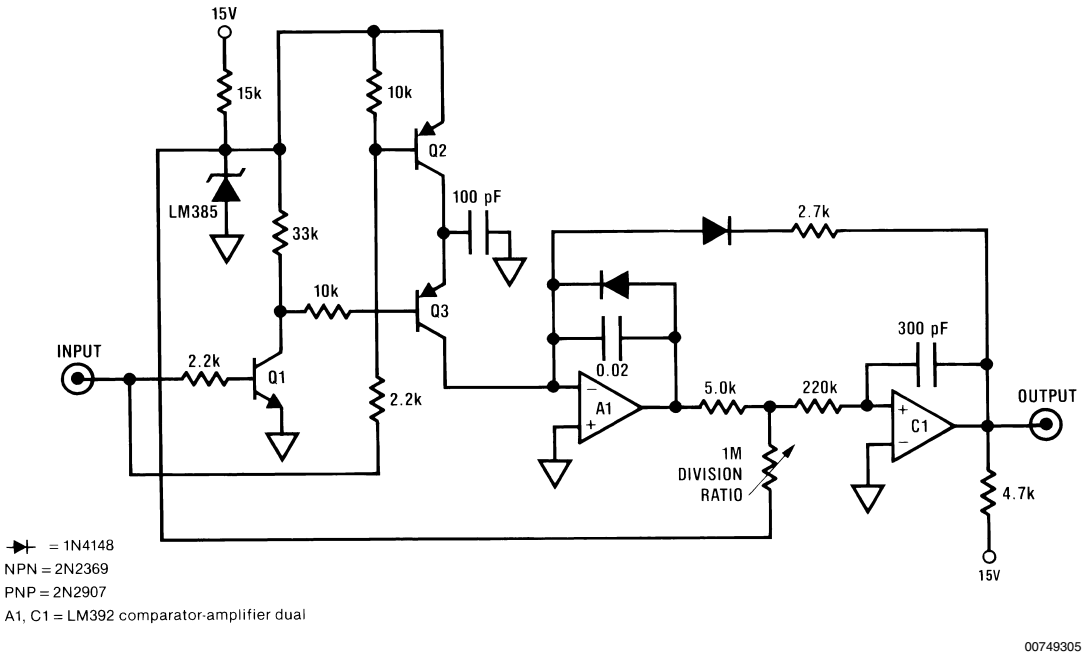


FIGURE 5.

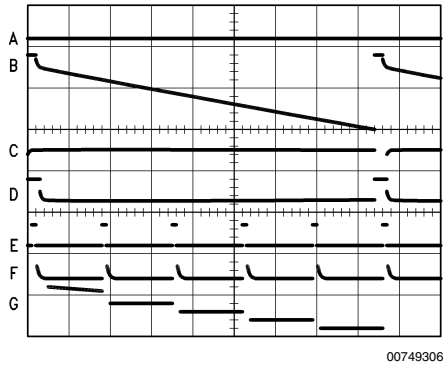


FIGURE 6.

Trace	Vertical	Horizontal
A	10V	500 µs
B	1V	500 µs
C	50V	500 µs
D	50V	500 µs
E	10V	50 µs

Trace	Vertical	Horizontal
F	10 mA	50 µs
G	0.1V	50 µs

Exponential V/F Converter for Electronic Music

Professional grade electronic music synthesizers require voltage controlled frequency generators whose output frequencies are exponentially related to the input voltages. *Figure 7* diagrams a circuit which performs this function with 0.25% exponential conformity over a range from 20 Hz to 15 kHz using a single LM392 and an LM3045 transistor array. The exponential function is generated by Q1, whose collector current will vary exponentially with its base-emitter voltage in accordance with the well known relationship between BE voltage and collector current in bipolar transistors. Normally, this transistor's operating point will vary wildly with temperature and elaborate and expensive compensation is required. Here, Q1 is part of an LM3045 transistor array. Q2 and Q3, located in the array, serve as a heater-sensor pair for A1, which servo controls the temperature of Q2. This causes the entire LM3045 array to be at constant temperature, eliminating thermal drift problems in Q1's operation. Q4 acts as a clamp, preventing servo lock-up during circuit start-up.

Exponential V/F Converter for Electronic Music (Continued)

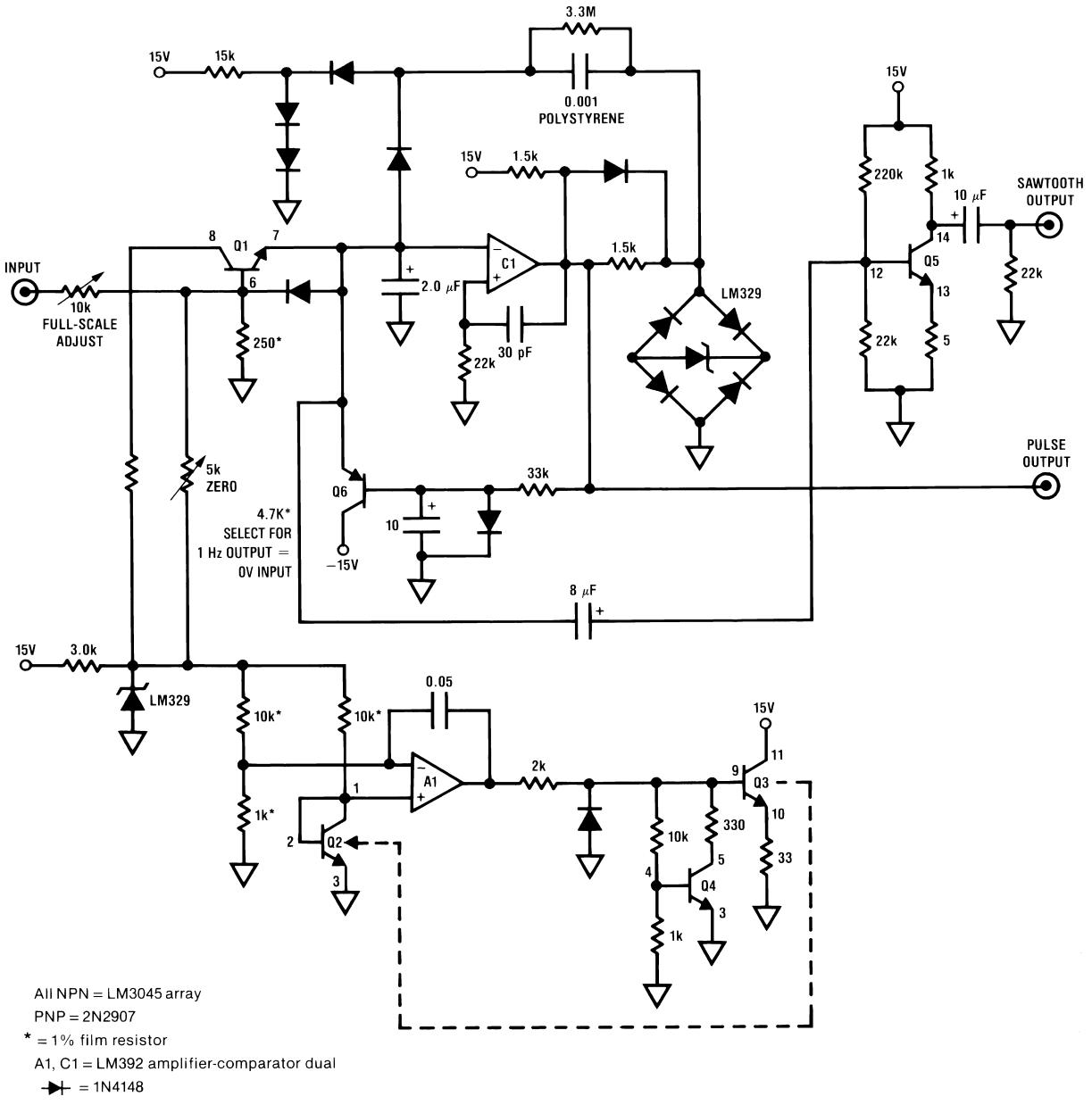


FIGURE 7.

Q1's current output is fed into the summing junction of a charge dispensing I/F converter. C1's output state is used to switch the 0.001 µF capacitor between a reference voltage and C1's "–" input. The reference voltage is furnished by the LM329 zener diode bridge. The comparator's output pulse width is unimportant as long as it permits complete charging and discharging of the capacitor. In operation, C1 drives the 30 pF-22k combination. This RC provides regenerative feedback which reinforces the direction of C1's output. When the 30 pF-22k combination decays, the positive feedback ceases. Thus, any negative going amplifier output will be followed by a positive edge after an amount of time governed by the 30 pF-22k time constant (Waveforms A and B, *Figure 8*). The actual integration capacitor in the circuit is the 2 µF electrolytic. This capacitor is never allowed to charge beyond 10 mV–15 mV because it is constantly being reset by charge dispensed from the switching of the 0.001 µF capacitor (Waveform C, *Figure 8*). Whenever the amplifier's output goes negative, the 0.001 µF capacitor dumps a quantity of charge (Waveform D) into the 2 µF capacitor, forcing it to a lower potential. The amplifier's output going negative also causes a short pulse to be transferred through the 30 pF capacitor to the "+" input. When this negative pulse decays out so that the "+" input is higher than the "–" input, the 0.001 µF capacitor is again able to receive a charge and the entire process repeats. The rate at which this sequence occurs is directly related to the current into C1's summing junction from Q1. Since this current is exponentially related to the

Exponential V/F Converter for Electronic Music (Continued)

circuit's input voltage, the overall I/F transfer function is exponentially related to the input voltage. This circuit can lock-up under several conditions. Any condition which would allow the 2 µF electrolytic to charge beyond 10 mV–20 mV (start-up, overdrive at the input, etc.) will cause the output of the amplifier to go to the negative rail and stay there. The 2N2907A transistor prevents this by pulling the "–" input towards –15V. The 10 µF-33k combination determines when the transistor will come on. When the circuit is running normally, the 2N2907 is biased off and is effectively out of the circuit. To calibrate the circuit, ground the input and adjust the zero potentiometer until oscillations just start. Next, adjust the full-scale potentiometer so that frequency output exactly doubles for each volt of input (e.g., 1V per octave for musical purposes). Repeat these adjustments until both are fixed. C1 provides a pulse output while Q5 AC amplifies the summing junction ramp for a sawtooth output.

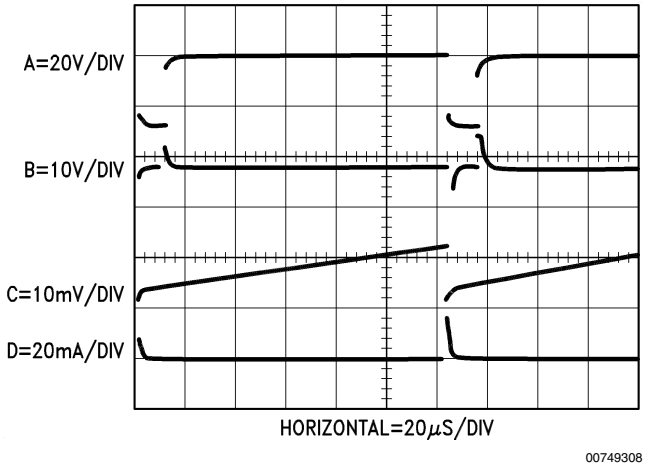
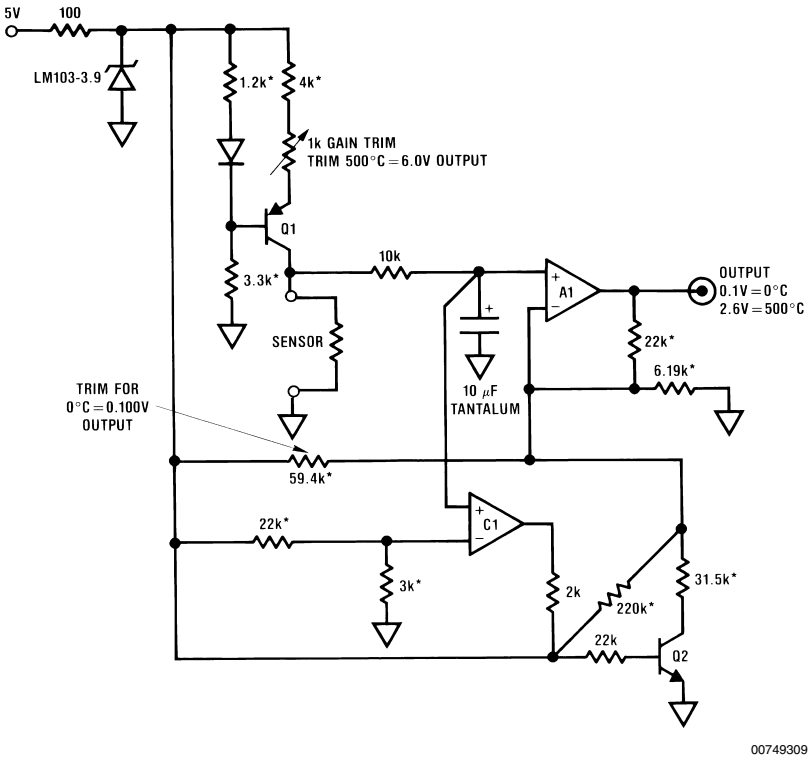


FIGURE 8.

Linearized Platinum RTD Thermometer

In *Figure 9* the LM392 is used to provide gain and linearization for a platinum RTD in a single supply thermometer circuit which measures from 0˚C to 500˚C with ±1˚C accuracy. Q1 functions as a current source which is slaved to the LM103-3.9 reference. The constant current driven platinum sensor yields a voltage drop which is proportionate to temperature. A1 amplifies this signal and provides the circuit output. Normally the slight nonlinear response of the RTD would limit accuracy to about ±3 degrees. C1 compensates for this error by generating a breakpoint change in A1's gain for sensor outputs above 250˚C. When the sensor's output indicates 250˚C, C1's "+" input exceeds the potential at the "–" input and C1's output goes high. This turns on Q2 whose collector resistor shunts A1's 6.19k feedback value, causing a gain change which compensates for the sensor's slight loss of gain from 250˚C to 500˚C. Current through the 220k resistor shifts the offset of A1 so no "hop" occurs at the circuit output when the breakpoint is activated. A precision decade box is used to calibrate this circuit. With the box inserted in place of the sensor, adjust 0˚C for 0.10V output for a value of 1000Ω. Next dial in 2846Ω (500˚C) and adjust the gain trim for an output of 2.60V. Repeat these adjustments until both zero and full-scale are fixed at these points.

Linearized Platinum RTD Thermometer (Continued)



Sensor = Rosemount
118 MF-1000-A
1000Ω at 0˚C

Q1 = 2N2907

Q2 = 2N2222A

A1, C1 = LM392 amplifier-comparator dual

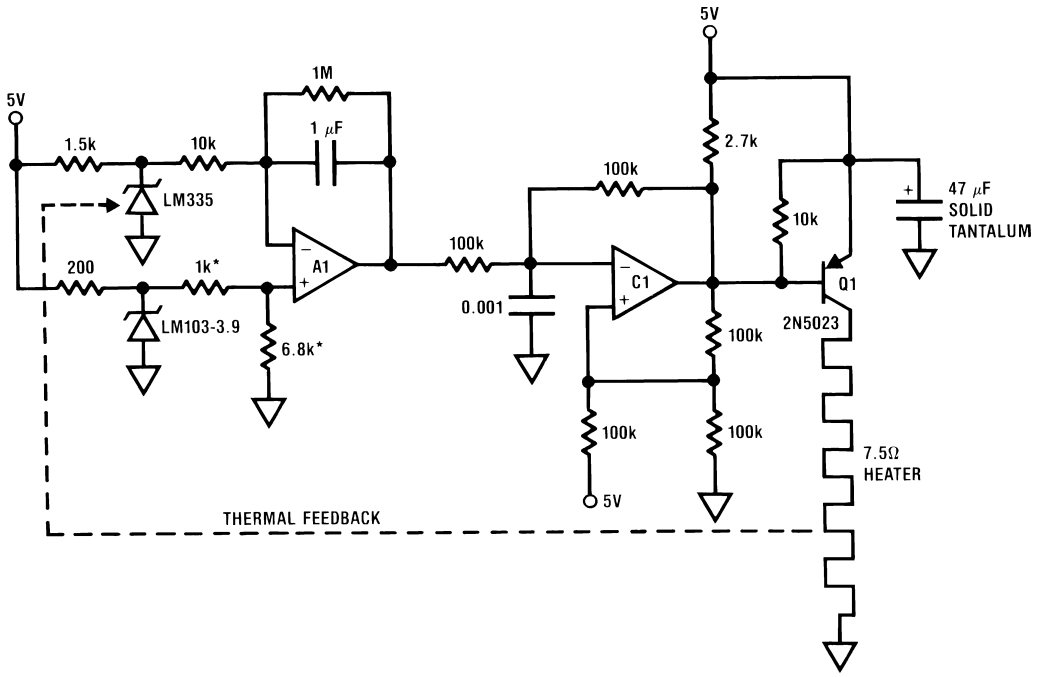
*metal film resistor

FIGURE 9.

Temperature Controller

Figure 10 details the LM392 in a circuit which will temperature-control an oven at 75˚C. This is ideal for most types of quartz crystals. 5V single supply operation allows the circuit to be powered directly from TTL-type rails. A1, operating at a gain of 100, determines the voltage difference between the temperature setpoint and the LM335 temperature sensor, which is located inside the oven. The temperature setpoint is established by the LM103-3.9 reference and the 1k–6.8k divider. A1's output biases C1, which functions as a pulse width modulator and biases Q1 to deliver switched-mode power to the heater. When power is applied, A1's output goes high, causing C1's output to saturate low. Q1 comes on and delivers DC to the heater. When the oven warms to the setpoint, A1's output falls and C1 begins to pulse width modulate the heater in servo control fashion. In practice the LM335 should be in good thermal contact with the heater to prevent servo oscillation.

Temperature Controller (Continued)



A1, C1 = LM392 amplifier-comparator dual

FIGURE 10.

References

1. *Transducer Interface Handbook,* pp. 220–223; Analog Devices, Inc.

2. "A New Ultra-Linear Voltage-to-Frequency Converter", Pease, R. A.; *1973 NEREM Record* Volume 1, page 167.

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System-Oriented DC-DC Conversion Techniques

National Semiconductor
Application Note 288
April 1998

In many electronic systems, the need arises to generate small amounts of power at voltages other than the main supply voltage. This is especially the case in digital systems where a relatively small amount of analog circuitry must be powered. A number of manufacturers have addressed this requirement by offering modular DC-DC converters which are PC mountable, offer good efficiency and are available in a variety of input and output voltage ranges. These units are widely applied and, in general, are well engineered for most applications. The sole problem with these devices is noise, in the form of high frequency switching spikes which appear on the output lines. To understand why these spikes occur, it is necessary to examine the operation of a converter.

A typical DC-DC converter circuit is shown in *Figure 1*. The transistors and associated components combine with the transformer primary to form a self-driven oscillator which provides drive to the transformer. The transformer secondary is rectified, filtered and regulated to obtain the outputs required. Typically, the transistors switch in saturated mode at 20 kHz, providing high efficiency square wave drive to the transformer. The output filter capacitors are relatively small compared to sine wave driven transformers and overall losses are quite low. The high speed, saturated switching of the transistors does, however, generate high frequency noise components. These manifest themselves as short duration current spikes drawn from the converter's input supply and as high speed spikes which appear on the output lines. In addition, the transformer can radiate noise in RF fashion. Manufacturers have dealt with these problems through careful converter design, including attention to input filter design, transformer construction and package shielding. *Figure 2* shows typical output noise of a good quality commercial DC-DC converter. The spikes are approximately 10 mV–20 mV in amplitude and occur at each transition of the switching transistors. In many applications this noise level is acceptable, but in data acquisition and other systems which work at 12-bit and higher resolutions, problems begin to crop up. In these situations, special system-oriented DC-DC converter techniques must be employed to insure against the problems outlined above.

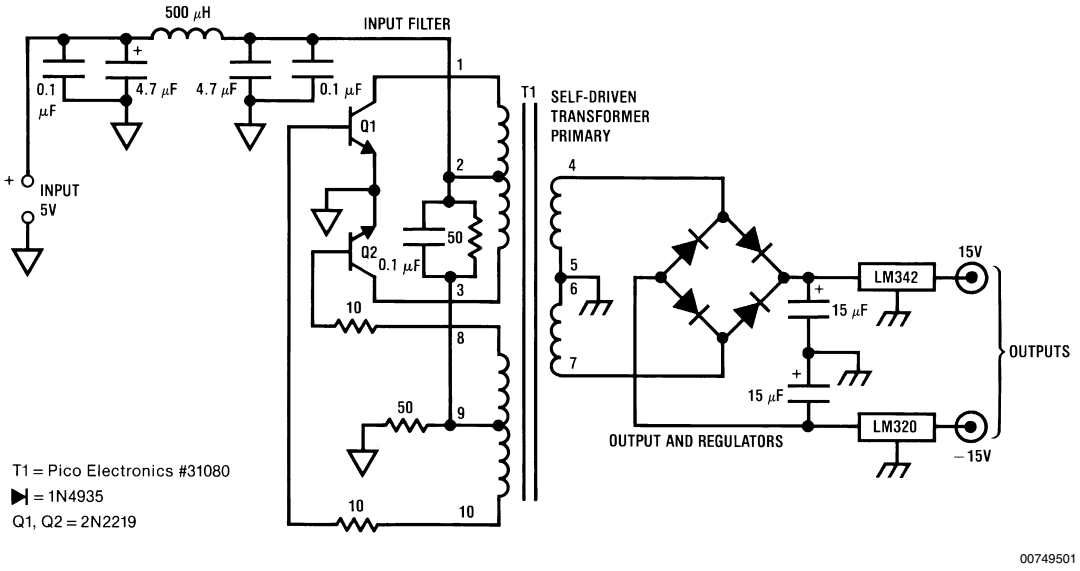


FIGURE 1.

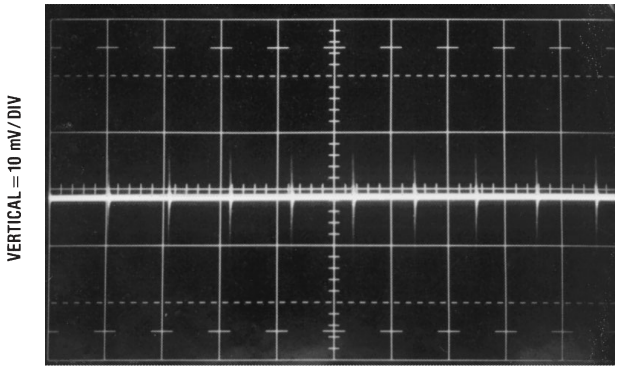


FIGURE 2.

Blank Pulse Converter

Figure 3 shows a converter which will supply 100 mA at ±15V from a 5V input. This design attacks the noise problem in two ways. The LM3524 switching regulator chip provides non-overlapping drive to the transistors, eliminating simultaneous conduction which helps keep input current spiking down. The LM3524 operates open loop. Its feedback connection (pin 9) is tied high, forcing the chip's outputs to full duty cycle. Internal logic in the LM3524 prevents the transistors from conducting at the same time. The components at pins 6 and 7 set the switching frequency. The LM3524's timing ramp biases the LM311 comparator to generate a blank pulse which "brackets" the output noise pulse. *Figure 4* shows the switching transistor waveforms (trace A and B) and the blank pulse (trace C) which is issued at each switching transition. The converter's output noise is shown in trace D. The blank pulse is used to alert the system that a noise spike is imminent. In this fashion, a critical A/D conversion or sample-hold operation can be delayed until the converter's noise spike has settled. This technique is quite effective, because it does not allow the system to "see" noise spikes during critical periods. This not only insures good system performance, but also means that a relatively simplistic converter design can be employed. The expense associated with low output noise (e.g., shielding, special filtering, etc.) can be eliminated in many cases. *Figure 5* details a converter design which uses a different approach to solving the same problem.

Blank Pulse Converter (Continued)

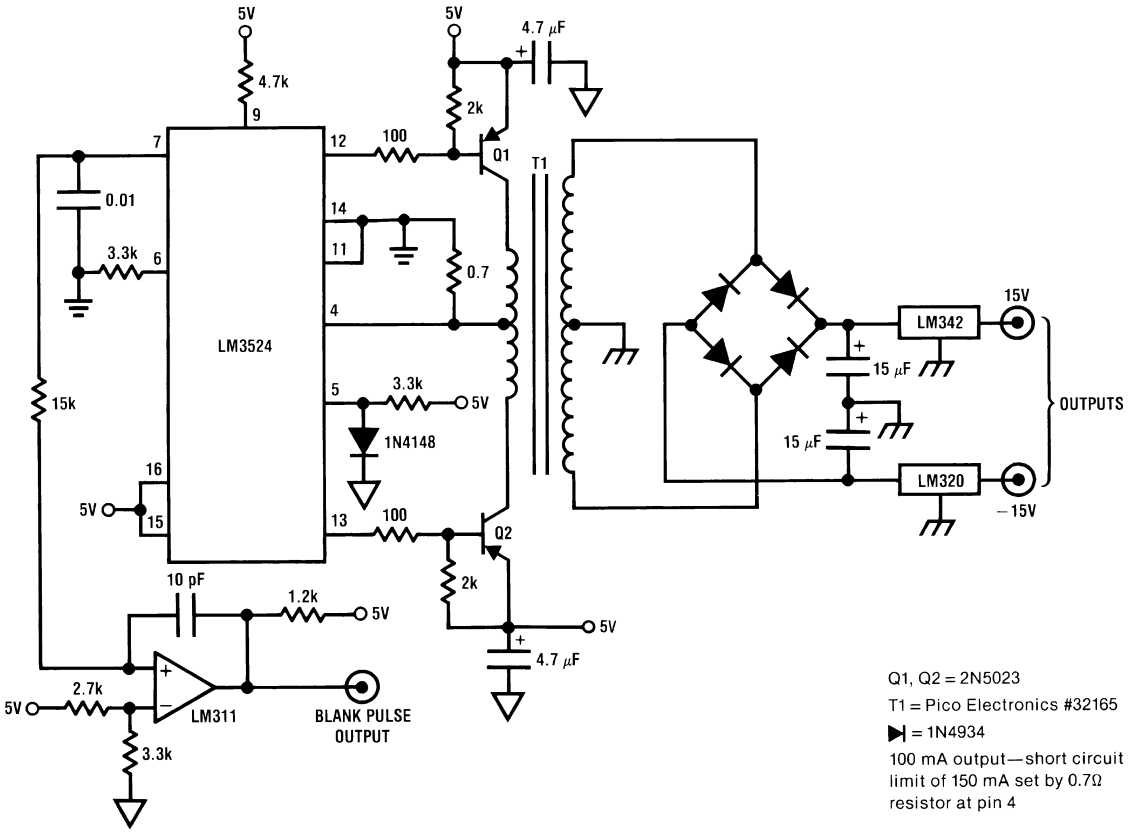


FIGURE 3.

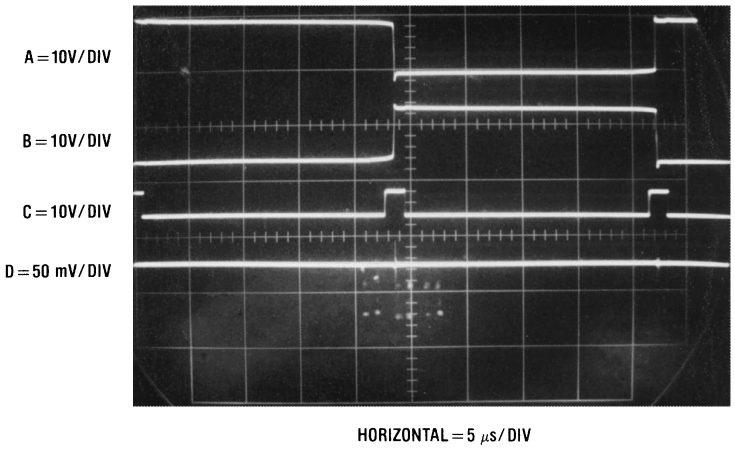


FIGURE 4.

Blank Pulse Converter (Continued)

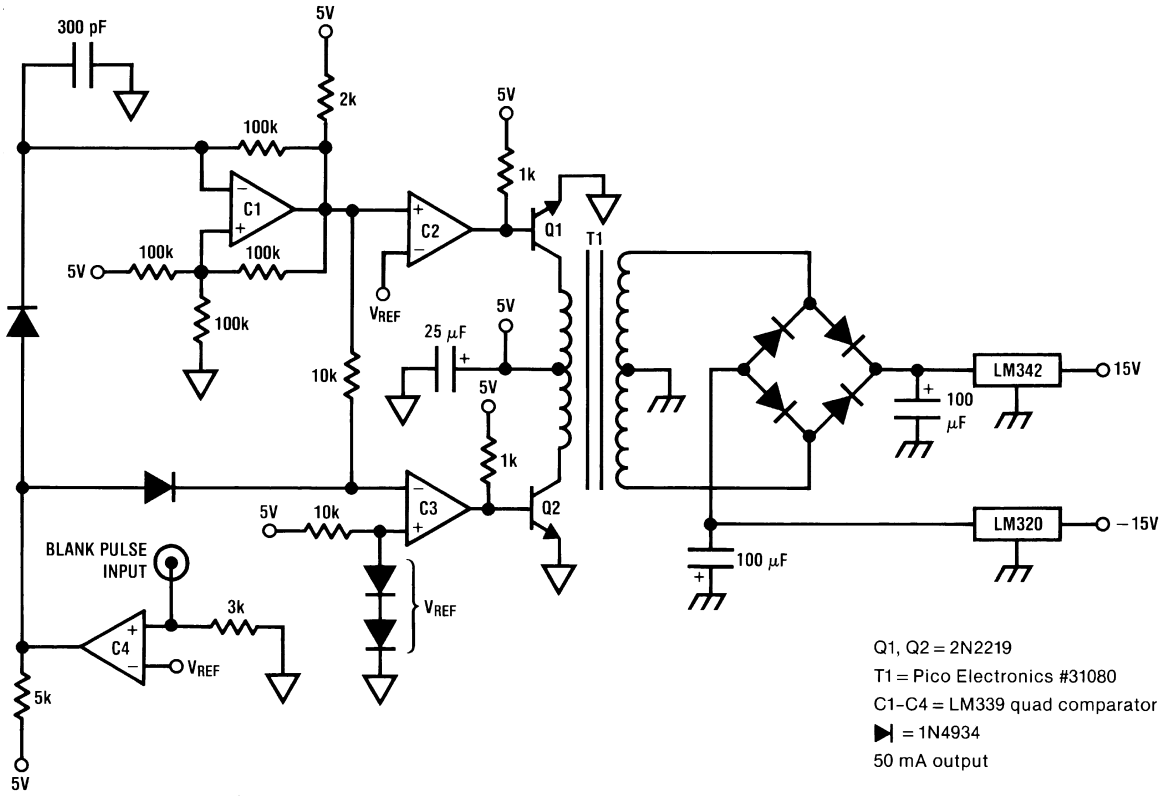


FIGURE 5.

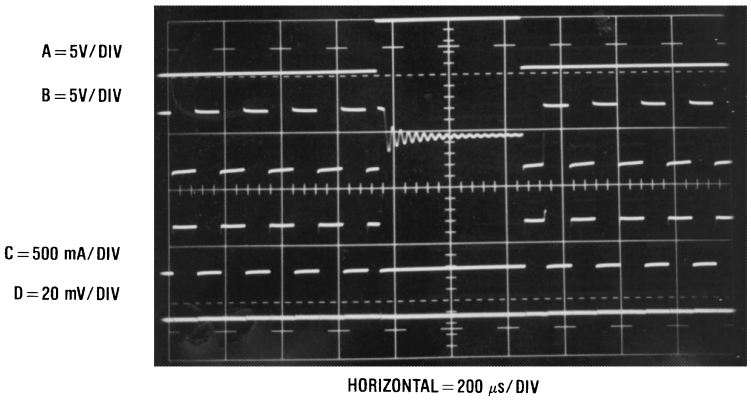


FIGURE 6.

Externally Strobed Converter

In *Figure 5* the system controls the converter, instead of the converter issuing blank commands. This arrangement uses an LM339 quad comparator to provide the necessary drive to the converter. C1 functions as a clock which provides drive to C2 and C3. These comparators drive the transistors (trace B, *Figure 6* is Q1's collector voltage waveform, while trace C details its current) to provide power to the transformer. When a critical system operation must occur, an external blank pulse (trace A) is applied to C4. C4's output goes high, shutting off all transformer drive. Under these conditions, the transformer current ceases (note voltage ringing on turn-off in trace B) and output noise (trace D) virtually disappears because the output regulators are powered only by the 100 µF filter capacitors. The value of these capacitors will depend directly on the output load and the length of the blank pulse. If synchronization to the system is desired, a system-derived 20 kHz square wave may be

Externally Strobed Converter

(Continued)

applied at C1's negative input through 2k, after removing the 300 pF capacitor and the 100k feedback resistor. The low noise during the blank pulse period affords ideal conditions for sensitive system operations. Although this approach allows great flexibility, the amount of off time is limited by the storage capacity of the output filter capacitors. In most systems this is not a problem, but some cases may require a converter which supplies low noise outputs at 100% duty cycles.

Sine Wave Driven Converter

Figure 7 diagrams a converter which sacrifices the efficient saturated-switch mode of operation to achieve an inherently low noise output at a 100% duty cycle. In this converter, sine wave drive is used to power the transformer. Q1 functions as a 20 kHz phase shift oscillator with Q2 providing an emitter-followed output. A1 and A2 are used to drive the transformer in complementary-bridge fashion (traces A and B, *Figure 8*). The high current output capability of the amplifiers, in combination with the transformer's paralleled primaries, results in a high power transformer drive. The transformer output is rectified, filtered and regulated in the usual fashion. Because the sine wave drive contains little harmonic content and current spiking, output noise is well below 1 mV (trace C, *Figure 8*). To adjust this circuit, ground the wiper arm of the 1k potentiometer and adjust the 100k value for minimum power supply drain. Next, unground the 1k potentiometer wiper arm and adjust it so that both A1 and A2's outputs are as large as possible without clipping. This circuit yields a low noise output on a 100% available basis but efficiency degrades to about 30%. In relatively low power converters such as this one (e.g., 50 mA output current) this is often acceptable.

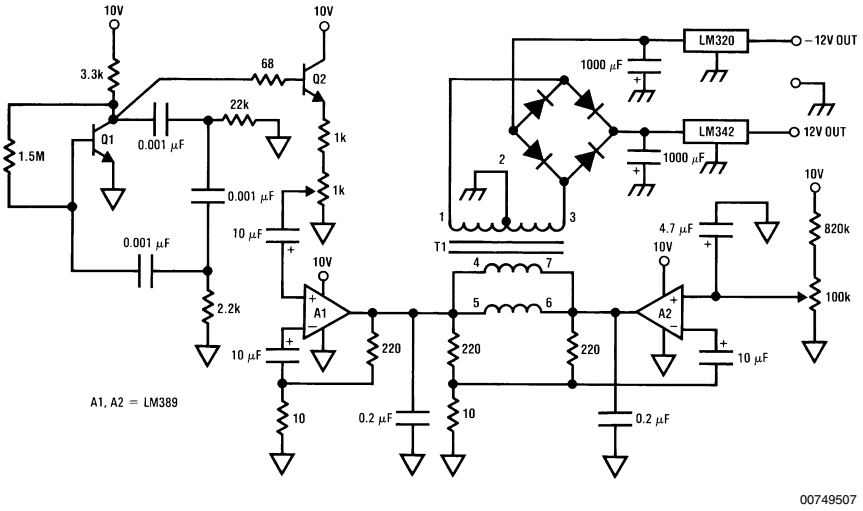


FIGURE 7.

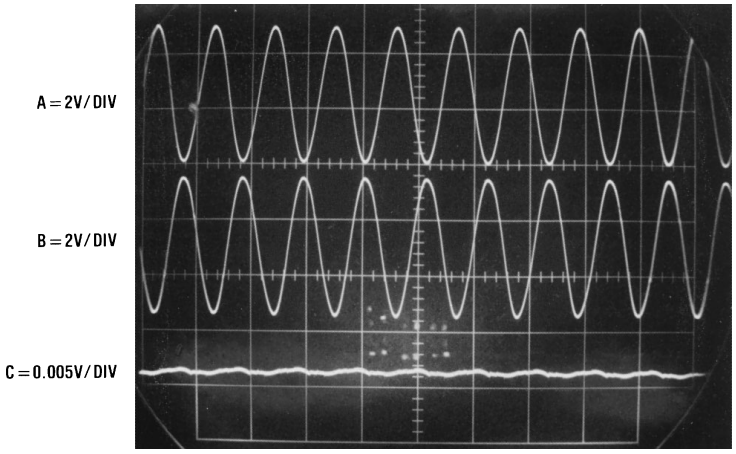


FIGURE 8.

Low Power Converter

Figure 9 shows a converter which operates from very low power. This circuit will provide 7.5V output from a 1.5V D cell battery. With a 125 µA load current (typically 20 CMOS ICs) it will run for 3 months. It may be externally strobed off during periods where lowest output noise is desired and it also issues a "converter running" pulse. This circuit is unusual in that the amount of time required for Q1 and Q2 to drive the transformer is directly related to the load resistance. The converter's output voltage is sensed by an LM10 op amp reference IC, which compares the converter output to its own internal 200 mV reference via the 5.1M-160k voltage divider. Whenever the converter output is below 7.5V, the LM10 output goes high, driving the Q1-Q2 pair and the transformer which form an oscillator. The transformer output is rectified and used to charge the 47 µF capacitor. When the capacitor charges to a high enough value, the LM10 output goes low and oscillation ceases. Trace A, *Figure 10* shows the collector of Q1, while trace B shows the output voltage across the 47 µF capacitor (AC coupled). It can be seen that each time the output voltage falls a bit the LM10 drives the oscillator, forcing the voltage to rise until it is high enough to switch the LM10 output to its low stage. The frequency of this regulating action is determined by the load on the converter output. To prevent the converter from oscillating about the trip point, the 0.1 µF unit is used to provide hysteresis of response. Very low loading of the converter will result in almost no on time for the oscillator while large loads will force it to run almost constantly. Loop operating frequencies of 0.1 Hz to 40 Hz are typical. The LM10 output state may be used to alert the system that the converter is running. A pulse applied to the LM10 negative input will override normal converter operation for low noise operation during a critical system A/D conversion.

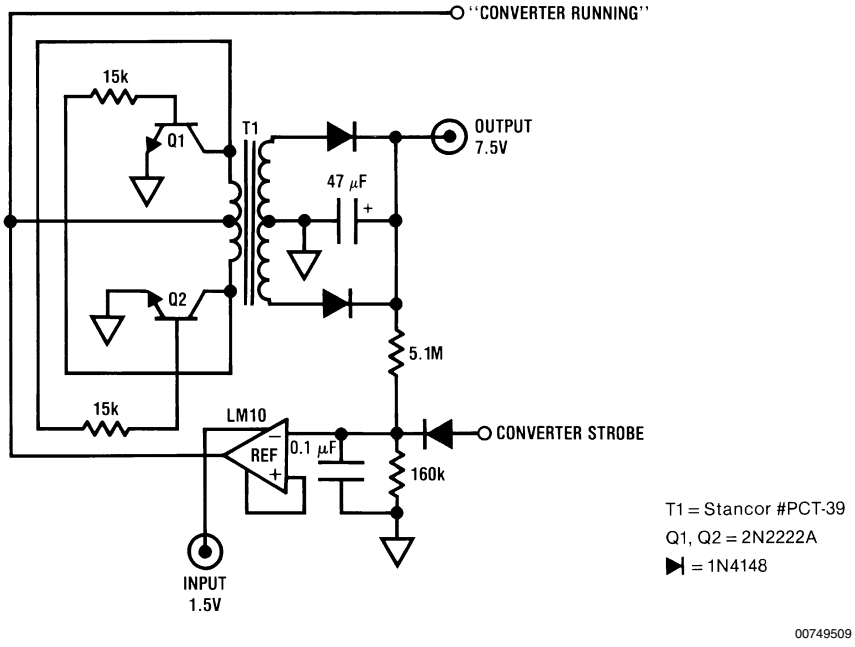


FIGURE 9.

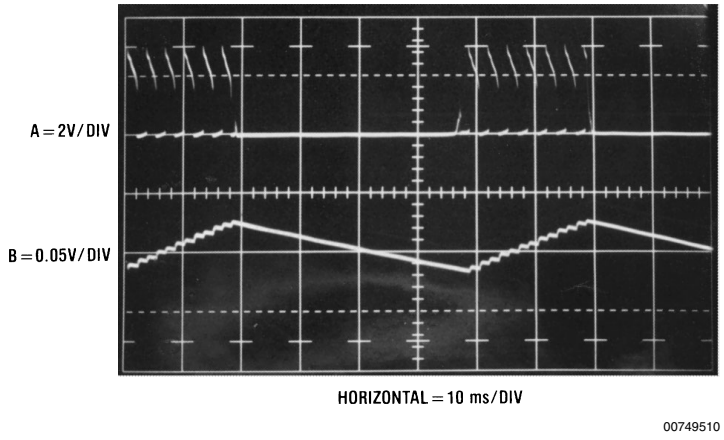


FIGURE 10.

Circuit Applications Of Analog Data Multiplexers

National Semiconductor
Application Note 289

Although designers are familiar with analog multiplexers in data acquisition systems, relatively little use is made of these devices in circuit-oriented applications. This is unfortunate, because IC analog multiplexers combine features which allow a variety of circuit functions to be implemented. The combination of multi-contact analog commutation, differential or single-ended switching and fully decoded logic addressing achieves complex circuit functions with surprising ease. The position servo of *Figure 1* furnishes an excellent example.

POSITION SERVO

The circuit of *Figure 1* uses an LF11508 multiplexer in a position servo scheme. In this arrangement the motor shaft may be programmed to stop at 8 discrete positions. Each position is fully programmable and any shaft position may be accessed in any sequence. Assume power has just been applied and the output of the 74C90 counter is "0000". This condition forces the LF11508 to close the switch associated with Pot #1's ("P1") wiper arm. The difference between P1's wiper potential and the 5k "pick-off" servo potentiometer is amplified by A2. The A1 followers unload the potentiometer outputs. A2's output is compared by the remaining A1 amplifiers, which are configured as a dual-limit comparator with deadband. Depending upon the polarity of A2's output, the appropriate comparator saturates high, turning on its associated driver transistor. This drives the motor in the necessary direction to force a mull at A2's output. When the null falls within the diode-generated .6-volt deadband, both comparator outputs will be low and the motor will stop.

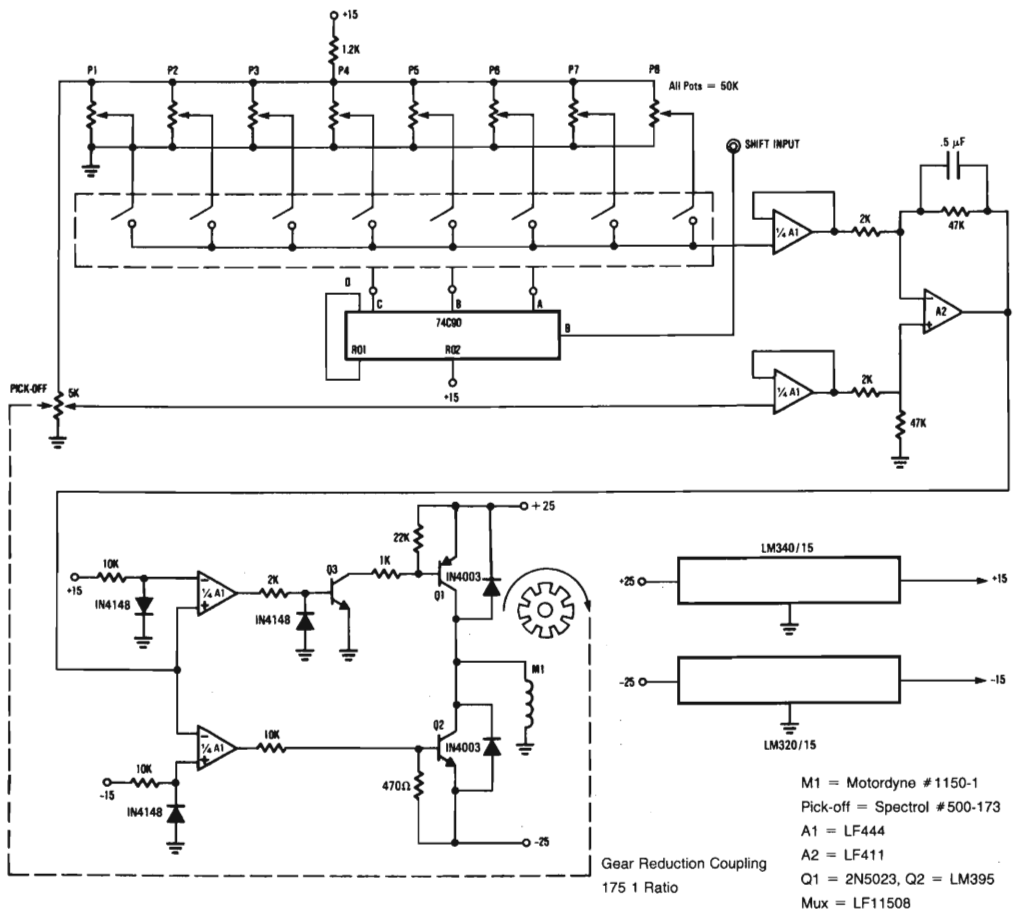
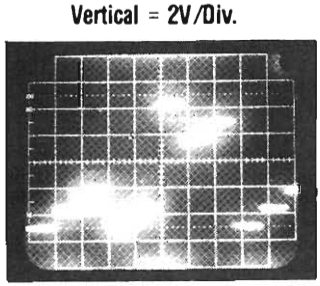


FIGURE 1



TL/H/5635–2

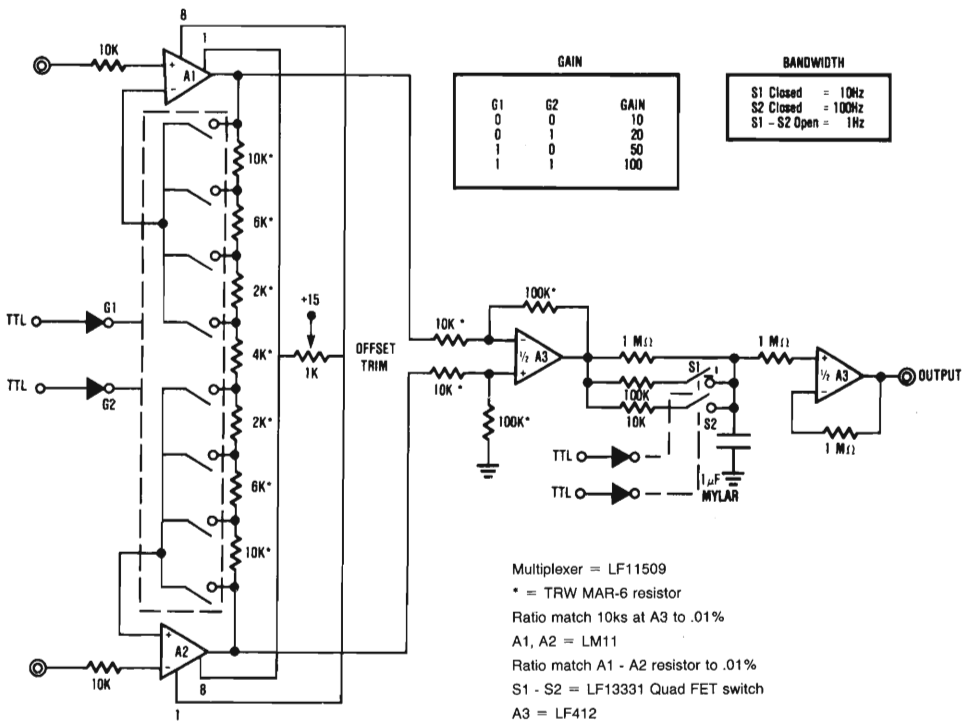
FIGURE 2

A2, operating at a gain of 30, provides adequate gain for precise positioning while the ±25-volt supplies and the motor-gearbox combination achieve good speed. The .5μf capacitor at A2 sets the loop roll-off.

Each time a pulse is applied to the "shift input," the multiplexer advances to the next position, closing the appropriate switch and forcing the servo to seek the position dictated by the potentiometer output. Because all potentiometers may be set to any potential, any desired positioning pattern may be obtained. *Figure 2*, a stored trace display of the multiplexer output bus, shows the servo at work. The photo shows that eight discrete positions are selected in a dispersed, non-montonic fashion. Any desired positioning sequence can be obtained by appropriate setting of the potentiometers. This circuit requires no voltage reference because the pick-off and position setting potentiometers are driven from the same source. In addition, because the shaft position program is "stored" in the potentiometer settings, the circuit requires no power-up initialization or sequencing.

TTL PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

Figure 3 depicts an instrumentation-type amplifier. The gain and frequency response may be programmed via TTL inputs. In this circuit, an LF11509 differentially-switched multiplexer is used to select the feedback resistors for A1 and A2. One-half of A3 is used to single-end the differential outputs of A1 and A2 at a gain of ten. A low-pass filter is formed by whatever resistor is connected to the 1μf capacitor via the LF13331 analog switches. This filter's output is buffered by the other half of A3 and presented as the circuit's output. The LM11s in the front end give this circuit 2μV/°C drift performance while CMRR of 100dB is obtainable with good resistor matching. Gain and bandwidth programming data are summarized in the tables shown in *Figure 3*.



TL/H/5635–3

FIGURE 3

PROGRAMMABLE SAMPLE-HOLD AMPLIFIER

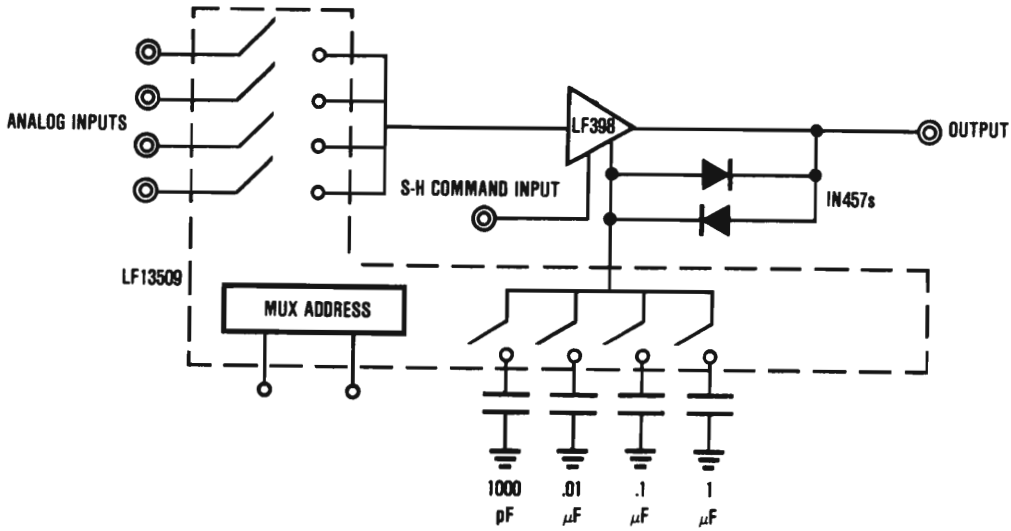
A differential input multiplexer is used to program the acquisition time and droop-rate characteristics of a sample-hold amplifier in *Figure 4*. In this circuit, one-half of the differential input LF13509 multiplexes four inputs to the LF398 sample-hold amplifier. The other half of the multiplexer is used to select the "hold-capacitor." Because one address code simultaneously switches both multiplexer halves, any desired hold-capacitor value can be used for any input combination. The attendant droop-rate acquisition-time performance range (see table in *Figure 4*) allows a very wide range of input signals to be handled.

SINGLE-PULSE SAMPLER

Figure 5 shows a circuit which captures a low repetition rate or single-shot waveform and presents it as a repetitive display on an oscilliscope. The display rate may be set to any desired value. Circuit operation is triggered by the event of interest. When the monitored event occurs (trace A, *Figure 6*), A1, an LM311 comparator, triggers low (trace B, *Figure 6*). This allows the 15k-1200pF RC combination at A2 to charge (waveform C, *Figure 6*), and A2's output is a pulse train (waveform D, *Figure 6*). Each pulse out of A2 is used to advance the 74C90 counter by one step. The 74C90's BCD output is fed to the 74C42, which decodes it into 8 discrete sequential outputs. These outputs are used once to trigger individual LF398 sample-hold amplifiers. In this manner, each individual sample-hold amplifier acquires a fraction of the waveform of interest. When the input waveform ceases, A1's output returns high, A2 stops emitting pulses and no further circuit action occurs. At this time, the 8 sample-hold amplifiers contain all the amplitude information necessary to reconstruct the original input waveform. This is accomplished by driving the clock input with a pulse train which is counted and presented to the LF11508 multiplexer address inputs by another 74C90. The multiplexer output bus is followed by A3, providing the circuit's output. As the multiplexer steps through its 8 states, the sampled and reconstructed version of the input waveform appears in a steady, repetitive display (trace E, Figure 6). The clock frequency may be varied to allow any desired oscilliscope sweep speed to be used.

AUTOMATIC, SELF-CALIBRATING STRAIN GAUGE READOUT

Figure 7 uses an LF13509 differential multiplexer in an autocalibration arrangement, which eliminates almost all errors in a strain gauge load cell transducer measurement. Errors due to drift with time and temperature are cancelled and individual transducers may be interchanged with no manual gain or zero recalibration required. In this system, 4 discrete operations are performed in order to determine the corrected output of the load cell. The start of a measurement cycle is initiated by the microprocessor commanding the LF13509 differential input multiplexer to position 1. In this position, the strain gauge bridge output is connected to the LH0038 instrumentation amplifier.



TL/H/5635–4

CAPACITOR	ACQUISITION TIME TO .01%	DROP RATE (VOLTS/SECOND)
1000pF	10μs	30mV
.01μF	25μs	3mV
.1μF	300μs	300μV
1μF	3ms	30μV

FIGURE 4

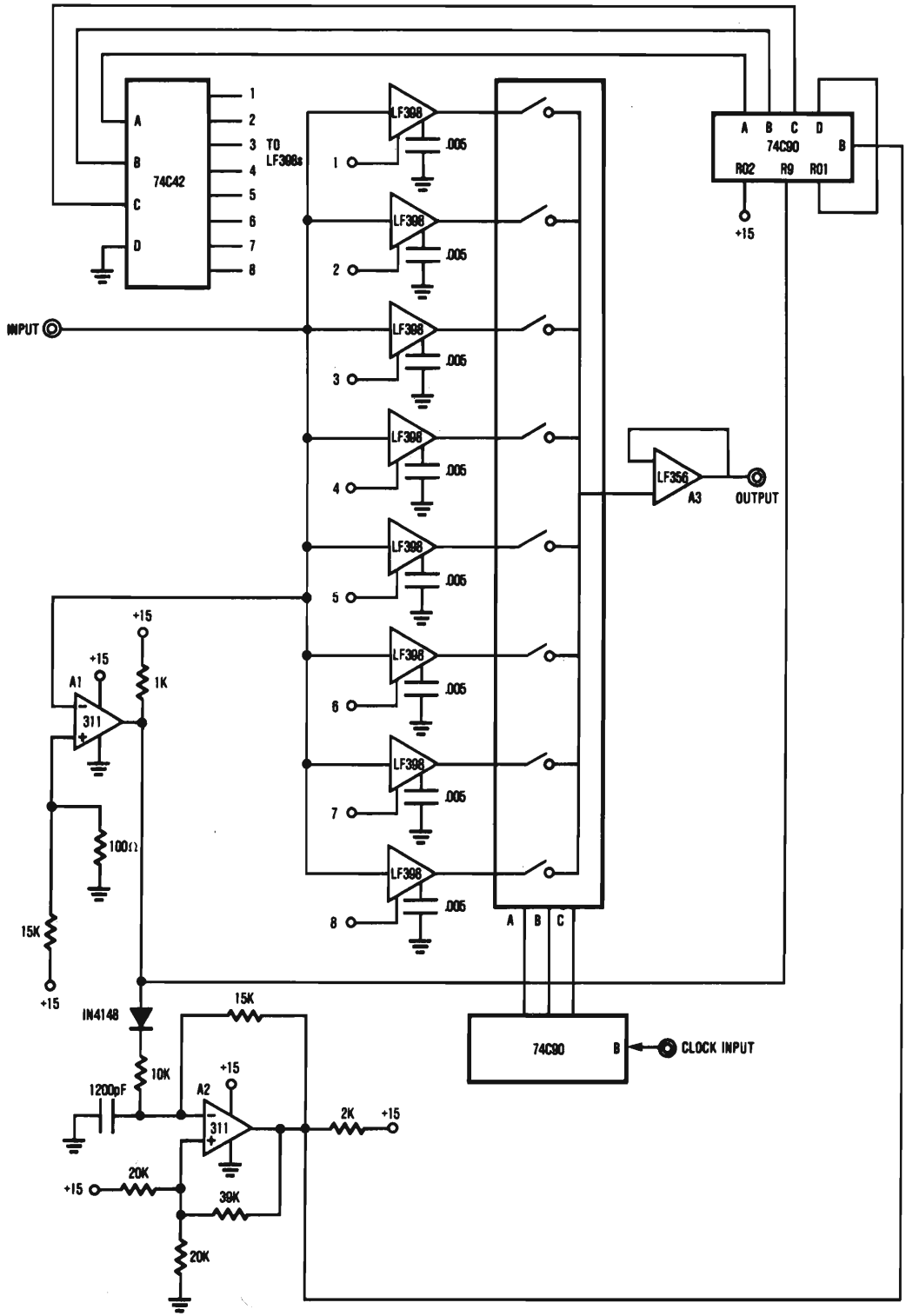
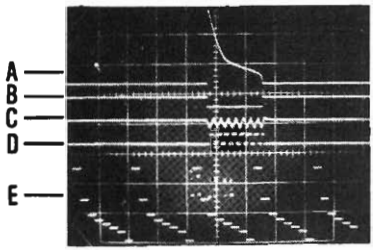


FIGURE 5

TL/H/5635–5

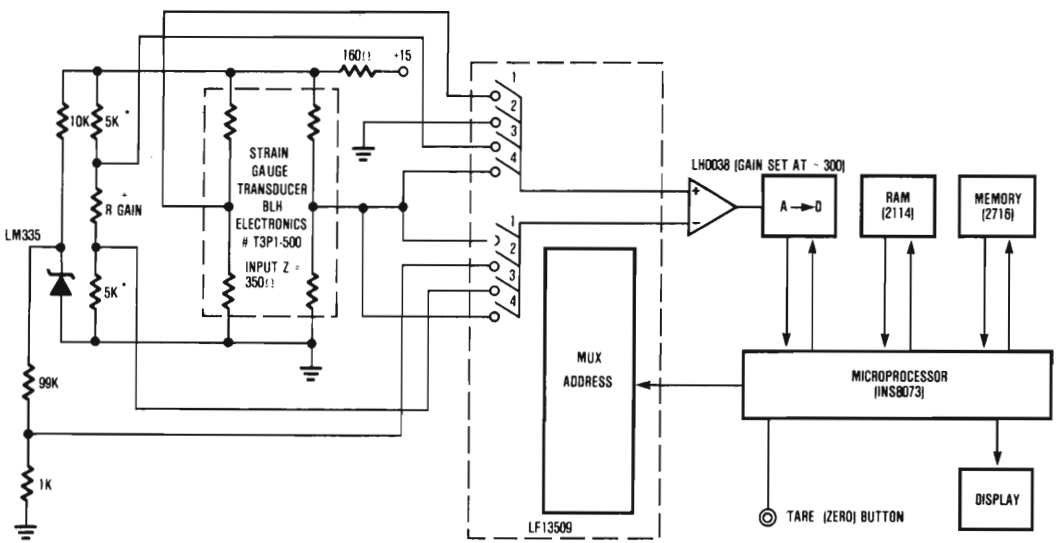


	VERTICAL	HORIZONTAL
A	2V	50 μs/DIV.
B	50V	50 μs/DIV.
C	10V	50 μs/DIV.
D	50V	50 μs/DIV.
E	2V	1 MILLISECOND/DIV.

TL/H/5635–6

FIGURE 6

This signal, which represents the transducer output, is amplified by the LH0038, converted by the A/D and stored in memory. The multiplexer is then switched to position 2. In this position, the output of the LM335 temperature sensor, which is located inside the load cell transducer, is determined and stored in memory. The relatively high-level LM335 output is resistively divided by 100 so the LH0038 does not saturate. When this measurement is completed, the multiplexer switches to position 3. In this position, the LH0038 inputs are connected across the middle resistor in a string of resistors. The voltage across this resistor represents the *precise* full-scale output voltage of the load cell transducer. This information allows the system to determine the gain slope of the transducer. In practice, the middle resistor in the string is physically located within the load cell connector. When any such equipped load cell is plugged into the system, the value of this resistor allows immediate and precise gain-slope compensation and eliminates the usual calibration requirements. The final position of the multiplexer connects the amplifier inputs to one side of the bridge. This determines the electrical zero in the system at the common mode output voltage of the stain gauge bridge.



TL/H/5635–7

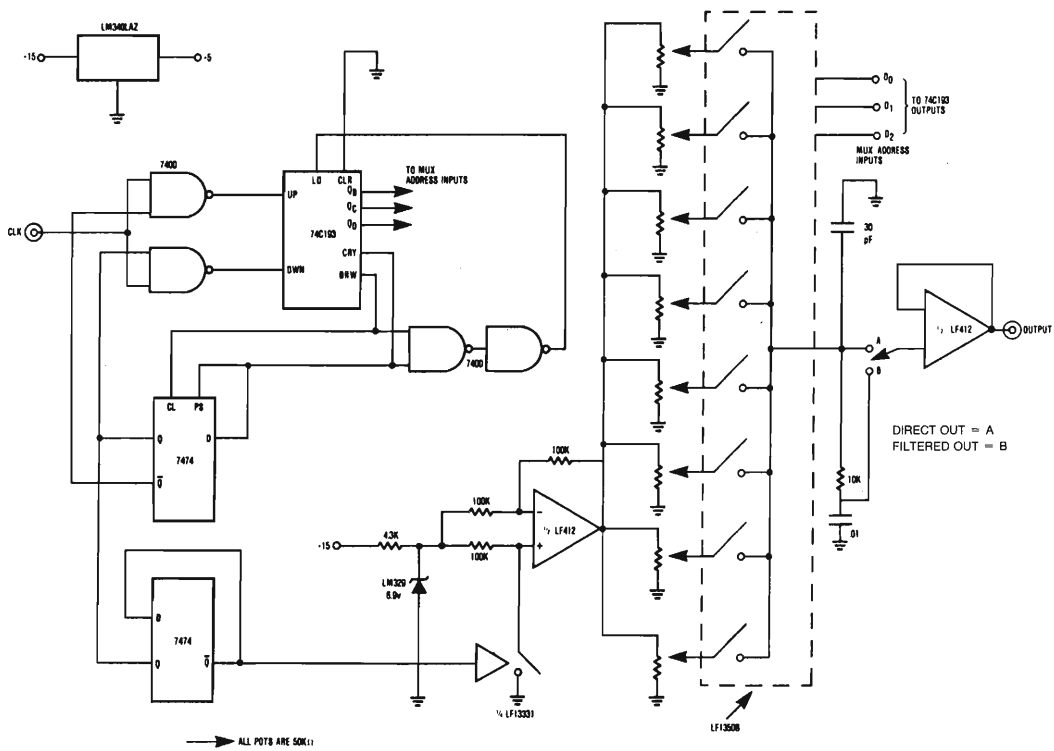
* = ULTRONIX 105A
.01%
\+ = SELECTED VALUE
TYPICAL 33.4Ω
ULTRONIX 105A

FIGURE 7

Physical zero information, e.g., "tare weight," is fed to the microprocessor via a push button which is depressed when no load is on the transducer. This operation need only be carried out when the system is first turned on. At this point, the microprocessor has values for zero, stain bridge output, precise full-scale output for the particular transducer in use, as well as transducer temperature and initial tare weight. Using this information, the microprocessor can determine the precise load on the transducer, regardless of drifts or initial individual transducer gain-slope tolerances. The temperature information provides a first-order correction for the relatively small effect of ambient temperature on gain slope and zero, while the gain resistor in the load cell allows complete interchangeability of load cells with no field calibration at all. The stability of this approach is entirely dependent on the resistors in the gain calibration string. The voltage drive to the bridge need not be stable, because it is common to the gain calibration string and ratio-metrically cancels. Multiplexer-fed systems of this type have achieved 1 part in 20,000 repeatability in industrial environments.

Programmable Waveform Generator

Figure 8 diagrams a way of using the 8-channel LF13331 multiplexer to generate a 32-piece approximation of a desired waveform. In this instance, a sinewave is used as an example. When pulses are applied to the clock input, the logic circuitry instructs the multiplexer to count up to 8 (74C193 count "up" and "down" inputs are traces A and B in *Figure 9*). When this operation is completed, the multiplexer is instructed to count down to zero. The logic then inverts the voltage supplied to the potentiometers at the multiplexer inputs. This is accomplished by grounding the positive input of the LF412 amplifier with LF13331 FET switch. This forces the LF412 output (trace C, *Figure 9*) to negative 6.9 volts. Concurrently, the logic instructs the multiplexer to count up to 8 and back down. At this point, the output of the LF412 is forced to positive 6.9 volts by turning off the LF13331, and the entire cycle repeats. If the potentiometers are set appropriately, a sinewave approximation of 32 steps results (trace D, *Figure 9*) at the circuit output. The filtered output of this waveform (trace E, *Figure 9*) contains less than .5% distortion (trace F, *Figure 9*). If the potentiometer outputs are deliberately mis-set, any form of sinewave distortion may be intentionally generated by lab work or listening tests, *Figure 10* shows the circuit output (trace A) under these conditions. Trace B, the filtered, output, is a good approximation of severe harmonic distortion. Trace C, the output of a distortion analyzer, indicates almost 7% distortion. The type and level of distortion, e.g., clipping, crossover, etc., may be programmed by adjusting the potentiometers.



TL/H/5635–8

FIGURE 8

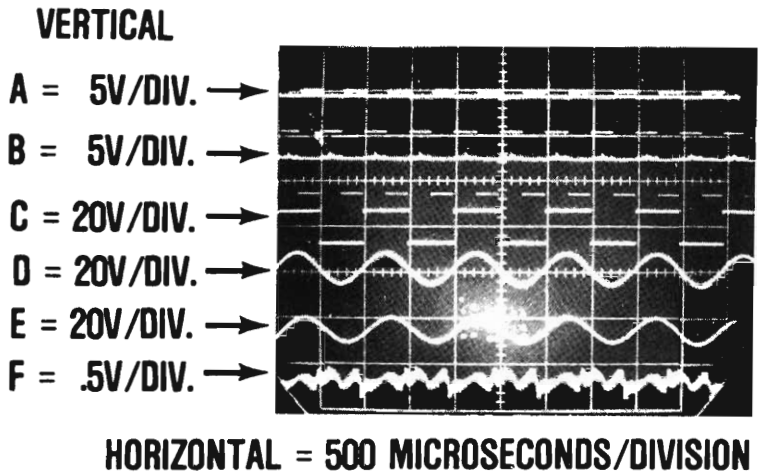


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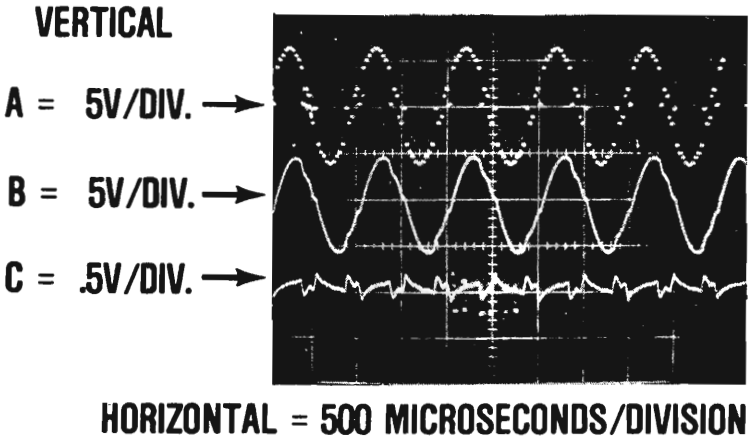
FIGURE 9



TL/H/5635–10

FIGURE 10

Applications of the LM3524 Pulse-Width-Modulator

National Semiconductor
Application Note 292
April 1998

The LM3524 Regulating Pulse-Width-Modulator is commonly used as the control element in switching regulator power supplies. This is in keeping with its intended purpose. Engineers closely associate this part with switching power supplies. Nevertheless, the flexible combination of elements (see box) within the LM3524 also allows it to be used in a number of other applications outside the power supply area. Because the device is inexpensive and operates off a single-sided supply, it can considerably reduce component count and circuit complexity in almost any application. The constant light intensity servo of *Figure 1* furnishes a good example.

Constant Light Intensity Servo

The circuit of *Figure 1* uses a photodiode's output to control the intensity of a small light bulb. The constant intensity output of the light bulb is useful in a number of areas, including opto-electronic component evaluation and quality control of photographic film during manufacture. In this circuit, the photodiode pulls a current out of the LF356 summing junction, which is directly related to the amount of light that falls on the photodiode's surface. The LF356 output swings positive to maintain the summing junction at zero and represents the photodiode current in amplified voltage form. This potential is compared at the LM3524 to the voltage coming from the 2.5k "intensity" potentiometer wiper. A stable voltage for the "intensity" control is taken from the LM3524's internal five-volt regulator. The difference between the LF356 output and the "intensity" potentiometer output is amplified at a gain of about 70 dB, which is set by the 1 MΩ value at pin 9. The LM3524 output transistors are paralleled and provide drive to the 2N2219 switch transistor. The 5.6k and .01 µF values set the switching frequency at about 30 kHz. Because the LM3524 forms a switched mode feedback loop around the light bulb and photodiode, the average power delivered to the light bulb will be controlled by the photodiode output, which is directly proportional to the lamp's output. Frequency compensation for this feedback loop is provided by the .001 µF capacitor, which rolls off the loop gain at a 1 ms time constant. *Figure 2* shows the wave forms in the circuit. Trace A is the 2N2219 collector and trace B is the AC-coupled LF356 output. Each time the 2N2219 collector goes low, power is driven into the lamp. This is reflected in the positive going ramp at the LF356's output. When the 2N2219 goes off, the lamp cools. This is shown in the negative going relatively slow ramp in trace B. It is interesting to note that this indicates the bulb is willing to accept energy more quickly than it will give it up. *Figure 3* elaborates on this. Here, trace A is the output of a pulse generator applied to the "step test" input and trace B is the AC-coupled LF356 output. When the pulse generator is high, the diode blocks its output, but when it goes low, current is drawn away from the "intensity" control wiper through the 22k resistor. This forces the servo to control bulb intensity at a lower value. This photo shows that the bulb servos to a higher output almost three times as fast as it takes to go to the lower output state, because the bulb more readily accepts energy than it gives it up. Surprisingly, at high intensity levels, the situation reverses because the increased incandescent state of the bulb makes it a relatively efficient radiator (*Figure 4*).

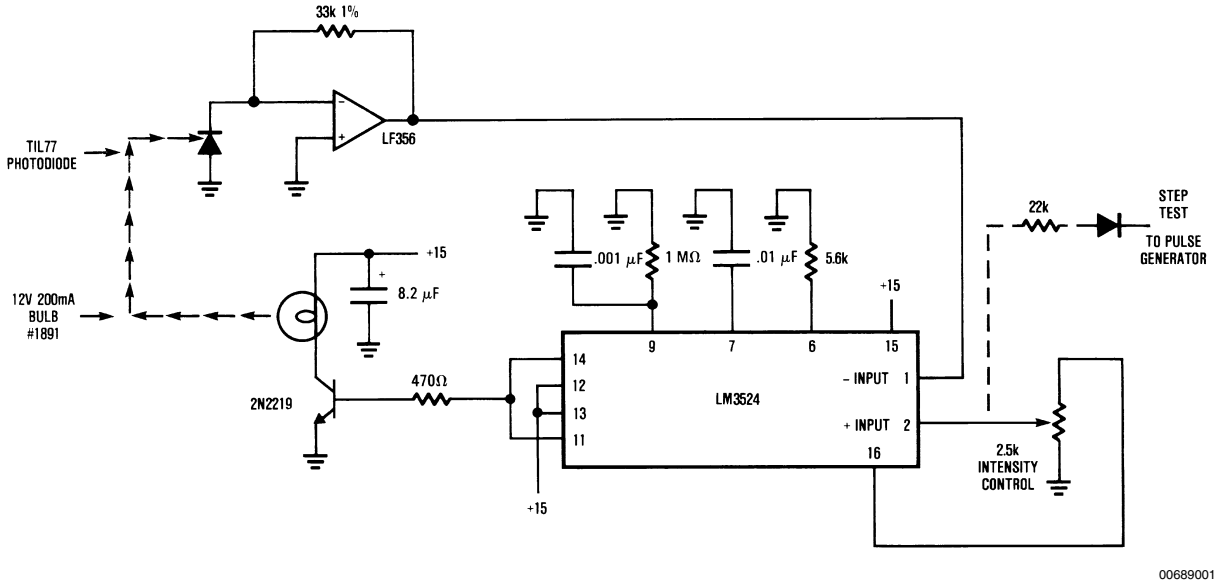
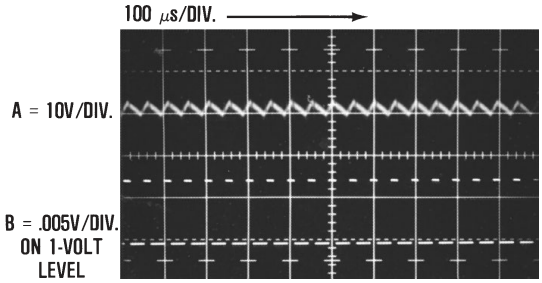


FIGURE 1.

Temperature-to-Pulse-Width Converter

The circuit in *Figure 5* uses the LM3524 to convert the output of an LM135 temperature transducer into a pulse width which can be measured by a digital system, such as a microprocessor-controlled data acquisition system. Although this example uses the temperature transducer as the input, the circuit will convert any 0.1 to 5V input applied to the 100 kΩ resistor into a 0–500 ms output pulse width with 0.1% linearity. In this circuit, the LM135's temperature-dependent output (10 mV/°K) is divided down and applied to A1's positive input. This moves A1's output high, driving the input to the LM3524's pulse-width modulation circuitry. The LM3524 pulse-width output is clipped by the LM185 reference and integrated by the 1 MΩ-0.1 µF combination. The DC level across the 0.1 µF capacitor is fed back to A1's negative input. This feedback path forces the LM3524's output pulse width to vary in a highly linear fashion according to the potential at A1's positive input. The overall temperature-to-pulse width scale factor is adjusted with the "gain trim" potentiometer. The 1000 pF capacitor provides stable loop compensation. A1, an LM358, allows voltages very close to ground to be sensed. This provides greater input range than the LM3524's input amplifier, which has a common mode range of 1.8–3.4V. The oscillator output pulse at pin 3 may be used to reset counters or other digital circuitry because it occurs just before the output pulse width begins.



00689002

FIGURE 2.

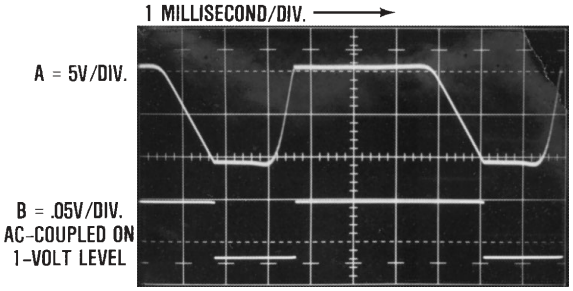


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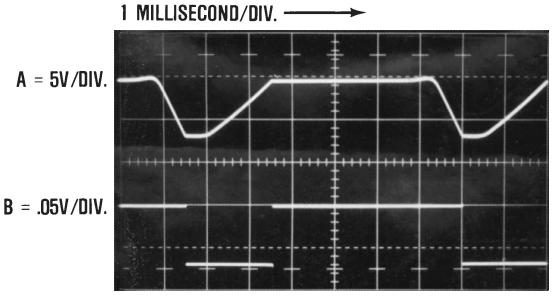
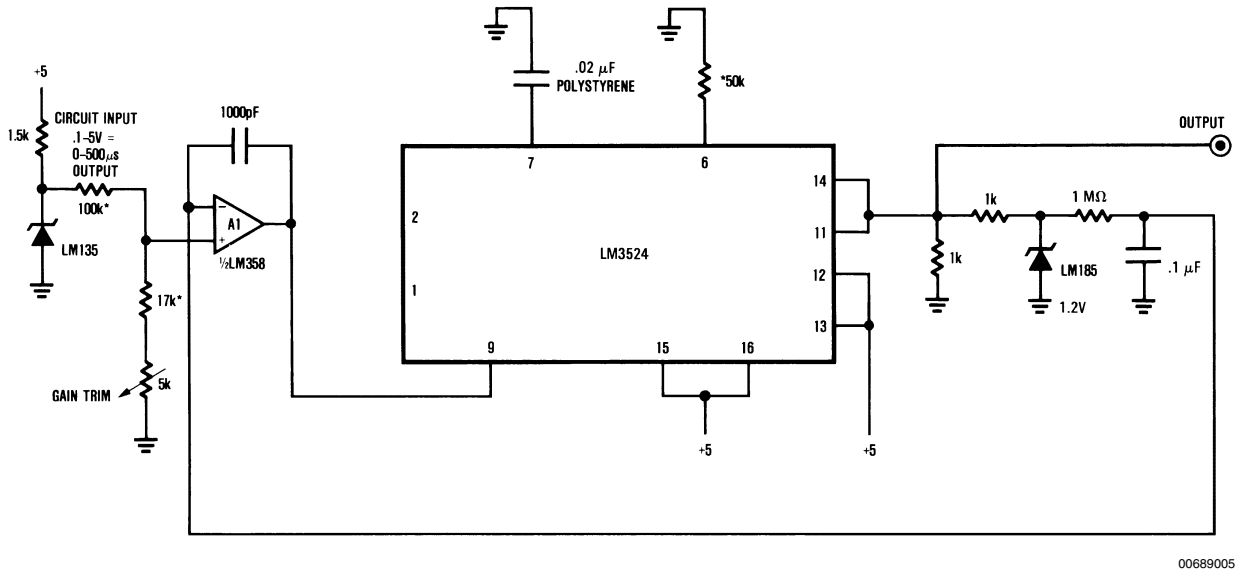
FIGURE 3.



00689004

FIGURE 4.

Temperature-to-Pulse-Width Converter (Continued)



*Metal Film Resistor

FIGURE 5.

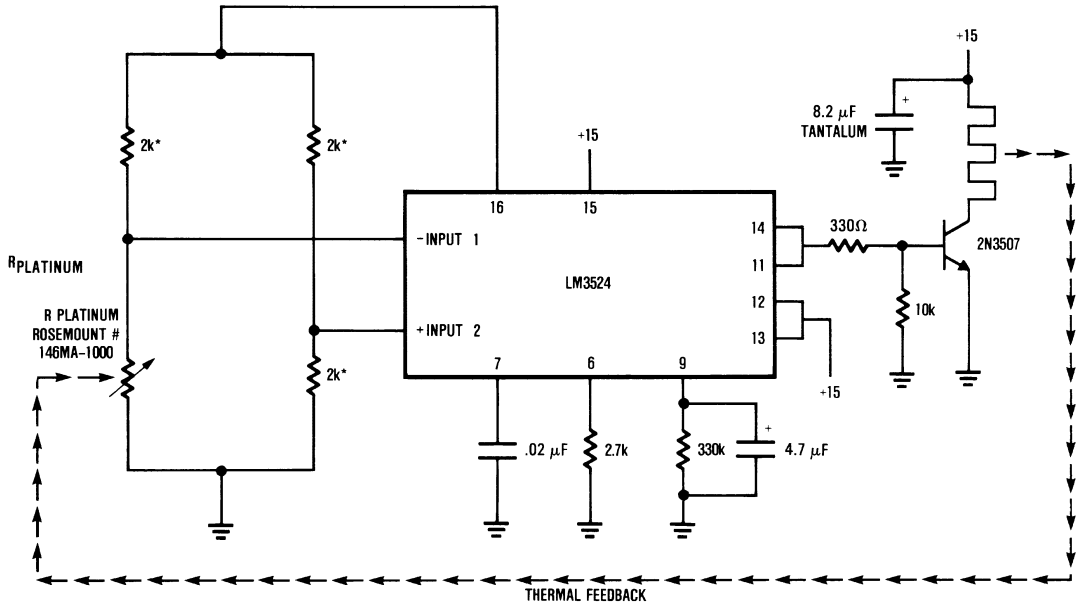
RTD Temperature Controller

Figure 6 is another temperature circuit which uses the LM3524 to control the temperature of a small oven. Here, a platinum RTD is used as a sensor in a bridge circuit made up of the 2 kΩ resistors. When power is applied, the positive temperature coefficient platinum sensor is at a low value and the LM3524's positive input is at a higher potential than its negative input. This forces the output to go high, turning on the 2N3507 and driving the heater. When the servo point is reached, the duty cycle of the heater is reduced from 90% (full on) to whatever value is required to keep the oven at temperature. The 330k-4.7 μF combination at the internal input amplifier's output sets the servo gain at about 55 dB at 1 Hz, more than adequate for most thermal-control applications. The 0.02 μF-2.7k combination sets the pulse frequency at about 15 kHz, far above the 1 Hz pole of the servo gain. If the sensor is maintained in close thermal contact with the heater, this circuit will easily control to .1˚C stability over widely varying ambients.

"SENSORLESS" Motor Speed Control

Figure 7 shows the LM3524 in an arrangement which controls the speed of a motor without requiring the usual tachometer or other speed pick-off. This circuit uses the back EMF of the motor to bias a feedback loop, which controls motor speed. When power is applied, the positive input of the LM3524 is at a higher potential than the negative input. Under these conditions, the output of the LM3524 is biased full on (90% duty cycle). The output transistors, paralleled in the common emitter configuration, drive the 2N5023 and the motor turns. (LM3524 output is waveform A, *Figure 8*; waveform B is the 2N5023 collector.) The LM3524 output pulse is also used to drive a 1000 pF-500 kΩ differentiator network whose output is compared to the LM3524's internal 5V reference. The result is a delayed pulse (*Figure 8*, waveform D), which is used to trigger an LF398 sample-hold IC. As the waveforms show, the sample-hold is gated high (ON) just as the 2N5023 collector stops supplying current to the motor. At this instant, the motor coils produce a flyback pulse, which is damped by the shunt diode. (Motor waveform is *Figure 8*, trace C). After the flyback pulse decays, the back EMF of the motor remains. This voltage is "remembered" by the sample-hold IC when the sample trigger pulse ceases and is used to complete the speed control loop back at the LM3524 input. The 10k-4k divider at the motor output insures the LF398's output will always be within the common range of the LM3524's input. The 10k-1 μF combination provides filtering during the time the LF398 is sampling. The diode associated with this time constant prevents any possible LF398 negative output from damaging the LM3524. The 10 MΩ resistor paralleling the 0.01 μF sampling capacitor prevents the servo from "hanging up" if this capacitor somehow manages to charge above the motor's back EMF value. The 39k-100 μF pair sets the loop frequency response. The maximum pulse-width-modulator duty cycle is clamped by the 2k-2k divider and diode at 80%, thus avoiding overshoot and aiding transient response at turn-on and during large positive step changes. The 60k-0.1 μF values at pins 6 and 7 set the pulse modulation frequency at 300 Hz.

"SENSORLESS" Motor Speed Control (Continued)



00689006

*TRW Type MAR-60 .1%

FIGURE 6.

"SENSORLESS" Motor Speed Control (Continued)

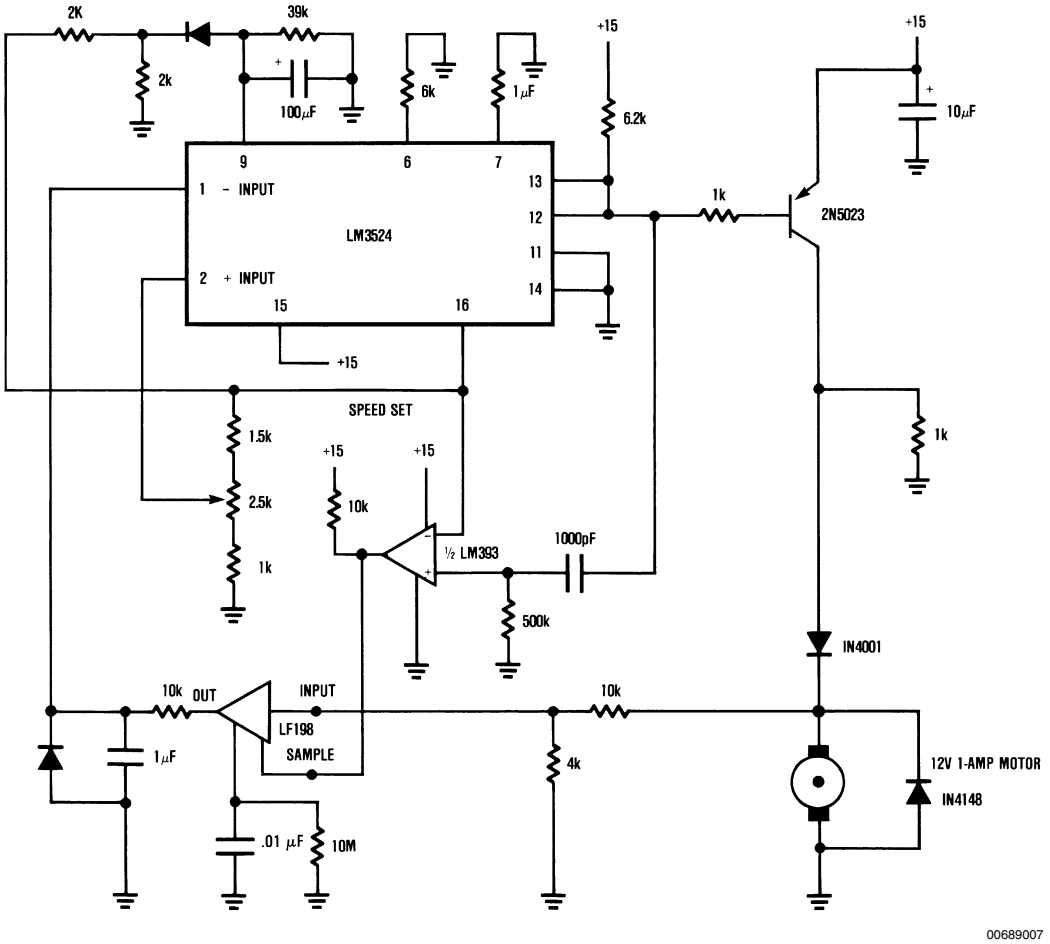


FIGURE 7.

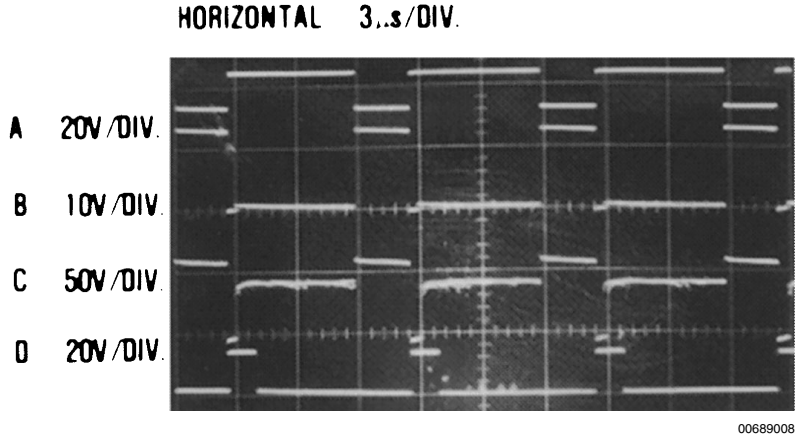
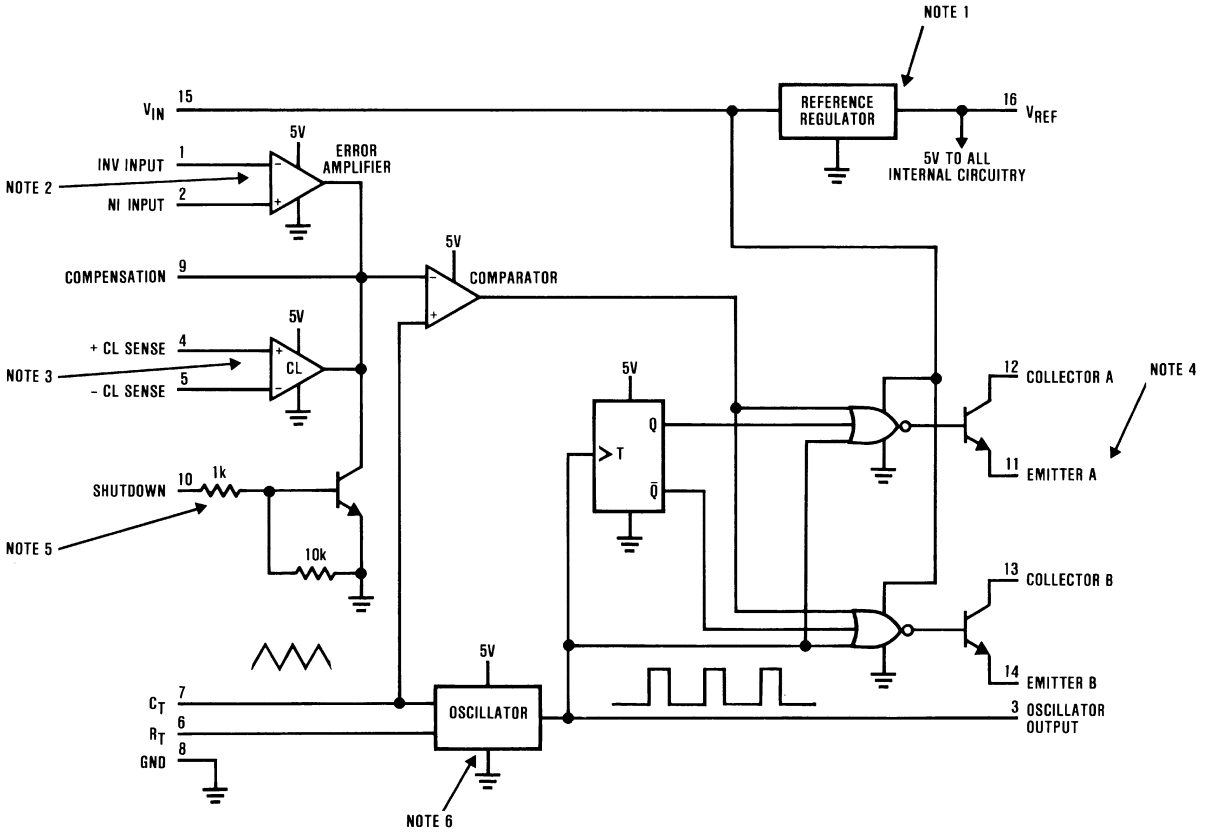


FIGURE 8.

"SENSORLESS" Motor Speed Control (Continued)

The LM3524 at a Glance



00689009

Note 1: 5V 50 mA regulator available to user.

Note 2: Transconductance diff. input amplifier. Gains from 40–80 dB available by resistor loading of output. 1.8–3.4V common mode input range.

Note 3: Over current sense comparator −0.7 to 1V common mode input range.

Note 4: Output transistors switch out of phase and may be paralleled. Up to 100 mA maximum output current.

Note 5: Transistor may be used to strobe LM3524 into an off state at its outputs.

Note 6: Oscillator typically frequency programmable for up to 100 kHz.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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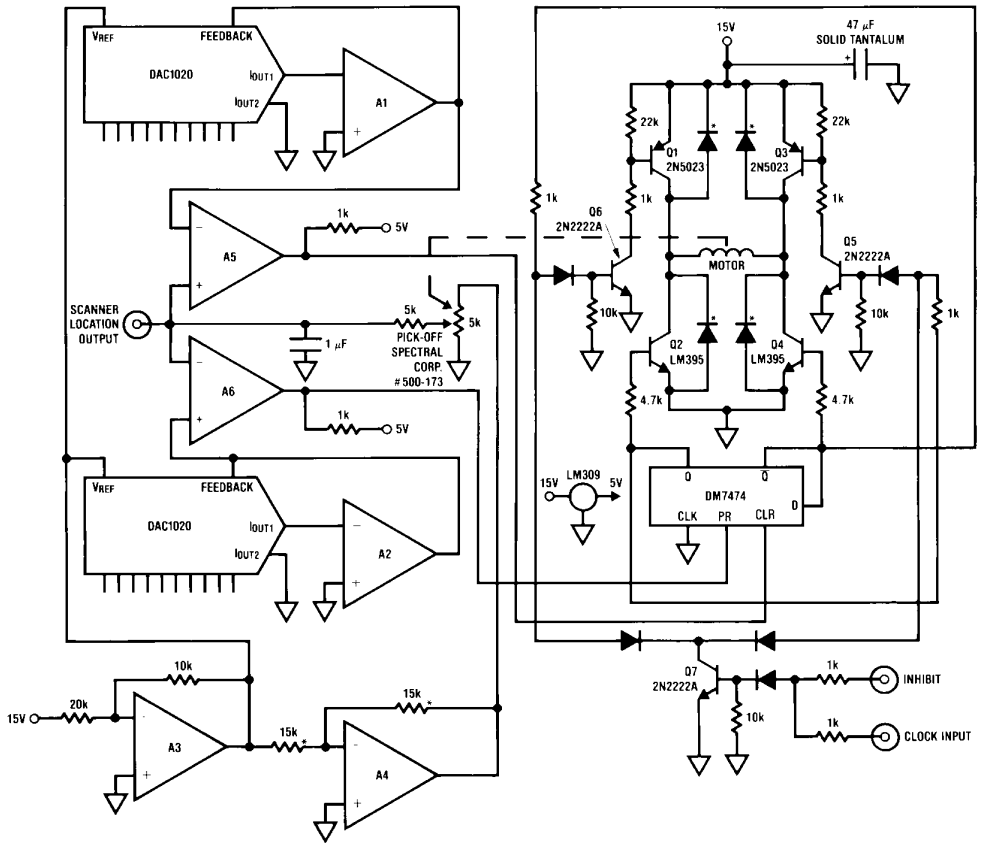
Control Applications of CMOS DACs

National Semiconductor
Application Note 293
March 1986

The CMOS multiplying digital-to-analog converter can be widely applied in processor-driven control applications. Because these devices can have a bipolar reference voltage their versatility is increased. In some control applications the DAC's output capabilities must be substantially increased to meet a requirement while others require substantial additional circuitry to drive a transducer or actuator. A good example of the latter is furnished by *Figure 1.*

SCANNER CONTROL

Biochemists use a procedure called ''scanning electrophoresis'' to separate cells from each other. In one form of this process the sample is contained within a vertical glass or quartz tube approximately 1 foot in length. When a high voltage potential is applied across the length of the tube the cells separate along the charge density gradient which runs along the tube's length. This results in a series of stripes



= 1N4148
= 1N4001
= 1% metal film, match 0.5%
Motor = Motordyne, Inc. #1150-1
A1, A2 = LF356
A3, A4 = LF353 dual
A5, A6 = LM393 dual

FIGURE 1

TL/H/5636–1

RRD-B30M115/Printed in U. S. A.

or bands within the tube as the individual cells, under the influence of the charge gradient, collect together. When separation is complete, the tube is mechanically scanned along its length by a photometer for optical density characteristics of each band. This information yields useful biochemical information to the experimenter. The scanner must be fully programmable so that it can be run between any two limits at a variety of speeds. In *Figure 1* the two DAC1020 D/A converters establish the limits of the scan. The 5k pick-off potentiometer furnishes scanner location information and the motor drives the scanner (via a gear-train). A5 and A6 are comparators, one of whose outputs goes low when either the high limit (A6 and its associated DAC) or low limit (A5 and its associated DAC) is exceeded. A1 and A2 furnish voltage outputs from the current output of the DACs. A3 and A4 are used to provide suitable reference voltages for the 5k pick-off potentiometer and the DAC reference inputs.

The DM7474 flip-flop is configured in a set-reset arrangement which changes output state each time either A5 or A6 goes low. When the lower limit of the scan is reached, A5 goes low, setting the DM7474's Q output too high. This turns on Q2, Q5 and Q3 resulting in current flow through the motor from Q3 to Q2. This forces the scanner to run towards its high limit. When this limit is reached, A6 goes low and the flip-flop changes state. This turns off the Q2, Q5, Q3 combination and the Q4, Q6, Q1 trio come on, forcing current through the motor in the opposite direction via the Q1-Q4 path. This causes the motor to reverse and proceed toward the lower limit. Q7 is driven by a width-modulated pulse train from the processor which is used to control the scanner's speed via Q5 and Q6. The diodes across Q1, Q2, Q3 and Q4 provide motor spike suppression and the internal current limiting in the LM395s (Q2-Q4) assures short circuit protection.

HIGH VOLTAGE OUTPUT FOR ATE

Testing high voltage components with automatic test equipment (ATE) is often inconvenient because a source of stable, controllable high voltage is required. Adding this capability to a piece of equipment can be expensive and time consuming if standard techniques are used. In *Figure 2* a circuit is shown which has been employed in the testing

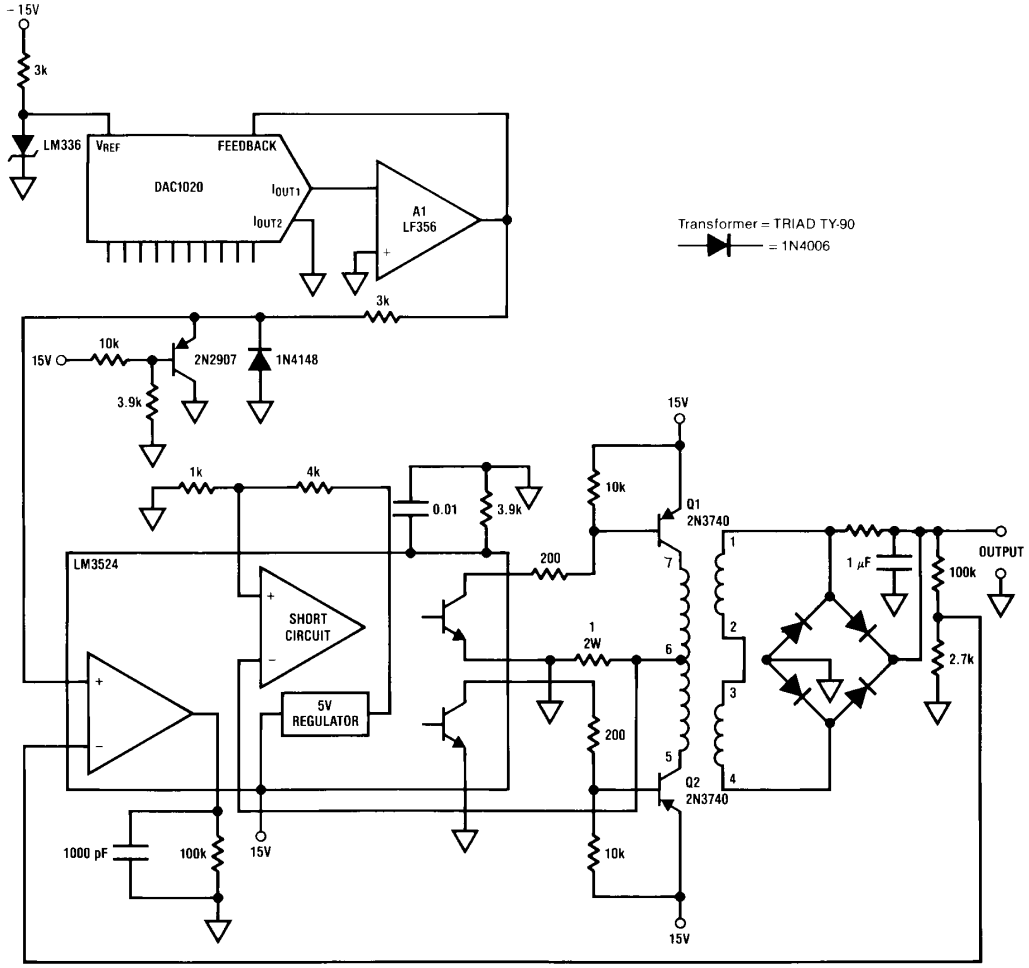


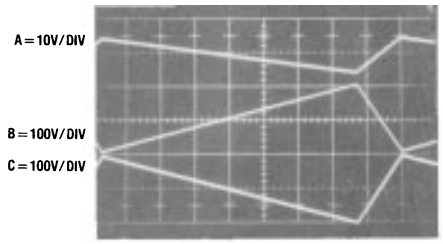
FIGURE 2

TL/H/5636–2

of high voltage transistors and zeners as well as fuse link blowing in PROMs. In this circuit, a high voltage output is developed by using a Toroidal DC-DC converter within a DAC-controlled pulse-width modulated feedback loop to obtain high voltage. The DAC1020 in conjunction with A1 supplies a setpoint to the LM3524 regulating pulse-width modulator. This set point needs to be within the LM3524's common mode input voltage range of 1.8V to 3.5V. The LM3524's outputs are used to drive the TY-90 toroid via Q1 and Q2. The high voltage square-wave transformer output is rectified and filtered and divided down by the 100k-2.7k string. This potential is fed back to the LM3524, completing a loop. Loop gain and frequency compensation are set by the 1000 pF-100k parallel combination, and the 1Ω resistor at pin 6 of the transformer is used to sense current for short circuit protection. Although the update rate into the DAC can be very fast, the 20 kHz switching of the transformer and the loop time constants determine the available bandwidth at the circuit's output. In practice, a full output sine wave swing of 100V into 1000Ω is available at 250 Hz.

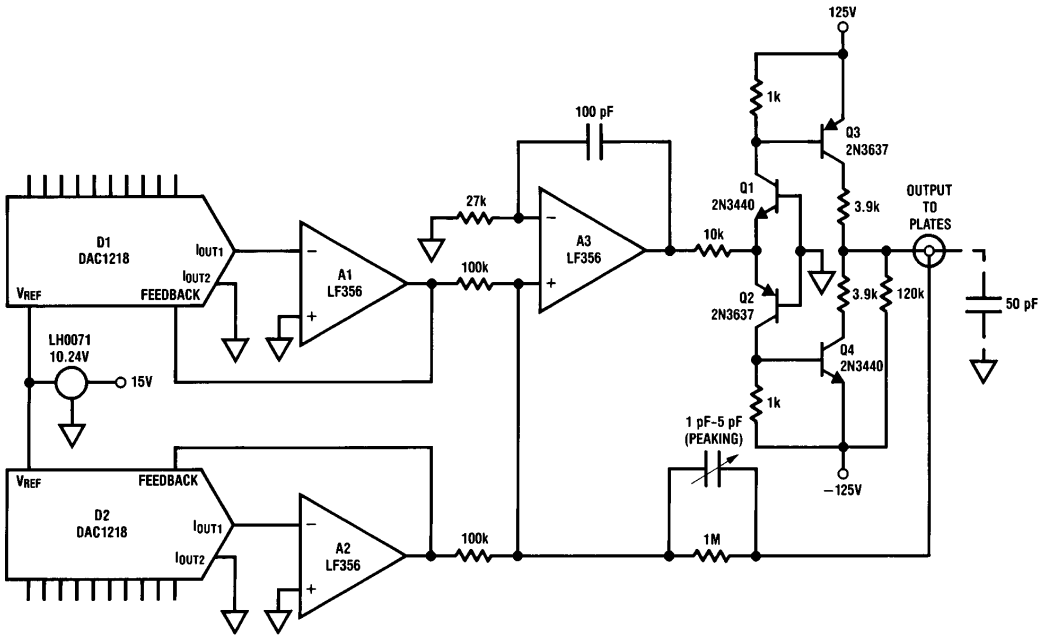
PLATE-DRIVING DEFLECTION AMPLIFIER

Another common high voltage requirement involves deflection plate modulation in CRT and electron-optics applications. *Figure 3* shows a pair of DAC1218s used to control both the static (DC) and dynamic (AC) drive to deflection plates in a piece of electron-optic equipment. In contrast to the previous high voltage circuit, this one has very little output current capability but greater bandwidth. The deflection plate load can be modeled as a 50 pF capacitor. In this application, the output of both DAC-amplifier pairs is summed at A3. In practice, one DAC will supply a DC level to the plate (bias) while the other one provides the plate's AC signal, typically a ramp. The high voltage plate drive is furnished by the Q1, Q2, Q3, Q4 configuration which is a complementary common-base-driven common-emitter output stage. Because the output current requirements are low, the usual crossover distortion problems may be avoided by returning the circuit's output to negative supply via the 120 kΩ resistor. This eliminates notch compensation circuitry and results in a simplified design. Because the high voltage stage inverts, overall negative feedback is achieved by returning the 1 MΩ feedback resistor to A3's positive input. The point now becomes the summing junction for both DAC-driven inputs and the feedback signal. The output of this circuit is clean and quick, as shown in *Figure 4.* In this figure, 2 complete DAC-driven amplifiers were used to produce the traces. Trace A is the output of A1, while the complementary high voltage outputs are shown in B and C.



TL/H/5636–3

FIGURE 4



TL/H/5636–4

FIGURE 3

TEMPERATURE LIMIT CONTROLLER

Certain biochemical reactions occur only within very specific temperature limits. The behavior of these reactions within and at the edges of these limits is of interest to biochemists. In order to study these reactions, a special temperature control scheme is required. To meet this requirement, the circuit of *Figure 5* has been employed. In this circuit A1, A3, A4 and A5 comprise a simple pulse-width modulating temperature controller. A4 is an integrator that generates a ramp which is periodically reset to zero by the 10 kHz clock pulse. This ramp is compared to A3 output by A5, which biased the LM395 switch to control the heater. A3's output will be determined by the difference between the temperature setpoint current through the 22.6 kΩ resistor and the current driven by the LM135 temperature sensor through the 10 kΩ resistor. Thermal feedback from the heater to the LM135 completes the loop. The 10M-1 μF values at A3 set loop response at 0.1 Hz.

Up to this point, the circuit functions as a fixed point temperature controller to provide a stable thermal baseline. To meet the application's requirement, however, the DAC1218 is driven by a slow digitally-coded triangle waveform. The DAC's output is fed to A2, whose output drives the 2 MΩ summing resistor. This causes the controller setpoint to vary slowly and predictably through the desired temperature excursion. This characteristic is observable on a strip-chart recording of the oven's temperature (*Figure 6)* over many hours.

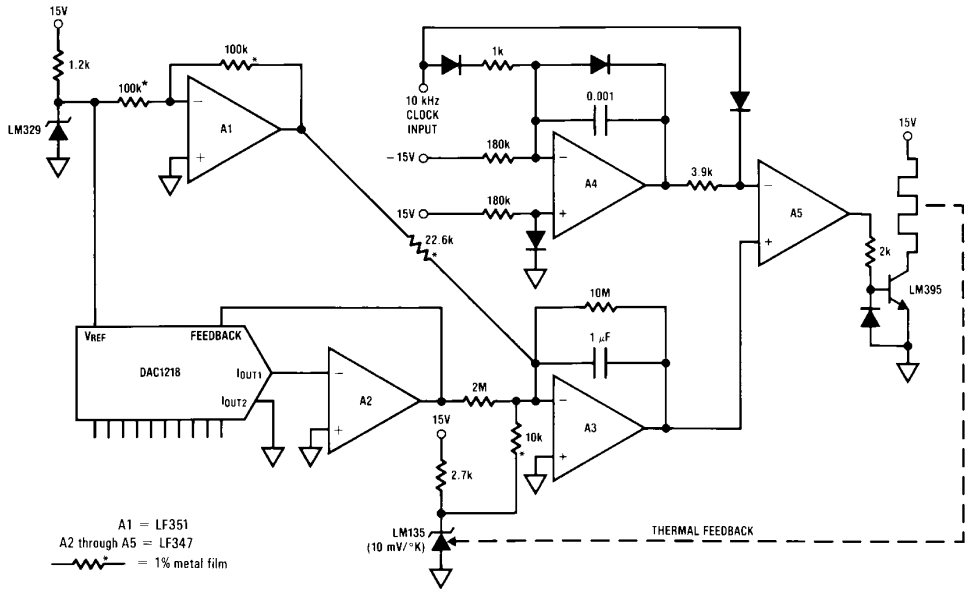
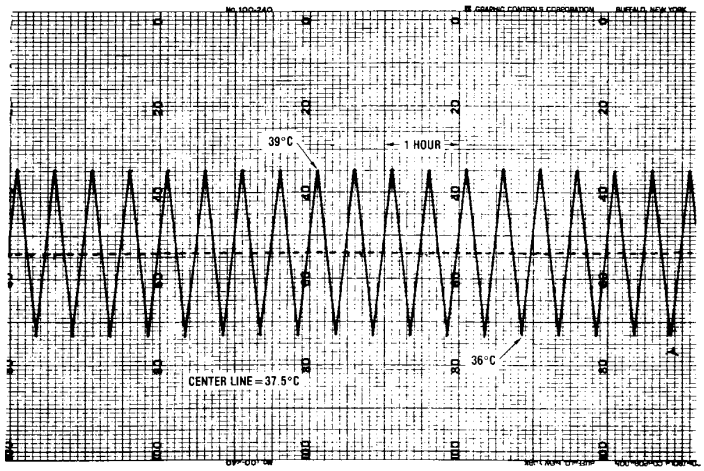


FIGURE 5

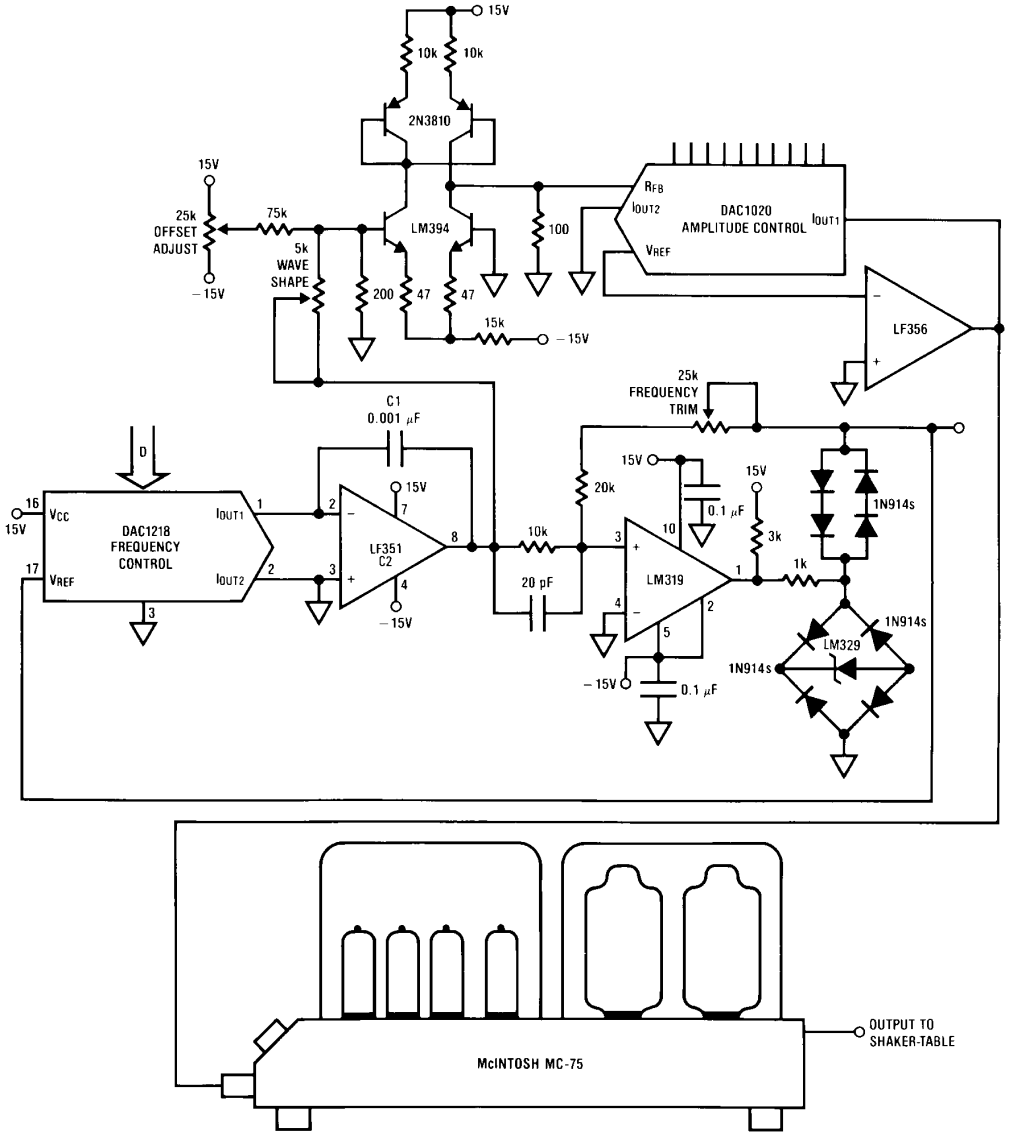


TL/H/5636–5

FIGURE 6

PROCESSOR CONTROLLED SHAKER-TABLE DRIVE

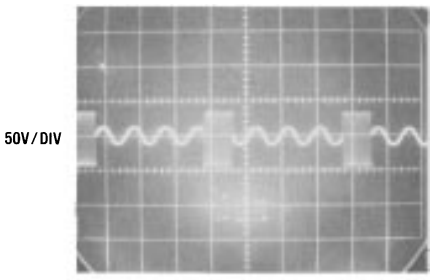
Shaker-tables are frequently employed to test finished assemblies for vibration induced failures under various conditions of frequency and amplitude. It is often desired to simulate vibration patterns which can greatly vary with duration, frequency and amplitude. In addition, it is useful to be able to vary both amplitude and frequency with precise control over wide dynamic ranges so that narrow resonances in the assembly under test may be observed. The circuit of *Figure 7* provides these capabilities. The DAC1218 is used to drive the LF351 integrator. The LF351's output ramps until the current through the 10k resistor just balances the current through the 20k resistor at pin 3 of the LM319 comparator. At this point the comparator changes state, forcing the zener diode bridge and associated series diode to put an equal but opposite polarity reference voltage. This potential is used as the DAC's reference input as well as the feedback signal to the LM319 "+" input. In this fashion, the integrator output forms a triangle waveform whose output is centered around ground. The DAC input coding controls the frequency, which may vary from 1 Hz to 30 kHz. Calibration is accomplished with the "frequency trim" potentiometer. The triangle waveform is shaped by the 2N3810-LM394 configuration which relies on the logarithmic relationship between V_{BE} and collector current in the LM394 to smooth the triangle into a sine wave. The two potentiometers associated with the



TL/H/5636–6

FIGURE 7

shaper are adjusted for minimum indicated distortion on a distortion analyzer. The DAC1020 and the LF356 are arranged in a DAC-controlled gain configuration which allows the amplitude of the sine wave to be varied over a range from millivolts to volts at the LF356 output. The low input impedance and high inductance of a typical shaker-table presents a difficult load for a solid state amplifier to drive, and vacuum tube amplifiers are frequently employed to avoid output stage failures. In this example, the amplifier specified is a well-known favorite for the job because its transformer-isolated input is immune to the inductive flyback spikes a shaker-table can generate. *Figure 8* shows the output waveform when both DACs are simultaneously updated. The output waveform changes in frequency and amplitude with essentially instantaneous response.



TL/H/5636–7

FIGURE 8

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Special Sample and Hold Techniques

National Semiconductor
Application Note 294
April 1982

Although standard devices (e.g., the LF398) fill most sample and hold requirements, situations often arise which call for special capabilities. Extended hold times, rapid acquisition and reduced hold step are areas which require special circuit techniques to achieve good results. The most common requirement is for extended hold time. The circuit of *Figure 1* addresses this issue.

EXTENDED HOLD TIME SAMPLE AND HOLD

In this circuit, extended hole time is achieved by ''stacking'' two sample and hold circuits in a chain. In addition, rapid acquisition time is retained by use of a feed-forward path. When a sample command is applied to the circuit (trace A, *Figure 2*), A1 acquires the input very rapidly because its 0.002 μF hold capacitor can charge very quickly. The sample command is also used to trigger the DM74C221 one-shot (trace B, *Figure 2*), which turns on the FET switch, S1. In this fashion, A1's output is fed immediately to the A3 output buffer. During the time the one-shot is high, A2 acquires the value of A1's output. When the one-shot drops low, S1 opens, disconnecting A1's output from A3's input. At this point A2's output is allowed to bias A3's input and the circuit output does not change from A1's initial sampled value. Trace C details what happens when S1 opens. A small glitch, due to charge transfer through the FET, appears but the steady state output value does not change. This circuit will acquire a 10V step in 10 μs to 0.01% with a droop rate of just 30 μV/second.

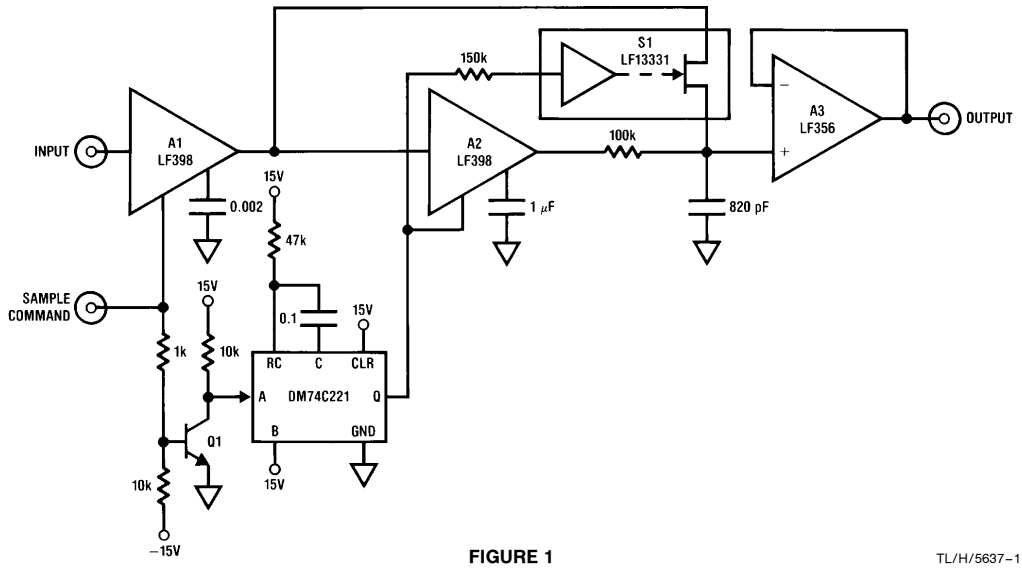

FIGURE 1

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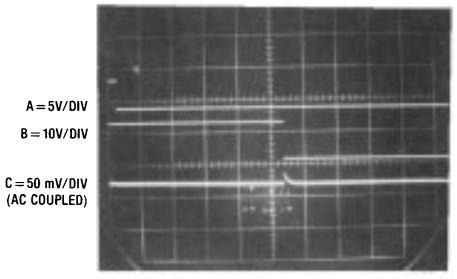

TL/H/5637–2

FIGURE 2

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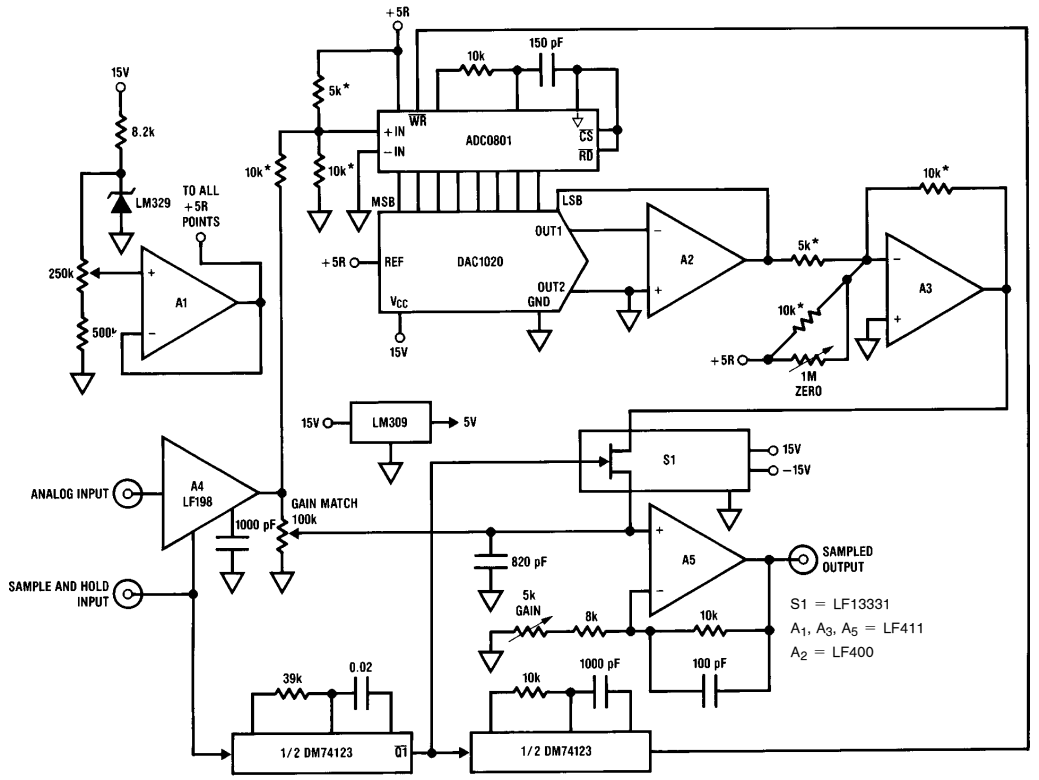


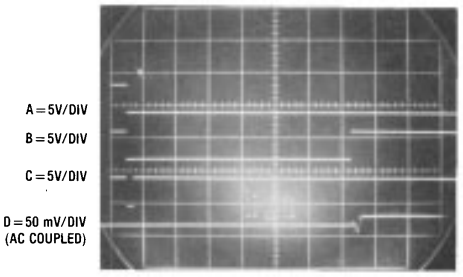
*Ratio match 0.1%

FIGURE 3

TL/H/5637–3

INFINITE HOLD SAMPLE AND HOLD

Figure 3 details a circuit which extends the hold time to infinity with an acquisition time of 10 μs. Once a signal has been acquired, this circuit will hold its output with no droop for as long as is desired. If this arrangement, A4's divided down output is fed directly to the circuit output via A5 as soon as a sample command (trace A, *Figure 4)* is applied. The sample command is also used to trigger the DM74123 one-shots. The first one-shot (trace B, *Figure 4)* is used to bias the FET switch OFF during the time it is low. The second one-shot (trace C, *Figure 4)* delivers a pulse to the ADC0801 A/D converter which then performs an A/D conversion on A4's output. The DAC1020, in combination with A2 and A3, converts the A/D output back to a voltage. The A/D/A process requires about 100 μs. When the one-shot (trace B) times out, its output goes high, closing the FET switch. This action effectively connects A3's output to A5 while disconnecting A4's output. In this manner, the circuit output will remain at the DC level that was originally determined by A4's sampling action. Because the sampled value is stored digitally, no droop error can occur. The precision resistors noted in the circuit provide offsetting capability for the unipolar A/D output so that a -10V to $+10$V input range can be accommodated. To calibrate this circuit, apply 10V to the input and drive the sample command input with a pulse generator. Adjust the gain match potentiometer so that minimum ''hop'' occurs at the circuit output when S1 closes. Next, ground the input and adjust the zero potentiometer for 0V output. Finally, apply 10V to the input and adjust the gain trim for a precise 10V circuit output. Once adjusted, this circuit will hold a sampled input to within the 8-bit quantization level of the A/D converter over a full range of $+10$V to -10V. Trace D, *Figure 4* shows the circuit output in great detail. The small glitch is due to parasitic capacitance in the FET switch, while the level shift is caused by quantization in the A/D. An A/D with higher resolution could be used to minimize this effect.



A, B, C HORIZONTAL = 20 μs/DIV
D HORIZONTAL = 2 μs/DIV

TL/H/5637–4

FIGURE 4

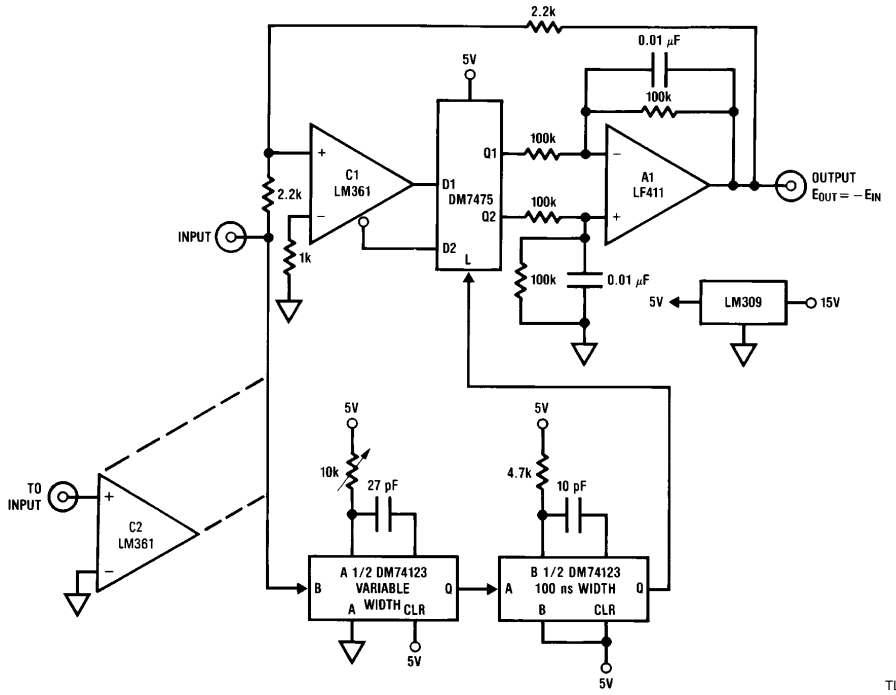
HIGH SPEED SAMPLE AND HOLD

Another requirement encountered in sample and hold work is high speed. Although conventional sample and hold circuits can be built for very fast acquisition times, they are difficult and expensive. If the input waveform is repetitive, the circuit of *Figure 5* can be employed. In this circuit a very fast comparator and a digital latch are placed in front of a differential integrator. Feedback is used to close a loop around all these elements. Each time an input pulse is applied, the DM7475 latch is opened for 100 ns. If the summing junction error at the LM361 is positive, A1 will pull current out of the junction. If the error is negative, the inverse will occur. After some number of input pulses, A1's output will settle at a DC level which is equivalent to the value of the level sampled during the 100 ns window. Note that the delay time of one-shot A is variable, allowing the sample pulse from one-shot B to be placed at any desired point on the input waveform. *Figure 6a* shows the circuit waveforms. Trace A is the circuit input. After the variable delay provided by one-shot A, one-shot B generates the sample pulse (trace B). In this case the delay has been adjusted so that sampling occurs at the mid-point of the input waveform, although any point may be sampled by adjusting the delay appropriately.

Figure 6b shows the circuit at work sampling a 1 MHz sine wave input. The optional comparator (C2) shown in dashed lines is used to convert the sine wave input into a TTL compatible signal for the DM74123 one-shot. Trace A is the sine wave input while trace B represents the output of C2. Trace C is the delay generated by one-shot A and trace D is the sample width window out of one-shot B. Note that this pulse can be positioned at any point on the high speed sine wave with the resultant voltage level appearing at A1's output.

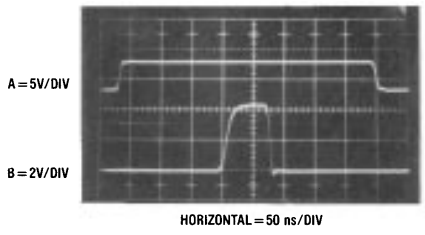
REDUCED HOLD STEP SAMPLE AND HOLD

Another area where special techniques may offer improvement is minimization of hold step. When a standard sample and hold switches from sample to hold, a large amplitude high speed spike may occur. This is called hold step and is usually due to capacitive feedthrough in the FET switches



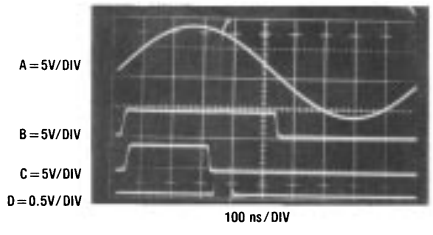
TL/H/5637–5

FIGURE 5



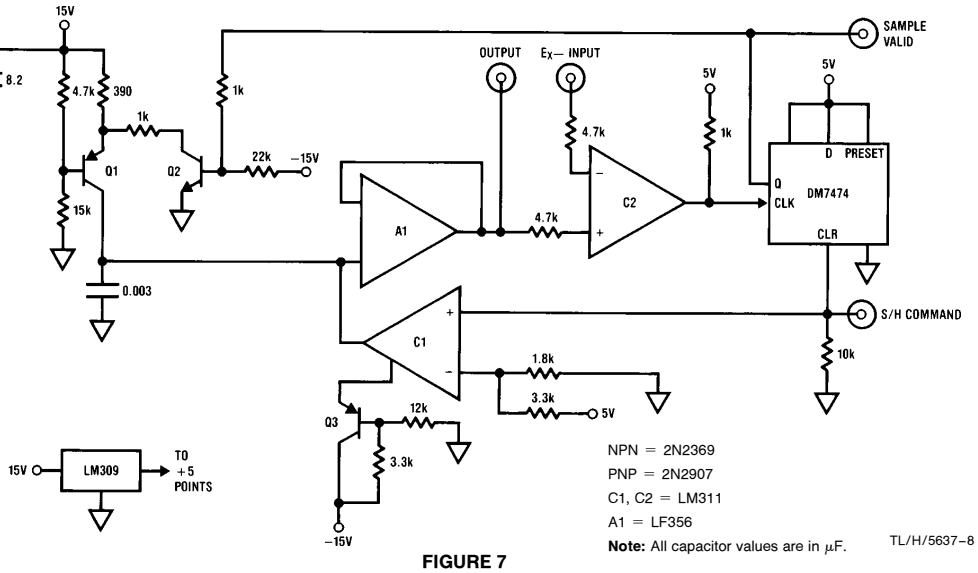
TL/H/5637–6

FIGURE 6a



TL/H/5637–7

FIGURE 6b



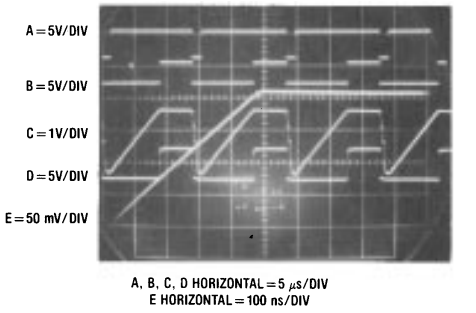
TL/H/5637–8

FIGURE 7

used in the circuit. The circuit of *Figure 7* greatly reduces hold step by using an unusual approach to the sample and hold function. In this circuit sampling is started when the sample and hold command input goes low (trace A,*Figure 8*). This action also sets the DM7474 flip-flop low (trace B, *Figure 8*). At the same time, C1's output clamps at Q3's emitter potential of −12V (trace C, *Figure 8*). When the sample pulse returns high, C1's output floats high and the 0.003 μF capacitor is linearly charged by current source Q1. This ramp is followed by A1, which feeds C2. When the ramp potential equals the circuit's input voltage, C2's output (trace D, *Figure 8*) goes high, setting the flip-flop high. This turns on Q2, very quickly cutting off the Q1 current source. This causes the ramp to stop and sit at the same potential at the circuit's input. The hold step generated when the circuit goes into hold mode (e.g., when the flip-flop output goes high) is quite small. Trace E, a greatly enlarged version of trace C, details this. Note the hold step is less than 10 mV high and only 30 ns in duration. Acquisition time for this circuit is directly dependent on the input value, at a rate of 5 μs/V.

REFERENCE

One IC Makes Precision Analog Sampler, S. Dendinger; EDN May 20, 1977.



TL/H/5637–9

FIGURE 8

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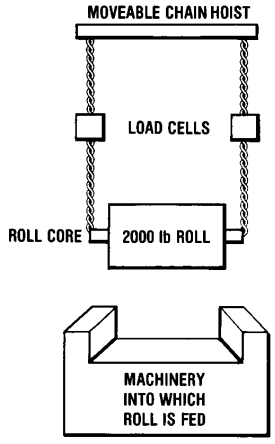
A High Performance Industrial Weighing System

National Semiconductor
Application Note 295
March 1982

The continuing emphasis on efficiency and waste control in the industrial environment has opened new applications areas for electronic measurement and control systems. Standard electronic techniques can be used to solve many of these application problems. In some areas, however, the measurement requirements are so demanding that novel and unusual circuit architectures must be employed to achieve the desired result. In particular, very high precision transducer-based measurements can be achieved by combining microprocessor and analog techniques. The performance achievable can surpass the best levels obtainable with conventional approaches.

An example of a requirement involves high resolution weighing of 2000 pound rolls of plastic material. In this application, the rolls must be weighed before they are fed into machinery which utilizes the plastic in a coating process. Because the plastic material is relatively expensive, and the number of rolls used over time quite large, it is desirable to keep close tabs on the amount of material actually used in production. This involves weighing the roll before it is used and then weighing the amount of material left on the roll core after it has unwound. In this fashion, the losses accumulated over hundreds of rolls can be tracked and appropriate action taken if the losses are unacceptable. *Figure 1* shows the way the rolls are handled and fed into the coating machinery. The desired weighing system performance specifications also appear in the figure. *Figure 2* shows the specifications for a typical high quality strain gauge load cell transducer. From this information, it can be seen that the electronic error budget is vanishingly small. The 3 mV/V specification on the load cell means that only 30 mV of full-scale is available for a typical 10V transducer excitation. The desired 0.01% resolution means that only 3μV referred-to-input error is allowable. In addition, the gain slope tolerance and temperature coefficients of the load cells, while small, seem to preclude meeting the required specifications. The 0.1% gain slope tolerance also appears to mandate the need for manual system recalibration whenever load cells must be replaced in the field. Finally, assuming these specifications can be met, an A/D converter which will hold near 15-bit stability over the required temperature range is required.

The key to achieving the desired performance is in the realization that the system must be designed as an *integrated* function instead of a group of interconnected signal conditioning blocks. Traditional approaches which rely on "brute force" high stability amplifiers and data converters cannot be successfully used to meet the required specifications.



TL/H/5638–1

FIGURE 1

Desired System Specifications

Accuracy, 0.03%
Stable Resolution, 0.01%
Operating Temperature Range, 10°C to 45°C
Full Load Cell Field Interchangeability
20,000 Count Display

FIGURE 2

Typical Load Cell Specifications

Gain Slope—3 mV/V Excitation ±0.1%
Recommended Excitation—10V
Gain Tempco—±0.0008%/°F
Zero Tempco—±0.0015/°F

RRD-B30M115/Printed in U. S. A.

The approach utilized is diagrammed in *Figure 3*. In this arrangement a microprocessor is used to effectively close an analog loop around the load cells with an instrumentation amplifier and an A/D converter. In this system, four discrete measurements are continuously performed on each load cell to determine its error corrected output. Corrections are made for zero and gain drift and a first-order temperature error correction is also made. The actual load cell output voltage is read to complete the measurement cycle. The start of a measurement cycle is initiated by the microprocessor commanding the LF13509 differential input multiplexer A to position 1 (See *Figure 4*). In this position, the amplifier inputs are connected to one side of the transducer bridge. This determines the electrical zero in the system at the common-mode output voltage of the bridge. Physical zero information (e.g., ''tare weight'') is fed to the microprocessor via a pushbutton which is depressed when no load is in the chain hoist. This operation need only be carried out when the system is first turned on. The multiplexer is then switched to position 2.

In this position, the LM163 inputs are connected across the middle resistor in a string of resistors. The voltage across this resistor represents the precise full-scale output voltage of the load cell transducer. Although the transducers are specified for only 0.1% interchangeability, the precise value of gain slope is furnished with each individual device. This information allows the system to determine the gain slope of the transducer. In practice, the middle resistor in the string is physically located within the load cell connector. When any such equipped load cell is plugged into the system, the value of this resistor allows immediate and precise gain slope compensation and eliminates the usual manual calibration requirements. When this measurement is completed, the multiplexer is switched to position 3. In this position the output of strain gage bridge A is connected to the LM163 instrumentation amplifier. This signal, which represents the transducer output, is amplified by the LM163, converted by the A/D and stored in memory. The fourth multiplexer operation is used to read the temperature of the load cell. In this position, the output of the LM335 temperature sensor, which is located inside the load cell transducer, is determined and stored in memory. The relatively high level LM335 output is resistively divided by 100 so the LM163 does not saturate. Two separate temperature terms, zero and gain TC, affect the load cell. Although the LM335 provides the absolute cell temperature, the sign of each temperature term in any individual cell will vary. Thus, not only the cell's temperature but the sign for both zero and gain terms must be furnished. This is accomplished by a pin strapping code inside the load cell's connector. This sequence of operations is also performed by multiplexer B for load cell B. When all the information for both transducers has been collected, the microprocessor can determine the actual weight of the roll. The temperature information provides a first-order correction for the relatively small effect of ambient temperature on the load cell's gain and zero terms.

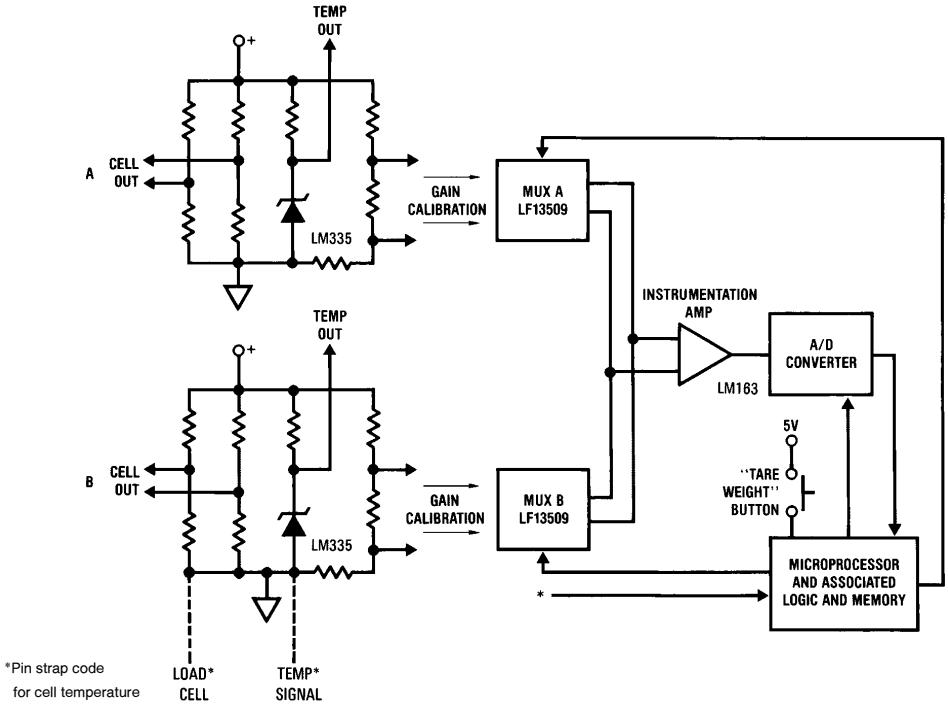
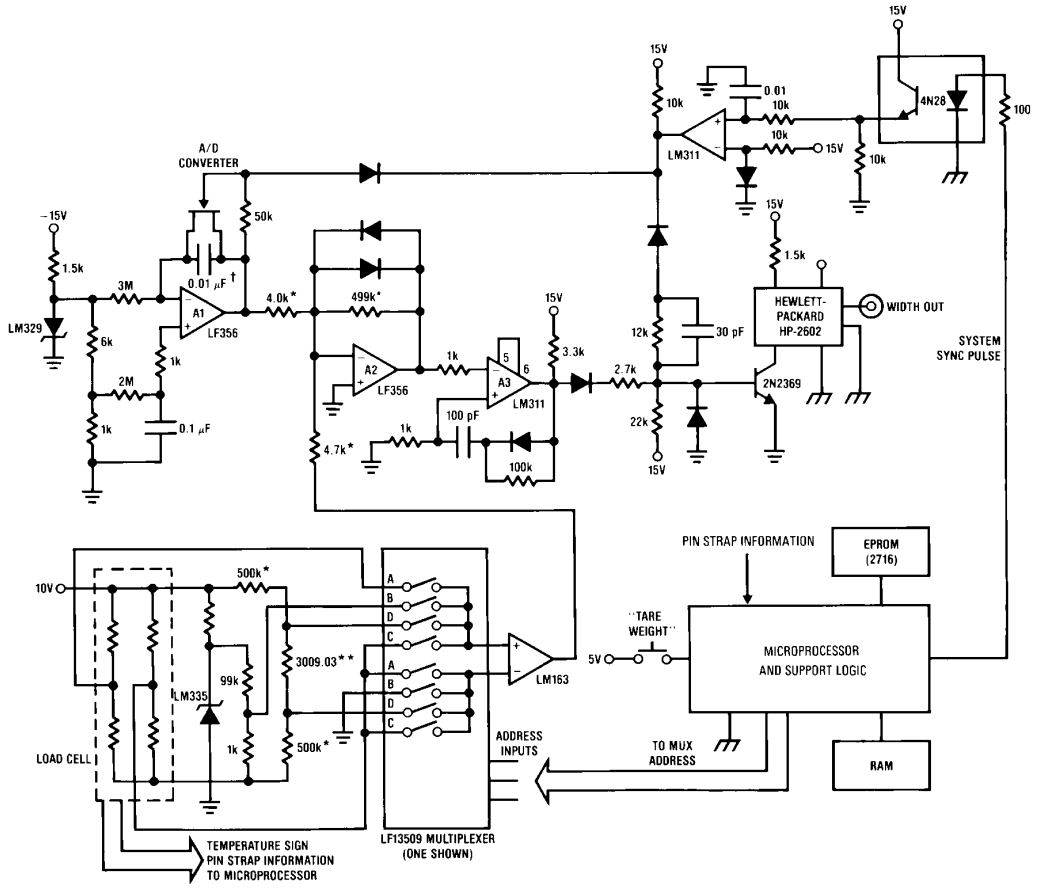


FIGURE 3

TL/H/5638–2

The gain calibration resistor string inside the load cell allows complete field interchangeability with no manual field calibration required. In practice, the load cell connector heads are modified by the addition of the resistor string, temperature sensor and temperature sign pin strapping after the cells have been purchased from the manufacturer. Connector types with the appropriate extra number of pins are substituted for the originals and the completed modified transducer is furnished as a unit to the end user. The stability of this approach is entirely dependent on the resistors in the gain calibration string. The voltage drive to the bridge need not be stable because it is common to the gain calibration string and ratiometrically cancels. Low pass filtering of electrical and mechanical noise is achieved by displaying the digitally-averaged value of a number of measurement cycles. It is worth noting that zero and gain drifts in the instrumentation amplifier and the A/D converter are continuously compensated for by the closed loop action of the microprocessor. The sole requirement for these components is that they be linear and have noise limits within the required measurement precision. In this manner, the zero and gain drifts of all active electronic components in the system are eliminated, which considerably simplifies the selection and design of these components.

A schematic diagram of the system appears in *Figure 4*. For purposes of clarity only, one load cell and its associated multiplexer are shown. Details of the microprocessor are also not included. The LF11509 multiplexer feeds the LM163 instrumentation amplifier. The LM163's output is routed to the A/D converter section which is composed of a ramp generator (A1) and a precision comparator circuit (A2-A3). The output of the A/D is a pulse width which varies with the LM163's output amplitude. This pulse width is fed to the microprocessor which uses it to gate a high speed clock. A



TL/H/5638–3

†Teflon

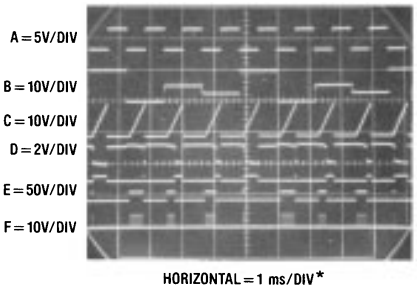
*Ultronix 104A ratio match 0.005%.

**Ultronix 104A, 0.01% value shown is ideal for precise 30 mV output load cell and must be selected at load cell test.

FIGURE 4

loop is completed by using the microprocessor to control the LF11509 multiplexer address inputs. Operation of the system is best understood by referring to *Figure 5*. Trace A is a system synchronizing pulse which is generated by the microprocessor. Trace B is the output of the LM163, which is connected to the multiplexer. Each time the synchronizing pulse goes low, the multiplexer advances one state. The leftmost multiplexer state in the photograph is the zero signal. The next state is the gain calibration, which is followed by the strain gage bridge output and then the temperature signal. The next 4 multiplexer states repeat this pattern for the other load cell. Each time the multiplexer changes state, the LM163 output is compared to the A1 ramp generator output (trace C) by the A2-A3 comparator. A2 acts as a preamplifier for the A3 comparator, insuring a low noise trip point. When the ramp is very close to balancing the current being pulled out of A2's summing junction by the LM163, A2 comes out of diode bound (trace D, *Figure 5*) and trips A3. The rapid slewing, high level signal from A2 allows A3 to have a noise free transition (trace E, *Figure 5*). This output is used to turn off a high speed clock (trace F, *Figure 5*) which was started at the beginning of the ramp (comparator-ramp-high speed clock detail shown in *Figure 6*). The waveforms show that the number of high speed pulses which occur at each multiplexer state varies with the LM163's output. Because the ramp is highly linear and the comparator very stable, a direct relationship between the number of high speed pulses and the LM163 output is assured. The final computed answer at which the microprocessor controlled loop arrives will nullify the effects of drift in the A/D converter and instrumentation amplifier.

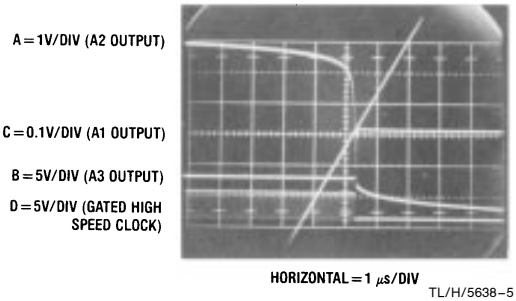
In practice, this system has met specifications in the industrial environment for which it was designed. It furnishes a good example of the type of intelligence which is becoming typical in industrial measurement and control apparatus. The interlocking of analog and digital techniques to solve a difficult measurement problem will become even more common in future applications.



TL/H/5638–4

*System operation normally occurs at a 2 Hz rate but has been sped up for photographic convenience.

FIGURE 5



TL/H/5638–5

Details of comparator-ramp-high speed clock interaction:

When A2's output comes out of bound (trace A), the A3 comparator responds with a clean, noise-free transition (trace B), causing the high speed clock burst to cease (trace D). Trace C shows the ramp, greatly expanded. A2-A3 trip point occurs just after the ramp passes center screen.

FIGURE 6

LIFE SUPPORT POLICY

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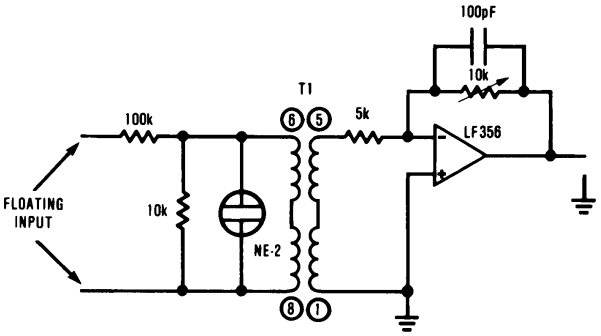
Isolation Techniques for Signal Conditioning

National Semiconductor
Application Note 298
May 1982

Industrial environments present a formidable challenge to the electronic system designer. In particular, high electrical noise levels and often excessive common mode voltages make safe, precise measurement difficult. One of the best ways to overcome these problems is by the use of isolated measurement techniques. Typically, these approaches utilize transformers or opto isolators to galvanically isolate the input terminals of the signal conditioning amplifier from its output terminal. This breaks the common ground connection and eliminates noise and dangerous common mode voltages. The conflicting requirements for good accuracy and total input/output galvanic isolation requires unusual circuit techniques. A relatively simple isolated signal conditioner appears in *Figure 1*.



00563902

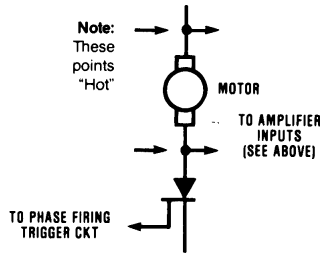
OUTPUT= INPUT ÷100 & ISOLATED T1=UTC #P2

To AC Line From Full Wave Bridge

FIGURE 1.

Floating Input High Voltage Motor Monitor

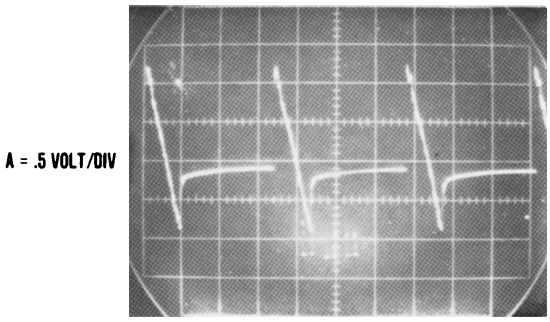
In this inexpensive circuit, a wideband audio transformer permits safe, ground referenced monitoring of a motor which is powered directly from the 115VAC line. *Figure 2* details the measurement arrangement. The floating amplifier inputs are applied directly across the brush-type motor. The 100k-10k string, in combination with the transformer ratio, provides a nominal 100:1 division in the observed motor voltage while simultaneously allowing a ground referenced output. The NE-2 bulb suppresses line transients while the 10k potentiometer trims the circuit for a precise 100:1 scale factor. To calibrate the circuit, apply a 10-volt RMS 1kHz sine wave to the floating inputs, and adjust the potentiometer for 100 millivolts RMS output. Full power bandwidth extends from 15Hz to 45kHz ± .25dB with the –3dB point beyond 85kHz. Risetime is about 10 microseconds. *Figure 3* shows the motor waveform at the ground referenced circuit output. The isolated, wideband response of the circuit permits safe monitoring of the fast rise SCR turn-on as well as the motor's brush noise.



00563901

AC Line From Full Wave Bridge

FIGURE 2.



00563903

FIGURE 3.

Isolated Temperature Measurement

Figure 4 shows a scheme which allows an LM135 temperature sensor to operate in a fully floating fashion. In this circuit, the LM311 puts out a 100 microsecond pulse at about 20Hz. This signal biases the PNP transistor, whose collector load is composed of the 1kΩ unit and the primary of T1. The voltage that develops across T1's primary (waveform A, *Figure 5*) will be directly dependent upon the value that the LM135 temperature sensor clamps the secondary at. Waveform B, *Figure 5* details the transformer primary current.

Isolated Temperature Measurement (Continued)

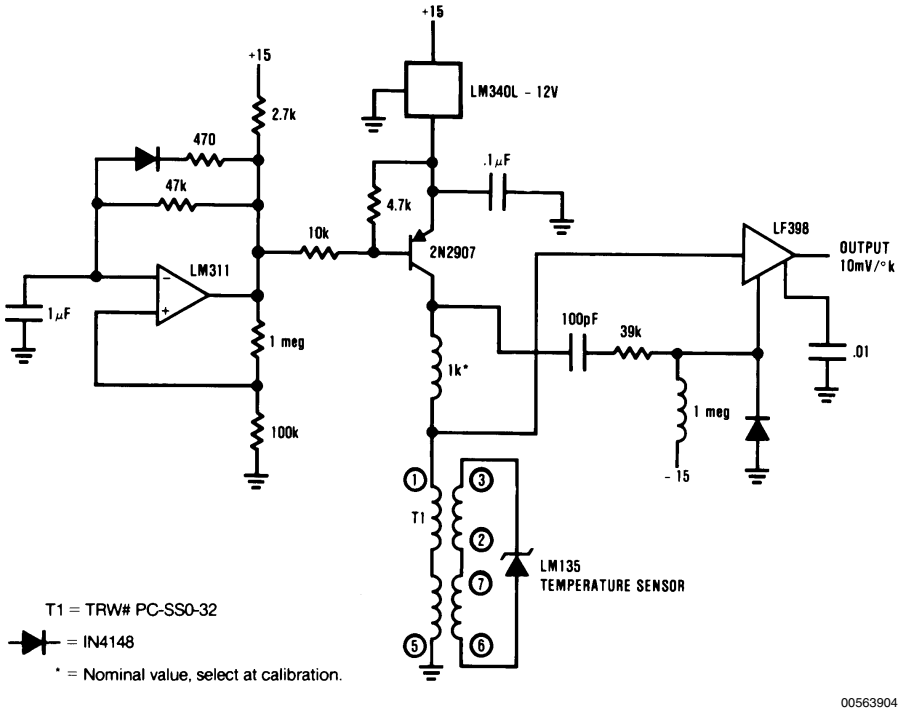


FIGURE 4.

This voltage value, of course, varies with the temperature of the LM135 in accordance with its normal mode of operation. The LF398 sample-and-hold IC is used to sample the transformer primary voltage and presents the circuit output as a DC level. The 100 pF-39k-1MΩ combination presents a trigger pulse (waveform C, *Figure 5*) to the LF398, so that the sampling period does not finish until well after the LM135 has settled. The LM340 12-volt regulator provides power supply rejection for the circuit. To calibrate, replace the LM135 with an LM336 2.5-volt diode of known breakdown potential. Next, select the 1kΩ valve until the circuit output is the same as the LM336 breakdown voltage. Replace the LM336 with the LM135 and the circuit is ready for use.

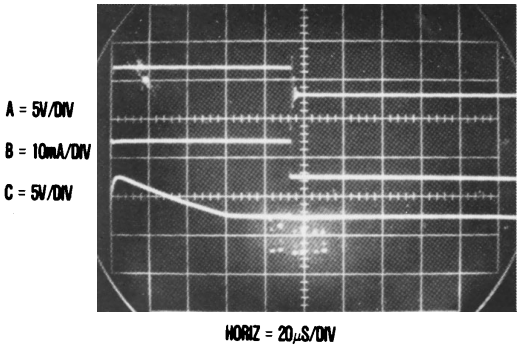


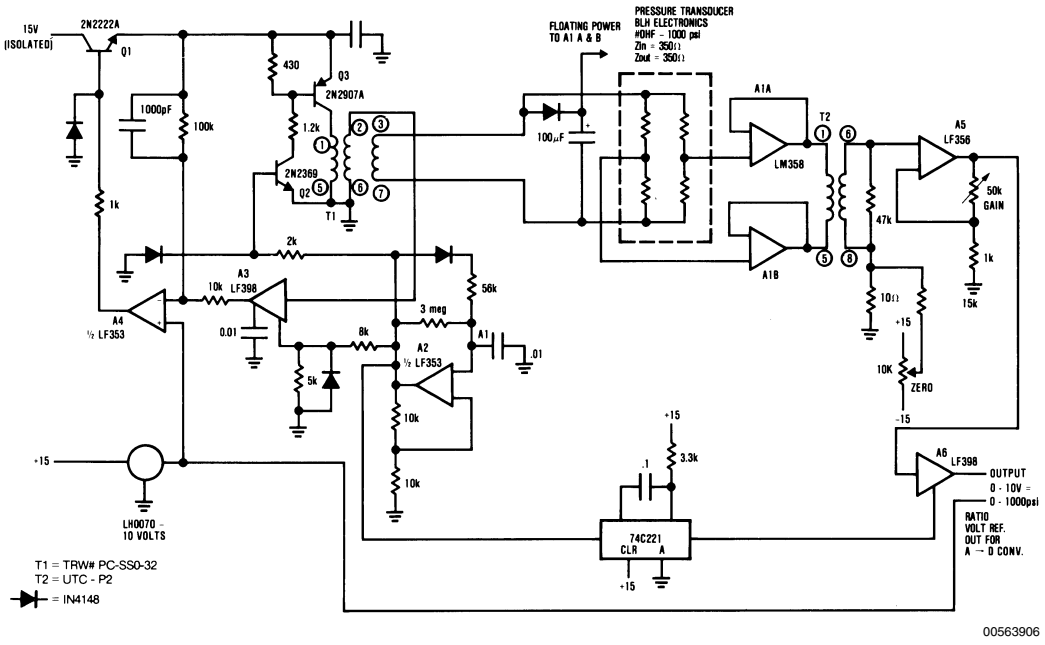
FIGURE 5.

Fully Isolated Pressure Transducer Measurement

Strain gauge-based transducers present special difficulties if total isolation from ground is required. They need excitation power in addition to their output signal. Some industrial measurement situations require that the transducer must be physically connected to a structure which is floating at a high common mode voltage. This means that the signal conditioning circuitry must supply fully floating drive to the strain gauge bridge, while also providing isolated transducer output signal amplification. *Figure 6* details a way to accomplish this. Here, the strain bridge is excited by a transformer which generates a pulse of servo-controlled amplitude. The pulse is generated by storing the sampled amplitude of the output pulse as a DC level, and supplying this information to a feedback loop which controls the voltage applied to the output switch. A2 functions as an oscillator which simultaneously drives Q2-Q3 and the LF398 (A3) sample mode pin. When A2's output pulse ends, A3's output is a DC level equal to the amplitude of the output pulse which drives the strain bridge. The dual secondary of T1 allows accurate magnetic sampling of the strain bridge output pulse without sacrificing electrical isolation. A3's output is compared to the LH0070 10-volt reference by A4, whose output drives Q1. Q1's emitter provides the DC supply level to the Q2-Q3 switch. This servo action forces the pulses applied to the strain gauge transducer (waveform A, *Figure 7*) to be of constant amplitude and equal to the 10-volt LH0070 reference output. Some amount of the pulse's energy is stored in the 100μF capacitor and used to power the LM358 dual (A1) followers.

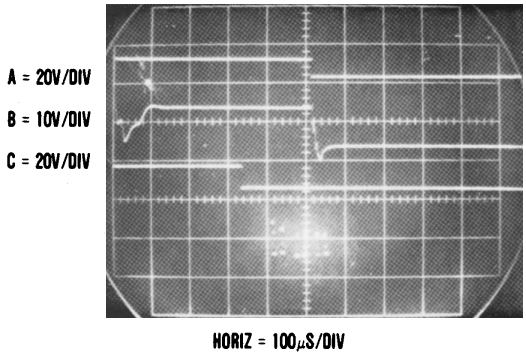
Fully Isolated Pressure Transducer Measurement (Continued)

These devices unload the output of the transducer bridge and drive the primary of T2. T2's secondary output amplitude (waveform B, *Figure 7*) represents the transducer output value. This potential is amplified by A5 and fed to A6, a sample-and-hold circuit. A6's sample command is a shortened version of the A2 oscillator pulse. The 74C221 generates this pulse (waveform C, *Figure 7*).



00563906

FIGURE 6.



00563907

FIGURE 7.

Because the A6 sample command falls during the settled section of T2's output pulse, A6's output will be a DC representation of the amplified strain gauge pressure transducer output. The LH0070 output may be used to ratiometrically reference a monitoring A/D converter. To calibrate this circuit, insert a strain bridge substitution box (e.g., BLH model 625) in place of the transducer and dial in the respective values for zero and full-scale output (which are normally supplied with the individual transducer). Adjust the circuit "zero" and "gain" potentiometers until a 0- to 10-volt output corresponds to a 0 to 1000psi pressure input.

1.5-Volt Powered Isolated Pressure Measurement

Figure 8 diagrams another pressure measurement circuit. This circuit presents a frequency output which is fully isolated by the transformer indicated. The entire circuit may be powered from a 1.5-volt supply, which may be derived from a battery or solar cells. The potentiometer output of the pressure transducer used is fed to a voltage-to-frequency converter circuit. In this V-F circuit, an LM10 op amp acts as an input amplifier, and forces the collector current of Q1 to be linearly proportional to V_{IN} for a range of 0 to +400 millivolts. Likewise, the reference amplifier of the LM10 causes Q2's output current to be stable and constant under all conditions. The transistors Q3-Q10 form a relaxation oscillator, and every time the voltage across C1 reaches 0.8-volt, Q6 is commanded to reset it to zero volts differential. This basic circuit is not normally considered a very accurate technique, because the dead time, while Q6 is saturated, will cause a large (1%) nonlinearity in the V-to-F transfer curve. However, the addition of R_X causes the reference current flowing through Q2 to include a term which is linearly proportional to the signal, which corrects the transfer nonlinearity.

1.5-Volt Powered Isolated Pressure Measurement (Continued)

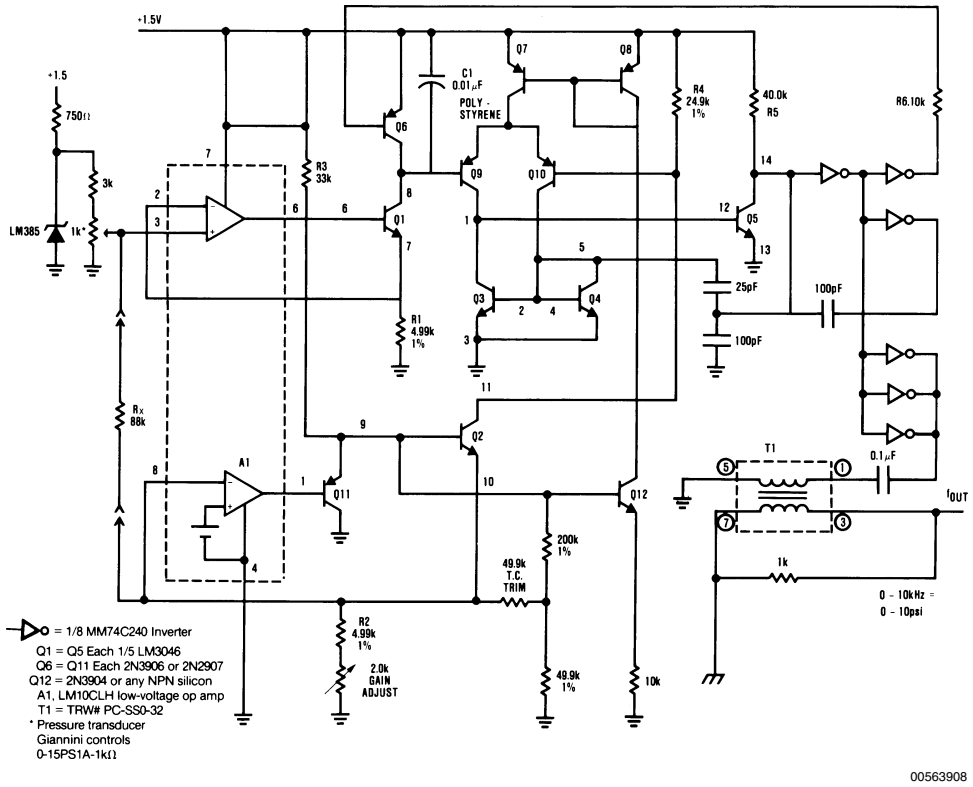


FIGURE 8.

The NSC MM74C240 inverters are employed because this IC has the only uncommitted inverters with such a low (0.6 to 0.8V) threshold that they can operate on a supply as low as 1.2 volts.

The 49.9k resistors which feed into Q2's emitter act as a gain tempco trim, as Q12's Vbe is used as a temperature sensor. If the output frequency is 100ppm/C too fast/hot, you can cut the resistor to 20k. If f is too slow/hot, add more resistance in series with the 49.9k. Total current drain for this circuit is about 1 milliampere.

Fully Isolated "Zero Power" Complete A/D Converter

Figure 9 shows a complete 8-bit A/D converter, which has all input and output lines fully floating from system ground. In addition, the A/D converter requires *no* power supply for operation! Circuit operation is initiated by applying a convert-command pulse to the "convert-command" input (trace A, *Figure 11*). This pulse simultaneously forces the "Data Output" line low (trace B, *Figure 11*) and propagates across the isolation transformer. The pulse appears at the transformer secondary (*Figure 10*, trace A) and charges the 100 μF capacitor to five volts. This potential is used to supply power to the floating A/D conversion circuitry. The pulse appearing at the transformer secondary is also used to start the A/D conversion by biasing comparator A's negative input low. This causes comparator A's output to go low, discharging the .06μF capacitor (waveform B, *Figure 10*). Simultaneously, the 10kHz oscillator (*Figure 10*, trace D), formed by comparator D and its associated components, is forced off via the 22k diode path. A second diode path also forces comparator D's output low (*Figure 10*, trace E). Note the cessation of oscillation during the time the convert command pulse is high. When the convert command pulse falls, the Q1-Q2 current source begins to charge the .06 μF capacitor. During this time, the 10 kHz comparator C oscillator runs, and comparator D's output is a stream of 10 kc clock pulses. When the ramp (trace B, *Figure 10*) across the .06 μF capacitor exceeds the circuit input voltage, comparator B's output goes high (trace C, *Figure 10*), forcing comparator D's output low. The number of pulses which appeared at comparator D's output is directly proportional to the value of the circuit's input voltage. These pulses are amplified by the two NPN transistors which are used to modulate the data pulse stream back across the transformer. The six series diodes insure that the modulated data does not appear at comparator A's input and trigger it. The pulses appear at the primary (*Figure 11*, trace A) as small amplitude spikes and are then amplified by the data output transistor, whose collector waveform is trace B or *Figure 11*. In this example a 0- to 3-volt input produces 0- to 300 pulses at the output. The 22k diode path averts a +1 count uncertainty error by synchronizing the 10kHz clock to the conversion sequence at the beginning of each conversion. The 500k potentiometer in the current source adjusts the scale factor. The circuit drifts less than 1LSB over 25˚C±20˚C and requires 45 milliseconds to complete a full scale 300 count conversion.

Fully Isolated "Zero Power" Complete A/D Converter (Continued)

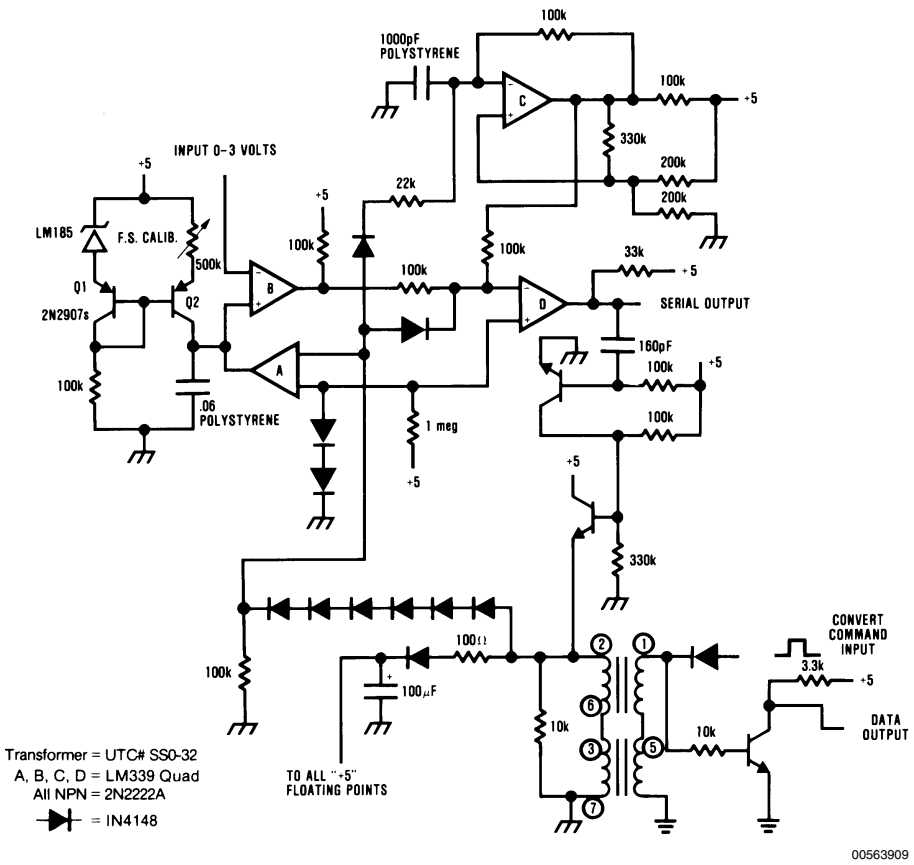
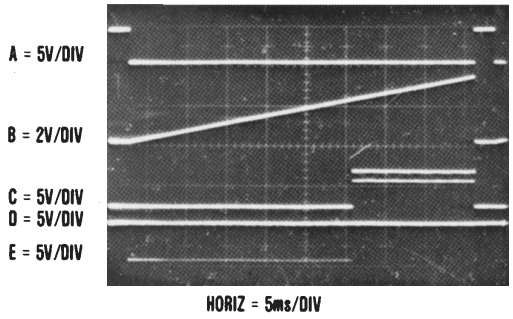


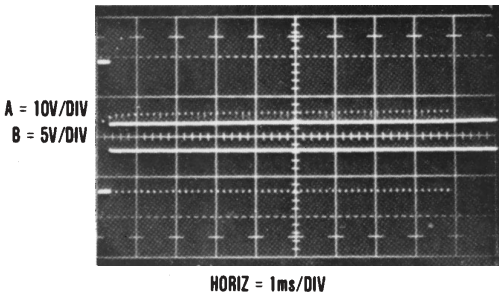
FIGURE 9.

Fully Isolated "Zero Power" Complete A/D Converter (Continued)



00563910

FIGURE 10.



00563911

FIGURE 11.

Complete, Floating Multiplexed Thermocouple Temperature Measurement

Figure 12 shows a complete, fully floating multiplexed thermocouple measurement system. Power to the floating system is supplied via T2, which runs in a self oscillating DC-DC converter configuration with the 2N2219 transistors. T2's output is rectified, filtered, and regulated to ±15 volts. An eight channel LF13509 multiplexer is used to sequentially switch 7 inputs and a ground reference into the LM11 amplifier. The LM11 provides gain and cold junction compensation for the thermocouples. The multiplexer is switched from the 74C93 counter, which is serially addressed via the 4N28 opto isolator. The ground referenced channel prevents monitoring instrumentation from losing track of the multiplexer state. The LM11's output is fed into a unity gain isolation amplifier. Oscillator drive for the isolation amplifier is derived by dividing down T2's pulsed output, and shaping the 74C90's output with A4 and its associated components. This scheme also prevents unwanted interaction between the T2 DC-DC converter and the isolation amplifier. This circuit, similar to the servo-controlled amplitude pulser described in *Figure 6*, puts a pulse across T1's primary. The amplitude of the pulse is directly dependent on the LM11's output value. T1's secondary receives the pulse and feeds into an LF398 sample-hold-amplifier. The LF398 is supplied with a delayed trigger pulse, so that T1's output is sampled well after settling occurs. The LF398 output equals the value of the LM11. In this fashion, the fully floating thermocouple information may be connected to grounded test equipment or computers. Effective cold-junction compensation results when the thermocouple leads and the LM335 are held isothermal. To calibrate the circuit, first adjust R3 for an LM11 gain of 245.7. Next, short the "+" input of the LM11 and the LM329 to floating common, and adjust R1 so that the circuit output is 2.982 volts at 25˚C. Then, remove the short across the LM329 and adjust R2 for a circuit output of 246 millivolts at 25˚C. Finally, remove the short at the LM11 input, and the circuit is ready for use.

Complete, Floating Multiplexed Thermocouple Temperature Measurement

(Continued)

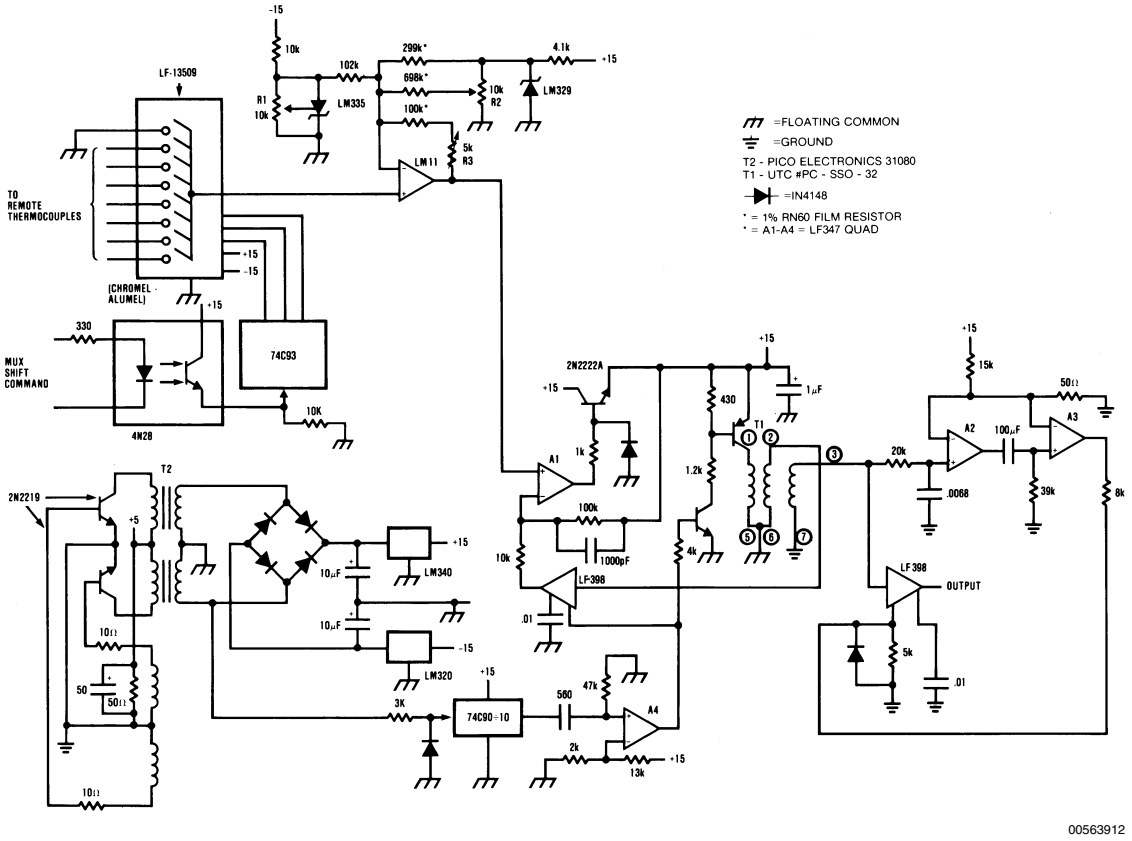


FIGURE 12.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Audio Applications of Linear Integrated Circuits

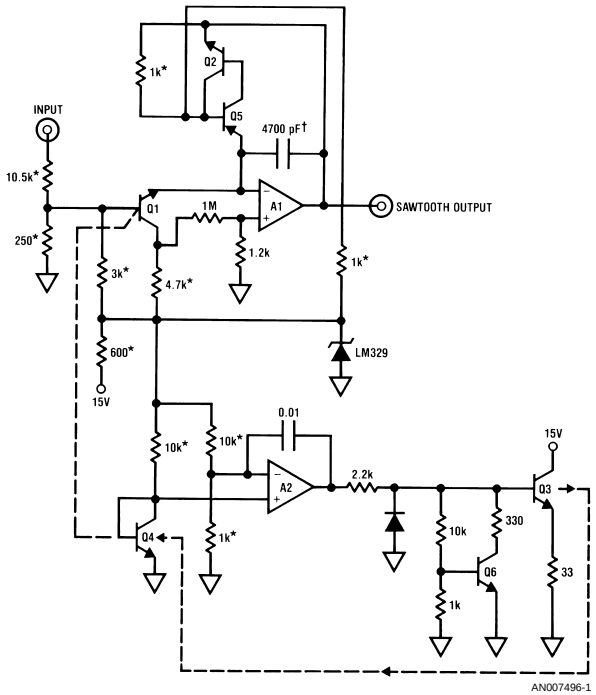
National Semiconductor
Application Note 299
April 1982

Although operational amplifiers and other linear ICs have been applied as audio amplifiers, relatively little documentation has appeared for other audio applications. In fact, a wide variety of studio and industrial audio areas can be served by existing linear devices. The stringent demands of audio requirements often mean that unusual circuit configurations must be used to satisfy a requirement. By combining off-the-shelf linear devices with thoughtful circuit designs, low cost, high performance solutions are achievable. An example appears in *Figure 1*.

EXPONENTIAL V-F CONVERTER

Studio-type music synthesizers require an exponentially responding V-F converter with a typical scale factor of 1V in per octave of frequency output. Exponential conformity requirements must be within 0.5% from 20 Hz–15 kHz. Almost all existing designs utilize the logarithmic relationship between V_{BE} and collector current in a transistor.

Although this method works well, it requires careful attention to temperature compensation to achieve good results. *Figure 1* shows a circuit which eliminates all temperature compensation requirements. In this circuit, the current into A1's summing junction is exponentially related to the circuit input voltage because of the logarithmic relationship between Q1's V_{BE} and its collector current. A1's output integrates negatively until the Q2-Q5 pair comes on and resets A1 back to 0V. Note that opposing junction tempcos in Q2 and Q5 provide a temperature compensated switching threshold with a small (100 ppm/°C) drift. The −120 ppm/°C drift of the polystyrene integrating capacitor effectively cancels this residual term. In this fashion, A1's output provides the sawtooth frequency output. The LM329 reference stabilizes the Q5-Q2 firing point and also fixes Q1's collector bias. The 3k resistor establishes a 20 Hz output frequency for 0V input, while the 10.5k unit trims the gain to 1V in per octave frequency doubling out. Exponential conformity is within 0.25% from 20 Hz to 15 kHz.



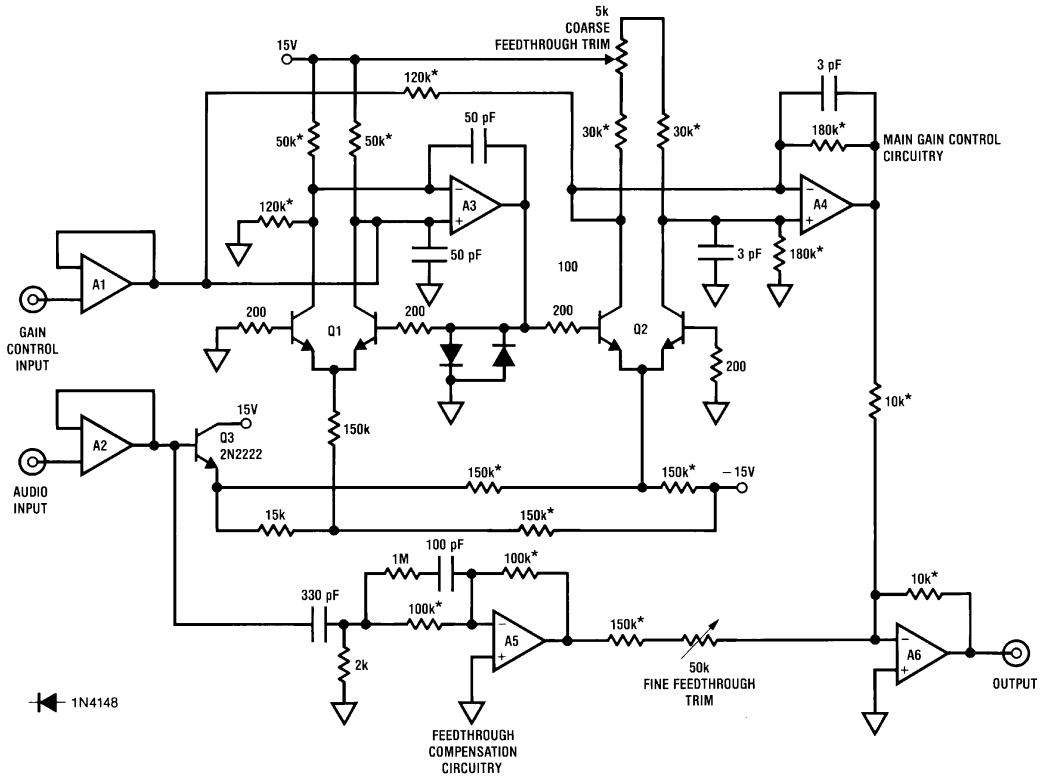
*1% metal film resistor
†Polystyrene
Q2 = 2N2222A
Q5 = 2N2907A
A1, A2 = LF412 dual
Q1, Q3, Q4, Q6 = LM3046 array

FIGURE 1.

The 1M–1.2k divider at A1's "+" input achieves first order compensation for Q1's bulk emitter resistance, aiding exponential conformity at high frequencies. A2 and its associated components are used to "brute-force" stabilize Q1's operating point. Here, Q3, Q4 and A2 form a temperature-control loop that thermally stabilizes the LM3046 array, of which Q1 is a part. Q4's V_{BE} senses array temperature while Q3 acts as the chip's heater. A2 provides servo gain, forcing Q4's V_{BE} to equal the servo temperature setpoint established by the 10k–1k string. Bias stabilization comes from the LM329. The Q6 clamp and the 33Ω emitter resistor determine the maximum power Q3 can dissipate and also prevent servo lock-up during circuit start-up. Q1, operating in this tightly controlled environment, is thus immune from effects of ambient temperature shift.

ULTRA-LOW FEEDTHROUGH VOLTAGE-CONTROLLED AMPLIFIER

A common studio requirement is a voltage-controlled gain amplifier. For recording purposes, it is desirable that, when the gain control channel is brought to 0V, the signal input feedthrough be as low as possible. Standard configurations use analog multipliers to achieve the voltage-controlled gain function. In *Figure 2*, A1–A4, along with Q1–Q3, comprise such a multiplier, which achieves about −65 dB of feedthrough suppression at 10 kHz. In this arrangement, A4 single ends a transconductance type multiplier composed of A3 along with Q1 and Q2. A1 and A2 provide buffered inputs. The −65 dB feedthrough figure is typical for this type of multiplier. A5 and A6 are used to further reduce this feedthrough figure to −84 dB at 20 kHz by a nulling technique. Here, the circuit's audio input is inverted by A5 and then summed at A6 with the main gain control output, which comes from A4. The RC networks at A5's input provide phase shift and frequency response characteristics which are the same as the main gain control multipliers feedthrough characteristics. The amount of feedthrough compensation is adjusted with the 50k potentiometer. In this way, the feedthrough components (and only the feedthrough components) are nulled out and do not appear at A6's output. From 20 Hz to 20 kHz, feedthrough is less than −80 dB. Distortion is inside 0.05%, with a full power bandwidth of 60 kHz. To adjust this circuit, apply a 20 Vp-p sine wave at the audio input and ground the gain control input. Adjust the 5k coarse feedthrough trim for minimum output at A4. Next, adjust the 50k fine feedthrough trim for minimum output at A6. For best performance, this circuit must be rigidly constructed and enclosed in a fully shielded box with attention give to standard low noise grounding techniques. *Figure 4* shows the typical remaining feedthrough at 20 kHz for a 20 Vp-p input. Note that the feedthrough is at least −80 dB down and almost obscured by the circuit noise floor.



*1% film resistor
A1–A2, A3–A4, A5–A6 = LF412 duals
Q1–Q2 = LM394 duals

FIGURE 2.

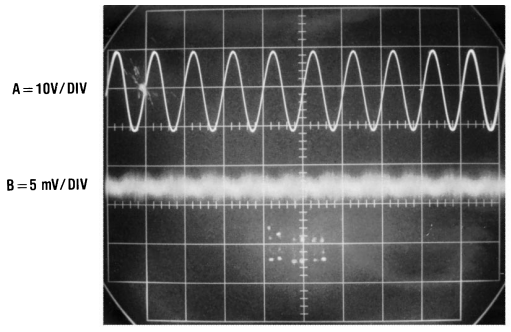
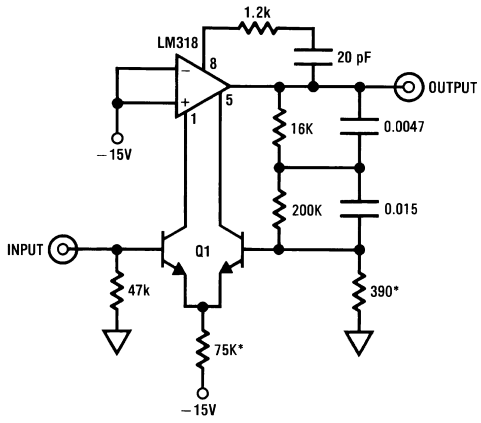


FIGURE 3.



Q1 = LM394

Frequency	Total Harmonic Distortion				
20	<0.002	<0.002	<0.002	<0.002	<0.002
100	<0.002	<0.002	<0.002	<0.002	<0.002
1000	<0.002	<0.002	<0.002	<0.002	<0.002
10000	<0.002	<0.002	<0.002	<0.0025	<0.003
20000	<0.002	<0.002	<0.004	<0.004	<0.007
Output Amplitude (Vrms)	0.03	0.1	0.3	1.0	5.0

FIGURE 4.

ULTRA-LOW NOISE RIAA PREAMPLIFIER

In *Figure 4*, an LM394 is used to replace the input stage of an LM118 high speed operational amplifier to create an ultra-low distortion, low noise RIAA-equalized phono preamplifier. The internal input stage of the LM118 is shut off by tying the unused input to the negative supply. This allows the LM394 to be used in place of the internal input stage, avoiding the loop stability problems created when extra stages are added. The stability problem is especially critical in an RIAA circuit where 100% feedback is used at high frequencies. Performance of this circuit exceeds the ability of most test equipment to measure it. As shown in the accompanying chart, harmonic distortion is below the measurable 0.002% level over most of the operating frequency and amplitude range. Noise referred to a 10 mV input signal is −90 dB down, measuring 0.55 µVrms and 70 pArms in a 20 kHz bandwidth. More importantly, the noise figure is less than 2 dB when the amplifier is used with standard phono cartridges, which have an equivalent wideband (20 kHz) noise of 0.7 µV. Further improvements in amplifier noise characteristics would be of little use because of the noise generated by the cartridge itself. A special test was performed to check for transient intermodulation distortion. 10 kHz and 11 kHz were mixed 1:1 at the input to give an rms output voltage of 2V (input = 200 mV). The resulting 1 kHz intermodulation product measured at the output was 80 µV. This calculates to 0.0004% distortion, quite a low level, considering that the 1 kHz has 14 dB (5:1) gain with respect to the 10 kHz signal in an RIAA circuit. Of special interest also is the use of all DC coupling. This eliminates the overload recovery problems associated with coupling and bypass capacitors. Worst-case DC output offset voltage is about 1V with a cartridge having 1 kΩ DC resistance.

MICROPHONE PREAMPLIFIER

Figure 5 shows a microphone preamplifier which runs from a single 1.5V cell and can be located right at the microphone. Although the LM10 amplifier-reference combination has relatively slow frequency response, performance can be considerably improved by cascading the amplifier and reference amplifier together to form a single overall audio amplifier. The reference, with a 500 kHz unity-gain bandwidth, is used as a preamplifier with a gain of 100. Its output is fed through a gain control potentiometer to the op amp, which is connected for a gain of 10. The combination gives a 60 dB gain with a 10 kHz bandwidth, unloaded, and 5 kHz, loaded with 500Ω. Input impedance is 10 kΩ.

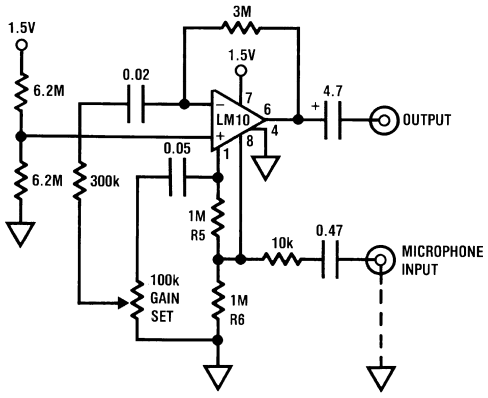


FIGURE 5.

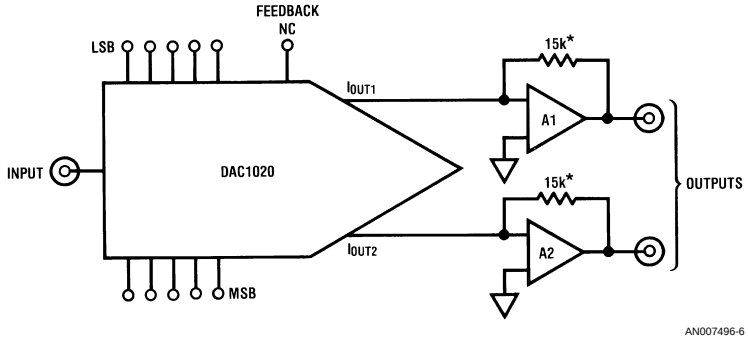
Potentially, using the reference as a preamplifier in this fashion can cause excess noise. However, because the reference voltage is low, the noise contribution which adds root-mean-square, is likewise low. The input noise voltage in this connection is $40\,nV - 50\,nV/\sqrt{Hz}$, approximately equal to that of the op amp.

One point to observe with this connection is that the signal swing at the reference output is strictly limited. It cannot swing much below 150 mV, nor closer than 800 mV to the supply. Further, the bias current at the reference feedback terminal lowers the output quiescent level and generates an uncertainty in this level. These facts limit the maximum feedback resistance (R5) and require that R6 be used to optimize the quiescent operating voltage on the output. Even so, one must consider the fact that limited swing on the preamplifier can reduce maximum output power with low settings on the gain control.

In this design, no DC current flows in the gain control. This is perhaps an arbitrary rule, designed to insure long life with noise-free operation. If violations of this rule are acceptable, R5 can be used as the gain control with only the bias current for the reference amplifier ($<$75 nA) flowing through the wiper. This simplifies the circuit and gives more leeway in getting sufficient output swing from the preamplifier.

DIGITALLY PROGRAMMABLE PANNER-ATTENUATOR

Figure 6 shows a simple, effective way to use a multiplying CMOS D-A converter to steer or pan an audio signal between two channels. In this circuit, the current outputs of the DAC1020, which are complementary, each feed a current-to-voltage amplifier. The amplifiers will have complementary voltage outputs, the amplitude of which will depend upon the address code to the DAC's digital inputs. *Figure 7* shows the amplifier outputs for a ramp-count code applied to the DAC digital inputs. The 1.5 kHz input appears in complementary amplitude-modulated form at the amplifier outputs. The normal feedback connection to the DAC is not used in this circuit. The use of discrete feedback resistors facilitates gain matching in the output channels, although each amplifier will have a ≈300 ppm/°C gain drift due to mismatch between the internal DAC ladder resistors and the discrete feedback resistors. In almost all cases, this small error is acceptable, although two DACs digitally addressed in complementary fashion could be used to totally eliminate gain error.



*1% film resistor A1, A2 = LF412 dual

FIGURE 6.

DIGITALLY PROGRAMMABLE BANDPASS FILTER

Figure 8 shows a way to construct a digitally programmable first order bandpass filter. The multiplying DAC's function is to control cut-off frequency by controlling the gain of the A3–A6 integrators, which has the effect of varying the integrators' capacitors. A1–A3 and their associated DAC1020 form a filter whose high-pass output is taken at A1 and fed to an identical circuit composed of A4–A6 and another DAC. The output of A6 is a low-pass function and the final circuit output. The respective high-pass and low-pass cut-off frequencies are programmed with the DAC's digital inputs. For the component values shown, the audio range is covered.

REFERENCES

Application Guide to CMOS Multiplying D-A Converters, Analog Devices, Inc. 1978

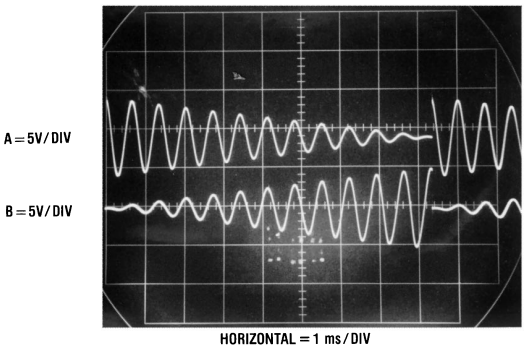
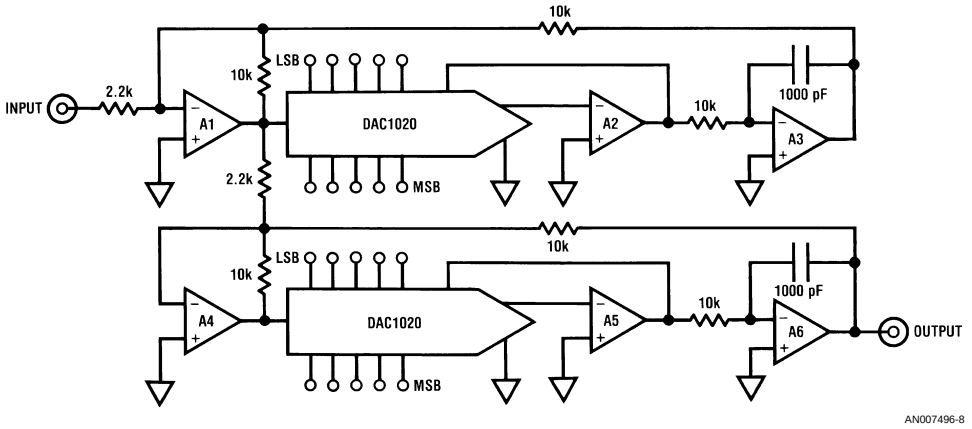


FIGURE 7.



A1, A2 = LF412 dual
A3, A4 = LF412 dual
A5, A6 = LF412 dual

FIGURE 8.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Signal Conditioning for Sophisticated Transducers

National Semiconductor
Application Note 301
January 1982

A substantial amount of information is available on signal conditioning for common transducers. Fortunately, most of these devices, which are used to sense common physical parameters, are relatively easy to signal condition. Further, most transducer-based measurement requirements are well served by standard transducers and signal conditioning techniques.

Some situations, however, require sophisticated transduction techniques with their attendant special signal conditioning requirements. This application note details signal conditioning and applications information for a diverse group of sophisticated and unusual tranducers. Because these devices are unusual or somewhat difficult to signal condition, relatively little material has appeared on how to design circuitry for them. Many of these devices permit measurements which cannot be accomplished in any other way. For this reason it is worthwhile to have a basic familiarity with their capabilities and what is required to signal condition them. The circuits shown are intended as instructive examples only, although each one has been constructed and tested. Every individual transducer application has a set of specifications and constraints which will require modification or revision of the circuits presented. Sources of additional information which feature more vigorous treatment are presented in a reference section at the end of the application note.

Photomultiplier Tube (PMT)

Perhaps the most versatile light detector available is the photomultiplier tube (PMT). These sensors allow single photon detection, sub-nanosecond rise time, bandwidths approaching 1 GHz and linearity of response over a range of 10^7. In addition, they feature extremely low noise, stable characteristics and very long life. *Figure 1* details a typical PMT along with a signal conditioning circuit. The tube is composed of a photosensitive cathode, an anode, a focusing electrode and ten dynode stages. In operation, the photocathode, which is high voltage biased with respect to the dynodes, emits photoelectrons when it is struck by light. These are focused into a beam and directed to the first dynode stage by the focus electrode. These arriving electrons impinge on the dynode, causing secondary emission to occur. As a result, a greater number of electrons leave the dynode and are then directed to the second dynode. In this fashion, a number (e.g.,10) of dynode stages are used to achieve overall gains of 10^6 to 10^8. The electrons from the final dynode are collected by the anode, which provides the output current of the tube. In contrast to other vacuum tubes, the PMT does not use a filament to thermionically generate electrons. Instead, the photocathode, in combination with incident light, initiates the electrons. The absence of a filament means there are no degradation, heat or outgassing problems and the life of a PMT is very long.

Signal conditioning involves generating a stable high voltage supply and accomplishing a low noise current-to-voltage conversion at the anode. In this example, a DC-DC converter is used to supply the dynode potentials to the tube. The supply is stabilized by the LF412 amplifier which drives the Q3-Q5 combination to complete a feedback loop around the Q1-Q2 driven transformer. The LM329 provides a stable servo reference. In general, the regulation of a PMT supply should be at least ten times greater than the required measurement gain stability because of the relationship between a PMT's gain slope and the high voltage applied. The cathode and dynodes are biased from the high voltage supply via divider resistors. The resistors distribute the dynode potentials in proportion to a ratio which is specified for each tube type. To prevent non-linear response, the current through the divider string should be at least ten times the maximum expected current out of the tube. Some high speed pulse applications can generate transient high tube currents which may require the small capacitors shown in dashed lines. The anode is the tube output and appears as an almost ideal current source. The LF412 amplifier performs a current-to-voltage conversion with the 1 MΩ resistor setting the output scale factor.

The PMT's combination of high speed and extreme sensitivity suits it to a variety of difficult light measurement chores. The remarkable photograph of *Figure 2* shows the actual rise and fall time characteristics (inverted) of a fast pulse of light produced by an LED. This photo was taken with a high speed PMT which was terminated directly into a 1 GHz bandwidth, 50Ω sampling oscilloscope.

Another PMT application exchanges speed for sensitivity in a nuclear medical instrument, the Gamma camera.

The Gamma camera operates by using the scintillation properties of special crystals which are placed in front of an array of PMTs. Small quantities of radioactive isotopes are introduced into the patient either by oral ingestion or injection. Specific isotopes collect at certain organs within the body. As the radioactive isotopes decay, gamma rays are emitted from the isotope concentration area. These rays are collimated by a lead plate containing many small holes which forms the front of the camera (*Figure 3*). This collimator allows only those rays which are at right angles to pass through the plate. The rest are absorbed in the lead. In this fashion the geometric shape of the gamma source is preserved and is presented to the scintillation crystal. The array of PMTs is located behind the crystal. The individual tubes respond to any given scintillation anywhere in the crystal with a distribution of signal strengths. This distribution is used by a processor to determine the precise point of scintillation in the crystal. Each of these scantillation locations is recorded on a CRT. After a length of time, this counting-integration process produces a picture of the organ on the CRT. *Figure 4* shows 7 such pictures of a pair of human lungs, taken 30 seconds apart over a 150 second period. In photo A, the administered radioactive isotope begins to collect in the lungs. In photo B, the lungs are saturated. During photos C, D, E, F and G, the isotope progressively decays. Normally, human lungs will clear after 120 seconds. This particular sequence shows evidence of an obstructive pulmonary disease which is most pronounced in the lower right lung.

Photomultiplier Tube (PMT) (Continued)

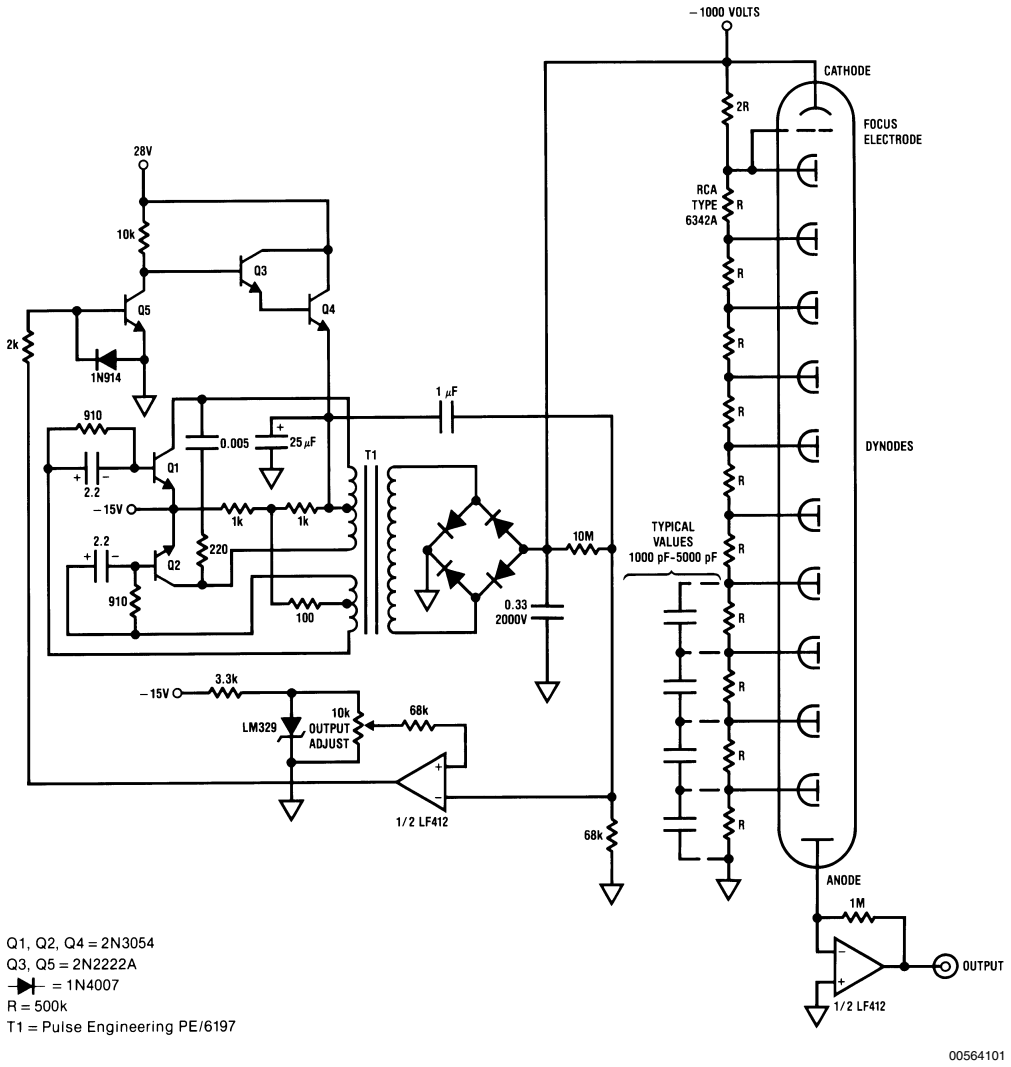


FIGURE 1.

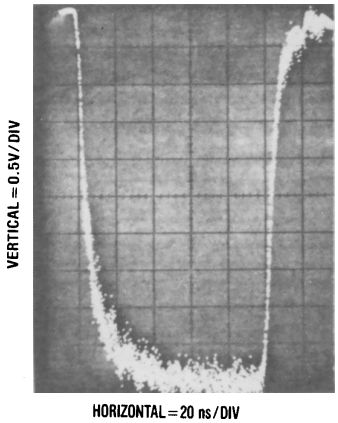


FIGURE 2.

Photomultiplier Tube (PMT)

(Continued)

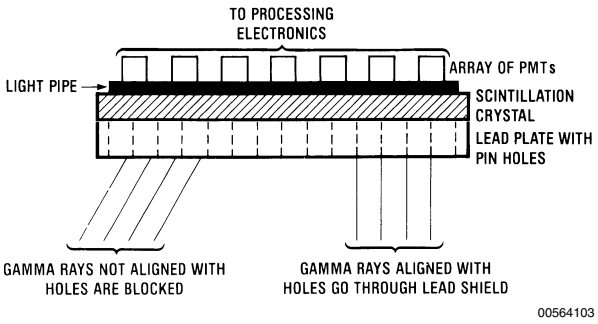


FIGURE 3.

Pyroelectric Detector

The pyroelectric detector represents another class of sophisticated photodetector. These ceramic-based radiation detectors feature an extraordinary light sensitivity range from microwatts to watts with excellent linearity. Their bandwidth is flat from the ultraviolet to the far infrared. Response is sub-nanosecond and the devices may be operated at room temperature; no cooling is required. A major difficulty and source of confusion with signal conditioning pyroelectrics is that they do not respond at DC. This limitation, which is in keeping with all ceramic-based transducers, is surmounted by using a light chopper in front of the detector. In this fashion, DC light inputs to the detector appear as a modulated carrier. These devices are used in industrial temperature measurement, spectroscopy and laser power meters. They are also used to measure high speed laser pulse characteristics.

For signal conditioning purposes, pyroelectrics can be modeled as either a current source with parallel capacitance or a voltage source with series capacitance. Because there is no resistive component, there is no resistive Johnson noise. *Figure 5a* shows a simple voltage mode set-up which can be used for fast pulses of high energy. In this circuit, the detector is terminated directly into a high speed 50Ω oscilloscope. In *Figure 5b*, a slower detector terminates into 1 MΩ and is unloaded by the LH0052 low bias FET amplifier. For

response time much longer than a few milliseconds, the optical chopper provides a modulated light signal to the detector. The amplifier output may be rectified to recover the DC component of the signal. *Figure 5c* shows a current mode signal conditioning circuit. The optical chopper is retained, but the detector is loaded directly into the summing junction of a low bias op amp composed of an LF411 and a pair of sub-picoamp bias FETs. The low bias current allows low energy light measurement.

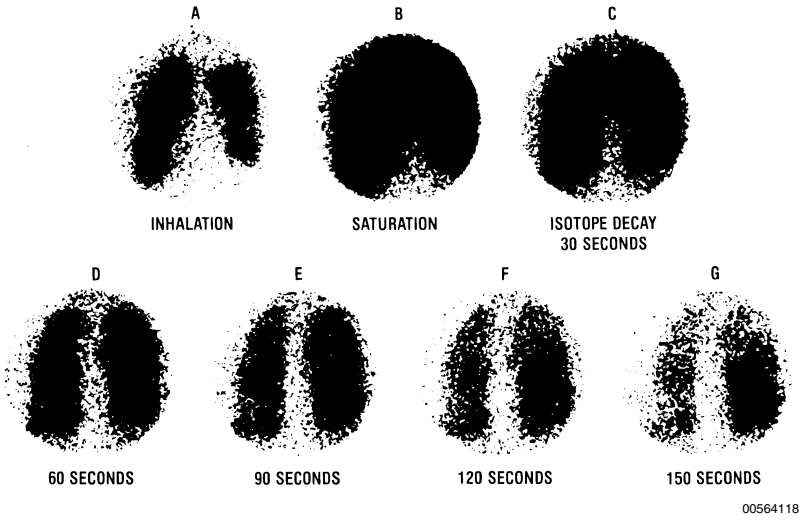
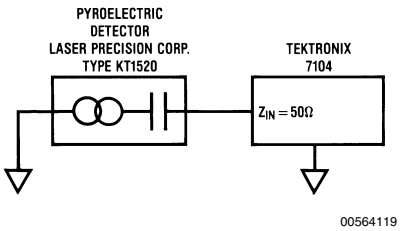
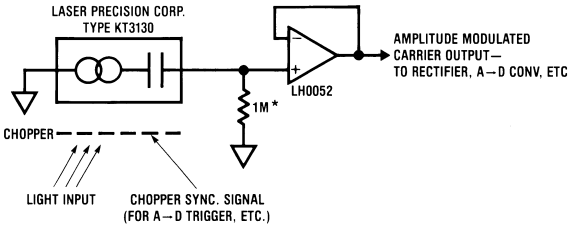


FIGURE 4.

Pyroelectric Detector (Continued)

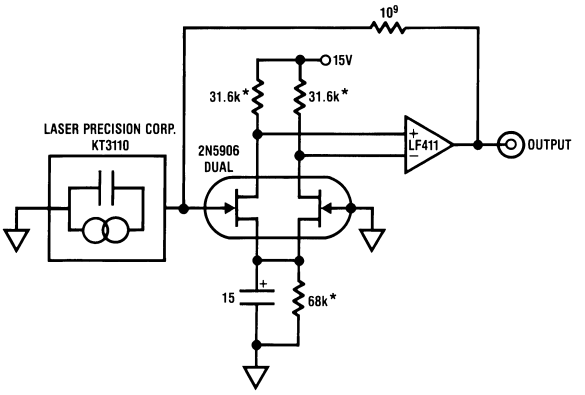


a



*TRW MAR 6 resistor, 1%

b



*TRW MAR 6 resistor, 1%

c

FIGURE 5.

Piezoelectric Ultrasonic Resonators

Piezoelectric ultrasonic tranducers are generically related to pyroelectrics in that they are also ceramic-based. These devices are used for both generation and reception of narrow band ultrasonic information. The characteristic resonance of these transducers, in a similar fashion to quartz crystals, is extremely narrow, allowing high Q, noise rejecting systems to be built around them. As transmitters, they are often driven very hard by steps several hundred volts high at low duty cycles. This permits substantial ultrasonic power to be generated and eases the burden of the receiver in the system (which could be the same transducer as the transmitter). Ultrasonic resonators are used in a wide variety of applications including liquid level detection, intrusion alarms, automatic camera focusing, cardiac ultrasonic profiling (echocardiography) and distance measuring equipment. *Figure 6* shows a signal conditioning circuit which capitalizes on the high Q, noise rejection characteristics and fast response of ultrasonic transducers to accomplish a difficult thermal measurement. This circuit is similar to a type developed to measure high speed temperature shifts in a gas medium.

In contrast to almost all other temperature sensors, it does not rely on its sensing element to come into thermal equality with the measurand. Instead, the relationship between the speed of sound and the temperature of the medium in which the sound is propagating is utilized to determine temperature. The speed of response is therefore very fast and the measurement is also non-invasive. The relationship between the speed of sound in any medium and temperature may be described by equations. As an example, the relationship in dry air is:

$$C = 331.5 \sqrt{\frac{T}{273}} \text{ meters/second,}$$

where C = speed of sound.

For any given value of C the absolute temperature is:

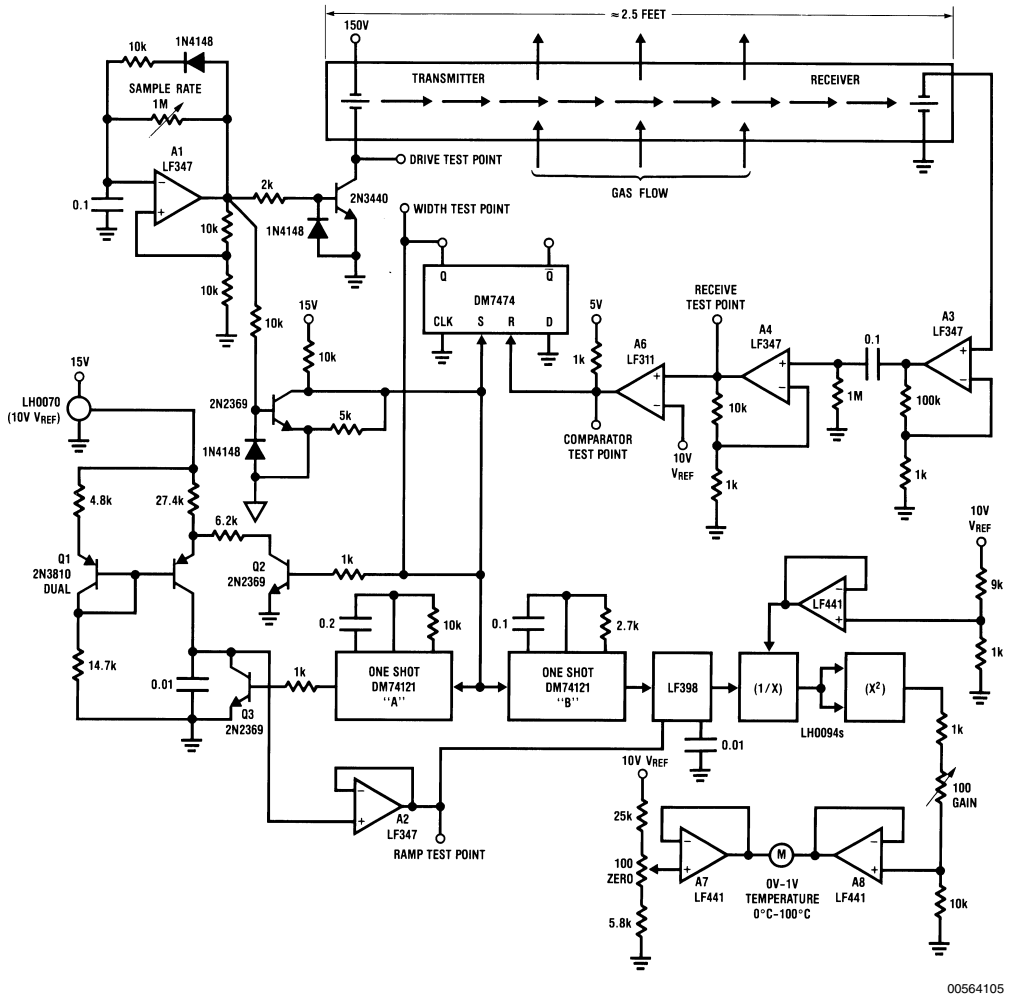
$$T = \frac{273}{(331.5)^2} \times C^2.$$

It is clear that because sound speed and the medium in which it travels have a predictable relationship, a temperature transducer can be composed of the medium itself. If the characteristics of the medium can be defined (e.g., its make up) the transmit time of a sonic pulse through it can be used to determine its temperature. If narrow band ultrasonic transducers are used, they will reject sonic noise that may be occurring in the medium.

Piezoelectric Ultrasonic Resonators (Continued)

A1 periodically generates a short pulse (waveform A, *Figure 7*) that drives the 2N3440 into conduction, forcing the ultrasonic 40 kHz transducer to emit a short burst at its resonant frequency. The 150V pulse amplitude allows substantial ultrasonic energy to be coupled into the medium. As this pulse is generated, the DM7474 flip-flop is set low (waveform C, *Figure 7*). After a length of time, determined by the distance between the ultrasonic transducers and the temperature of the gas, the sonic pulse arrives at the receiving transducer and is amplified by A3 and A4 (A4's output is waveform B, *Figure 7*). This amplified output triggers A6, which resets the flip-flop high. During the time the flip-flop was low, the 2N3810 current source was allowed to charge the 0.01 µF capacitor (waveform D, *Figure 7*). When the flip-flop is reset high, Q2 comes on and the charging ceases. The A2 follower output sits at the capacitor's DC potential, which is related to the sonic transit time in the gas stream. The LF398 sample-hold is triggered by the "B" DM74121 one shot and samples A2's output. The LF398's output feeds two LH0094 multi-function non-linear converters which are arranged to linearize the speed of sound versus temperature relationship. The output of this configuration is the gas temperature which is displayed on the meter. Gain and zero trims are provided via the A7 and A8 networks. When A1 issues another pulse, the DM74121 "A" one shot resets the 0.01 µF capacitor to 0V and the entire process repeats.

It is worth noting that no bandwidth limiting of any kind is employed at the A3-A4 receiver despite their compound gain of 1000. This would seem to invite noise sensitivity problems in a sonic system, but the high Q ultrasonic transducer provides almost ideal noise rejection. *Figure 8* shows the amplified output of the received pulse superimposed on the output of a boardband microphone placed in the sonic path. Boardband noise 100 dB greater than the 40 kHz pulse is pumped into the sonic path. Virtually complete noise rejection occurs and signal integrity is maintained.



00564105

Ultrasonic transducers = Massa MK-109

FIGURE 6.

Piezoelectric Ultrasonic Resonators (Continued)

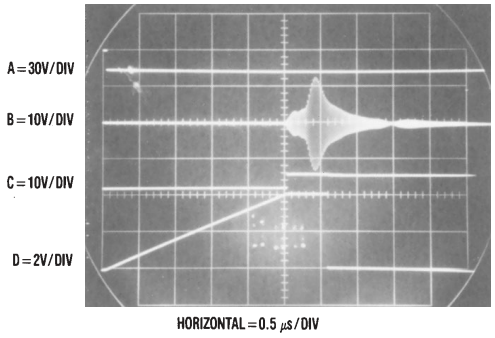


FIGURE 7.

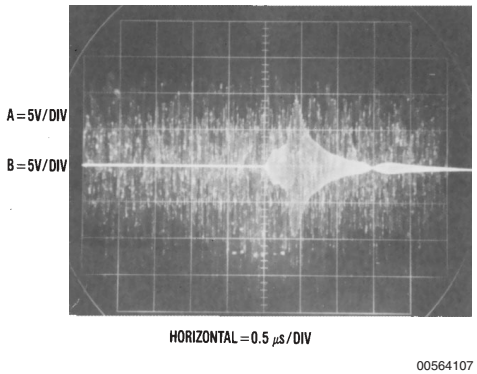


FIGURE 8.

Piezoelectric Accelerometer

Another piezoelectric-based transducer is the piezoelectric accelerometer. These devices utilize the property of certain ceramic materials to produce charge when subject to mechanical excitation. These accelerometers use a mass coupled to the piezoelectric element to generate a force on the element in response to an acceleration's frequency and amplitude. Calibration and sensitivity can be varied by selecting the piezoelectric materal and altering the configuration and amount of the mass. The best way to signal condition these devices is to employ an amplifier configuration that is directly sensitive to their charge-type output. Charge amplifiers use low bias current op amps with capacitive feedback. Output voltage will depend upon the charge out of the accelerometer which is related to the applied acceleration.

In *Figure 9*, the transducer looks directly into the ground potential summing junction of an op amp. Because of this, there is no voltage difference between the interconnecting cable center conductor and its shield. This eliminates cable capacitance effects on the transducer output and allows long cable runs. It is advisable to use cable specified for low triboelectric charge effects for best performance, although this is usually only a factor with relatively low output devices. The $10^{11}\Omega$ resistor provides a DC feedback path, while the variable capacitor sets the sensitivity of the charge-to-voltage conversion. When the accelerometer shown is mounted on a hand-held voltmeter and dropped on the floor, the instantaneous acceleration to which the voltmeter is subjected can be determined. In *Figure 10*, the stored trace display shows an instantaneous force of almost 1000G with smaller forces generated as the voltmeter bounces 3 times over 60 ms. (It is recommended that this experiment be performed with a borrowed voltmeter.)

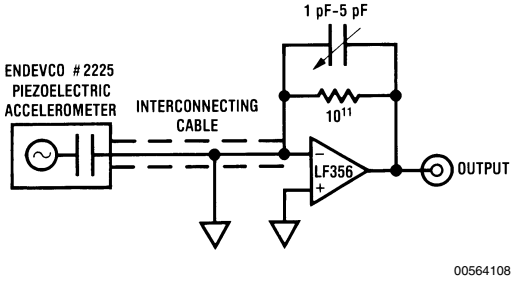


FIGURE 9.

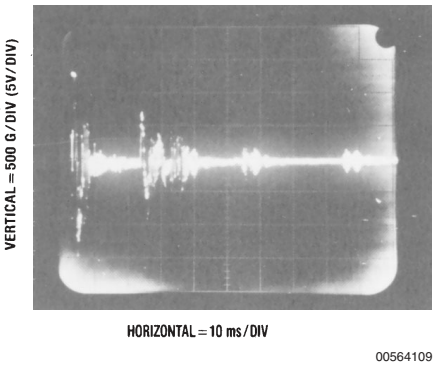


FIGURE 10.

Linear Variable Differential Transformer (LVDT)

The linear variable differential transformer (LVDT) offers zero-friction position sensing with good precision. Although potentiometers are easy to signal condition and allow high precision they cannot match the nearly infinite life and zero-friction of the LVDT approach. LVDTs are available in both rotary and stroke mechanical configurations. The LVDT is basically a transformer (*Figure 11*) with a movable core. The primary is driven with a sine wave which is usually amplitude stabilized. The two matched secondaries are connected in series-opposed fashion. When the movable core is positioned in the magnetic (and usually geometric) center of the transformer, the secondaries' outputs cancel and no net secondary voltage appears. This is called the null position.

Linear Variable Differential Transformer (LVDT) (Continued)

As the core is moved from null, the differential in flux coupled to the two secondaries produces a net voltage difference across them.

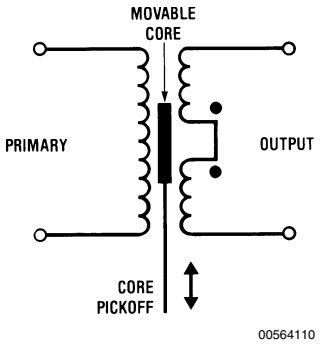


FIGURE 11.

This is the output of transducer. Good transducer performance (e.g., null cancellation characteristics, linearity, etc.) requires manufacturer attention to winding techniques, magnetic shielding, material choices and other issues. Rectifying and filtering the output signal will yield only amplitude information. Optimum signal conditioning requires a phase sensitive demodulation scheme. This gives the amplitude and also polarity information necessary to determine on which side of null the LVDT core is.

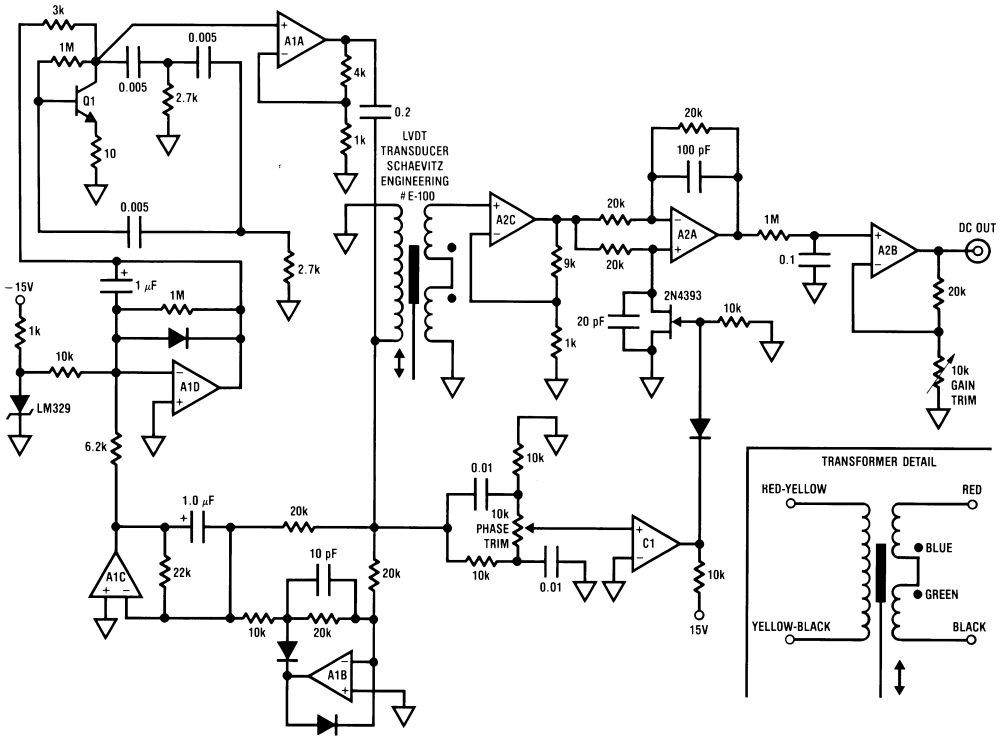
Figure 12 shows a circuit which does this. Waveforms of operation are given in *Figure 13*. In this circuit, Q1 and its associated components from a phase shift oscillator which runs at 2.5 kHz, the manufacturer's specified transducer operating frequency. A1A amplifies and buffers Q1's output and drives the LVDT (waveform A, *Figure 13*). Since the transducer's output will vary with drive level, feedback is used to stabilize the 2.5 kHz amplitude. A1C and A1D full wave rectify a sample of the drive waveform. A1C's filtered output is applied to A1D, a servo amplifier. A1D compares A1C's output to the LM329 reference and drives the Q1 oscillator to complete an amplitude stabilization loop. The LVDT's output is amplified by A2C and fed to A2A. A2A is a unity gain ampilifer whose sign alternates between "+" and "–". Synchronous switching for A2A comes from C1 (waveform B, *Figure 13*), which is driven by the modulation sine wave output via a phase shift network. The phase trim network compensates phase shift in the LVDT and ensures that C1 switches at the zero crossings relative to A2A's output. When C1's output is low, the 2N4393 FET is off and A2A's positive input (waveform C, *Figure 13*) receives signal. When the sine wave reverses polarity, C1's output goes high, turning on the FET, which grounds A2A's "+" input. Under these conditions A2A is always switching its amplification's sign from "+" to "–" in synchronism with the sine wave output from the LVDT. A2A's phase sensitive output, in this case positive, appears in trace D, *Figure 13*. A2B provides a scaled and filtered DC output. To trim the circuit, set the LVDT to at least ½ physical displacement and adjust the phase trim for maximum output indication. Next, adjust the gain trim for the desired circuit output at full-scale LVDT displacement.

Force-Balanced Pendulous Accelerometer

The operating principles of the LVDT are applied in the force-balanced pendulous accelerometer. Transducers of this type feature wide dynamic range, high linearity and very high accuracy. *Figure 14* shows one form of a conceptual force-balanced pendulous accelerometer. The device operates by using an LVDT-type pick-off to determine the position of the pendulum. The DC output of the LVDT is fed to a servo amplifier which drives the torque coil. The magnetic output of the torque coil completes a servo loop around the pendulum, forcing it to become immobile. Because the torque coil's field can attract only the pendulum, a second bias coil provides a steady force for the torque coil to work against. When an input acceleration occurs along the sensitive axis, the servo applies the necessary current to the torque coil to keep the pendulum from moving. The amount of current required is directly proportional to the value of the input acceleration. Because the pendulum never moves, transducer linearity and accuracy can be very high. In addition, wide dynamic range is possible. Force-balanced accelerometers are widely applied in aircraft inertial guidance systems, aerospace applications, seismic monitoring, shock and vibration studies, oil drilling platform stabilization and similar applications. In recent years these accelerometers have become available in complete signal conditioned packages, although there are a number of applications where it is desirable to independently signal condition the transducer. *Figure 15* shows a detailed schematic of such signal conditioning. The pick-off circuitry is similar to the LVDT shown in *Figure 12* and does not require further comment. The bias coil is driven by the LH0002 boosted LF347 (A1A) which is in a current sensing feedback configuration. For the accelerometer shown, the manufacturer specifies

60 mA of bias coil current. Torque pulses are applied by servo amplifier A3B, which is biased from the LVDT demodulator output. The output of the circuit is taken across the 100Ω resistor in series with the torque coil. Servo gain is set at A3B while damping for the loop is provided by the 1 µF unit in A3B's feedback loop. In addition, accelerometer damping is controlled by stabilizing the temperature of the mechanical assembly. This is accomplished by A3C, which is set up as a simple on-off temperature controller. The interior of the accelerometer is filled at manufacture with a liquid whose viscosity provides appropriate damping characteristics at a specified temperature, in this case 180˚F. Accelerometers of this type routinely yield 100ppm accuracy from ranges of 20 mG to 100G.

Force-Balanced Pendulous Accelerometer (Continued)



00564125

= N914 = N914

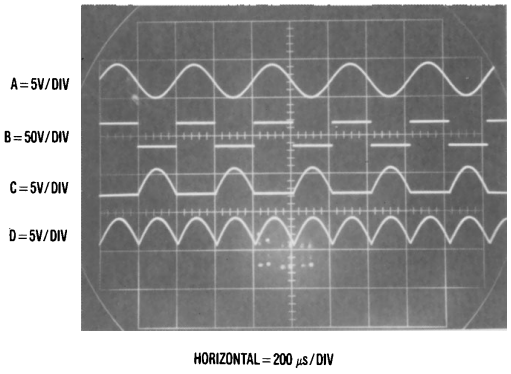
A1 = LF347

A2 = LF347

C1 = LM311

Q1 = 2N2222

FIGURE 12.



00564112

FIGURE 13.

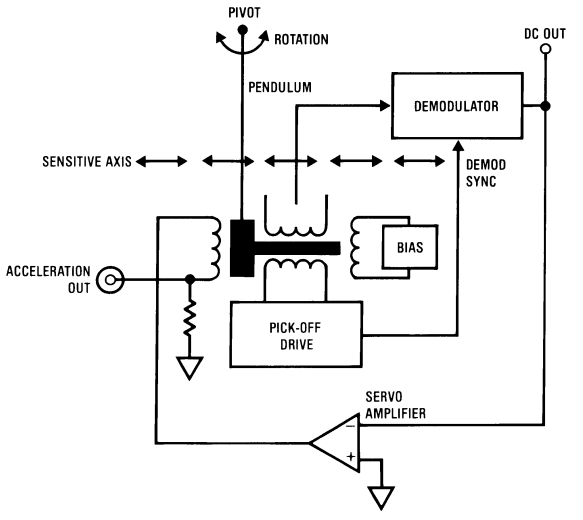


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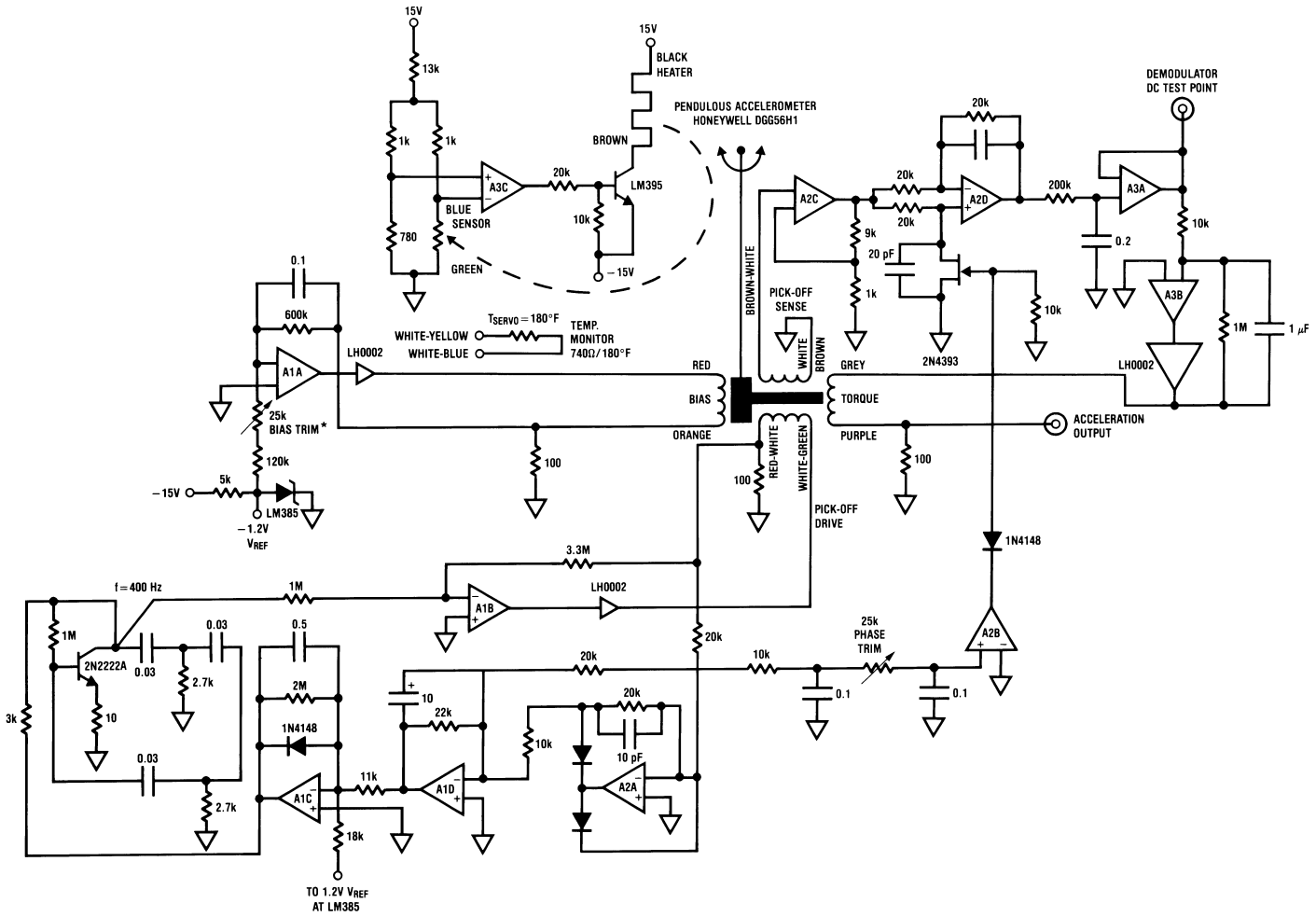
FIGURE 14.

Force-Balanced Pendulous Accelerometer (Continued)



00564113

*Adjust to 60 mA bias loop current

A1, A2, A3 = LF347

FIGURE 15.

Rate Gyro

The rate gyro is another form of high performance inertial measuring transducer. It consists of an electrically driven gyroscope with a captive spin axis. Normal gyros are free of restraint and maintain position when moved. The rate gyro is held captive and forced to move with the physical input. By measuring the force generated as the gyro opposes its restraining mechanism, rate-of-angle change information can be deduced. *Figure 16* shows signal conditioning for a typical rate gyro. An LVDT-type pick-off is used and synchronous demodulation-type circuitry very similar to *Figure 15* is employed. Note the high voltage drive to the gyro motor (26 Vrms) supplied by the boosted LM143. Because of their long life and high precision rate, gyros are frequently employed in inertial guidance systems, drilling platform stabilization systems and other critical applications.

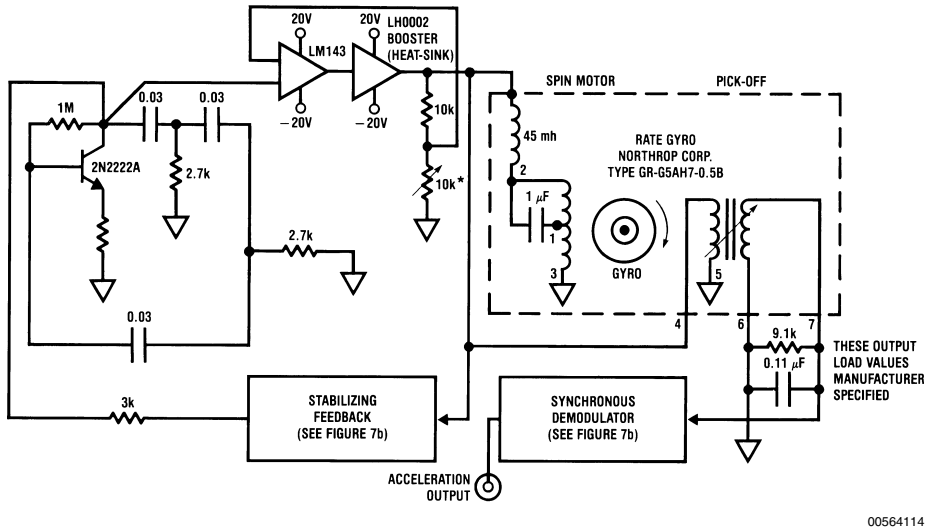
Flux Gate

A flux gate transducer converts an external magnetic field (such as that of the earth's) into an electric output. A variety of flux gate configurations exist, the simplest being a piece of easily saturable ferrous material wrapped around a cylinder (*Figure 17*). An alternating current is passed along the axis of the cylinder which periodically saturates the material, first clockwise and then counter-clockwise.

A pick-up winding is wrapped around the cylinder. While the ferrous material is between saturation extremes, it maintains a certain average permeability. While in saturation, this permeability (μ = dB/dH) becomes one (an increase in driving field H produces the same increase in flux B). If there is no component of magnetic field along the axis of the cylinder, the flux change seen by the pick-up winding is zero since the excitation flux is normal to the axis of the winding. If, on the other hand, a field component is present along the cylindrical axis, then each time the ferrous material goes from one saturation extreme to the other it produces a pulse output on the signal pick-up winding that is proportional to the external magnetic field and the average permeability of the material. Since this saturation-to-saturation transition occurs twice each excitation period (fundamental), the frequency of signal out of the pick-up windings is twice the excitation frequency.

These transducers find use in metal detectors, submarine locating gear, electronic compasses, oil surveys, and other areas where measurement of the strength or locally caused disturbance of the earth's magnetic field is of interest. Flux gate transducers are capable of measuring variations in the earth's magnetic field within one gamma (10^{-5} oersteds). Two axis flux gates can be used to construct an electronic compass. More recent flux gate design employs a core-shaped transducer, which is essentially two cylinder types bent together at the ends to form a closed magnetic path. This permits lower driving power and allows the use of commercially available tape-wound cores to be used to construct the transducer. A simple flux gate and its signal conditioning appears in *Figure 18*. Excitation to the flux gate is provided by the complementary signal output from the CD4047s. The transistor drives a transformer which is tuned for resonance. This converts the square wave output of the CMOS oscillator into a sinusoidal waveform. This sinusoidal excitation voltage is then converted by the transformer into a high level AC drive current at the excitation frequency which is used to drive the sensor.

The output of the sensor signal winding is an AC signal at twice the excitation frequency and is directly proportional in amplitude to the external axial magnetic field. This second-harmonic of the excitation frequency is then phase detected with a circuit similar to the demodulators shown in *Figures 12, 15*. A portion of the DC output signal may be fed back (shown in dashed lines) to the signal winding to provide a closed loop negative feedback system. This feedback signal produces a field in the sensor which opposes the signal being measured. The high forward gain of the signal channel along with the closed loop negative feedback system ensure good stability and linearity of the output signal.



*Adjust for 26 Vrms output

FIGURE 16.

Flux Gate (Continued)

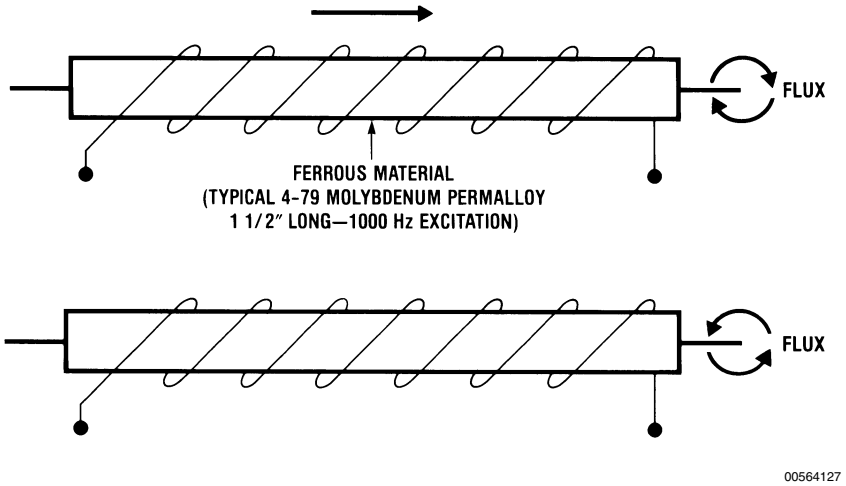


FIGURE 17.

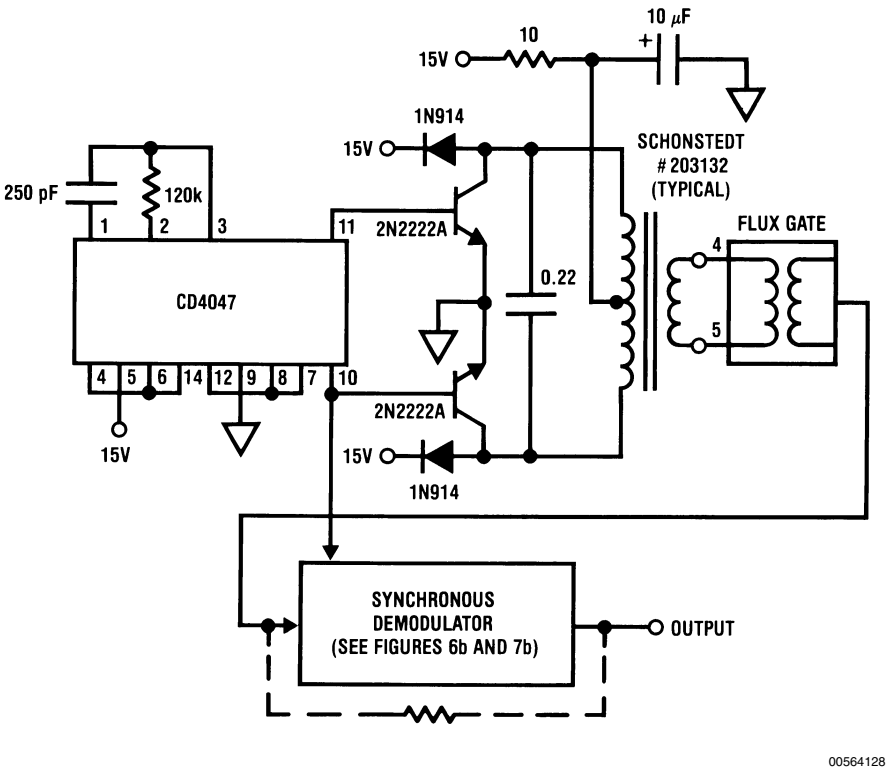


FIGURE 18.

Low Power Strain Gauge Bridge Signal Conditioning

In most cases, strain gauge bridges do not require unusual signal conditioning techniques. When low power consumption is necessary, special circuitry must be employed to eliminate the high current consumption of strain gauge-based transducers. Normally, the 350Ω input impedance of these devices requires substantial drive to achieve a usable output. For a typical 10V drive level, 35 mA are required; hardly compatible with low power or battery operation. The circuit shown in *Figure 19* provides complete signal conditioning for strain gauge transducers while using only 1.8 mA average current out of a 9V transistor radio battery. The output of the circuit is an 8-bit word produced by an A-D converter. The key to achieving low power operation is to pulse power at low duty cycles to the transducer and its signal conditioning circuitry. In *Figure 20*, A1A oscillates at

Low Power Strain Gauge Bridge Signal Conditioning (Continued)

about 1 Hz. Each time A1A's output goes high (waveform A, *Figure 20*), Q1 comes on, turning on the LM330 5V regulator. This places 5V at Q2's collector. Concurrently, A1B amplifies the output of the pulse-edge shaping network at its input and provides voltage overdrive to emitter-follower Q2, forcing it into saturation. This causes an edge shaped pulse to be applied to the strain gauge bridge (waveform B, *Figure 20*). This pulse is also used to power A2 and the ADC0804 A-D converter. The slow edge shaping limits the DV/DT seen by the transducer as it is pulsed. This eliminates possible deleterious effects on transducer performance over time, due to the continuous abrupt step functions being applied. The transducer bridge output is monitored by the A2 quad, which serves as a differential input (A2A and A2B), single-ended output (A2C and A2D) amplifier. A2D's output (waveform C, *Figure 20*) feeds the ADC0804 A-D converter. The A-D is triggered by a delayed pulse generated by the A1C and A1D pair (waveform D, *Figure 20*). This pulse is positioned so that it occurs after A2D's output has settled to final value. To calibrate the circuit, apply zero physical load to the transducer shown and adjust the zero trim so the A-D converter is just below indicating 1 LSB output. Next, apply (or electrically simulate) 10,000 lbs. and adjust the gain trim for a full output code at the A-D converter.

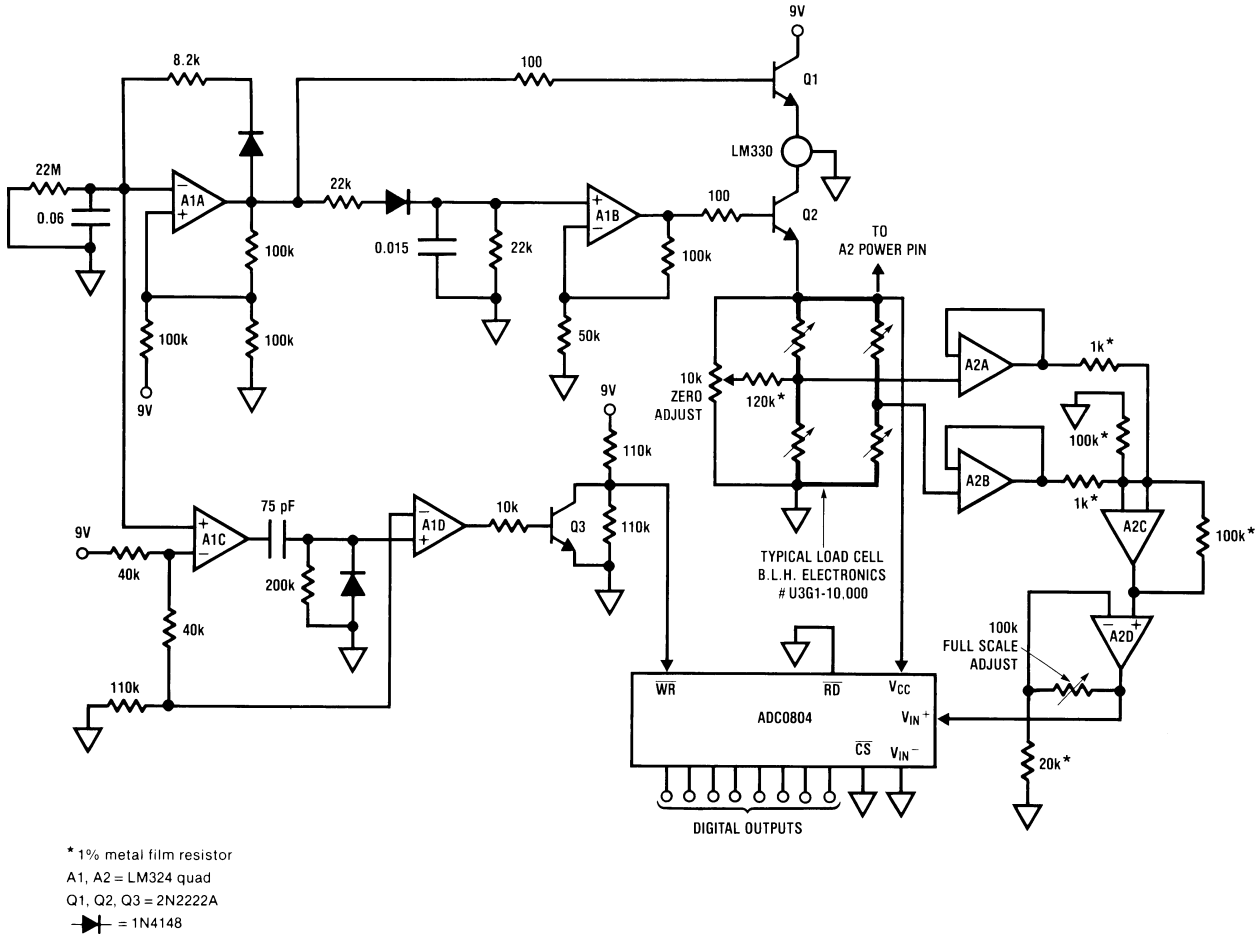


FIGURE 19.

Low Power Strain Gauge Bridge Signal Conditioning (Continued)

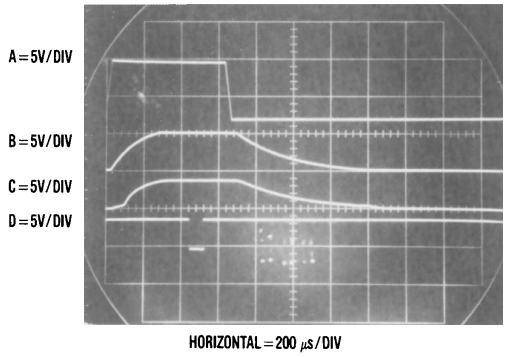


FIGURE 20.

References

RCA Photomultiplier Handbook; RCA Electro-Optics Division; Lancaster, PA

The Pyroelectric Thermometer: A Sensor for Measuring Extremely Small Temperature Changes; S.B. Lang, McGill University; 1971 International Symposium on Temperature; Washington D.C.

A User's Guide to Pyroelectric Detection; Electro-Optical Systems Design; November 1978

Pyroelectric Detectors and Detection Systems; Laser Precision Corp.; Utica, NY

Multiplier Application Guide; Analog Devices Inc.; Norwood, MA; (pages 11–13)

Ultra-Sonic Thermometry using Pulse Techniques; Lynnworth and Carnevale; Panametrics Corporation; Waltham, MA

Handbook of Measurement and Control; Schaevitz Engineering; Pennsauken, NJ

Self-Balancing Flux Gate Magnetometers; William Geyger; AIEE Transactions, Vol. 77, May 1958; Communication and Electronics

A Low Cost Precision Inertial Grade Accelerometer; H.D. Morris; Systron-Donner Corp.; DGON Symposium on Gyro Technology, 1976

Short Form Catalog; ENDEVCO Corporation; San Juan Capistrano, CA

Bulletin 31, MK109 Ultrasonic Transducer; Massa Corporation; Hungham, MA

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Northrop Corporation, Precision Products Division

RCA Electro-Optics Division

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Theory and Applications of Logarithmic Amplifiers

National Semiconductor
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A number of instrumentation applications can benefit from the use of logarithmic or exponential signal processing techniques. The design and use of logarithmic/exponential circuits are often associated with involved temperature compensation requirements and difficult to stabilize feedback loops. For these considerations and others, designers tend to avoid these circuits. Hybrid and modular logarithmic/exponential devices are available commercially, but are quite expensive and earn very high profits for their manufacturers.

The theory and construction of these circuits are actually readily understood. *Figure 1* shows an amplifier which provides a logarithmic output for a linear input current or voltage. For input currents, the circuit will maintain 1% logarithmic conformity over almost 6 decades of operation. This circuit is based, as are most logarithmic circuits, on the inherent logarithmic relationship between collector current and V_{BE} in bipolar transistors. Q1A functions as the logging transistor in this circuit and is enclosed within A1A's feedback loop, which includes the 15.7 kΩ-1 kΩ divider. The circuit's input will force A1A's output to achieve whatever value is required to maintain its summing junction at zero potential. Because Q1A's response is dictated by the logarithmic relationship between collector current and V_{BE}, the output of A1A will be the logarithm of the circuit input. A1B and Q1B provide compensation for Q1A's V_{BE} temperature dependence. A1B servos Q1B's collector current to equal the 10 µA current established by the LM329 reference diode and the 700 kΩ resistor. Since Q1B's collector current cannot vary, its V_{BE} is also fixed. Under these conditions only Q1A's V_{BE} will be affected by the circuit's input. The circuit's output is a function of:

$$E_{OUT} = \frac{15.7k + 1k}{1k}(V_{BE}Q1B - V_{BE}Q1A)$$

For Q1A and Q1B operating at different collector currents, the V_{BE} difference is:

$$\Delta V_{BE} = \frac{KT}{q} \log_e \frac{I_{CQ1A}}{I_{CQ1B}}$$

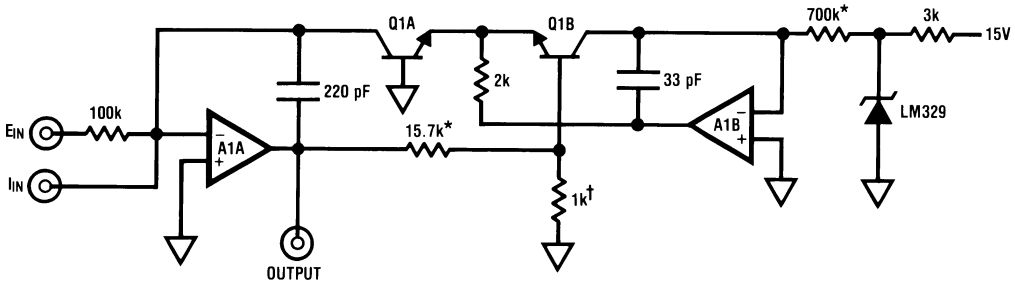
where K=Boltzmann's constant
T=temperature °K
q=charge of an electron.

If both equations are combined, the circuit output for a voltage input is:

$$E_{OUT} = \frac{-KT}{q} \frac{15.7k + 1k}{1k} \log_e \frac{E_{IN} \bullet 700k}{6.9V \bullet 100k}$$

where 6.9V=V_Z of LM329
100k=input resistor
$E_{IN} \geq 0$.

This confirms that the circuit output voltage is logarithmically related to the circuit's input. Without some form of compensation, the scale factor will change with temperature. The simplest way to avoid this is to have the 1 kΩ value vary with temperature. For the device shown, compensation is within 1% over −25°C to +100°C. The circuit's gain is set by the 15.7 kΩ-1 kΩ divider to a factor of 1V/decade.



*1% film resistor

†1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series.

A1A, A1B = LF412 dual

Q1A, Q1B = LM394 dual

FIGURE 1.

This circuit may be easily turned around to generate exponentials. In *Figure 2*, Q1A is driven from the input via the 15.7 kΩ divider. Q1B's collector current varies exponentially with its V_{BE}, and A1B provides a voltage output representation of this action.

These circuits are easy to construct and use if a few considerations are kept in mind. Because of the V_{BE} and scale factor temperature dependences, it is important that Q1A, Q1B and the 1 kΩ resistor be kept at the same temperature. Since Q1 is a dual monolithic device, both halves will track. The resistor should be mounted as closely as possible to Q1, and these components should be kept away from air currents or drafts. The KT/q factor for which the resistor compensates varies at about 0.3%/˚C, so a few degrees difference between Q1 and the resistor will introduce significant error.

Once the theory and construction techniques are understood, the circuits can be applied. *Figure 3* shows a way to achieve very precise control of a rotary pump, used to feed a biochemical fermentation process. In this example, the exponentiator, composed of Q1 and A1A, is driven from input amplifier A1D. Q1B's collector current, instead of biasing a voltage output amplifier as in *Figure 2*, pulls current from the A1B integrator which ramps up (trace A, *Figure 4*) until it is reset by level triggered A1C (A1C output is trace B, *Figure 4*). The 100 pF capacitor provides AC positive feedback to A3C's "+" input (trace C, *Figure 4*). The magnitude of the current that Q1B's collector pulls from A1B's summing junction will set the frequency of operation of this oscillator. Note that the operation of the exponentiator is similar to the basic circuit in *Figure 3* because A1B's summing junction is always at virtual ground. A1C's output drives the MM74C76 flip-flop to bias the output transistors with 4-phase drive for a stepper motor which runs the pump head. In practice, the exponentiator allows very fine and predictable control for very slow pump rates (e.g., 0.1 rpm-10 rpm of the stepper motor), aiding tight feedback control of the fermentation process. When high pump rates are required, such as during process start-up or when a wide feedback control error exists, the exponentiator can be voltage directed to the top of its range. To calibrate the circuit, ground V_{IN} and adjust the 0.1 Hz trim until oscillation just ceases. Next, apply 7.5V at V_{IN} and adjust the 600 Hz trim for 600 Hz output frequency. *Figure 5* shows a circuit similar to *Figure 3*, except that a more accurate V-F converter is used. This circuit is intended for laboratory and audio studio applications requiring an oscillator whose frequency changes exponentially with an applied input sweep voltage. Applications include swept distortion measurements (where this circuit's output is used to drive a sine coded ROM-DAC combination or analog shaper) and music synthesizers. The V-F converter employed allows better than 0.15% total conformity over a range of 10 Hz-30 kHz. The voltage reference used to drive A1A's input resistor is derived from the LM331A's internal reference and is scaled by A1B, which also biases the zero trim setting. The DM74C74 provides a square wave output for applications requiring a waveform with substantial fundamental frequency content. The 0.15% conformity performance achieved by this circuit will meet almost any synthesizer or swept distortion measurement and the scale factor may be easily varied. To trim, apply OV to the input and adjust zero until oscillation (typically 2 Hz-3 Hz) just starts. Next, apply –8V and adjust the 5k unit for an output frequency of 30 kHz. For the values given, the K factor of the exponentiator will yield a precise doubling in frequency for each volt of input (e.g., 1V in per octave out).

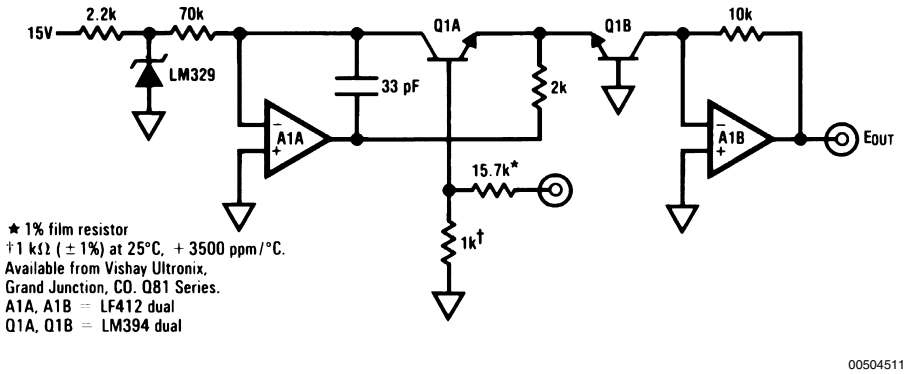


FIGURE 2.

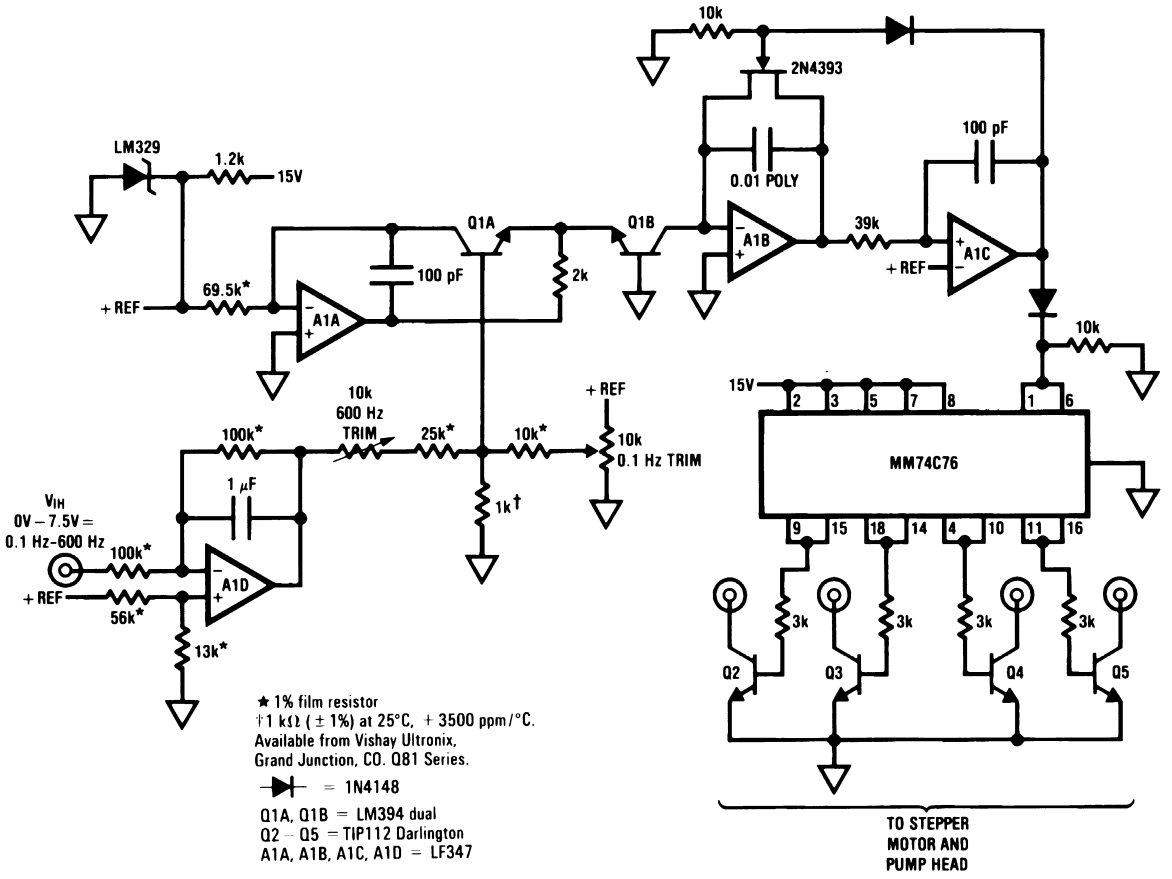


FIGURE 3.

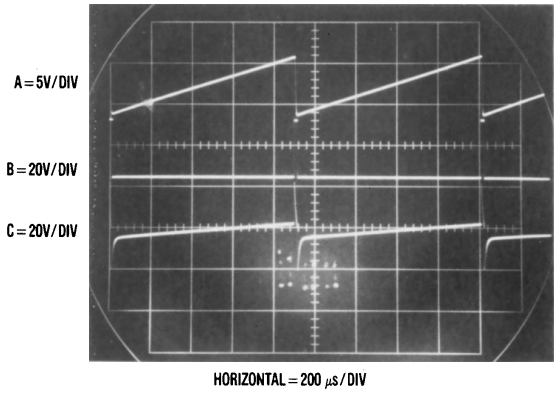
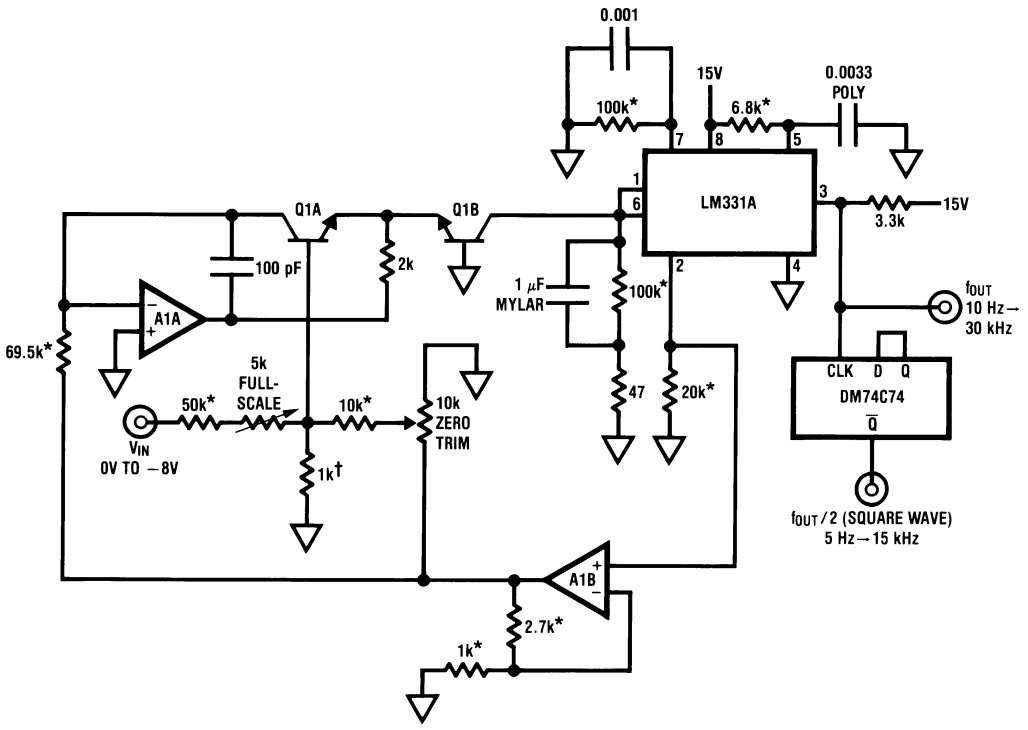


FIGURE 4.



*1% film resistor

†1 kΩ (±1%) at 25˚C, +3500 ppm/˚C.
Available from Vishay Ultronix,
Grand Junction, CO, Q81 Series.

A1A, A1B = LF412 dual

Q1A, Q1B = LM394 dual

FIGURE 5.

Figure 6 shows a way to use the exponentiator circuit in a non-invasive, high reliability gas gauge which was designed for use in irrigation pump arrangements in remote locations. The application calls for a highly reliable gas gauge to be retrofitted to large fuel tanks which supply pump motors. It is desirable to run the gas tanks down as closely to empty as possible to eliminate condensation build-up without running out of fuel. This acoustically-based scheme operates by bouncing an ultrasonic pulse off the liquid level surface and using the elapsed time to determine the fuel remaining. This time is converted to a voltage, which is exponentiated to provide a readout with high resolution for nearly empty tanks. The 60 Hz derived clock pulse (trace A, *Figure 7*) drives the transistor pair to bias the ultrasonic transducer with a 100V pulse. Concurrently, the DM74C74 flip-flop is set high (trace C, *Figure 7*) and the DM74C221 one-shot (trace D, *Figure 7*) is used to disable the output of the receiver amplifier. The acoustic pulse bounces off the gasoline's surface and returns to the transducer. By this time, the disable pulse has gone low and the A1A, A1B, A1C and C1 receiver responds (trace B, *Figure 7*) to the transducer's output. C1's output resets the flip-flop low via the DM74C04 inverter. The width of the 60 Hz flip-flop output pulse represents the transit time and the fuel remaining. This width is voltage clamped and integrated at A1D, whose output drives the exponentiator. The 1V/decade scale factor of the exponentiator means that the last 20% of the meter scale corresponds to a tank with only 2% fuel remaining. The first 10% of the meter indicates 80% of the tank's capacity.

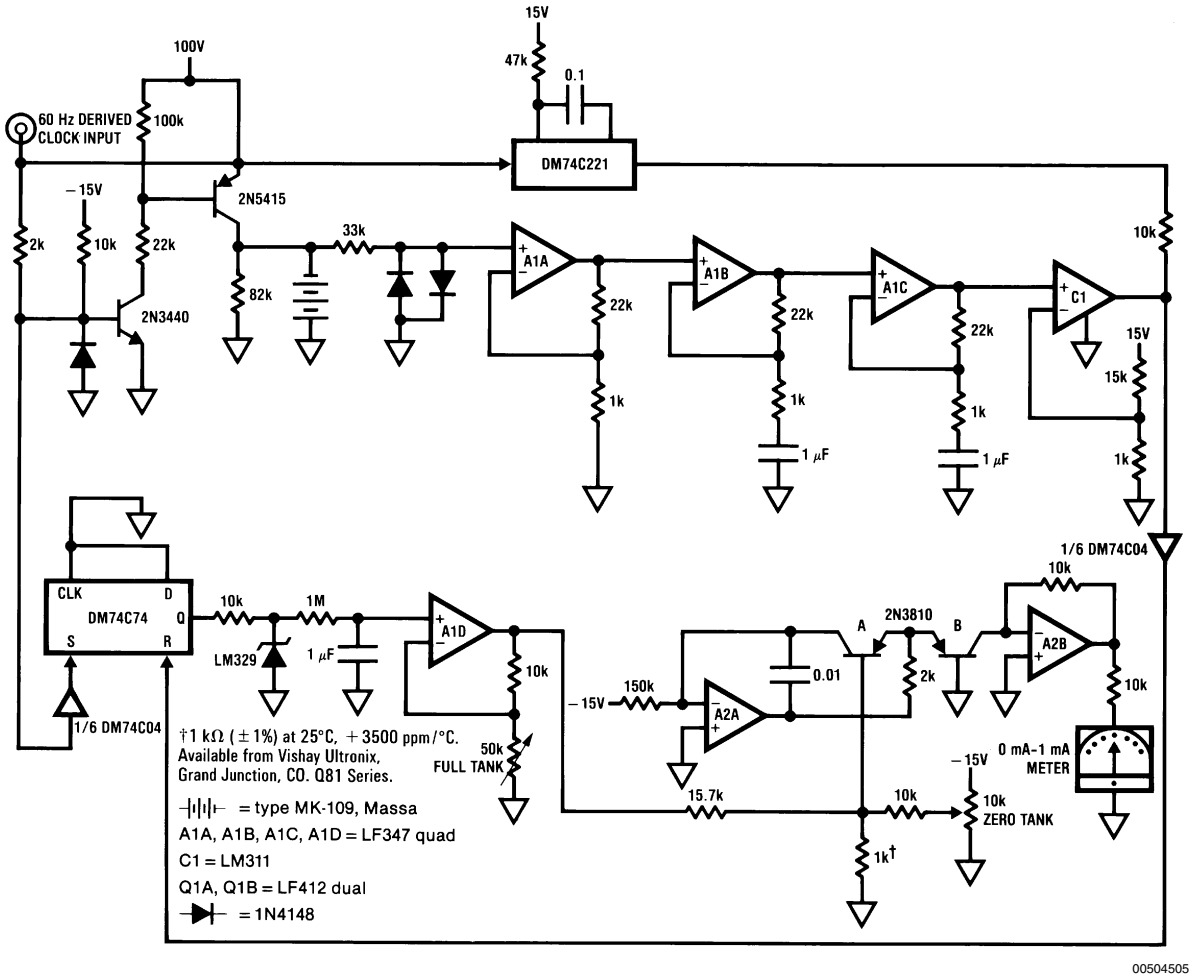


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FIGURE 6.

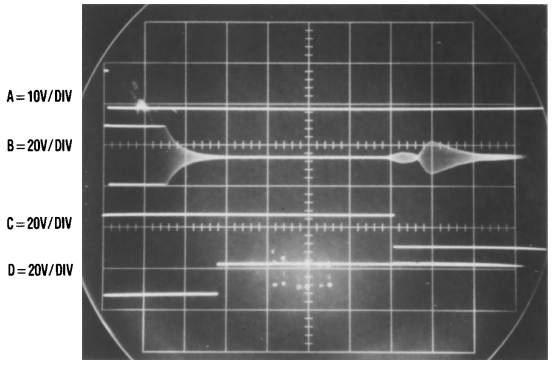

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FIGURE 7.

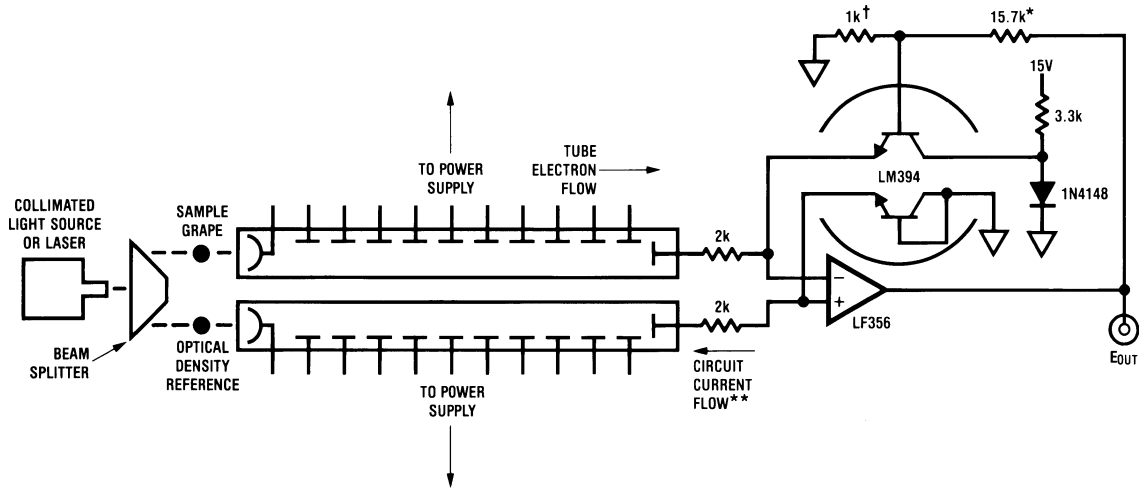
The last application determines density by using photometry. In this arrangement, a light source is optically split (*Figure 8*) and the resultant two beams drive light through a sample and an optical density reference. In this case, the optical sample is a grape, and the photometric set-up is used to correlate the optical density of the grape with its ripeness. Two photomultiplier tubes detect the light passed by the sample and the reference. The ratio of the photomultiplier outputs, which may vary over a wide range, is dependent upon the optical density difference of the sample and the reference. The tubes' output feed a log *ratio* amplifier. This configuration dispenses with the fixed current reference nor-

mally employed, and substitutes the output of the reference channel photomultiplier. In this fashion, the log amplifier's output represents the ratio between the densities of the sample and reference channels over a wide dynamic range. Variations in the light source intensity have no effect. Strictly speaking, the LF356 inputs are not at virtual ground, and an imperfect current-to-voltage conversion should result. In fact, the output impedance of the photomultipliers is so high that errors are minimal. The most significant log conformance error source in this simple log circuit is the fact that the transistor's collectors are at slightly different potentials. For the application shown, this uncertainty is not significant.

References

Non-Linear Circuits Handbook; Analog Devices, Inc.

Logarithmic Converters, Application Note AN-30; R. C. Dobkin; National Semiconductor Corporation.



*1% film resistor†1 kΩ (±1%) at 25˚C, +3500 ppm/˚C.
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Grand Junction, CO, Q81 Series.
**≈ 10 µA nominal but may vary from
10^{-4}A to 10^{-9}A

FIGURE 8.

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