ALPHA & OMEGA SEMICONDUCTOR, INC.

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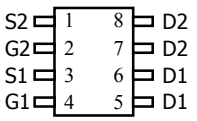
AO4826A
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

The AO4826A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

Features

V_{DS} (V) = 55V
I_D = 7.9A
$R_{DS(ON)}$ < 20mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 25mΩ (V_{GS} = 4.5V)



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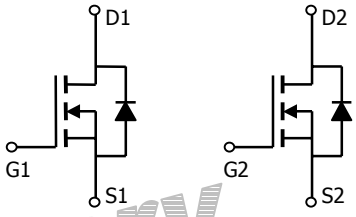

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	55	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	7.9	A
	T_A=70°C		6.3	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25°C	P_D	2	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	50	62.5	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		73	110	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	31	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	55			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	2.2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8.0A		17	20	mΩ
		T_J=125°C				
		V_{GS}=4.5V, I_D=7A		21	25	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8.0A		23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		1910		pF
C_{oss}	Output Capacitance			186		pF
C_{rss}	Reverse Transfer Capacitance			128		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=8A		42.8		nC
Q_g(4.5V)	Total Gate Charge			22		nC
Q_{gs}	Gate Source Charge			5.4		nC
Q_{gd}	Gate Drain Charge			13		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=3.9Ω, R_{GEN}=3Ω		7.7		ns
t_r	Turn-On Rise Time			6.2		ns
$t_{D(off)}$	Turn-Off DelayTime			29.7		ns
t_f	Turn-Off Fall Time			23.4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8.0A, dI/dt=100A/µs		32		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8.0A, dI/dt=100A/µs		38.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.