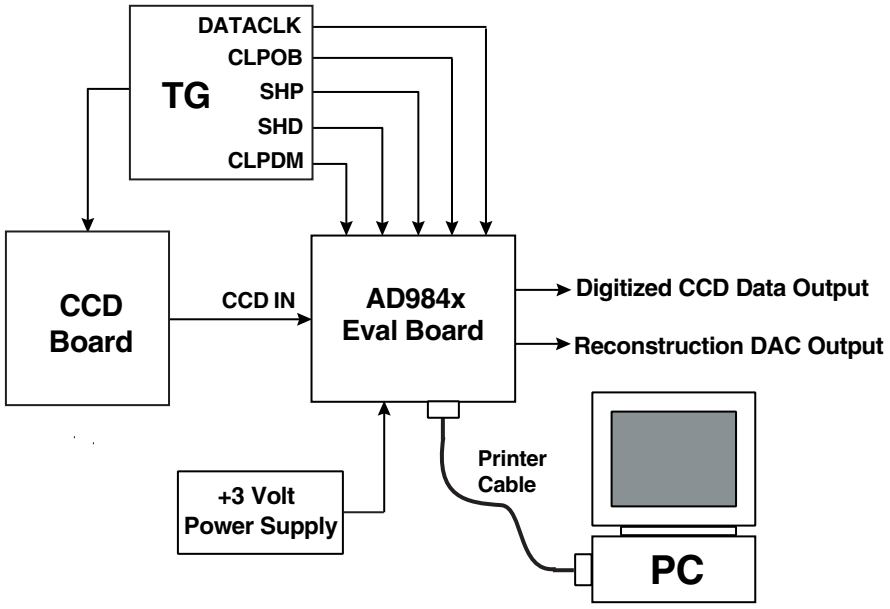
# AD984X EVALUATION BOARD




*AD984x Evaluation System Block Diagram*

## EQUIPMENT REQUIRED

**AD984x Evaluation Board**

**Software executable files (included with board)**

**Micro-Centronics Printer Cable (included with board)**

**+3 Volt Power Supply**

**Input Signal Source from CCD or generator**

**Timing Generator or other clock source**

**PC with Windows 95 or 98, standard ECP-mode parallel port, and minimum 1024x768 Color Display**

## RUNNING THE EVALUATION SYSTEM

Step 1- Configure the software. If the PC does not have Labview 5.1 installed, then it may be necessary to run the exectuble file set.exe under the "Runtime" directory. This program will install the files needed for the evaluation board software to run properly. Once these files have been installed, the PC is ready to run the eval board executable files (Step 3).

Step 2- Configure the hardware. Connect the +3V power supply to the AD984x evaluation board (+5V for the output drivers is optional, see next section). Connect the desired input signal from a CCD or signal generator. Connect the clock signals SHP, SHD, DATACLK, CLPOB, and CLPDM (and HD/VD if the PxGA® is going to be used). Connect the Micro-Centronics printer cable from the PC's parallel port to the evaluation board. The PC's parallel port should be configured in normal ECP mode.

Step 3- Run the software executable file:

ad9843a.exe - use with AD9840A, 43A, & 44A
ad9842a.exe - use with AD9841A, 42A, 45A, & 46A

By default, the program screen will be operating when first opened. The configuration screen should appear as shown on page 2. This program is used to configure the AD984x internal registers to the desired values. Use the "QUIT" button to temporarily stop the program. Click the arrow in the upper-left corner of the window to continue running the program.

Step 4- Acquire the AD984x's output data. The data outputs from the 40-pin connector on the evaluation board may be captured using a logic analyzer, data acquisition card, or image processor chip.

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REV. 0



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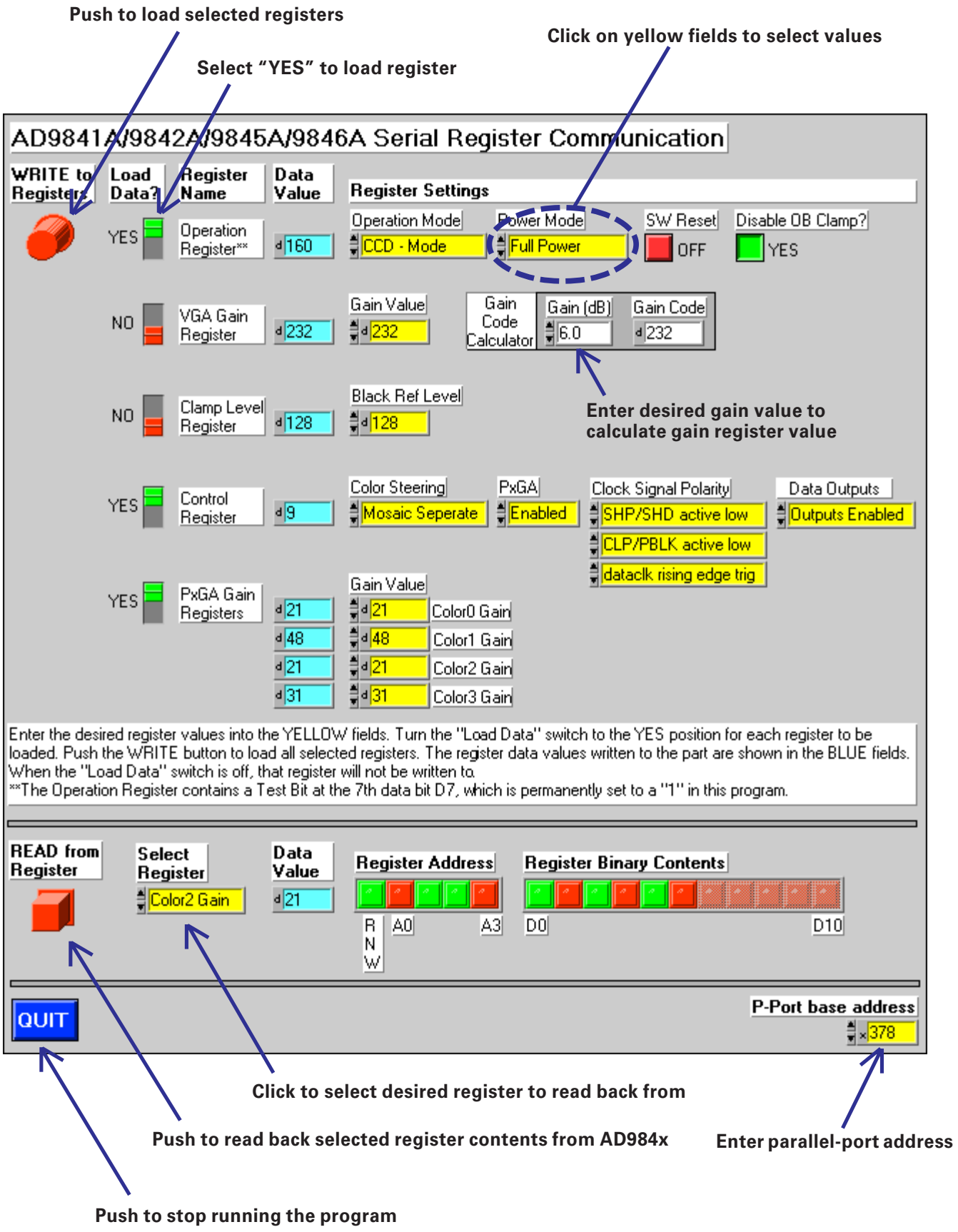
**AD9841A/9842A/9845A/9846A EVALUATION SOFTWARE WINDOW**



**BOARD CONNECTIONS (see AD984X Schematic.pdf)**

**Power Supply Connectors**

J21 +3D: +3V supply for the input side of the output buffers. Always connect to +3V supply.
+3/+5D: +3V or +5V supply for the output buffers. If 5V output levels are needed at the output connector J18, connect 5V supply here. If 3V levels are sufficient, then install the +3D:+3/+5D jumper (JP10) located above J21. IF DIFFERENT VOLTAGES ARE USED FOR +3D and +3/+5D, DO NOT CONNECT THIS JUMPER.

J22 VDD: +3V supply for the AD984x device. Datasheet specifications are given for +3.0V. Operational range is from +2.7 V to +3.6 V.

**Input Signal Connectors**

J9 CCDIN: Input for the CCD signal. If the 50Ω termination is not need, this resistor may be removed. Or, the other side of JP2 may be used to connect to the CCD signal.

J11 AUX: Input for either AUX1 or AUX2 channels of the AD984x. Install JP4 to use the AUX1 channel. Install JP5 to use the AUX2 channel. Install JP4 and JP17 to DC-couple into the AUX1 channel.

**Output Connectors**

J1 DAC Iout: The reconstruction DAC has a current output, and is loaded with 50Ω at J1. J1 can be directly connected to an oscilliscope to observe the AD984x's reconstructed digtal output data.

J18 Buffered digital output data from AD984x. Logic level determined by power supply level of J21 +3/+5D.

**Clock Signals**

J1 SHD
J2 CLPDM
J3 SHP
J4 CLPOB
J5 PBLK
J6 DATACLK
J7 VD (only use with AD9841A/9842A/9845A/9846A)
J8 HD (only use with AD9841A/9842A/9845A/9846A)

All SMA clock connectors are terminated with 50Ω. These resistors may be removed. When the SMA connectors are used, the jumpers on the header JP1 should be installed. JP1 may also be used as a connector by removing the jumpers and directly connecting the clock signals to the odd-numbered pins 1-15. PBLK may be shorted high permanently by installing JP23.

**PC-Host Connection for Serial Communication**

J19 Connect to the PC's parallel port using the microcentronics cable.

**JUMPER DESCRIPTIONS**

JP1 Install these 8 jumpers when using the SMA clock inputs.

JP2 Install when using the CCDIN SMA input.

JP4 Install to connect the AUX SMA input to the AUX1 channel.

JP5 Install to connect the AUX SMA input to the AUX2 channel.

JP6 SL. Install when using the PC software to load the AD984x registers.

JP7 SCK. Install when using the PC software to load the AD984x registers.

JP8 SDATA. Install when using the PC software to load the AD984x registers.

JP10 Install to short the +3D and +3/+5D supplies together.

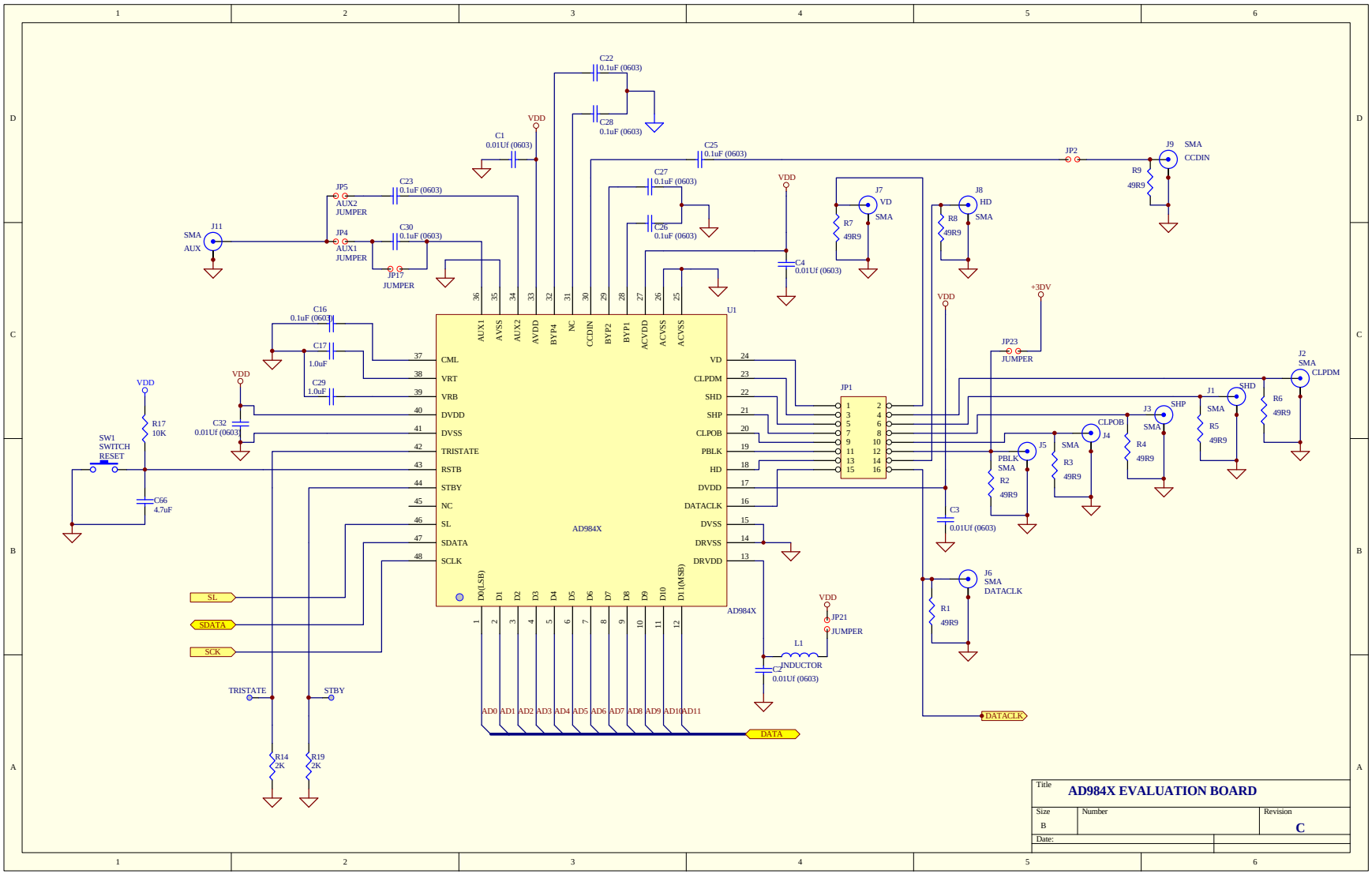
JP17 Install to DC-Couple the AUX signal into the AUX1 channel.

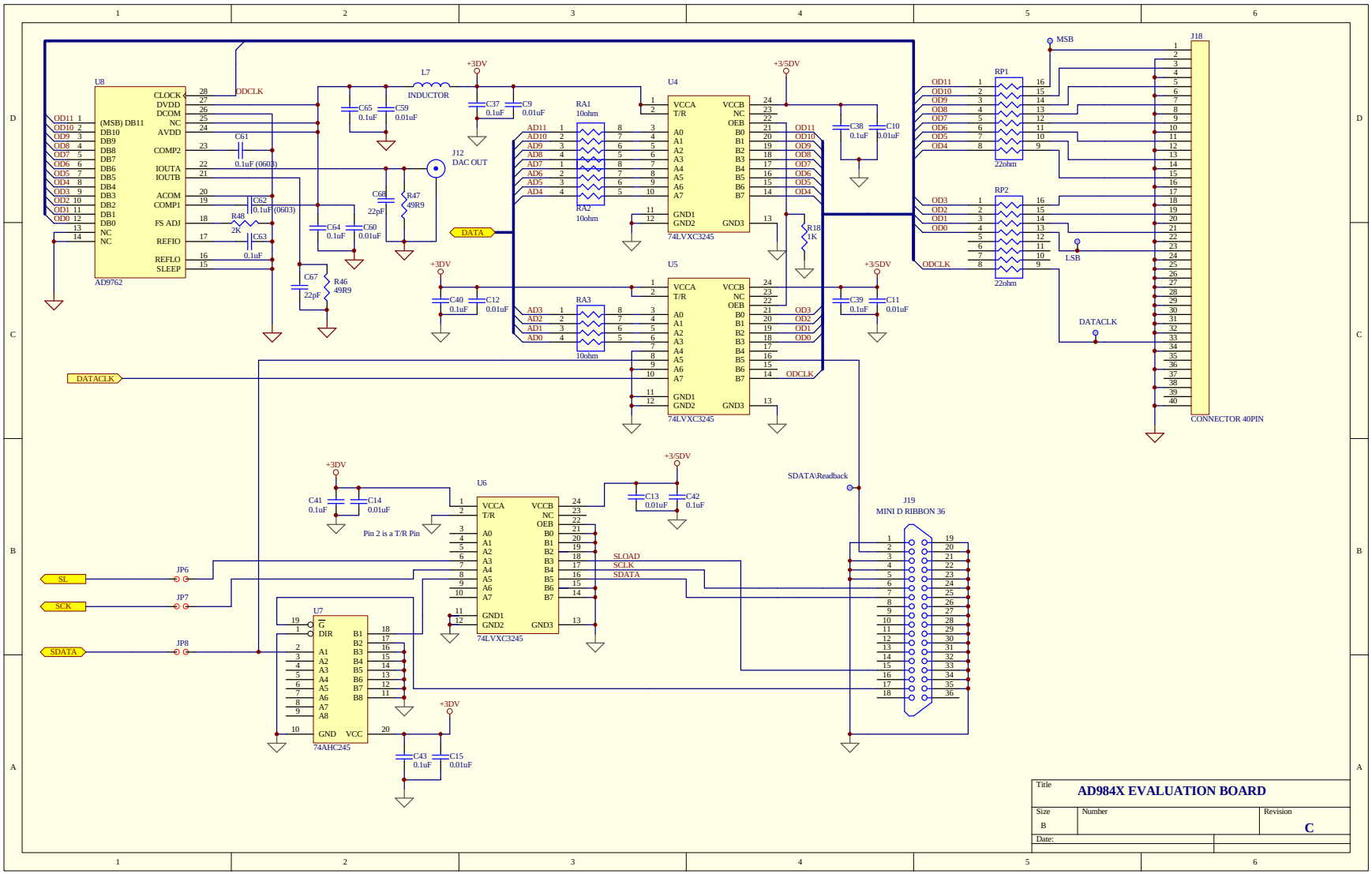
JP21 Install to connect the AD984x's DRVDD power supply to VDD. If a different driver supply voltage is desired, this jumper may be removed and used as a dedicated DRVDD supply connection.

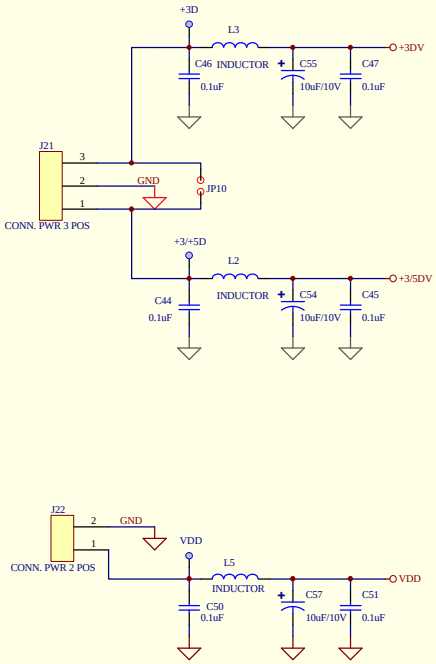
JP23 Install to connect PBLK to +3V (disabling PBLK).

**Typical Input Configurations**

| Configuration | Input | JP2 | JP4 | JP5 | JP17 |
|---|---|---|---|---|---|
| Basic CCD-mode | J9 | short | don't care | don't care | don't care |
| Grounded-Input Test | J9 open | short | don't care | don't care | don't care |
| AUX1 Mode (AC-Coupled) | J11 | don't care | short | open | open |
| AUX1 Mode (DC-Coupled) | J11 | don't care | short | open | short |
| AUX2 Mode | J11 | don't care | open | short | don't care |


C22 0.1uF (0603)
C28 0.1uF (0603)
C1 0.01Uf (0603)
VDD
C25 0.1uF (0603)
JP2
J9 SMA CCDIN
R9 49R9
C27 0.1uF (0603)
C26 0.1uF (0603)
JP5 AUX2 JUMPER
C23 0.1uF (0603)
JP4 AUX1 JUMPER
C30 0.1uF (0603)
JP17 JUMPER
J11 SMA AUX
C4 0.01Uf (0603)
J7 VD SMA
R7 49R9
J8 HD SMA
R8 49R9
+3DV
JP23 JUMPER
J2 SMA CLPDM
C16 0.1uF (0603)
C17 1.0uF
C29 1.0uF
C32 0.01Uf (0603)
U1
AUX1 AVSS AUX2 AVDD BYP4 NC CCDIN BYP2 BYP1 ACVDD ACVSS ACVSS
CML VRT VRB DVDD DVSS TRISTATE RSTB STBY NC SL SDATA SCLK
VD CLPDM SHD SHP CLPOB PBLK HD DVDD DATACLK DVSS DRVSS DRVDD
AD984X
D0(LSB) D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11(MSB)
JP1
J1 SMA SHD
J3 SMA SHP
J4 SMA CLPOB
J5 SMA PBLK
R6 49R9
R5 49R9
R4 49R9
R3 49R9
R2 49R9
SW1 SWITCH RESET
R17 10K
C66 4.7uF
C3 0.01Uf (0603)
J6 SMA DATACLK
R1 49R9
SL
SDATA
SCK
TRISTATE
STBY
R14 2K
R19 2K
L1 INDUCTOR
C2 0.01Uf (0603)
JP21 JUMPER
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11
DATA
DATACLK
Title
AD984X EVALUATION BOARD
Size B
Number
Revision C
Date:


U8
AD9762
ODCLK
L7
INDUCTOR
+3DV
+3/5DV
C65 0.1uF
C59 0.01uF
C37 0.1uF
C9 0.01uF
C61 0.1uF (0603)
C62 0.1uF (0603)
C68 22pF
R47 49R9
J12 DAC OUT
R48 2K
C63 0.1uF
C64 0.1uF
C60 0.01uF
C67 22pF
R46 49R9
DATA
RA1 10ohm
RA2 10ohm
RA3 10ohm
U4
U5
74LVXC3245
C40 0.1uF
C12 0.01uF
C38 0.1uF
C10 0.01uF
C39 0.1uF
C11 0.01uF
R18 1K
RP1 22ohm
RP2 22ohm
MSB
LSB
J18
CONNECTOR 40PIN
DATACLK
U6
C41 0.1uF
C14 0.01uF
C13 0.01uF
C42 0.1uF
Pin 2 is a T/R Pin
SDATA\Readback
J19
MINI D RIBBON 36
SLOAD
SCLK
SDATA
JP6
JP7
JP8
SL
SCK
U7
74AHC245
C43 0.1uF
C15 0.01uF
Title
AD984X EVALUATION BOARD
Size
B
Number
Revision
C
Date:

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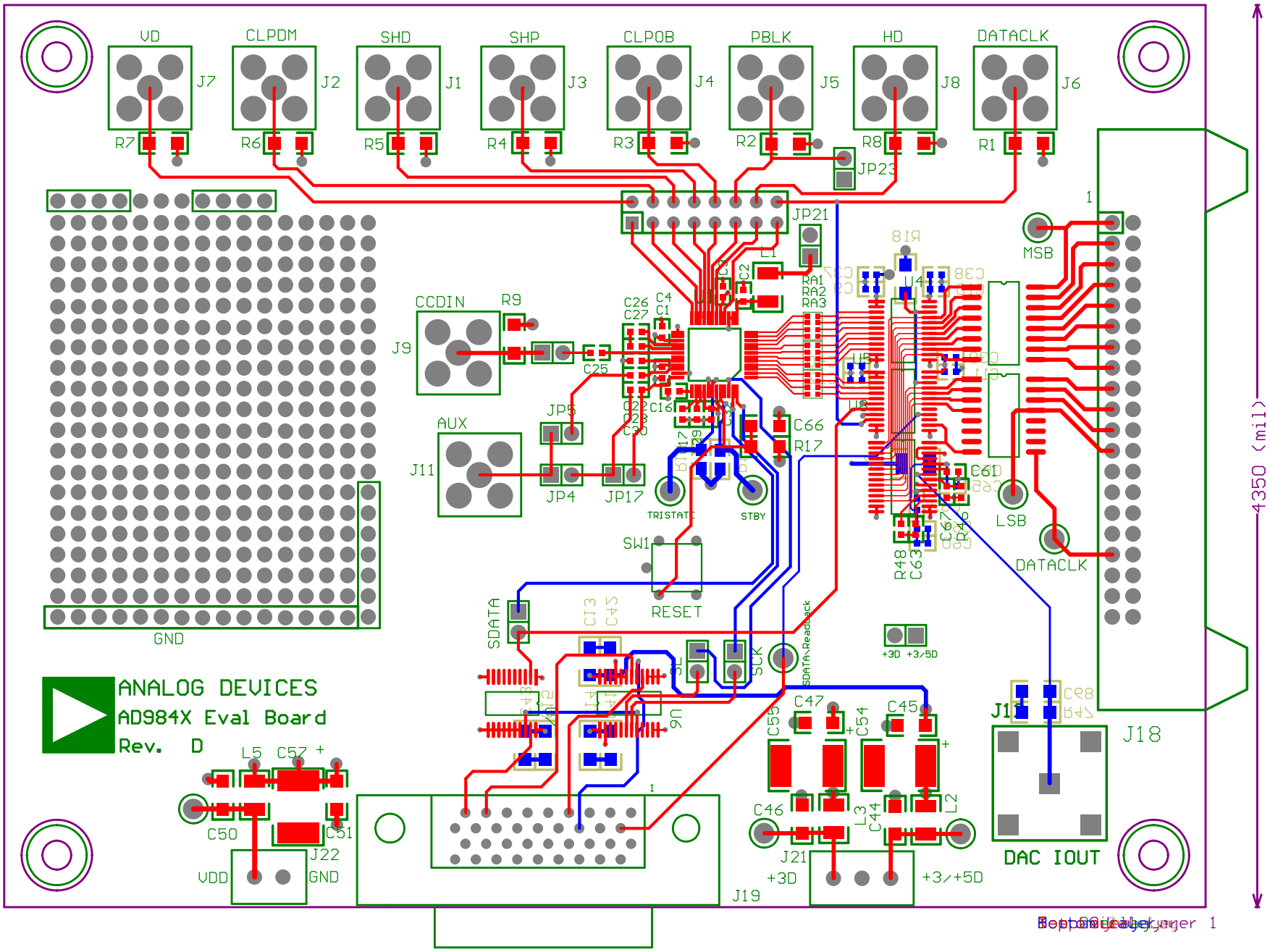
|---|---|---|
| Title | **AD984X EVALUATION BOARD** | |
| Size: B | Number: | Revision: **C** |
| Date: | | |


VD
CLPDM
SHD
SHP
CLPOB
PBLK
HD
DATACLK
J7
J2
J1
J3
J4
J5
J8
J6
R7
R6
R5
R4
R3
R2
R8
R1
JP23
JP21
MSB
LSB
DATACLK
CCDIN
J9
R9
AUX
J11
JP5
JP4
JP17
TRISTATE
STBY
SW1
RESET
SDATA
SCK
SDATA\Readback
+3D
+3/5D
GND
ANALOG DEVICES
AD984X Eval Board
Rev. D
L5
C57
C50
C51
J22
VDD
GND
J19
C47
C54
C45
C55
C46
C44
L3
L2
J21
+3D
+3/+5D
J18
DAC IOUT
4350 (mil)
5805 (mil)