# *TOPSwitch®-GX* Forward Design Methodology

## Application Note AN-30

## Introduction

The single-ended forward converter topology is often the best solution for AC-DC applications that require higher powers and higher output currents than are practical from flyback converters. The forward converter extends the power capability of *TOPSwitch-GX* to greater than 200 W for high current outputs.

The feature set of *TOPSwitch-GX* offers the following advantages in single-ended forward designs:

- Built-in soft-start
- Built-in under-voltage lockout
- Built-in adjustable current limit
- Programmable duty cycle reduction to limit duty cycle excursion at high line and transient load conditions
- Higher efficiency (typically >70%)
- Very good light-load efficiency
- Voltage mode control for simpler loop designs with magnetic amplifier post-regulators
- Built-in remote on-off
- Low component count
- Improved EMI

### Scope

This application note is for engineers designing an AC-DC power supply using *TOPSwitch-GX* in a single-ended forward converter. It addresses single input voltage 230 VAC or doubled 115 VAC input, but does not address universal input (85 V to 265 V) designs. The document highlights design parameters that are fundamental to the use of *TOPSwitch-GX* in a single-ended forward converter. It offers a procedure to compute transformer turns, output inductance and other design parameters. This procedure enables designers to build an operational prototype in the shortest possible time. Refinement of the prototype hardware after bench evaluation will lead to a final design.

The design methodology presented here is sufficiently general to cover a variety of single-ended forward designs, including power supplies for personal computers. It provides for multiple outputs with coupled inductors, independent multiple outputs, and outputs with both linear or magnetic amplifier post regulators.

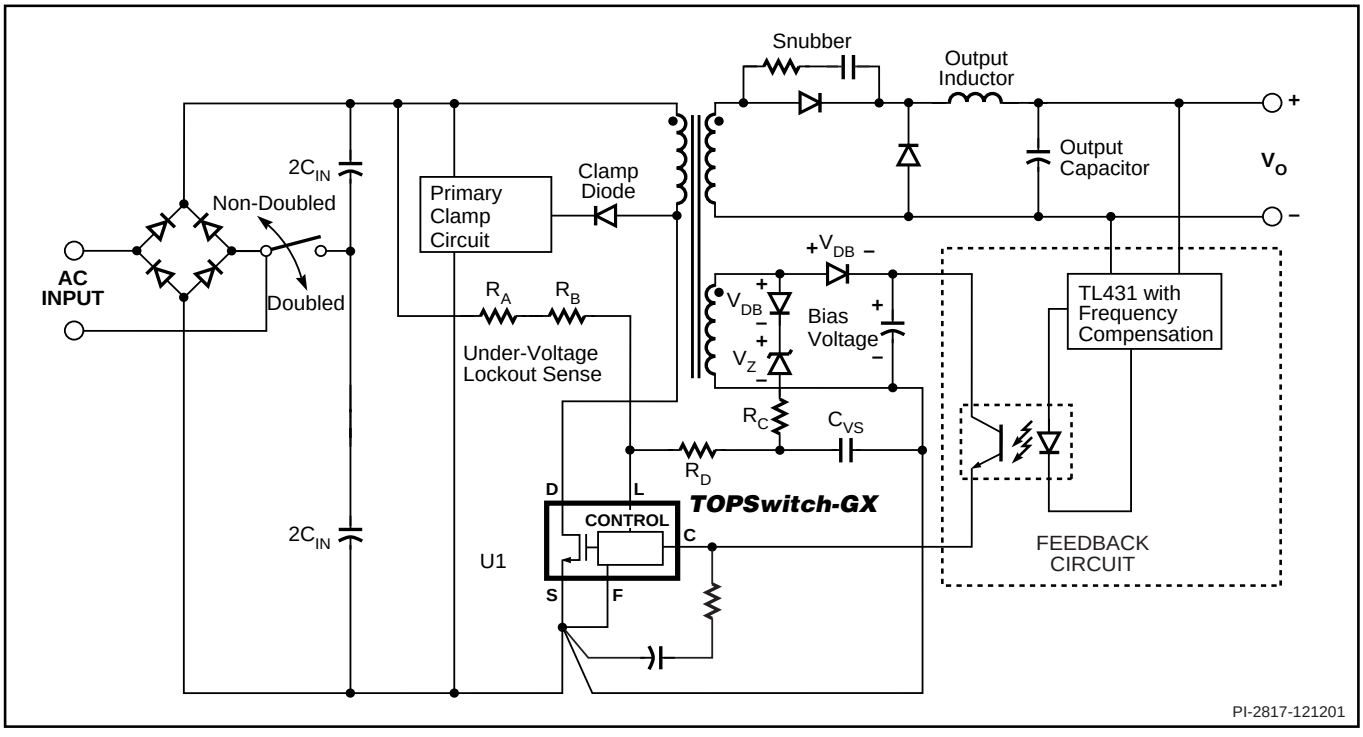



*Figure 1. Typical Configuration of TOPSwitch-GX in a Single-Ended Forward Converter.*

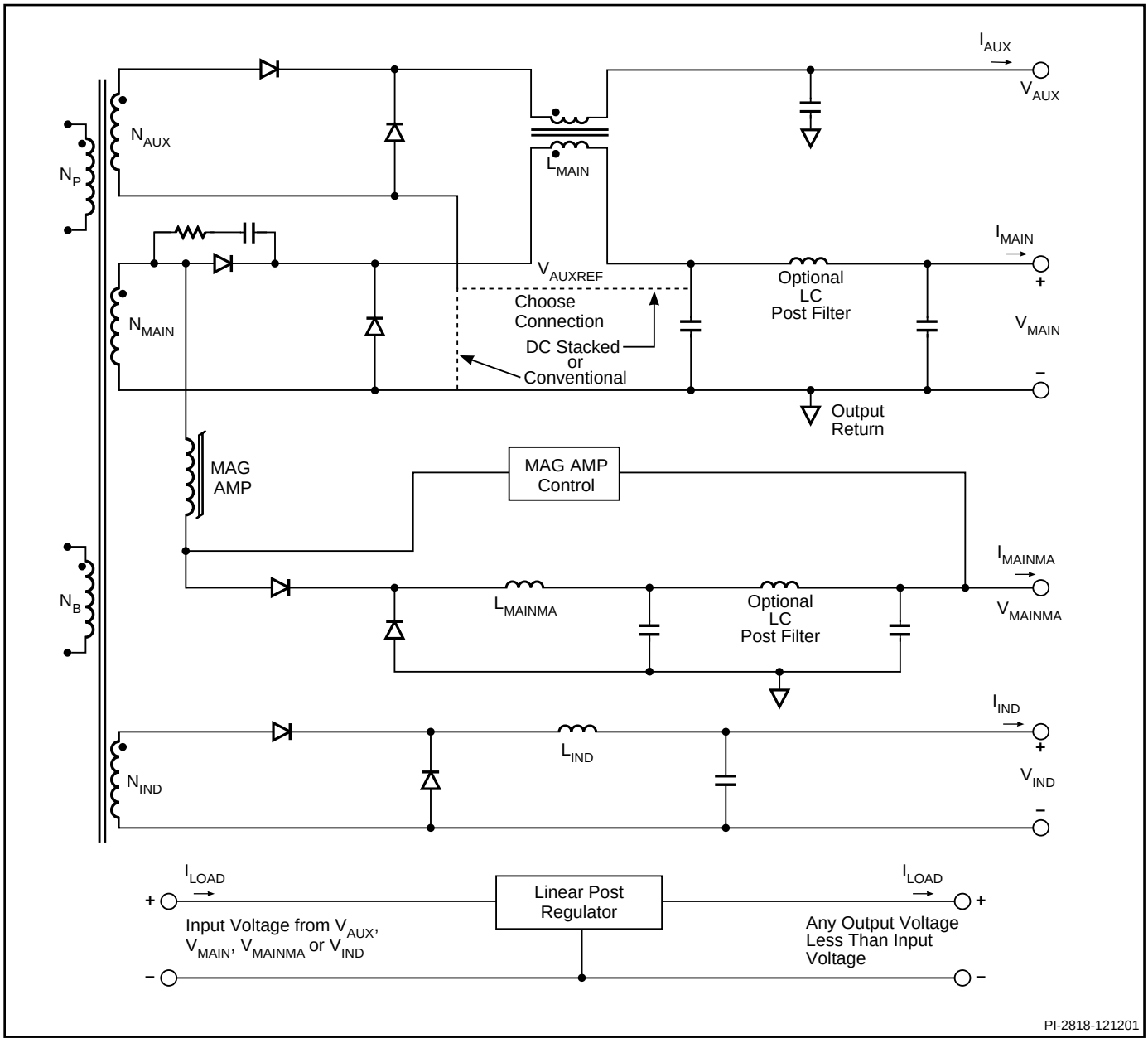



*Figure 2. General Output Options for the Forward Converter Described in the Methodology.*

This document does not address the design of magnetic amplifiers nor linear regulators. It determines design parameters for the transformer and the inductors, but does not give construction details for those magnetic components. Such details are deferred to other application notes and component suppliers. References [1] through [6] are good sources of information for the design of transformers and inductors. Software for design of magnetic amplifiers is available from [5]. Reference [1] is also an excellent resource for other important topics in power electronics.

## Design Methodology Overview

The methodology assumes the reader knows the theory of operation of the forward converter and the fundamentals of power supply design. It is a companion to the *PI Expert* software for forward converter design (available from the Power Integrations Web site). Designers are advised to check Power Integrations' Web site at *www.powerint.com* for the latest application information.

This presentation uses a typical combination of output options for illustration of the methodology (see Figure 2). This document

gives the basic expressions illustrating the methodology. The *PI Expert* software uses more complex versions of these expressions containing additional parameters to account for non-ideal effects. Thus, results from the software may not exactly match the computations from expressions in this document.

This document assumes a non-doubled input configuration. *PI Expert* includes modified expressions for both doubler and non-doubler input configurations. To simplify the expressions, all outputs are assumed to operate in continuous conduction mode, consistent with the worst case design at maximum load. At lower load conditions it is possible for individual outputs to operate in discontinuous conduction mode.

The methodology begins with an explanation of the general converter topology. It then presents the design flow, showing the major tasks in a high level flowchart. After a review of the nomenclature and definitions of variables, it discusses the details of the design procedure. Rationale, assumptions and expressions are given to help the designer enter parameters and interpret results. A complete list of variables used in the expressions follows in Appendix A. Appendix B offers a procedure for hardware verification. A worked example is presented in Appendix C.

## General Converter Topology

Figure 1 shows a typical single-ended forward converter using *TOPSwitch-GX*. Detail is focused on the primary side of the transformer because the circuits on the secondary are conventional and covered in other literature.

Resistors $R_A$ and $R_B$ set the under-voltage lockout threshold. Resistor network $R_A$, $R_B$, $R_C$, and $R_D$ with capacitor $C_{VS}$ adjusts the maximum duty ratio as a function of the input voltage. This methodology gives the procedure to determine proper values for the resistors and the capacitor.

Another key element in the use of *TOPSwitch-GX* is the primary clamp ($C_{CP}$, D1, VR1, VR2 and VR3 in Figure 10) which resets the transformer flux and limits the maximum drain voltage. This methodology assumes use of this Zener-capacitor clamp circuit. Guidance for selection of components for this particular clamp is included in this application note.

The topic of clamp circuits is deferred to a separate application note. Designers may choose to use their own clamp circuits with the restriction that ***resonant clamps, (for example, LCD clamps–inductor/capacitor/diode) and reset windings are not recommended***. The internal current sense of *TOPSwitch-GX* does not allow the high reset current of a resonant clamp to be excluded from the sensed drain current.

This methodology uses an ordinary optically isolated feedback circuit that is common in voltage mode systems with a two-pole response. The frequency compensation will in general require two zeros and two poles to obtain the phase margin desired for most applications. While the design of the feedback circuit is a separate topic beyond the scope of this application note, the general topology of the circuit is discussed.

### Output Options

Salient features of the output circuits are illustrated in Figure 2. Multiple secondary windings of the transformer may be configured in many different ways to give several options for regulated and unregulated output voltages.

All applications will have only one main output. This is the voltage that is regulated directly by *TOPSwitch-GX* through the optically isolated feedback circuit. In general, any number of auxiliary outputs may be derived from other secondary windings and regulated indirectly by means of a coupled inductor that they share with the main output.

The secondary windings for the auxiliary outputs may be configured in two different ways. The conventional configuration connects one side of the auxiliary winding to the main output return. This connection is used when the auxiliary output is the opposite polarity of the main output. An alternative configuration, sometimes known as the DC stacked connection, has one side of the auxiliary winding referenced to the main output instead of the output return. It has the advantage of better regulation of the auxiliary output voltage than the non-stacked arrangement, but is limited to outputs that are greater in magnitude and of the same polarity as the main output voltage.

Any number of unregulated output voltages may be derived from circuits that do not share an inductor with any other outputs. They are related to the main output only through separate secondary windings on the transformer. Their inductors are independent of the others. These outputs typically are referenced to the output return, but alternatively they may be referenced to any potential that the isolation of the transformer will tolerate.

Multiple tightly regulated voltages may be obtained with either linear or switching post regulators. These external regulators may be added to any output, including the main output. They are simply additional loads on those output voltages.

A particularly useful type of switching post regulator is the magnetic amplifier, which uses a saturating magnetic element as an independently controlled switching device. While a magnetic amplifier can in theory be operated from any output, this methodology restricts the connection to the main output only.

Since it is not possible to treat every combination of output

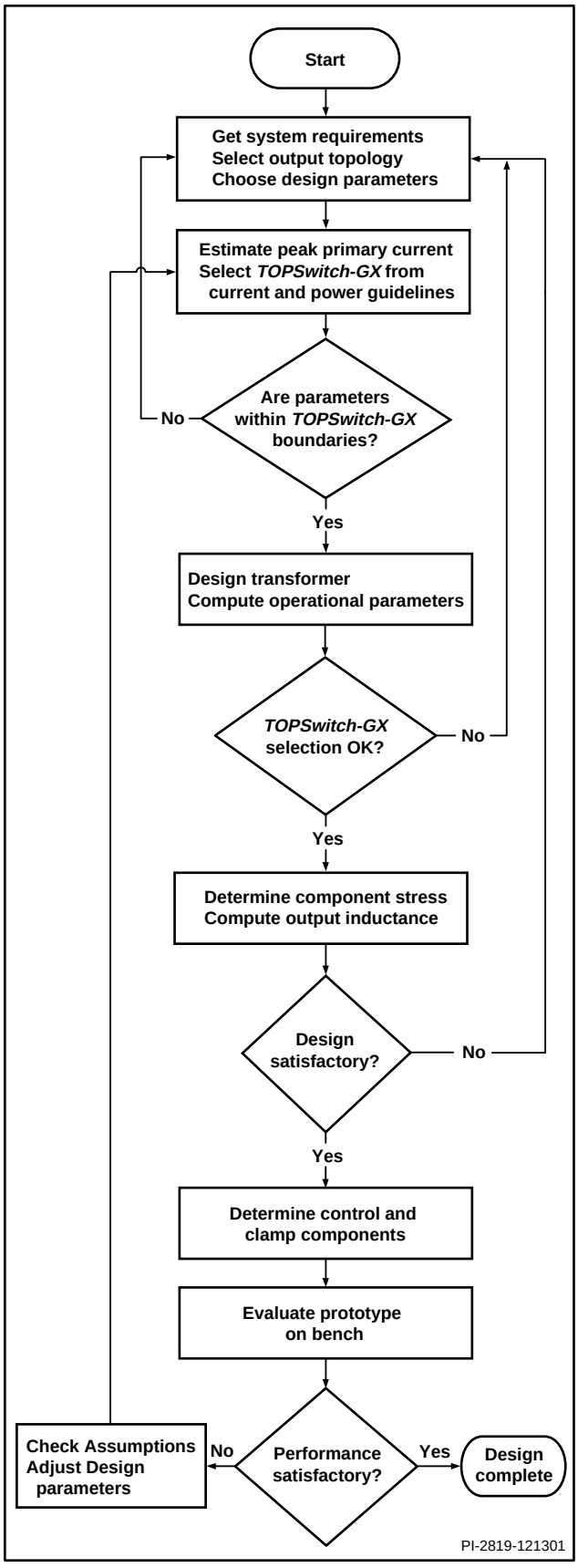



*Figure 3. Flowchart Showing Major Tasks in the Design of Forward Converters with TOPSwitch-GX.*

options in this presentation, the methodology will be restricted to those that are typical for power supplies in personal computers. Therefore, this methodology allows the following options:

- One main output
- A maximum of one auxiliary output that may be DC stacked to the main output or referenced to output return
- A maximum of one independent output
- A maximum of one magnetic amplifier post regulator that operates from the secondary winding for the main output
- Any number of linear post regulators that may operate from any output

## Design Flow

Figure 3 is an abbreviated flowchart of the major tasks in the design methodology. The important decision blocks involve the selection of the proper *TOPSwitch-GX* device for the application, and the designer's satisfaction with the overall design.

All designs begin with the definition of requirements. The next section discusses the parameters a designer needs to know before the design can start.

Parameters for the forward converter are dominated by the output specifications. The designer will have to choose a topology that is appropriate for the application. An application that calls for only one output is simplest, while a requirement for several outputs with complex loading needs careful consideration. It may be necessary to go through several designs to select the most satisfactory configuration.

Knowledge of system requirements and selection of the output topology allow the designer to compute the magnetic parameters. These are turns ratios for the transformer and the coupled inductor (if the design has an auxiliary output), plus values of inductance for independent outputs and the output inductor for the magnetic amplifier (also called mag amp). The output inductor for the mag amp is different from the inductive switching element (sometimes called a saturable reactor, saturable core, or saturable choke), that is not addressed in this note.

The peak primary current can be computed from the turns ratios established for the transformer along with the ripple current in the output inductors. This allows selection of the appropriate *TOPSwitch-GX*. It must have sufficient current limit to handle the maximum steady-state load and must have enough additional margin to accommodate peak loads and transients. Another consideration in the selection of the *TOPSwitch-GX* is power dissipation in the device. A device that can handle the steady-state and peak primary currents does not guarantee ability to meet thermal limitations – this is an independent consideration.

The efficiency of the power system is an important consideration in every design. The designer should have a goal for the efficiency of the system at the start of the design, based on reasonable allowances for power lost in the specific areas of the power supply.

The efficiency goal should take into account losses in the transformer, inductors, output rectifiers, and clamp circuits. Most high power designs have some form of power factor correction (PFC). The type of PFC will affect the efficiency. For example, the voltage drop on a passive PFC (a large inductor in series with the AC line input) will reduce the minimum input voltage at the converter, and will also reduce system efficiency.

Total system efficiency should consider losses in the AC input circuit, including the EMI filter, that are not part of this design methodology. Only a bench evaluation can determine the actual efficiency of the power supply. If the efficiency is not satisfactory, the designer must revise the values of component parameters or change the output topology for a repeat design.

If the requirements call for a holdup time, the designer must determine the amount of bulk input capacitance that is required to achieve the specified holdup time from the designated input voltage. It is often necessary to adjust parameters by iteration to meet the objectives of the design.

*PI Expert* performs the calculations to allow the designer to see the interactions of the variables immediately.

After the values of the major power components are determined, the designer needs to check voltage and current stress to select components with the proper ratings. Then the designer can choose values for small signal components that set voltage detection thresholds and other control parameters.

The final step is an evaluation of a prototype on the bench. This is the only way to confirm that the design is satisfactory, and to get necessary information to adjust the parameters if a redesign is necessary.

## Definition of Variables

Table 1 gives a set of system parameters that should be known at the start of the design. The list is general, so all the parameters will not necessarily be relevant to all applications. Some values will be given by the system specification, while others are the designer's choice.

The notation in this document uses descriptive subscripts to keep track of variables. Quantities that refer to the main output are designated with the subscript $_{MAIN}$. Variables associated with an auxiliary output are identified by the subscript $_{AUX}$, and those related to an independent output have the subscript $_{IND}$.

| Name | Description |
|---|---|
| $\eta$ | Total system efficiency |
| $f_L$ | AC mains frequency |
| $f_S$ | *TOPSwitch-GX* switching frequency |
| $I_{AUX}$ | Current from auxiliary output |
| $I_{IND}$ | Current from independent output |
| $I_{MAIN}$ | Current from main output |
| $I_{MAINMA}$ | Current from magnetic amplifier |
| $t_H$ | Holdup time |
| $V_{ACMAX}$ | Maximum AC input voltage |
| $V_{ACMIN}$ | Minimum AC input voltage |
| $V_{ACNOM}$ | Nominal AC input voltage |
| $V_{ACUV}$ | AC under-voltage threshold |
| $V_{AUX}$ | Auxiliary output voltage |
| $V_{AUXREF}$ | Auxiliary output reference voltage |
| $V_{DROPOUT}$ | Lowest DC bus voltage for regulation |
| $V_{DSOP}$ | Maximum drain-to-source voltage |
| $V_{HOLDUP}$ | DC bus voltage at start of $t_H$ |
| $V_{IND}$ | Independent output voltage |
| $V_{MAIN}$ | Main output voltage |
| $V_{MAINMA}$ | Magnetic amplifier output voltage |

*Table 1. System Parameters Needed to Start a Design.*

These conventions are used to identify voltages, currents, and components.

When there is more than one output in a category, the individual members are distinguished by numbers appended to the subscript, as in $_{IND1}$, $_{IND2}$ and $_{IND3}$ for three independent outputs. Quantities related to the magnetic amplifier have $_{MA}$ appended to the subscript, as in $_{MAINMA}$ referring to the magnetic amplifier on the secondary winding for the main output. This notation has the generality necessary to expand the allowable output options.

Turns ratios on magnetic components are designated by lower case n with appropriate subscripts, while actual numbers of turns are distinguished by upper case N with identifying subscripts.

There are a few other variables and notations that need definition. Figure 4 shows a section of output circuitry that identifies some important electrical quantities. Each output of a forward converter has two diodes. One is designated the forward diode and the other is the catch diode. Associated quantities have $_F$ or $_C$ appended to their respective subscripts.

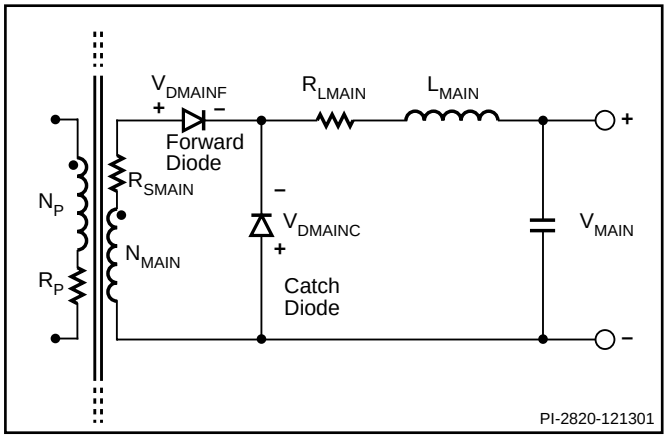



*Figure 4. Output Circuit with Parameter Definitions.*

Voltage drops on diodes have subscripts with the prefix $_D$ for the conduction drop and $_{PIV}$ for the reverse blocking voltage. The only exception to this convention is for drain-to-source voltages, which will be obvious from context.

Figure 4 also shows series resistances that the designer can include to get better predictions of performance.

## Detailed Design Procedure

This methodology guides the designer through a procedure that determines parameters for prototype hardware. After bench evaluation, the designer refines the parameters to meet all requirements.

The design can start with knowledge of only the most basic system requirements. For example, the forward voltage drops on diodes and the resistances of transformer windings are seldom known very accurately at the beginning of a new design. Results of the design with default values will guide the designer to select particular components with known parameters. Figure 5 gives an expanded flowchart that includes the detailed steps which follow.

**Step 1. Establish system requirements.**
Determine the parameters in Table 1. These should be available from a system specification of the power supply's application.

The software will compute and display the maximum and minimum DC bus voltages to the converter from the AC inputs. The need to know maximum and minimum voltages is obvious. The optional nominal input voltage $V_{ACNOM}$ helps determine the turns ratios of the transformer. The goal is to set the unregulated output voltages at their nominal values when the input is at its nominal value. The designer may choose any value between $V_{ACMAX}$ and $V_{ACMIN}$ to be the nominal value.

The peak DC bus voltage (non-doubled) is

$$V_{MAX} = V_{ACMAX}\sqrt{2} \qquad (1)$$

while the DC bus voltage at the valley of the ripple at the minimum steady state AC input is

$$V_{MIN} = \sqrt{2V_{ACMIN}^2 - \frac{2P_O\left(\frac{1}{2f_L} - t_C\right)}{\eta_{DC}C_{IN}}} \qquad (2)$$

where $P_O$ is the total output power, $t_C$ is the conduction time of the bridge rectifier, $\eta_{DC}$ is the efficiency exclusive of losses in the AC input circuit, and $C_{IN}$ is the capacitance at the input to the converter. Use 3 ms for $t_C$ and use the total system efficiency $\eta$ for $\eta_{DC}$ if no better estimates are available. A good initial value for $C_{IN}$ is 1 μF per watt multiplied by $P_O$.

The designer should carefully choose the value of $t_C$ when using passive PFC input (a large inductor in the AC line), since this approach significantly increases the diode conduction time. Also, the voltage waveform will deviate from a sinusoid, causing some error in the prediction of Equations (1) and (2).

Remember to use the input voltage to linear regulators, not the regulated output voltage, to compute the total output power. The dissipation in the linear regulator is part of the load on the converter.

The nominal DC bus voltage is defined to be

$$V_{NOM} = \frac{\sqrt{2}}{2}\left[V_{ACNOM} + \sqrt{V_{ACNOM}^2 - \frac{P_O\left(\frac{1}{2f_L} - t_C\right)}{\eta_{DC}\,C_{IN}}}\right] \qquad (3)$$

This is simply the midpoint between the peak and valley of the ripple voltage on the input capacitor (non-doubled).

**Step 2. Set ripple current in the output inductors.**
Choose the ripple current factor $K_{\Delta I}$. Figure 6 shows how it is related to the average output current. $K_{\Delta I}$ is a useful parameter for design because it directly influences the size of the output inductor. It also affects the peak primary current and the RMS current in the output capacitors.

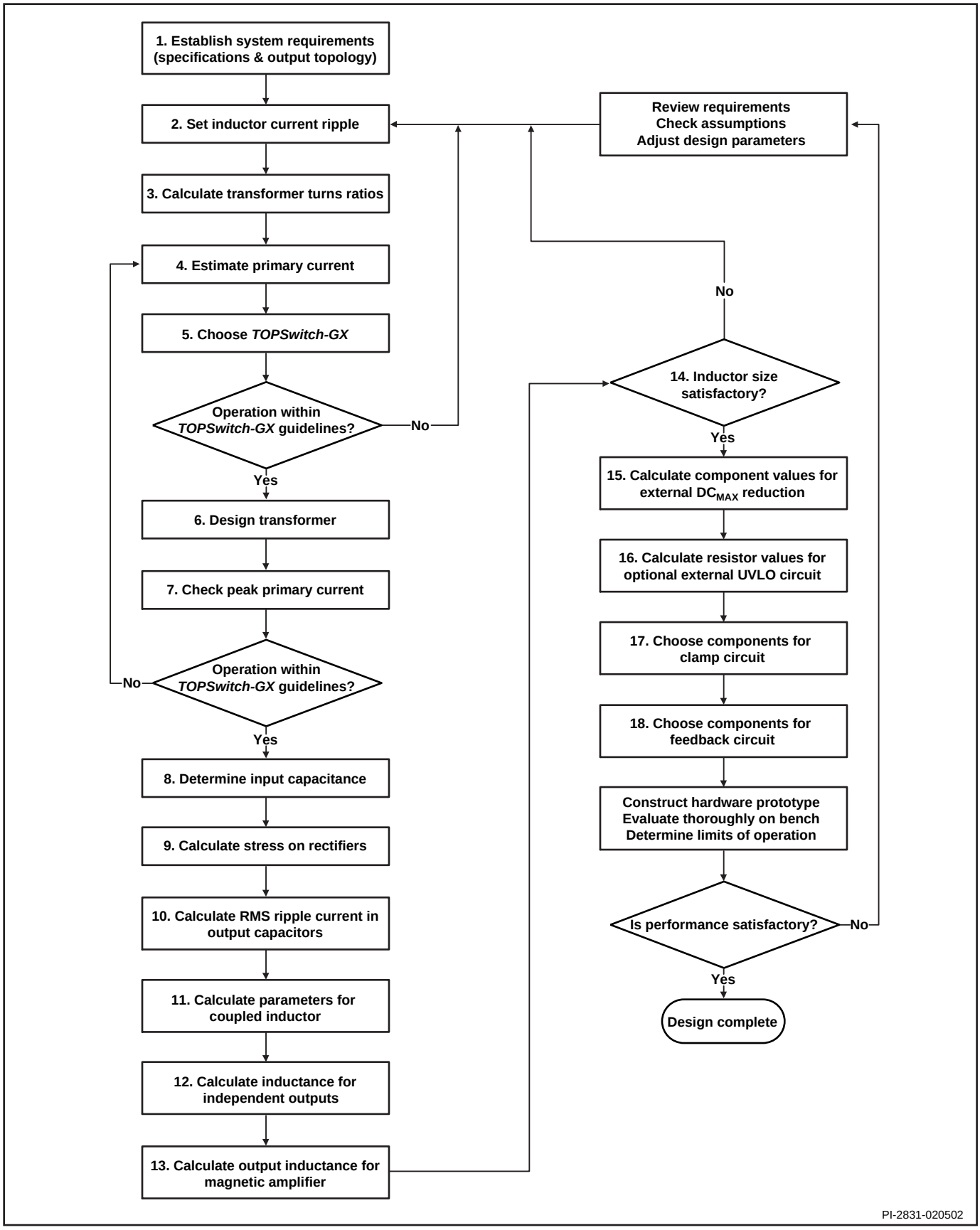



*Figure 5. Expanded Flow Chart Showing Detailed Steps in Forward Design Methodology.*

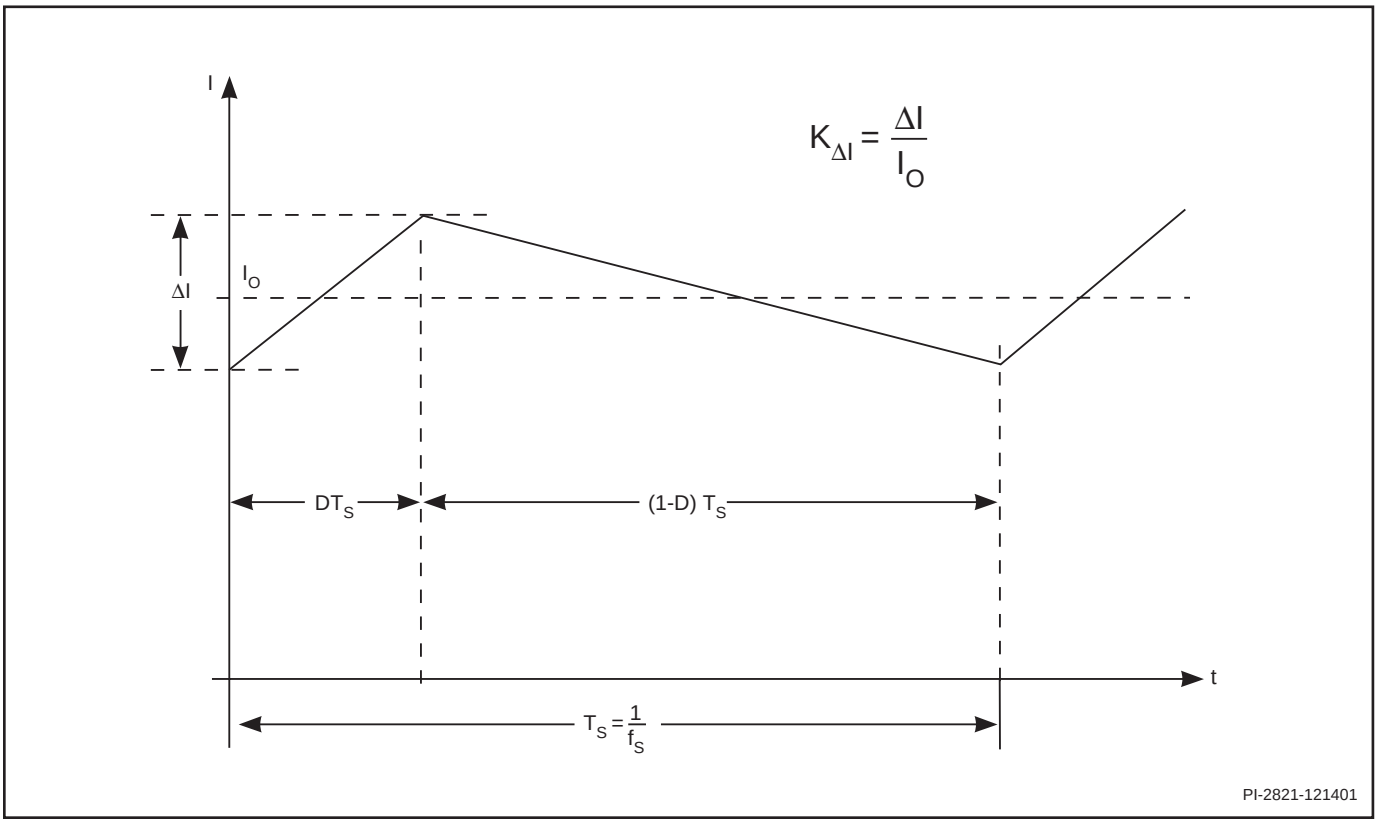



*Figure 6. Inductor Current Showing Definition of $K_{\Delta I}$.*

The ripple current in the inductor depends on the converter's operating point. In general, $K_{\Delta I}$ will change with the duty ratio according to the relationship

$$K_{\Delta I} = K_{\Delta I0}(1 - D) \qquad (4)$$

where $K_{\Delta I0}$ is the limit as the duty ratio approaches zero. The expression that relates $K_{\Delta I0}$ to the inductance L for a given generic output is

$$K_{\Delta I0} = \frac{V_{OUTPUT} + V_{D(OUTPUT)C}}{LI_{OUTPUT} f_S} \qquad (5)$$

where $V_{D(OUTPUT)C}$ is the voltage on the catch diode when it is conducting.

$K_{\Delta I}$ will be between 0.15 and 0.3 for most practical designs. The $K_{\Delta I}$ corresponding to the highest input voltage is used for calculations. All dependent quantities should then be computed for the designer's inspection. Since the duty ratio at the highest input voltage will usually be very small, $K_{\Delta I0}$ is usually a very good approximation to the worst case $K_{\Delta I}$.

If any outputs have nonzero minimum load, use the minimum load as a guide for the upper limit on $K_{\Delta I}$. The best regulation across multiple outputs at minimum load is obtained when

$$K_{\Delta I} \le 2\left(\frac{I_{MINIMUM}}{I_{MAXIMUM}}\right) \qquad (6)$$

where $I_{MINIMUM}$ and $I_{MAXIMUM}$ are the respective minimum and maximum average output currents.

The common $K_{\Delta I}$ at full load allows calculation of the inductance. The designer has the option to change any value of any inductor to suit particular requirements. The change in inductance will change the $K_{\Delta I}$ for that particular inductor.

For coupled inductors, $K_{\Delta I}$ indicates the ripple component of the total ampere turns, not ripple current on any individual winding.

**Step 3. Calculate turns ratios for the transformer.**
Turns ratios on the transformer are computed with respect to the main output winding. The primary-to-main turns ratio is fixed by the input and output voltages and the maximum duty ratio, which is limited by the maximum drain-to-source voltage that is set by the designer. The maximum duty ratio to guarantee reset of the transformer is

$$D_{MAX\_RESET} \le 1 - \frac{V_{DROPOUT}}{V_{DSOP}} \le 0.74 \qquad (7)$$

where $V_{DROPOUT}$ is the DC bus voltage at the end of the holdup time and $V_{DSOP}$ is the maximum drain-to-source voltage on the *TOPSwitch-GX* during operation. The minimum recommended value for $V_{DROPOUT}$ is 130 V, while $V_{DSOP}$ is usually less than the breakdown voltage of 700 V by a comfortable safety margin. A safety margin of 15% is typical, giving 600 V for $V_{DSOP}$.

The maximum duty ratio for the converter occurs at $V_{DROPOUT}$. This must be reduced as a function of line voltage from the $DC_{MAX}$ of *TOPSwitch-GX* by external circuitry in Step 15. The recommended maximum duty ratio $D_{MAX}$ for the forward converter application depends on the operating input voltage range. For a 3:1 operating range ($V_{MAX}$:$V_{DROPOUT}$) 70% is typical. As the operating range reduces so does the value of $D_{MAX}$. For a 2:1 operating range a value of 50% would be selected.

First, compute the turns ratios for the primary and the auxiliary winding. The turns ratio on the primary of the transformer is

$$n_P = \frac{V_{DROPOUT} - V_{DS}}{\left(V_{MAIN} + V_{DMAINC}\right)\left(\frac{1 - D_{MAX}}{D_{MAX}}\right) + V_{MAIN} + V_{DMAINF}} \quad (8a)$$

Where $V_{DS}$ is the average drain-to-source voltage during the on-time of *TOPSwitch-GX*:

When $V_{DMAINF}$ and $V_{DMAINC}$ are the same value $V_{DMAIN}$, this equation simplifies to:

$$n_P = \frac{\left(V_{DROPOUT} - V_{DS}\right)D_{MAX}}{V_{MAIN} + V_{DMAIN}} \quad (8b)$$

The turns ratio for the auxiliary winding is

$$n_{AUX} = \frac{V_{AUX} + V_{DAUXC} - V_{AUXREF}}{V_{MAIN} + V_{DMAINC}} \quad (9)$$

Equation (8) is valid for systems where the leakage inductance of the transformer is negligible. This is a reasonable assumption because the leakage inductance must be minimized for low power dissipation and proper operation of the clamp circuit. Leakage inductance reduces the effective duty ratio on the secondary circuits by delaying the turn-off of the catch diodes. The effect can be significant in designs with very high output currents. To compute the turns ratio for the primary winding when leakage inductance is a consideration, subtract the constant

$$\delta_D = \frac{L_{MAINLK} I_{MAINSEC}}{V_{MAIN}} D_{MAX} f_S \quad (10)$$

from $D_{MAX}$ in Equation (8). In Equation (10), $L_{MAINLK}$ is the leakage inductance of the secondary winding of the main output, $I_{MAINSEC}$ is the winding current required to turn off the catch diode of the main output, and $f_S$ is the switching frequency. Note that in the DC stacked connection for the auxiliary output, the winding for the main output carries the current of the main output plus the current of the stacked auxiliary outputs.

Next, compute the duty ratio $D_{NOM}$ that corresponds to the nominal input voltage.

$$D_{NOM} = \frac{V_{MAIN} + V_{DMAINC}}{\frac{V_{NOM}}{n_P} - V_{DMAINF} + V_{DMAINC}} \quad (11)$$

This allows a better estimate of the turns ratio that will produce the desired independent output voltage.

$$n_{IND} = \frac{V_{IND} + V_{DINDF}\,D_{NOM} + V_{DINDC}\left(1 - D_{NOM}\right)}{V_{MAIN} + V_{DMAINF}D_{NOM} + V_{DMAINC}\left(1 - D_{NOM}\right)} \quad (12)$$

Finally, compute the turns ratio for the bias winding so that the bias voltage is greater than eight volts. This value is the CONTROL pin voltage, 5.8 V, plus the 2.2 V saturation voltage of the optocoupler's phototransistor at $V_{DROPOUT}$.

The turns ratio for the bias winding is then

$$n_B \geq n_P\left(\frac{8\text{ volts} + V_{DB}}{V_{DROPOUT}}\right) \quad (13)$$

where $V_{DROPOUT}$ is the minimum DC bus voltage for regulation and $V_{DB}$ is the voltage drop on the rectifier for the bias voltage. Check that the breakdown voltage on the phototransistor of the optocoupler is higher than the bias voltage at the highest transient input voltage.

**Step 4. Calculate the primary current.**
Find the peak and RMS values for the primary current. This is a preliminary estimate from the system parameters. It allows the designer to assess the suitability of his application for *TOPSwitch-GX* as early as possible.

Figure 7 shows typical primary current waveforms for forward converters with and without a magnetic amplifier post regulator. Figure 7(a) is without a magnetic amplifier, whereas Figure 7(b) shows the effect of one magnetic amplifier post regulator. *TOPSwitch-GX* determines the duty ratio D to regulate the main output, whereas the post regulator sets $D_{MA}$ independently by its own local feedback to regulate the output voltage from the magnetic amplifier.

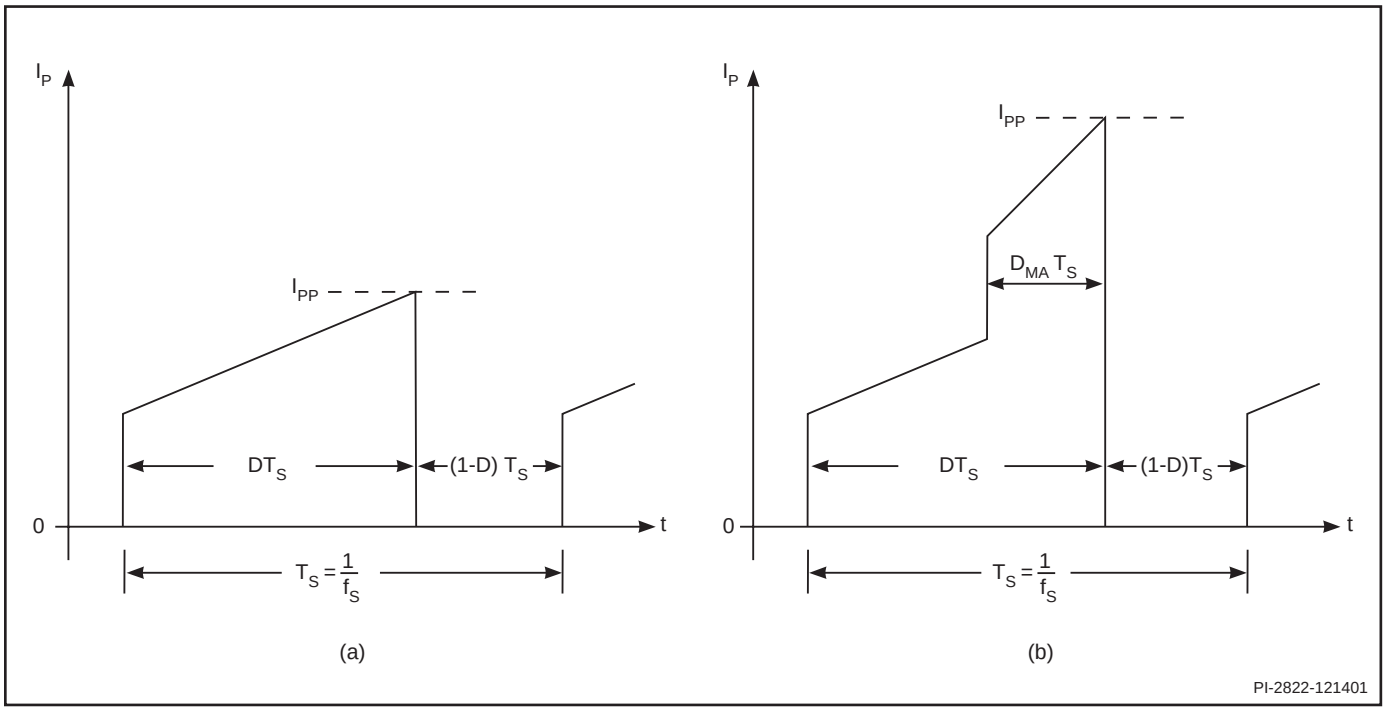



*Figure 7. Typical Primary Current Waveforms for a Converter Without Magnetic Amplifier (a) and with a Mag Amp (b).*

The computation is simply the reflection of peak currents in the secondary circuits by the ideal turns ratios of the transformer. Using the principle that the sum of the ampere turns for an ideal transformer is zero, the instantaneous primary current for a transformer with W secondary windings is just

$$I_P = \frac{1}{n_P}\sum_{j=1}^{W} i_j n_j \qquad (14)$$

where $i_j$ is the current in the secondary winding with turns ratio $n_j$. Thus, for a transformer with three secondary windings, the primary current would be the sum $i_1n_1+i_2n_2+i_3n_3$ divided by the turns ratio of the primary. Note that since all turns ratios are defined with respect to the main output winding, the turns ratio of the main output winding is 1. Equation (14) may also be used with the actual number of primary turns $N_p$ substituted for the turns ratio $n_p$, and the actual secondary turns $N_j$ substituted for the turns ratios $n_j$.

This estimate does not include the effect of magnetizing current in the transformer, which will be determined after the transformer is designed. The magnetization current will raise the peak value of this estimate by typically less than 10% worst case.

The computation in *PI Expert* includes the ripple current in the output inductors to find the peak primary current. Ripple current is ignored to calculate the RMS value. The resulting error in the RMS current is less than 1% for practical values of inductance and current. The RMS current is computed at the duty ratio that corresponds to $V_{ACMIN}$ because worst case steady-state resistive losses occur at that operating point.

**Step 5. Choose the appropriate *TOPSwitch-GX* device.**
Select a *TOPSwitch-GX* according to the requirements for peak primary current and acceptable power dissipation. For operation of the converter in continuous conduction mode it is recommended to operate the device at no more than 80% of its current limit for ordinary thermal design. To reduce device dissipation it is possible to use a *TOPSwitch-GX* device that has a lower $R_{DS(ON)}$ when the current limit is adjusted accordingly. Lowering $I_{LIMIT}$ externally (using a programming resistor to the X pin), takes advantage of the lower $R_{DS(ON)}$ of the larger device while maintaining the same level of overload protection.

The external current limit reduction factor is

$$K_I = \frac{\text{External Current Limit}}{\text{Data Sheet Current Limit}} \qquad (15)$$

where $0.4 \le K_I \le 1.0$, and is set by the value of a resistor connected between the X pin and SOURCE pin. Refer to the *TOPSwitch-GX* data sheet for details.

With external current limit reduction, the actual (external) current limit is

$$I_{XLIMIT} = I_{LIMIT}K_I \qquad (16)$$

Remember to check the maximum and minimum tolerance on $I_{LIMIT}$ from the data sheet for the selected device. Allow margin to guarantee that the peak primary current $I_{PP}$ is less than the minimum value of $I_{XLIMIT}$ at high temperature. With minimum device $I_{LIMIT}$, check that

$$I_{PP} \le 0.96\ I_{LIMIT} \text{for } K_I = 1$$
$$I_{PP} \le 0.86\ I_{XLIMIT} \text{for } K_I < 1 \quad (17)$$

Adjust the system specifications if the peak current is too high for the largest device. While some specifications are fixed, others are adjustable at the discretion of the designer. Raising the minimum input voltage will give lower peak current.

**Step 6. Design the transformer.**

The transformer design can be either completed in-house or delegated to a qualified supplier of custom magnetics. An outside supplier needs to know the turns ratios and the recommended restrictions on flux density to start a design. Even if the ultimate design will be done outside, it is beneficial to do a rough design in-house. A proposed design with actual numbers of turns on each winding will reduce the time required to obtain a satisfactory transformer.

The maximum recommended flux density for this application is

$$B_{PEAK} \le 0.3 \text{ tesla } (3000 \text{ gauss}) \quad (18)$$

and the recommended maximum change in flux density per switching period (AC flux density) is

$$B_M \le 0.2 \text{ tesla } (2000 \text{ gauss}) \quad (19)$$

The constraint on $B_M$ sets the minimum number of turns for a particular core, while the limit on $B_{PEAK}$ restricts the maximum transient duty ratio. Although peak flux density under steady-state conditions can be calculated, the designer should allow sufficient margin to avoid saturation under transient conditions.

To start the design, select a core that is likely to meet the size and efficiency requirements of the application. Since the voltages and turns ratios are determined, all that remains is to find the actual number of turns and the size of wire for each winding.

Compute the minimum turns for the main output.

$$N_{MAIN} \ge \frac{V_{MAIN} + V_{DMAINF}}{B_M A_e f_s} \quad (20)$$

where $A_e$ is the effective area of the core. Units in the above expression are volts, tesla, meter$^2$ and hertz. Round $N_{MAIN}$ upward to the next integer value.

Compute the turns for the other power windings.

$$N_P = n_P N_{MAIN}$$
$$N_{AUX} = n_{AUX} N_{MAIN} \quad (21)$$
$$N_{IND} = n_{IND} N_{MAIN}$$

Round $N_P$ downward to the next integer. Round $N_{AUX}$ and $N_{IND}$ to the nearest integer.

Compute the turns for the bias winding.

$$N_B = N_P \left( \frac{8 \text{ volts} + V_{DB}}{V_{DROPOUT}} \right) \quad (22)$$

Round $N_B$ upward to the nearest integer value.

Designers should use copper foil instead of wire for windings of few turns that carry high current. It is very important to the success of the design to minimize leakage inductance.

Compute an estimate of the peak magnetizing current.

The primary inductance in henries is

$$L_P = \frac{\mu_0 A_e N_P^2}{\frac{\ell_e}{\mu_r} + \ell_g} \quad (23)$$

where $\mu_0$ is the permeability of free space, $A_e$ is the effective area, $\ell_e$ is the effective path length in the core and $\ell_g$ is the length of the air gap (see Zero Gap Transformer section). The dimensionless relative permeability $\mu_r$ is given by

$$\mu_r = \frac{A_L \ell_e}{400\pi A_e} \quad (24)$$

Units in the above two expressions are the SI basic units with the exception of inductance coefficient $A_L$, which has the conventional units of nH/turn$^2$.

With no gap, the primary inductance in henries is simply

$$L_{P|NO\ GAP} = A_L N_P^2 \times 10^{-9} \quad (25)$$

Now the peak magnetizing current is given by

$$I_{MP} = \frac{V_{MIN} D_{MAX}}{L_P f_S} \quad (26)$$

Units in the above expression are amperes, volts, henries and hertz. The magnetizing current should be less than 10% of the primary current for reasonable power dissipation in the clamp circuit.

Estimate the power lost in the core from the manufacturer's data on the core material, operating frequency and $B_M$. Copper losses may be estimated from the resistance and RMS current in each winding. If the estimates indicate excessive loss, repeat the design with a larger core.

### Zero Gap Transformers

For highest efficiency in this application with the simple Zener clamp circuit, it is recommended that the transformer core have no air gap. While an air gap reduces the remnant flux density and stabilizes the primary inductance, it increases the stored energy that must be processed by the clamp circuit.

With the use of a suitable reset scheme, transformer saturation is not a problem in the absence of an air gap. Using this methodology and the recommended clamp scheme, the design restricts peak flux density and the clamp circuit produces negative magnetizing current during reset.

The negative magnetizing current during reset prevents flux build-up in the transformer during successive switching periods. Even with no intentional gap in the transformer core, mechanical imperfections will always give a finite effective gap (when calculating with *PI Expert* a value of 0.02 mm is used). If an air gap is desired for other reasons, it should be as small as possible.

**Step 7. Check primary current.**

Use the actual number of turns from the design of the transformer to compute the peak and RMS current on the primary. Primary current was estimated in Step 4 with an ideal turns ratio before the transformer was designed. Add the peak of the magnetizing current to obtain actual peak of the primary current under steady-state conditions.

Designers should be aware that the primary current observed on prototype hardware may be lower than predicted because the circuit that resets the flux in the transformer allows a negative average magnetizing current, as mentioned previously in Step 6 in the section on Zero Gap Transformers. The design, however, must allow for conditions when the magnetizing current adds to the reflected secondary currents.

**Step 8. Determine the input capacitance for holdup time.**

The holdup time must be specified at a minimum voltage $V_{HOLDUP}$. This is often, but not always $V_{MIN}$. For maximum flexibility, this methodology allows the designer to determine the value of input capacitance required to obtain a given holdup time from an arbitrary input voltage.

If a DC voltage is specified to mark the beginning of the holdup time, the minimum required input capacitance is

$$C_{IN} \geq \frac{2P_O t_H}{\eta_{DC}\left(V_{HOLDUP}^2 - V_{DROPOUT}^2\right)} \qquad (27)$$

where $P_O$ is the total output power that corresponds to the efficiency at the DC bus, $\eta_{DC}$ and $t_H$ is the holdup time.

If an AC voltage $V_{ACHOLDUP}$ is specified to mark the beginning of the holdup time, the minimum required input capacitance (no doubler) is

$$C_{IN} \geq \frac{2P_O}{\eta_{DC}}\left(\frac{2\left(t_H - t_C\right) + \frac{1}{f_L}}{2V_{ACHOLDUP}^2 - V_{DROPOUT}^2}\right) \qquad (28)$$

where $t_C$ is the conduction time of the AC input rectifiers and $f_L$ is the frequency of the AC power line. Again, note that $t_C$ will increase significantly if the design has passive PFC.

The efficiency $\eta_{DC}$ excludes losses in the AC input circuit and EMI filter. No power is dissipated in the AC input circuit during the holdup time because the AC input is disconnected. The lower system efficiency $\eta$ that includes the AC input losses would give a value of $C_{IN}$ that is larger than required.

Compare the value from Equation (27) or (28) with the estimate for $C_{IN}$ in Step 1. Adjust $C_{IN}$ in Step 1 and repeat the calculations until the computed value is approximately the same as in Step 1.

**Step 9. Calculate stress on rectifiers.**

*PI Expert* calculates voltage and current stress on rectifiers for guidance in selection of appropriate components. The recommended derating factor for peak inverse voltage is 80%. Derating for the currents is generally not necessary.

Thus, the recommended voltage rating for the input bridge rectifier is

$$V_{PIVAC} = 1.25\sqrt{2}V_{ACMAX} \qquad (29)$$

Current ratings for rectifiers are average values, not RMS. The current rating for the bridge rectifier is computed from

$$I_{DAVBR} = \frac{P_O}{\eta_{DC}V_{LL}} \qquad (30)$$

where $V_{LL}$ is the average DC bus voltage at the lowest steady-state line voltage (no doubler).

$$V_{LL} = \frac{\sqrt{2}}{2}\left[V_{ACMIN} + \sqrt{V_{ACMIN}^2 - \frac{P_O\left(\frac{1}{2f_L} - t_C\right)}{\eta_{DC}C_{IN}}}\right] \qquad (31)$$

Calculations of the peak inverse voltage on the output rectifiers use $V_{MAX}$, $V_{DSOP}$, and the output voltages with the turns on the transformer windings.

Calculations of worst case average current in the catch diodes are with the duty ratio that corresponds to the maximum input voltage. A very good approximation to the average rectifier current is then just the output current. Current in the forward diodes is computed with $D_{MAX}$. Note that with DC stacked outputs, the rectifiers on the main output must conduct the sum of the currents of the main and auxiliary outputs.

In general, the stress will be different for the forward diode and the catch diode on the same output. Designers will have to consider the one with the greater stress when choosing components that contain both diodes in the same package.

**Step 10. Calculate RMS ripple currents in output capacitors.**
Currents in the output capacitors are computed at the maximum loads. In continuous conduction mode, the RMS ripple current is given by

$$I_{RMS} = \frac{K_{\Delta I} I_{OUTPUT}}{2\sqrt{3}} \qquad (32)$$

where $K_{\Delta I}$ is for the particular output under consideration. This expression is reliable for independent outputs and for a main output with no coupled inductors. For converters with auxiliary outputs, Equation (32) is only an estimate. Ripple currents in the individual windings of coupled inductors depend on magnetic coupling coefficients, parasitic voltage drops, and other quantities in the circuit that are difficult to predict. Therefore, designers must evaluate prototype hardware on the bench to confirm that the assumptions of the design are valid for a particular application.

**Step 11. Calculate parameters for the coupled inductor.**
The coupled inductor allows the auxiliary outputs to have better regulation than independent outputs, with the penalty of increased complexity of the inductor.

*PI Expert* allows two options for the topology of the auxiliary output. The auxiliary output may be referenced to the main output voltage for the best regulation or to output return when necessary. The reference must be at output return to obtain a negative auxiliary output with a positive main output.

Turns ratios for the coupled inductor are the same as the ratios for the transformer. The turns ratio of a coupled inductor for a converter that has one auxiliary output is, in terms of the actual number of turns,

$$\frac{N_{LMAIN}}{N_{LAUX}} = \frac{N_{MAIN}}{N_{AUX}} \qquad (33)$$

Inductance is computed for the winding that is on the main output. The computation is based on $K_{\Delta I}$, which considers the total ampere turns of the coupled inductor, not just the current in one winding. The inductance of the winding for the main output, valid for only the DC stacked configuration, is

$$L_{MAIN} = \frac{V_{MAIN} + V_{DMAINC}}{K_{\Delta I0}\left(I_{MAIN} + I_{AUX}\left(\frac{N_{LAUX}}{N_{LMAIN}} + 1\right)\right) f_S} \qquad (34)$$

*PI Expert* gives the designer the turns ratio, the total ampere turns, and the peak energy stored in the inductor. The designer has the option to change these parameters by adjustment of the $K_{\Delta I}$ for each inductor.

These quantities assist the designer to obtain an appropriate inductor of either his own design or one from a qualified supplier. Bench evaluation of the prototype will determine if fine adjustment of the turns is necessary in the final configuration.

**Step 12. Calculate inductance for independent outputs.**
Calculation of the inductance for independent outputs is straightforward and similar to the computation of the parameters for the coupled inductor. Design of the component is simplified because there is no turns ratio associated with an inductor that has only one winding. *PI Expert* computes the inductance and the peak stored energy. This information is useful for selection of magnetic cores from catalogs.

**Step 13. Calculate output inductance for the magnetic amplifier.**
*PI Expert* computes the output inductor for a magnetic amplifier post regulator in the same way as for an independent output. It does not address the magnetic switching element.

**Step 14. Adjust output inductors if necessary.**
The designer may modify the $K_{\Delta I}$ of any inductor to accommodate special requirements. If the value or the estimated physical size of the computed inductor is not satisfactory, adjust the individual $K_{\Delta I}$ to achieve the desired result.

**Step 15. Calculate component values for external reduction of $DC_{MAX}$.**
The maximum duty ratio ($DC_{MAX}$) of *TOPSwitch-GX* must be restricted to avoid saturation of the transformer during transient loading. A network of four resistors and a capacitor ($R_A$, $R_B$, $R_C$, $V_Z$, $R_D$ and $C_{VS}$ in Figure 1 and Figure 1 of Appendix B) determines a variable upper limit on the duty ratio. Adjustment of the maximum duty ratio with input voltage allows enough deviation beyond the steady-state operating point to respond to transients while maintaining enough time in every switching cycle for the transformer to reset.

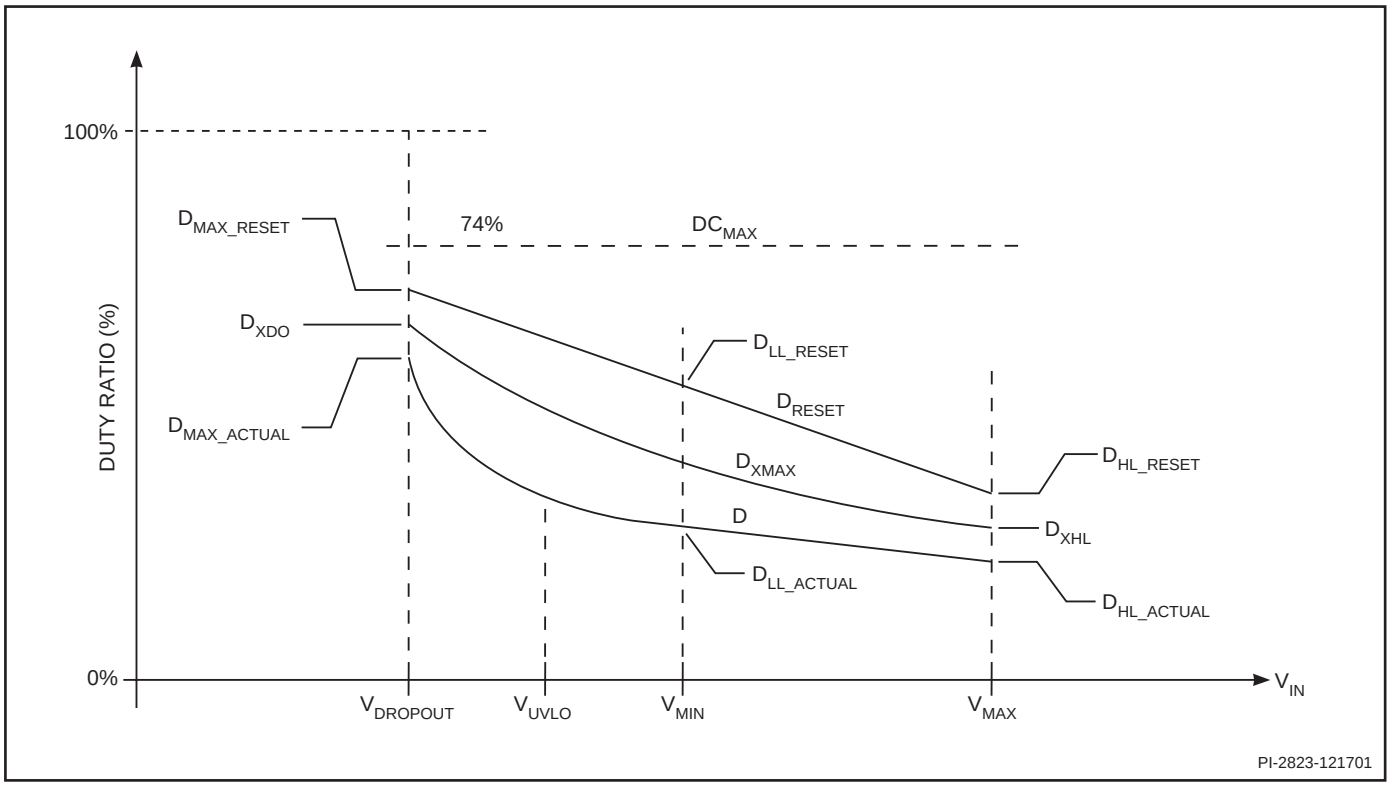



*Figure 8. Boundaries of Voltages and Duty Ratio Related to the Selection of $R_A$, $R_B$, $R_C$ and $R_D$ with $C_{VS}$ in Figure 1.*

The resistor network also sets the threshold for line under-voltage lockout. Protection from over-voltage is generally not a concern for this topology since it uses a Zener clamp to provide a hard limit on the drain-to-source voltage.

The resistors are matched to the capacitor to form an integrator with an appropriate time constant to give a cycle-by-cycle duty ratio limit. The integration of the voltage on the bias winding gives the external duty ratio limit a desirable relationship to the flux in the transformer. The circuit adjusts the duty ratio limit to set an upper bound on the volt-second product, and to balance the volt-second product during *TOPSwitch-GX* on and off times. The dynamic nature of the circuit allows greater freedom and precision in the design without interference from the line over-voltage threshold limit.

Figure 1 shows the locations of resistors $R_A$, $R_B$, $R_C$ and $R_D$ with capacitor $C_{VS}$. Several important quantities related to their values are illustrated in Figure 8. The broken vertical lines in Figure 8 mark the boundaries of the DC bus voltage for minimum and maximum operating voltages, the line under-voltage lockout threshold, and the lowest input voltage that will guarantee regulation of the output.

The broken horizontal line shows the maximum guaranteed duty cycle of *TOPSwitch-GX*. A value of 74% is recommended for design.

The lowest curve is the duty ratio D that corresponds to steady-state operation at a given input voltage. The straight line with negative slope is the maximum duty ratio $D_{RESET}$ that will still guarantee reset of the transformer for a given $V_{DSOP}$. The converter must always operate with D less than $D_{RESET}$ to avoid saturation of the transformer. The curved line between the D and $D_{RESET}$ lines is the external duty ratio limit $D_{XMAX}$ that is set by the resistors.

The designer must choose the components to set the curve of $D_{XMAX}$ at a desired position between the boundaries of $D_{RESET}$ and D for a given set of specified voltages.

*PI-Expert* prompts the user to enter several parameters that are important to the computation of the resistor values. Some parameters are from the *TOPSwitch-GX* data sheet while others are design choices. The software suggests default and typical values. The designer can enter maximum and minimum values to check worst case situations.

The components are calculated to satisfy the constraints of four parameters: $D_{XDO}$ (external duty ratio limit at $V_{DROPOUT}$), $D_{XHL}$ (external duty ratio limit at $V_{MAX}$), $V_{UVLO}$ (input voltage where the *TOPSwitch-GX* starts switching), and the maximum transient input voltage $V_{OV}$ that is greater than $V_{MAX}$.

While there are four resistors, only three are unknown because $R_A$ and $R_B$ are identical by definition. They are connected in series to keep the voltage across each one below its maximum rating. The three unknown resistors and one capacitor make four unknown quantities that are determined by the four constraints.

Figure 8 illustrates the general case where $D_{XDO}$ is between the actual duty ratio $D_{MAX\_ACTUAL}$ and $D_{MAX\_RESET}$ at the input voltage $V_{DROPOUT}$. If the converter is not required to respond to transient loads at the end of the holdup time, $D_{XDO}$ and $D_{MAX\_ACTUAL}$ can be set to $D_{MAX\_RESET}$. Since response to transient loads is usually required at $V_{MAX}$, the designer will want to set $D_{XHL}$ at a comfortable margin between $D_{HL\_ACTUAL}$ and $D_{HL\_RESET}$.

Begin with the computation of values for $R_A$ and $R_B$ to set the line under-voltage threshold $V_{ACUV}$.

$$R_A = R_B = \frac{V_{ACUV}\sqrt{2}}{2I_{UV}} \quad (35)$$

where $V_{ACUV}$ is the AC input voltage (non-doubled) required for the converter to start, and $I_{UV}$ is the line under-voltage threshold current of the L pin of *TOPSwitch-GX* from the datasheet. Choose the nearest standard resistor value for $R_A$ and $R_B$.

Define intermediate variables to make the expressions easier to write and interpret.

$$m_{IL} \equiv \frac{D_{IL1} - D_{IL2}}{I_{L2} - I_{L1}} \quad (36)$$

$$I_{LD0} \equiv \frac{D_{IL}}{m_{IL}} + I_L \quad (37)$$

$$R_{AB} \equiv R_A + R_B \quad (38)$$

$$V_{BZL} \equiv V_{DB} + V_Z + V_L \quad (39)$$

In Equation (36), $D_{IL1}$ and $D_{IL2}$ are respectively the values of $DC_{MAX}$ at currents $I_{L1}$ and $I_{L2}$ into the L pin. Obtain these values from the data sheet. Use the typical values at first. Then check that the circuit will perform properly at the high and low ends of the tolerance range.

In Equation (37), $D_{IL}$ is the value of $DC_{MAX}$ at current $I_L$ into the L pin. Use the same $D_{IL1}$ with $I_{L1}$ or $D_{IL2}$ with $I_{L2}$ as in Equation (36). Either pair will give the same result. $I_{LD0}$ has a physical interpretation that cannot be realized: if the duty ratio reduction characteristic continued along its linear slope, it would reach zero at the current $I_{LD0}$.

The voltages $V_{DB}$, $V_Z$ and $V_L$ are respectively the forward drop of the rectifier in series with the Zener diode and $R_C$, the Zener voltage, and the voltage on the L pin as shown in Figure 1. The Zener diode is chosen as required to raise the curve of $D_{XMAX}$ at the low input voltages. It may not be necessary in all applications. The Zener voltage is 6.8 V in this example.

Next, select a value for $D_{XHL}$ that is between $D_{HL\_ACTUAL}$ and $D_{HL\_RESET}$.

$$D_{HL\_ACTUAL} = \frac{V_{MAIN} + V_{DMAINC}}{\left(V_{MAX} - V_{DS}\right)\frac{N_S}{N_P} - V_{DMAINF} + V_{DMAINC}} \quad (40)$$

$$D_{HL\_RESET} = 1 - \frac{V_{MAX}}{V_{DSOP}} \quad (41)$$

Find the range of permissible values for $D_{XDO}$. To compute the upper and lower bounds on $D_{XDO}$, define the intermediate variable $K_{XDO.}$

$$K_{XDO} \equiv m_{IL}\left(I_{LD0} - \frac{V_{MAX}}{R_{AB}} - \frac{D_{XHL}}{m_{IL}}\right)\left(\frac{V_{DROPOUT}\frac{N_B}{N_P} - V_{BZL}}{V_{MAX}\frac{N_B}{N_P} - V_{BZL}}\right) \quad (42)$$

The upper bound for $D_{XDO}$ is then

$$D_{XDO} < m_{IL}\left(I_{LD0} - \frac{V_{DROPOUT}}{R_{AB}}\right) - K_{XDO} \quad (43)$$

and the lower bound for $D_{XDO}$ is

$$D_{XDO} > \frac{m_{IL}\left(I_{LD0} - \frac{V_{DROPOUT}}{R_{AB}}\right)}{1 + \frac{K_{XDO}}{D_{XHL}}} \quad (44)$$

Choose an appropriate value for $D_{XDO}$ between $D_{MAX\_RESET}$ and $D_{MAX\_ACTUAL}$ that also satisfies the boundaries of (43) and (44).

Next, compute the intermediate constants $r_1$ and $r_2$.

$$r_1 \equiv \frac{\left(V_{DROPOUT}\frac{N_B}{N_P} - V_{BZL}\right)D_{XDO}}{I_{LD0} - \frac{V_{DROPOUT}}{R_{AB}} - \frac{D_{XDO}}{m_{IL}}} \quad (45)$$

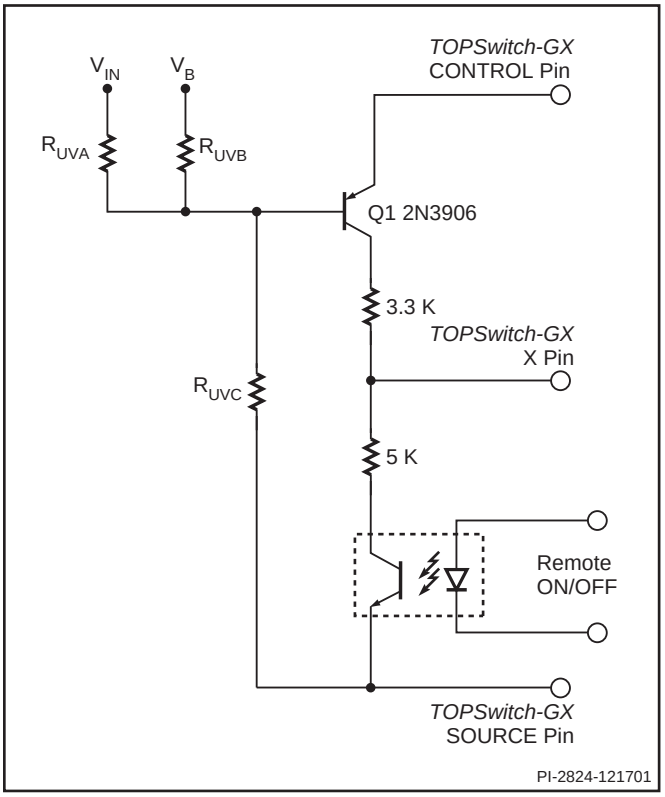



*Figure 9. External Under-Voltage Lockout Circuit.*

$$r_2 \equiv \frac{\left(V_{MAX}\frac{N_B}{N_P} - V_{BZL}\right)D_{XHL}}{I_{LD0} - \frac{V_{MAX}}{R_{AB}} - \frac{D_{XHL}}{m_{IL}}} \qquad (46)$$

Compute the values for the resistors $R_D$ and $R_C$.

$$R_D = \frac{r_1 - r_2}{D_{XDO} - D_{XHL}} \qquad (47)$$

$$R_C = r_1 - D_{XDO}R_D \qquad (48)$$

Select the nearest standard resistor values for $R_C$ and $R_D$.

Verify that the parameters are within the desired range with the actual component values.

$$V_{ACUV} = \frac{I_{UV}}{\sqrt{2}}\left(R_A + R_B\right) \qquad (49)$$

This is the AC input voltage (non-doubled) where the converter will begin to operate.

The external duty ratio limit at any DC bus voltage $V_{IN}$ may be computed from the expression

$$D_{MAX} = \frac{v_B + \sqrt{v_B^2 + 4v_Av_C}}{2v_A} \qquad (50)$$

where

$$v_A = \frac{R_D}{m_{IL}} \qquad (51)$$

$$v_B = V_{BZL} + I_{LD0}R_D - \frac{R_C}{m_{IL}} - V_{IN}\left(\frac{R_D}{R_{AB}} + \frac{N_B}{N_P}\right) \qquad (52)$$

$$v_C = R_C\left(I_{LD0} - \frac{V_{IN}}{R_{AB}}\right) \qquad (53)$$

Now choose an appropriate value for the capacitor. Proper choice of the capacitor allows the converter to operate safely with transient input voltages greater than $V_{MAX}$. The line overvoltage feature of *TOPSwitch-GX* is not used in the conventional fashion in this application. The circuit operates in an over-voltage mode that reduces the maximum duty ratio further by reduction of the switching frequency. The value of the capacitor $C_{VS}$ is chosen to give the desired behavior in the over-voltage mode.

Select an input voltage $V_{OV}$ greater than $V_{MAX}$ that marks the onset of over-voltage operation. Then compute the maximum duty ratio $D_{XOV}$ that corresponds to the specification in the *TOPSwitch-GX* data sheet for the Line Over-Voltage Threshold Current $I_{OV}$.

$$D_{XOV} = D_{IL} - m_{IL}\left(I_{OV} - I_L\right) \qquad (54)$$

Here $D_{IL}$, $m_{IL}$ and $I_L$ are the same as in Equations (36) and (37).

Finally, compute the capacitor value as

$$C_{VS} = \frac{\left(I_{OV} - \frac{V_{OV}}{R_{AB}}\right)\left(\left(1 - D_{XOV}\right)T_S - t_{R(ON)}\right)}{K_{OVHYS}I_{OVHYS}R_D} \qquad (55)$$

where

$T_S$ is the switching period $1/f_S$ in normal operation
$t_{R(ON)}$ is the Remote ON Delay
$I_{OVHYS}$ is the hysteresis of the IOV threshold
$K_{OVHYS}$ is a constant selected by the designer.

The first three parameters are taken from the data sheet. The constant $K_{OVHYS}$ is selected to provide sufficient ripple voltage

on the capacitor for reliable operation of the circuit. The recommended range for $K_{OVHYS}$ is 3 to 5. Choose the nearest standard value for capacitor $C_{VS}$.

These expressions to compute the component values have been simplified for ease of presentation. Some variables related to parasitic elements have been ignored.

If any of the results are not satisfactory, choose different standard values for the resistors or a different voltage for the Zener diode. Gross deviations from the desired results may require different values for the parameters chosen at the beginning of this step, since some sets of parameters may not be compatible.

**Step 16. Calculate values for resistors in optional external under-voltage lockout circuit.**

The resistor network that determines the characteristics of the external duty ratio limit sets the minimum voltage where the converter begins to operate. The contributions of current from the bias voltage create too much hysteresis for the circuit to be useful as an under-voltage detector after the converter begins to operate. Therefore, the external under-voltage circuit in Figure 9 is recommended for applications where a positive turn-off threshold is desired.

Choose a value $V_{ACUVL}$ for the turn-off threshold and a value $V_{ACUVX}$ that is approximately midway between $V_{ACUVL}$ and $V_{ACUV}$:

$$V_{ACUVL} < V_{ACUVX} < V_{ACUV} \qquad (56)$$

The corresponding DC bus voltages (non-doubled) are

$$V_{UVX} = V_{ACUV}\sqrt{2} \qquad (57)$$

$$V_{UVX} = V_{ACUVX}\sqrt{2} \qquad (58)$$

$$V_{UVL} = \sqrt{2V_{ACUVL}^2 - \frac{2P_O\left(\frac{1}{2f_L} - t_C\right)}{\eta_{DC}\, C_{IN}}} \qquad (59)$$

Define the intermediate variable $v_1$ that considers the voltage $V_{C(SHUNT)}$ on the CONTROL pin and the base-emitter voltage on the transistor.

$$v_1 = V_{C(SHUNT)} - V_{BEQ1} \qquad (60)$$

Compute the approximate value of $R_{UVA}$ to meet the constraint of maximum power dissipation. Assume a 50% derating for a resistor that can dissipate $P_{RUVA}$ watts.

$$R_{UVA} = \frac{2V_{MAX}^2}{P_{RUVA}} \qquad (61)$$

A typical resistor for this purpose will have a power rating of $P_{RUVA}$ = 125 mW. Choose the nearest standard value for $R_{UVA}$.

Then compute $R_{UVB}$ and $R_{UVC}$.

$$R_{UVB} = R_{UVA}\left(\frac{\frac{N_B}{N_P}V_{UVL} - v_1}{V_{UVX} - V_{UVL}}\right) \qquad (62)$$

$$R_{UVC} = R_{UVA}\left(\frac{v_1}{V_{UVX}}\right) \qquad (63)$$

Choose the nearest standard values for $R_{UVB}$ and $R_{UVC}$. Then check $V_{ACUVL}$ and $V_{ACUVX}$ with the actual resistor values.

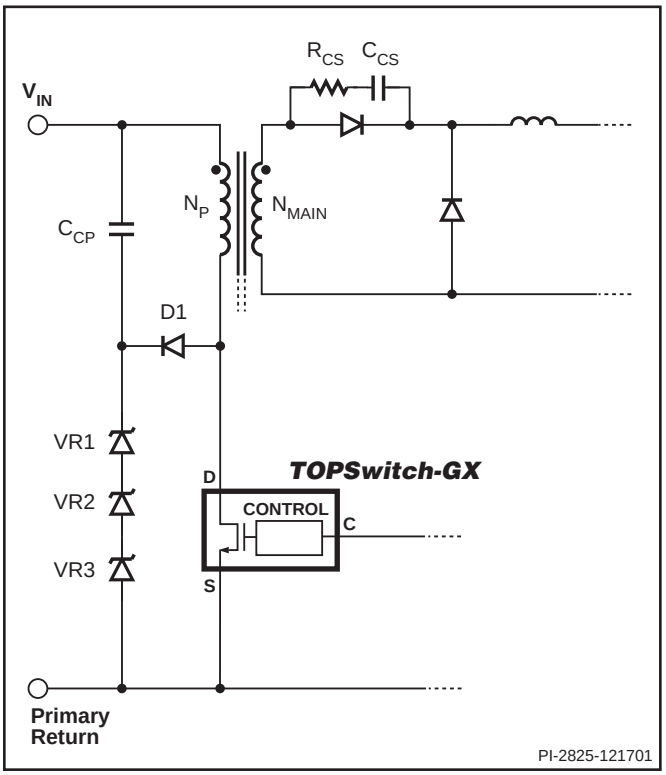



*Figure 10. Recommended Clamp Circuit.*

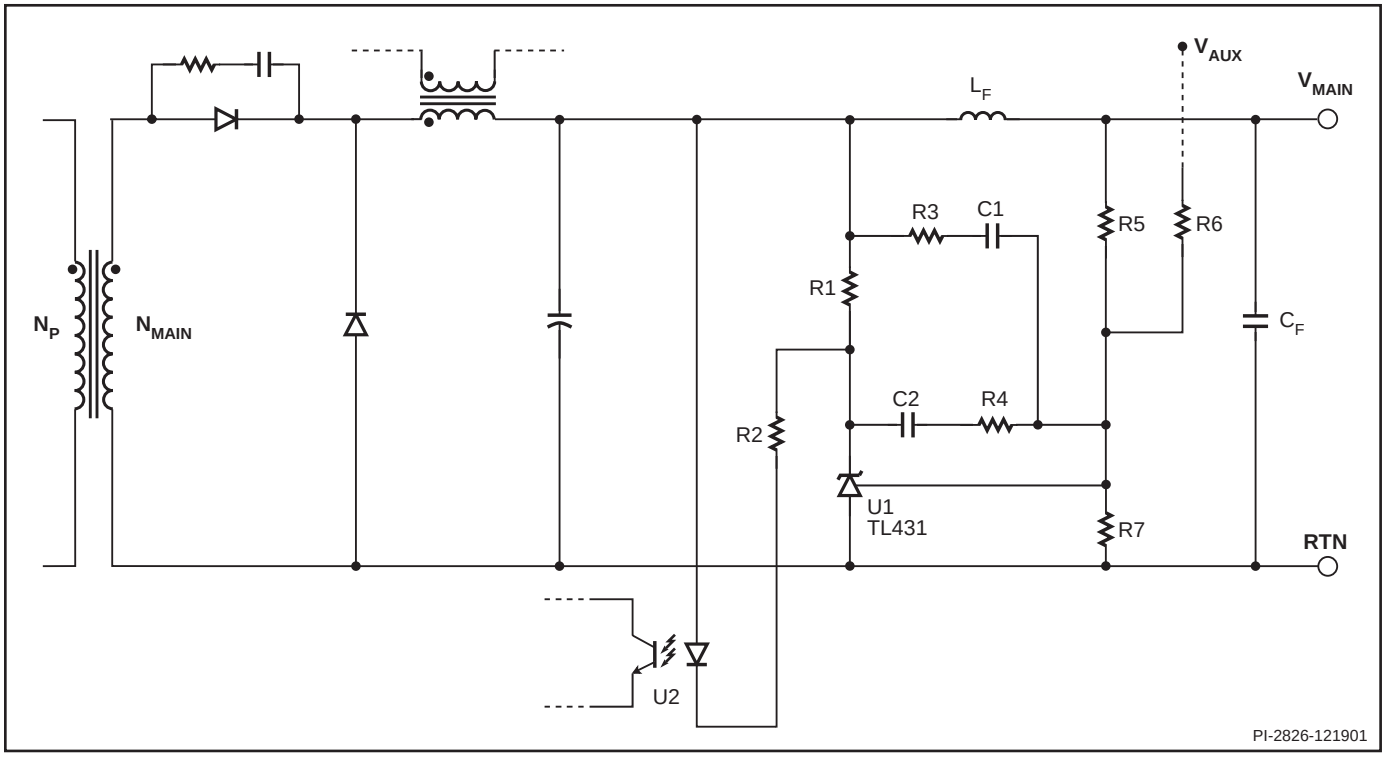



*Figure 11. General Configuration of Feedback Circuit for Forward Converter with TOPSwitch-GX.*

$$V_{UVL} = \frac{v_1\left(\frac{R_{UVB}}{R_{UVC}} + 1\right)}{\frac{R_{UVB}}{R_{UVA}} + \frac{N_B}{N_P}} \qquad (64)$$

$$V_{ACUVL} = \sqrt{\frac{V_{UVL}^2}{2} + \frac{P_O\left(\frac{1}{2 f_L} - t_C\right)}{\eta_{DC}\, C_{IN}}} \qquad (65)$$

$$V_{ACUVX} = \frac{v_1}{\sqrt{2}}\left(1 + \frac{R_{UVA}}{R_{UVC}}\right) \qquad (66)$$

If $V_{ACUVL}$ and $V_{ACUVX}$ are not satisfactory, adjust the values of the resistors.

**Step 17. Choose components for the clamp circuit.**
Figure 10 shows connections for the elements of a Zener clamp circuit that is suitable for many applications. Capacitor $C_{CP}$, diode D1 and the string of Zener diodes are on the primary side of the transformer. Resistor $R_{CS}$ and capacitor $C_{CS}$ are on the secondary side of the transformer.

This arrangement limits the voltage on the drain of the *TOPSwitch-GX* to approximately the sum of the voltages of the string of Zener diodes. It also recovers most of the energy from leakage inductance and magnetization inductance, and returns it to the input or delivers it to the output.

Select the Zener diodes to limit the drain voltage to $V_{DSOP}$. Choose the voltage, size and number of diodes in the string to achieve the desired $V_{DSOP}$ and to handle the power dissipation. This arrangement is adequate for applications where the clamp circuit dissipates less than 5 W.

Capacitor $C_{CP}$ supplements the natural stray capacitance on the drain node to absorb energy that comes mostly from the leakage inductance. The value must be selected empirically because it is difficult to predict natural stray capacitance and leakage inductance accurately enough to calculate a proper value. Energy not absorbed by the capacitance will be dissipated in the Zener string, so $C_{CP}$ cannot be too small. If $C_{CP}$ is too large, its voltage will change too slowly to allow the transformer to reset during transients. Typical values for $C_{CP}$ are in the neighborhood of 2 nF.

Diode D1 must be a slow recovery type such as a 1N5407. The recovery of D1 removes enough charge from $C_{CP}$ to stabilize its voltage and to discharge some of its stored energy into the primary of the transformer. This energy returns to the input on the next switching cycle.

The remaining components are connected across the forward diode on the main output. Energy from leakage inductance on the secondary and magnetization inductance of the transformer charges $C_{CS}$ when the *TOPSwitch-GX* turns off. The energy from $C_{CS}$ is delivered to the output during the next switching cycle. Resistor $R_{CS}$ provides damping for oscillations that would otherwise occur from the resonance of $C_{CS}$ with stray inductance.

Typical values are in the neighborhood of 0.1 µF for $C_{CS}$ and 1 Ω for $R_{CS}$. The resistor must dissipate power that corresponds to the charge and discharge of $C_{CS}$ each cycle. It typically will dissipate less than 1 watt. Proper values must be determined empirically from evaluation of prototype hardware.

**Step 18. Choose components for the feedback circuit.**
The pulse width modulator in *TOPSwitch-GX* sets the duty ratio according to the current into the CONTROL pin. *TOPSwitch-GX* senses the drain current for protection only, and does not use it for control purposes. Thus, forward converters with *TOPSwitch-GX* operate with a voltage-mode control that modulates the converter's duty ratio directly according to an error signal from the regulated output voltage. Voltage mode control provides sufficient loop bandwidth and is fully able to meet all the specifications for PC Main and other high power applications.

The general configuration of the feedback circuit for a forward converter with *TOPSwitch-GX* is illustrated in Figure 11. It shows a typical connection of a TL431 voltage regulator with an optocoupler and components for frequency compensation. There is an optional connection to $V_{AUX}$ to improve the regulation of the auxiliary output by sharing regulation with the main output. This general technique is common in all types of multiple output regulators.

While the design of the feedback loop is beyond the scope of this application note, it is useful to consider the general circuit of Figure 11. The components are chosen to provide regulation of output voltages and to shape the frequency characteristics of the control loop. Proper design of the feedback components is important not only for the stability of the system, but also for transient response of the output.

Inductor $L_F$ with capacitor $C_F$ reduces high frequency noise on the main output. As such, it introduces phase shift in the small signal response that would make loop compensation difficult if the only feedback for the main output were taken from the voltage on $C_F$. To avoid difficulties with the feedback loop, information about the main output is taken from two places.

Low frequency information that is most important to the DC regulation comes mainly through the path formed by resistor divider of R5, R6 and R7. The voltage on R7 is the reference voltage of the TL431 when $V_{MAIN}$ and $V_{AUX}$ are at their desired values.

High frequency information that is most important in the transient response comes through the path formed by the optocoupler's diode and R2. This same technique is commonly used with *TOPSwitch-GX* in flyback converter applications.

The values of R1, R3, R4, C1 and C2 are chosen to shape the frequency response. The choices are influenced by the components on the CONTROL pin and equivalent series resistance of the output capacitor, which can be important features of the loop gain. Designers must make proper measurements of loop gain and transient response on prototype hardware to confirm that the converter performs as desired under all specified conditions.

## Evaluation of Prototype Hardware

The design that results from the steps of the previous section contains the uncertainties of the initial assumptions. Performance must be validated with measurements on prototype hardware before the design is complete.

At this stage in the procedure, the designer will have enough information to build a circuit that will operate at nominal conditions for evaluation on the bench. The designer must test the circuit at all the limits of specified performance. Measurements will indicate which changes to the original assumptions are necessary. A successful design is obtained after repetition of the procedure with parameters adjusted from measurements on the hardware.

The evaluation should include observation of the drain-to-source voltage on *TOPSwitch-GX* under steady state operation and transient conditions. Apply power to the converter slowly with minimum loads. Then exercise the loads on the outputs in different combinations, first at the nominal input voltage and then at the extremes of input voltage.

Observe the behavior at various static loads before going to transient loading. Check for excessive power dissipation in the clamp circuit. A useful technique is to monitor the average current in the string of Zener diodes in the clamp circuit with a low value resistor in series. A capacitor in parallel with the resistor will develop a voltage proportional to the average current through the diodes. The product of this voltage and the clamp voltage gives an indication of the power dissipation in the Zener diodes.

Monitor the drain current when the output has steady-state overload and during transient loading. The waveform will provide important information about the operation of the converter and the limits of the design. Check that the current

limit of the *TOPSwitch-GX* is sufficient for all the specified conditions.

Check that the transformer does not saturate under all steady-state combinations of line and load. Verify the proper design of the circuit to limit maximum duty ratio with the procedure in Appendix B.

Check the ripple on all the output voltages with several combinations of input voltage and output loading, particularly if the design uses a coupled inductor. Verify that the under-voltage thresholds are within design limits for startup and for shutdown.

## Key Design Considerations

While the design of forward converters with *TOPSwitch-GX* has much in common with designs that use discrete transistors and controllers, some important differences must be considered. Attention to these items will significantly reduce the time to arrive at a successful design.

- A proper clamp circuit is required to control the maximum drain voltage. Resonant clamp circuits are not recommended. While the example clamp circuit in this document is suitable for moderate power levels, the circuit will need modification to adapt to applications that require the dissipation of more power.

- Leakage inductance of the transformer affects the power dissipation in the clamp circuit. High leakage inductance will prohibit the use of simple clamp circuits. Be aware that a magnetic amplifier post regulator will greatly increase the effective leakage inductance of the transformer.

- The primary inductance of the transformer affects the power dissipation in the clamp circuit. Maximize the primary inductance to reduce the magnetizing current and the energy that must be processed by clamp circuit.

- Use a slow diode for the rectifier D1 in the clamp circuit. A fast diode will greatly increase the amount of energy that the clamp must dissipate.

- Remember that the components $R_{CS}$ and $C_{CS}$ on the secondary are important components of the clamp circuit. Failure to include this network will cause excessive power dissipation in the clamp components on the primary.

- Confirm in bench evaluations that $C_{CP}$ in the clamp circuit on the primary is not too large. Perform transient load tests at low and high input voltages. Monitor the drain voltage waveform for volt-second balance to be certain that the transformer does not saturate.

- Check the temperature of the Zener diodes VR1, VR2 and VR3 in the clamp circuit under maximum load at low input voltage and with repetitive transient loading. If the power supply does not have a latching shutdown for fault conditions, check it under a sustained short circuit on the output. There could be excessive heating if $C_{CP}$ is too small, the primary inductance of the transformer is too low, or if the leakage inductance it too high.

- Match the current limit to the load. Use the X pin to program the current limit lower, especially if a larger *TOPSwitch-GX* is selected for thermal or efficiency reasons.

## References

[1] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, Second Edition. Kluwer Academic Publishers, 2001. ISBN 0-7923-7270-0.

[2] Colonel Wm. T. McLyman, Transformer and Inductor Design Handbook, Second Edition. Marcel Dekker, Inc., 1988. ISBN 0-8247-7828-6.

[3] Colonel Wm. T. McLyman, Magnetic Core Selection for Transformers and Inductors, A User's Guide to Practice and Specification, Second Edition. Marcel Dekker, Inc, 1997. ISBN 0-8247-9841-4.

[4] Colonel W. T. McLyman, Designing Magnetic Components for High Frequency dc-dc Converters. Kg Magnetics, Inc., 1993. ISBN 1-883107-00-8.

[5] Micrometals Inc., 5615 E. La Palma Avenue, Anaheim, CA 92807 USA; *www.micrometals.com*.

[6] MAGNETICS, P.O. Box 391, Butler, PA 16003-0391 USA, *www.mag-inc.com*.

# Appendix A
# Table of Nomenclature

| Name in AN-30 | Description |
|---|---|
| $\delta_D$ | Difference between actual and effective duty ratio that results from leakage inductance in the transformer. |
| $\eta$ | Total system efficiency (lower case Greek letter eta). |
| $\eta_{DC}$ | Efficiency excluding losses in AC input circuit and EMI filter. Used in computation of input capacitance required for holdup time. $\eta_{DC} \geq \eta$. |
| $\mu_0$ | Permeability of free space ($4\pi$ x $10^{-7}$ H/m). |
| $\mu_r$ | Relative permeability of ferrite core material (lower case Greek letter mu). Dimensionless. |
| $A_e$ | Effective cross-sectional area of transformer core. |
| $A_L$ | Inductance coefficient of ungapped transformer core. |
| $B_M$ | Maximum AC flux density in transformer core. |
| $B_{PEAK}$ | Maximum flux density in the power transformer. |
| $C_{IN}$ | Total bulk capacitance at the DC input to the converter. |
| $C_{VS}$ | Capacitor in circuit for external reduction of $DC_{MAX}$. |
| D1 | Diode in primary clamp circuit. |
| D | Duty ratio of *TOPSwitch-GX* at a given operating point. |
| $D_{HL\_ACTUAL}$ | Duty ratio at the highest operational DC input voltage $V_{MAX}$. |
| $D_{HL\_RESET}$ | Maximum duty ratio to guarantee reset of the transformer at DC input voltage $V_{MAX}$. |
| $D_{IL}$ | Maximum duty ratio at current $I_L$. |
| $D_{IL1}$ | The $DC_{MAX}$ at current $I_{L1}$ into the L pin of *TOPSwitch-GX*. |
| $D_{IL2}$ | The $DC_{MAX}$ at current $I_{L2}$ into the L pin of *TOPSwitch-GX*. |
| $D_{LL\_ACTUAL}$ | Duty ratio at lowest steady state DC input voltage $V_{MIN}$. |
| $D_{LL\_RESET}$ | Maximum duty ratio to guarantee reset of the transformer at DC input voltage $V_{MIN}$. |
| $D_{MA}$ | The duty ratio of the magnetic amplifier. |
| $D_{MAX}$ | The maximum duty of T*OPSwitch-GX* at the lowest operational DC input voltage $V_{DROPOUT}$. |
| $D_{MAX\_ACTUAL}$ | Actual duty ratio of *TOPSwitch-GX* at the lowest operational DC input voltage $V_{DROPOUT}$. |
| $D_{MAX\_RESET}$ | Maximum duty ratio to guarantee reset of the transformer at DC input voltage $V_{DROPOUT}$. This is less than maximum duty cycle $DC_{MAX}$. |
| $D_{NOM}$ | Duty ratio at nominal input voltage. |
| $D_{RESET}$ | Maximum duty ratio to guarantee reset of the transformer at a given operating point. |
| $D_{XDO}$ | Highest maximum duty cycle as set by current into the L pin of *TOPSwitch-GX* with external components. Occurs at DC input voltage $V_{DROPOUT}$. |
| $D_{XHL}$ | The lowest maximum duty cycle as set by current into the L pin of *TOPSwitch-GX* with external components at DC input voltage $V_{MAX}$. |
| $D_{XOV}$ | The maximum duty ratio that corresponds to $I_{OV}$. |
| $DC_{MAX}$ | Maximum default duty cycle of *TOPSwitch-GX* (see Data Sheet). |
| $f_L$ | AC line frequency. |
| $f_S$ | *TOPSwitch-GX* switching frequency. |
| $i_j$ | Instantaneous current in secondary winding j of the transformer. |
| $I_{AUX}$ | Output current of the auxiliary output |
| $I_{DAVBR}$ | Current rating for the bridge rectifier. |
| $I_L$ | Current into the L pin of *TOPSwitch-GX*. |

| Name in AN-30 | Description |
|---|---|
| $I_{L1}$ | Current into the L pin of *TOPSwitch-GX* to give $DC_{MAX}$ of $D_{IL1}$. |
| $I_{L2}$ | Current into the L pin of *TOPSwitch-GX* to give $DC_{MAX}$ of $D_{IL2}$. |
| $I_{LD0}$ | Intermediate variable to compute values of components in circuit for external reduction of $DC_{MAX}$. |
| $I_{MAIN}$ | Output current of the main output. |
| $I_{MAINMA}$ | Output current of the magnetic amplifier on the secondary winding for the main output. |
| $I_{MAINSEC}$ | Current in the secondary winding of the main output required to stop conduction of the main catch diode. |
| $I_{MAXIMUM}$ | Maximum average output current for a specific output. |
| $I_{MINIMUM}$ | Minimum average output current for a specific output. |
| $I_{MP}$ | Peak value of the magnetizing current of the transformer referred to the primary winding. |
| $I_{IND}$ | Output current of the independent output. |
| $I_{OUTPUT}$ | Average current on a given output. |
| $I_{OV}$ | Line over-voltage threshold current for the L pin of *TOPSwitch-GX* (see data sheet). |
| $I_{OVHYS}$ | Hysteresis of the $I_{OV}$ threshold (see data sheet). |
| $I_P$ | Instantaneous current in the primary of the transformer. |
| $I_{PP}$ | Peak current in the primary of the transformer. |
| $I_{RMS}$ | RMS current in an output capacitor. |
| $I_{UVHYS}$ | Hysteresis in line under-voltage threshold current (see data sheet). |
| $I_{XLIMIT}$ | *TOPSwitch-GX* current limit with external current limit reduction. |
| $K_I$ | External current limit reduction factor. |
| $K_{\Delta I0}$ | Maximum theoretical value of the ripple current factor for an output inductor, approached as D goes to zero. |
| $K_{\Delta I}$ | Ripple current factor for an output inductor at a given operating point. |
| $K_{OVHYS}$ | Constant used to compute value of capacitor in circuit for external reduction of $DC_{MAX}$. |
| $K_{XDO}$ | Intermediate variable to compute values of components in circuit for external reduction of $DC_{MAX}$. |
| $\ell_e$ | Effective path length of transformer core. |
| $\ell_g$ | Length of air gap in transformer core. |
| $L_{MAIN}$ | Inductance of the coupled inductor measured at the winding for the main output with other windings open. |
| $L_{MAINLK}$ | Leakage inductance of the transformer on the secondary winding for the main output. |
| $L_{MAINMA}$ | Output inductor in the magnetic amplifier regulator on the secondary winding for the main output. |
| $m_{IL}$ | Maximum Duty Cycle Reduction Slope (a positive number). |
| $L_P$ | Inductance of the primary of the transformer with all other windings open. |
| $n_{AUX}$ | Turns ratio of the auxiliary output winding with respect to the main output winding. |
| $n_{IND}$ | Turns ratio of the independent output winding with respect to the main output winding. |
| $n_j$ | Turns ratio of secondary winding j of the transformer with respect to the main output winding. |
| $n_P$ | Turns ratio of the primary winding with respect to the main output winding. |
| $N_j$ | Actual number of turns for secondary winding j on the transformer. |
| $N_{AUX}$ | Number of turns for the auxiliary winding on the transformer. |
| $N_B$ | Number of turns for the bias winding on the transformer. |
| $N_{IND}$ | Number of turns for the independent winding on the transformer. |
| $N_{MAIN}$ | Number of turns for the main output winding on the transformer. |

| Name in AN-30 | Description |
|---|---|
| $N_P$ | Number of turns for the primary winding on the transformer. |
| $P_O$ | Total output power of the power supply. |
| $P_{RUVA}$ | Power dissipation in the resistor $R_{UVA}$. |
| $r_1$ | Intermediate variable to compute values of components in circuit for external reduction of $DC_{MAX}$. |
| $r_2$ | Intermediate variable to compute values of components in circuit for external reduction of $DC_{MAX}$. |
| $R_A$ | Resistor in the network that sets the line under-voltage threshold $V_{ACUV}$. |
| $R_{AB}$ | Intermediate variable to compute values of components in circuit for external reduction of $DC_{MAX}$. |
| $R_B$ | Resistor in the network that sets the line under-voltage threshold $V_{ACUV}$. |
| $R_C$ | Resistor in circuit for external reduction of $DC_{MAX}$. |
| $R_D$ | Resistor in circuit for external reduction of $DC_{MAX}$. |
| $R_{LMAIN}$ | Resistance of the winding of the output inductor for the main output. |
| $R_P$ | Resistance of the primary winding of the transformer. |
| $R_{SMAIN}$ | Resistance of the secondary winding for the main output. |
| $R_{UVA}$ | Resistor in optional external under-voltage lockout circuit. |
| $R_{UVB}$ | Resistor in optional external under-voltage lockout circuit. |
| $R_{UVC}$ | Resistor in optional external under-voltage lockout circuit. |
| $t_C$ | Conduction time of the bridge rectifier. |
| $t_H$ | Holdup time. |
| $t_{R(ON)}$ | Remote ON Delay of *TOPSwitch-GX*. (See data sheet). |
| $T_S$ | Switching period of *TOPSwitch-GX*, equal to $1/f_S$. |
| $v_1$ | Intermediate variable to compute resistors in optional external under-voltage lockout circuit. |
| $v_A$ | Intermediate variable to compute values of $D_{XMAX}$. |
| $v_B$ | Intermediate variable to compute values of $D_{XMAX}$. |
| $v_C$ | Intermediate variable to compute values of $D_{XMAX}$. |
| $V_{ACHOLDUP}$ | Steady state AC input voltage that corresponds to the beginning of the holdup time. |
| $V_{ACMAX}$ | Maximum steady-state AC input voltage. |
| $V_{ACMIN}$ | Minimum steady-state AC input voltage. |
| $V_{ACNOM}$ | AC input voltage where independent output voltages should be at their nominal values. |
| $V_{ACUV}$ | Minimum AC input voltage where converter must start. |
| $V_{ACUVL}$ | AC input voltage where the converter shuts off with optional external UVLO circuit. |
| $V_{ACUVX}$ | AC input voltage where the optional external UVLO circuit enables the *TOPSwitch-GX* when input voltage is rising from zero. |
| $V_{AUX}$ | Voltage on the auxiliary output. |
| $V_{AUXREF}$ | Reference voltage for the auxiliary output in the DC stacked topology. This is usually $V_{MAIN}$. |
| $V_{BZL}$ | Intermediate variable in the computation of components for $DC_{MAX}$ reduction circuit. |
| $V_{DAUXC}$ | Voltage drop on the catch diode of the auxiliary output when the diode is conducting. |
| $V_{DB}$ | Voltage drop on the diode of the bias winding when the diode is conducting. |
| $V_{DINDC}$ | Voltage drop on the catch diode of the independent output when the diode is conducting. |
| $V_{DINDF}$ | Voltage drop on the forward diode of the independent output when the diode is conducting. |
| $V_{DMAIN}$ | Voltage drop on the catch diode and the forward diode of the main output when the two are identical. |

| Name in AN-30 | Description |
|---|---|
| $V_{DMAINC}$ | Voltage drop on the catch diode of the main output when the diode is conducting. |
| $V_{DMAINF}$ | Voltage drop on the forward diode of the main output when the diode is conducting. |
| $V_{DROPOUT}$ | Lowest DC input voltage that will guarantee a regulated output. |
| $V_{DS}$ | Average drain-to-source voltage on the *TOPSwitch-GX* during its on-time. |
| $V_{DSOP}$ | Maximum drain-to-source voltage on the *TOPSwitch-GX* during operation. |
| $V_{HOLDUP}$ | DC input voltage that marks the beginning of the holdup time $t_H$. |
| $V_{IN}$ | Voltage on the bulk input capacitance $C_{IN}$. |
| $V_{IND}$ | Voltage on the independent output. |
| $V_L$ | Voltage on the L pin of *TOPSwitch-GX* with positive current. |
| $V_{LL}$ | Average DC input voltage at $V_{ACMIN}$. |
| $V_{MAX}$ | Maximum DC input voltage, equivalent to the peak value of $V_{ACMAX}$. |
| $V_{MAIN}$ | Regulated DC voltage on the main output. |
| $V_{MAINMA}$ | Regulated DC voltage from the magnetic amplifier derived from the secondary winding for the main output. |
| $V_{MIN}$ | Valley of the rectified AC input voltage at $V_{ACMIN}$. |
| $V_{NOM}$ | Nominal DC input voltage. Midpoint between peak and valley of the ripple voltage on $C_{IN}$ when the AC input voltage is $V_{ACNOM}$. |
| $V_{PIVAC}$ | Recommended voltage rating for the bridge rectifier. |
| $V_{UVH}$ | DC input voltage corresponding to $V_{ACUV}$. |
| $V_{UVL}$ | DC input voltage corresponding to $V_{ACUVL}$. |
| $V_{UVLO}$ | Minimum DC input voltage for *TOPSwitch-GX* to start, set by resistor on from DC input voltage to L pin. |
| $V_{UVX}$ | DC input voltage corresponding to $V_{ACUVX}$. |
| $V_Z$ | Voltage of the Zener diode in the $DC_{MAX}$ reduction circuit. |
| W | Number of secondary windings on the transformer. |

# Appendix B
# Procedure for Verifying Duty Ratio Reduction Circuit

Predictions from analytic expressions are only as accurate as their inputs. It is always advisable to confirm the desired operation of circuits with actual hardware before they are released to production. Reduction of the maximum duty ratio of *TOPSwitch-GX* is particularly important in the forward converter application. Therefore, users are strongly advised to follow this simple procedure to confirm the correct operation of the circuit to reduce the maximum duty ratio.

Add the circuits and instrumentation as shown in Figures B1 and B2 to the forward converter under evaluation as described in the steps below. This setup allows independent adjustment of the input voltage and the regulated main output voltage while monitoring the current into the L pin.

1. Connect the AC input section in the non-doubling configuration. Add enough extra bulk capacitance in parallel with $C_{IN}$ to make the ripple voltage negligible. Alternatively, the converter may be operated from a high voltage DC power supply instead of from the AC source. Insert the parallel combination of a 100 Ω resistor and a 0.1 μF capacitor in series with the L pin. Monitor the voltage across the resistor with a digital voltmeter. Place a 1 kΩ resistor in each lead of the voltmeter to avoid interference from common

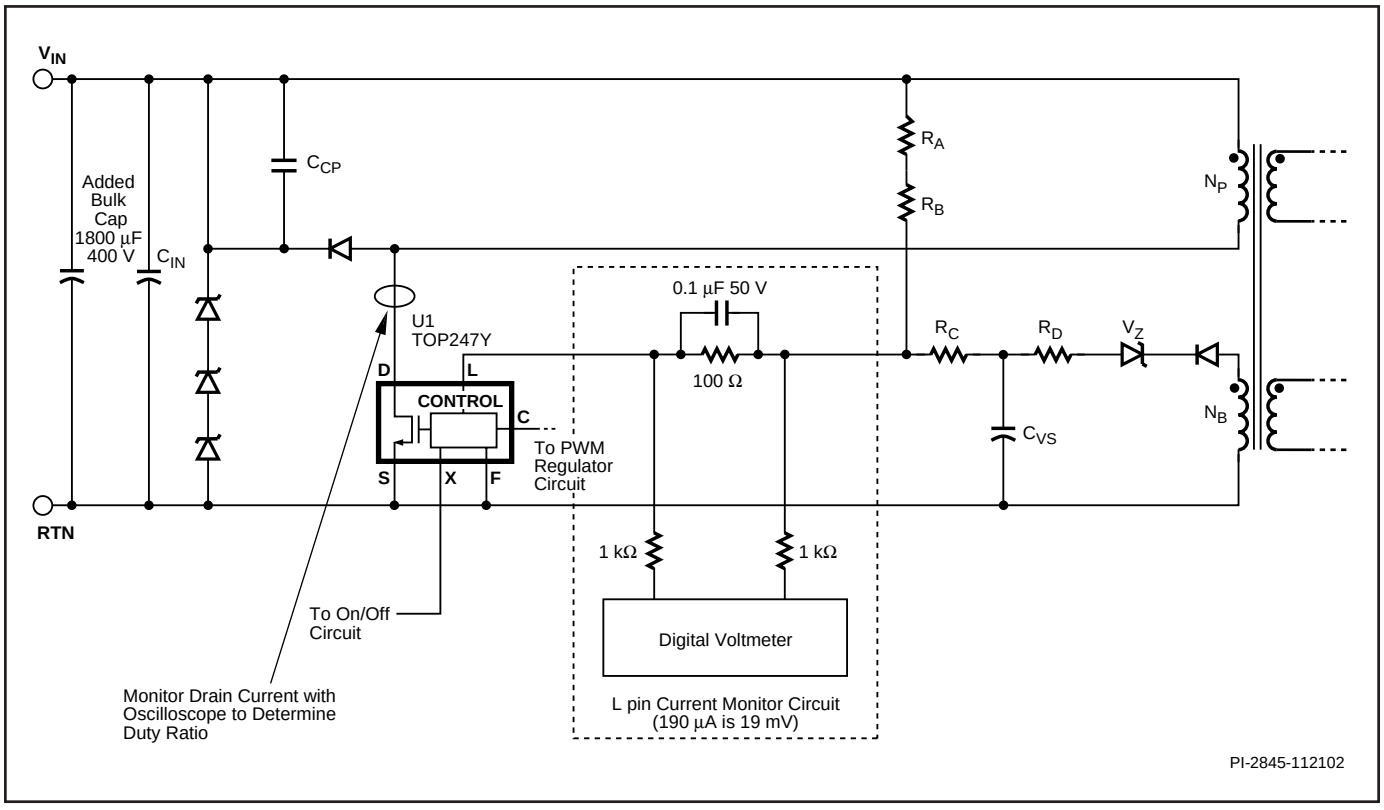



*Figure B1. Setup to Measure Current into LINE-SENSE (L) Pin.*

mode noise. Monitor the current in the DRAIN pin of *TOPSwitch-GX* with a current probe and an oscilloscope. Connect an adjustable low voltage DC power supply to the feedback circuit as shown in Figure B2.

2. Set the oscilloscope to read the duty ratio from the waveform of the *TOPSwitch-GX* drain current. Most digital oscilloscopes will provide a direct readout of the numerical value.

3. Adjust the low voltage DC power supply to 15 V.

4. Operate the converter at full load. Adjust $V_{IN}$ to the value that corresponds to the duty ratio limit specified in the data sheet for a device at the low end of the tolerance range. The DC input voltage for these conditions is given by

$$V_{IN} = \frac{V_{BZL} + I_L\left(R_D + \frac{R_C}{D_{IL}}\right)}{\frac{N_B}{N_P} + \frac{1}{R_{AB}}\left(R_D + \frac{R_C}{D_{IL}}\right)} \qquad \text{(B1)}$$

where $D_{IL}$ is the minimum $DC_{MAX}$ at the $I_L$ of 190 μA, and the other terms are as they are defined in the text and Appendix A.

5. Adjust the duty ratio to $D_{IL}$ by forcing the main output to regulate at a higher voltage. To do this, reduce the voltage of the bench power supply from 15 V until the duty ratio measured from the drain current is $D_{IL}$.

6. Verify that the current into the L pin is within 5% of $I_L$. The voltmeter should read 19 mV when $I_L$ is 190 μA.

If it is not possible to adjust the circuit to meet these conditions, the circuit is not guaranteed to operate properly with all devices in the specified range of tolerance. Repeat the design with revised parameters.

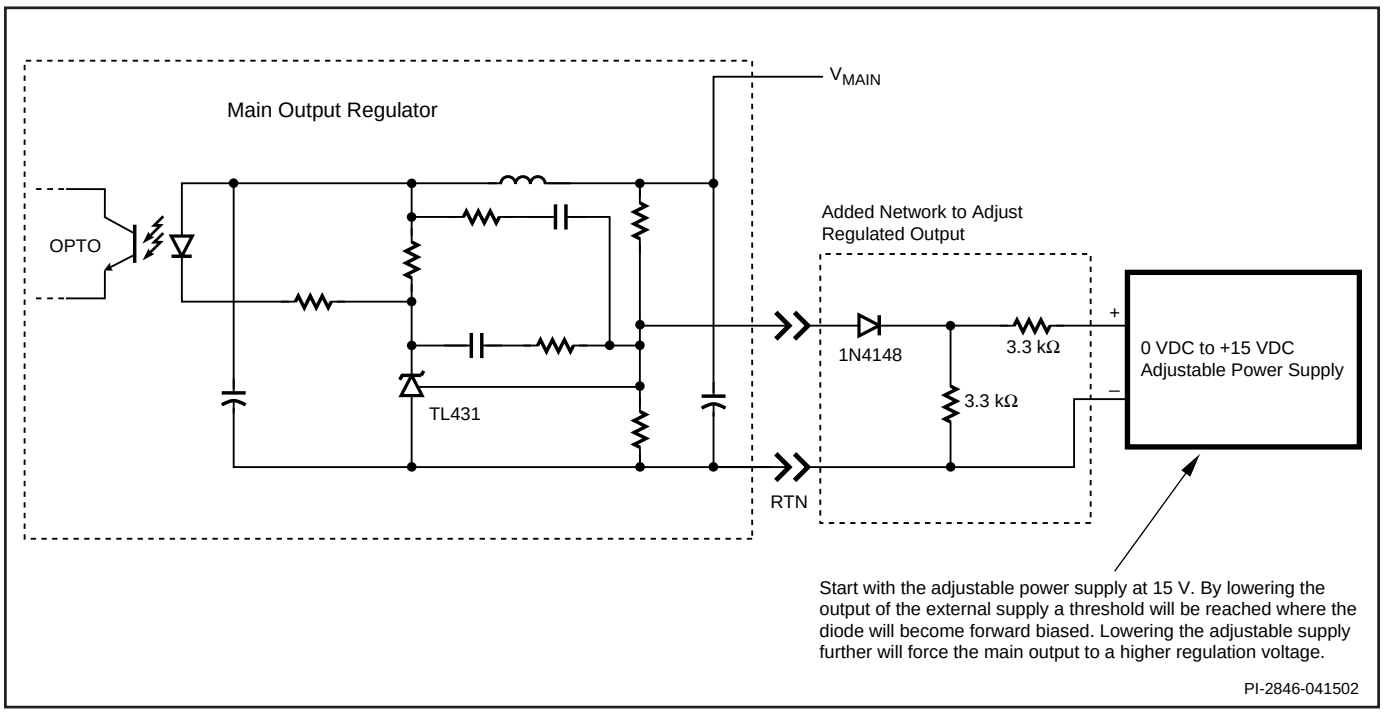



*Figure B2. Circuit to Adjust Main Regulated Output Voltage to Higher Value.*

# Appendix C
# Introduction

This appendix describes a worked example that shows how to use the *TOPSwitch-GX* forward design spreadsheet, to calculate values for key components, such as the input capacitance, transformer number of turns and duty cycle reduction circuitry, used on the EP-12 145 W doubled mains prototype board. The design spreadsheet can be found in the *PIXls* utility as part of the *PI Expert* design tool version 4.0.3 and above.

The worked example and spreadsheet uses the same design equations as presented in the design methodology. However, rather than following the flow chart in the methodology, the worked example follows the order of the spreadsheet. Thus step (a) in worked example does not correspond to step 1 from AN-30, and so on.

Since the EP-12 has a doubler input stage, the calculations within this document address the design in the doubled mode.

Note that both AN-30 and the design spreadsheet assume single input voltage ranges. Universal input designs are not supported.

## Step by Step Example for EP-12

Note: All user inputs are in column B and all calculated results are in column F of the spreadsheet.

**Step (a). Enter the Power supply Output specifications:** $V_{MAIN}$, $I_{MAIN}$, $V_{MAINMA}$, $I_{MAINMA}$, $V_{AUX1}$ and $I_{AUX1}$

| | |
|---|---|
| Enter the mainwindingoutputvoltage $V_{MAIN}$ = 5 V | **(VMAIN, B3)** |
| Enter the main winding full load current $I_{MAIN}$ = 12 A | **(IMAIN, B4)** |
| Enter the mag-amp winding output voltage $V_{MAINMA}$ = 3.3 V | **(VMAINMA, B5)** |
| Enter the mag-amp winding full load current $I_{MAINMA}$ = 12 A | **(IMAINMA, B6)** |
| Enter the auxiliary winding output voltage $V_{AUX1}$ = 12 V | **(VAUX1, B7)** |
| Enter the auxiliary winding full load current $I_{AUX1}$ = 4 A | **(IAUX1, B8)** |

**Step (b). Define system requirements:** $V_{ACMAX}$, $V_{ACMIN}$, $f_L$, $f_S$, $V_O$, $P_O$, $\eta$, $t_H$

| | |
|---|---|
| Set minimum AC input voltage = 90 V. | **(VACMIN, B14)** |
| Set maximum AC input voltage = 132 V | **(VACMAX,B15)** |
| Line frequency $f_L$ = 50 Hz | **(fL, B19)** |
| Power supply Efficiency Estimate: If no better value available use 75%. | **(EFF, B22)** |
| Hold-up time $t_H$ = 16 ms | **(th, B21)** |
| Set bridge rectifier conduction time. | |
| If no better value available use default value $t_C$ = 3 ms | **(tc, B20)** |

**Step (c). Calculation of Minimum and Maximum DC input voltages:** $V_{MIN}$, $V_{MAX}$

The spreadsheet calculates the maximum DC input voltage, $V_{MAX}$, at AC high line and minimum DC input voltage $V_{MIN}$, at AC low line for which the supply remains in regulation under steady state operating conditions.

For the EP-12 prototype, these values are calculated as follows

| | |
|---|---|
| $V_{MAX}$ = 373 V | **(VMAX, F17)** |
| $V_{MIN}$ = 188 V | **(VMIN, F16)** |

**Step (d). Determine dropout voltage:** $V_{DROPOUT}$

The dropout voltage determines the point where the converter looses regulation, at the end of holdup time, due to reaching maximum duty cycle.

The dropout voltage, $V_{DROPOUT}$, and maximum duty cycle are linked. For a higher dropout voltage the designer has to enter a lower value for $D_{MAX\_GOAL}$ and for a lower dropout voltage the designer should entger higher value of $D_{MAX\_GOAL}$. This ensures the operating duty-cycle is within an acceptable range.

As an initial estimate for a 3:1 operating range ($V_{MAX}$ : $V_{DROPOUT}$), $D_{MAX\_GOAL} = 0.7$ and for a 2:1 operating range, $D_{MAX\_GOAL} = 0.5$.

In EP-12 prototype the dropout voltage is low, to maximize holdup time, so a relatively high value for $D_{MAX\_GOAL}$ has been selected. (Operating range is 373 V to 132 V or 2.8:1).
Set dropout voltage $V_{DROPOUT} = 132\ V$ **(VDROPOUT, F24)**
Set the maximum duty-cycle $D_{MAX\_GOAL} = 0.7\ V$ **(DMAX_GOAL, F25)**

**Step (e). Determine the bulk capacitance:** $C_{IN}$
The spreadsheet checks for the input capacitance value based on hold-up time and output power. The user should decide on a hold-up time first and then try different values of input capacitance such that no warnings are shown. This indicates that with the chosen capacitor value, it is possible to meet the desired hold-up time.

Assume 1µF/W for doubled mains applications as a starting point. We thus have
$C_{IN} = 1\mu F/W \times 147.6\ W = 147.6\ \mu F$
Select next larger standard value.

Note: The EP-12 design has a double input configuration. A doubler circuit has two capacitors in series, each of which have a value which is twice that calculated above.

Selecting the next larger standard value for twice 147.6 µF, we have $2 \times C_{IN} = 330\ \mu F, 200\ V$

The actual value entered in the spreadsheet is $C_{IN} = 165\ \mu F$ **(CIN, B18)**

**Step (f). Selection of Rectifier diode drops (Vf):** $V_{DMAIN}$, $V_{DMAINMA}$, $V_{DAUX1}$, $V_{DB}$
The spreadsheet automatically selects the type of rectifier (ultra-fast or Schottky) based on the output voltage. The corresponding diode drops are listed as follows:
The voltage drop on main winding rectifier diode $V_{DMAIN} = 0.5\ V$ **(VDMAIN, F41)**
The voltage drop on mag-amp rectifier diode $V_{DMAINMA} = 0.5\ V$ **(VDMAINMA, F42)**
The voltage drop on auxiliary winding diode $V_{DAUX1} = 0.7\ V$ **(VDAUX1, F43)**
The voltage drop on bias winding rectifier $V_{DB} = 0.7\ V$ **(VDB, F45)**

The values calculated by the spreadsheet may be overridden by entering the desired voltage drop in column B (B41 to B45).

**Step (g). Selection of Bridge Rectifier Diode based on peak inverse voltage and average rectifier current**: $V_{PIVAC}$, $I_{DAVBR}$
The recommended voltage rating for input bridge rectifier is given in Equation (29).
$V_{PIVAC} = 467\ V$ **(VPIVAC, F49)**

Current ratings for rectifiers have average values not RMS values. The current rating for the bridge rectifier can be calculated from Equation (30) in AN-30.
$I_{DAVBR} = 0.714\ A$ **(IDAVBR, F50)**

**Step (h). Selection of Ripple current factor:** $K_{\Delta I}$
$K_{\Delta I}$ is defined in AN-30. It is a ratio of the ripple in the output current to the average current in the output inductor. This determines the size of the output inductor. As recommended in AN-30 choose $K_{\Delta I}$ between 0.15 and 0.3.

For the EP12 design, this value was selected as $K_{\Delta I} = 0.15$ **(KDI, B27)**

**Step (i). Selection of *TOPSwitch-GX* and related parameters:** $I_P$, $K_I$, $RX$, $VDS$
The operating peak drain current is calculated as $I_P = 2.45$ A **(IP, F84)**

Select an appropriate *TOPSwitch* according to peak primary current as well as for power dissipation.

The TOP247Y was selected and has a minimum current limit of 3.34 A. Current limit should be externally programmed to approximately 8-12% above the operating peak drain current, that is $I_{XLIMIT} = I_P \times 1.11 = 2.45 \times 1.11 = 2.712\ A$.

The external current-limit reduction factor is given by Equation (15) in AN-30

$$K_I = \frac{2.712}{3.34} = 0.81$$

Set external current limit reduction factor $K_I = 0.81$ **(KI, B35)**

The external current limit is reduced from 3.34 A to 2.712 A using a current limit-program resistor. The external current limit resistor is calculated by the spreadsheet as RX = 7.78 kΩ **(RX, F36)**
TOPSwitch switching frequency fs = 132 kHz **(FS, D34)**

On the prototype board an 8.3 kΩ resistor was used. The larger value was required to compensate for the additional voltage drop caused by the remote on-off circuit.

The spreadsheet also estimates the ON state drain to source voltage drop.
*VDS = 8.1 V* **(VDS, F38)**

**Step (j). Selection of the "R-FACTOR"**
The R-Factor is an estimate of percentage of power lost in the transformer windings, diode and PC board trace resistance. Typically this value is less than 10% for most well designed power supplies. Use this value if no better data are available.
*R-Factor = 9%* **(RFACTOR, B61)**

**Step (k). Selection of number of turns for transformer windings:** $N_{MAIN}, N_P, N_{AUX1}, N_B$
The number of turns for all outputs are calculated by the spreadsheet. In EP-12 these values are as follows:
Number of turns on main winding $N_{MAIN} = 3$ **(NMAIN, F64)**
Number of turns on Primary winding $N_P = 45$ **(NP, F67)**
Number of turns on auxiliary winding $N_{AUX1} = 4$ **(NAUX1, F69)**
Number of bias winding turns $N_B = 6$ **(NB, F68)**

Check all outputs on prototype hardware to conform that they are within acceptable limits.

**Step (l). Selection of Optocoupler and Transformer Core Parameters.**
**Selection of Optocoupler:** $V_{CEO}$
The bias winding should provide a minimum of 8 V on the collector of the photo transistor at the lowest operating voltage.

When no external under-voltage circuit is used the lowest operating voltage may be much lower than expected. Increase bias turns to increase minimum bias voltage.

At higher input voltages the collector voltage should not exceed $V_{CEO}$, the collector to emitter breakdown voltage. The spreadsheet calculates this maximum blocking voltage imposed on the optocoupler as:
$V_{CEO}$ = 49.8 **(VCEO OPTO, F120)**

Select an optocoupler with a high blocking voltage. Typically a 60 V ($V_{CEO}$) optocoupler is used.

**Transformer core parameters:** *M, L, BM, BP*
Set safety margin M. Use 3 mm for margin wound with 115 VAC doubled input. Set to zero if triple insulated secondary windings are used. In the EP-12 prototype 3 mm margin is selected.

Enter margin *M = 3 mm* **(M, B62)**

Calculate the number of primary layers. Start with 1 layer, and check for warnings. The spreadsheet calculates the primary side wire cross sectional areas based on number of layers, number of turns and bobbin winding width. In the EP-12 prototype 1 layer corresponds to a wire size of AWG 26, but due to skin effect is not fully utilized. Using 0.8 layers, does not fill up the bobbin entirely, but has an acceptable winding resistance and current density.

Enter number of layers *L = 0.8* **(L, B63)**

The spreadsheet also calculates the wire gauge as (AWG-28).

Maximum operating flux density, *BM*, is the flux density under conditions of full load, and high line. The spreadsheet calculates and returns this value. Check that this value is less than 2000 gauss.

*BM = 1816 gauss* **(BM, F74)**

Peak flux density is the maximum allowable flux density in the core under transient conditions. This value is also calculated by the spreadsheet. Check that this value does not exceed 3000 gauss.

*BP = 2884 gauss* **(BP, F75)**

**Step (m). Transformer design parameters:**
Verify that the maximum and minimum limits of the *TOPSwitch-GX* duty-cycle reduction parameters for both high-end and low-end tolerance parts lie within the reset and regulating limits for any given input voltage.

**Reset parameters:** $DMAX_{RESET}, DLL_{RESET}, DHL_{RESET}$
Referring to the curve in Figure 8 these three parameters define the core-reset curve for the transformer.
$DMAX_{RESET}$ = 0.79 **(DMAX RESET, F145)**
$DLL_{RESET}$ = 0.63 **(DLL RESET, F152)**
$DHL_{RESET}$ = 0.36 **(DHL RESET, F157)**

**Max duty-ratio (Low-end Tolerance part) parameters:** $DXDO_{MIN}, DXLL_{MIN}, DXHL_{MIN}$
To ensure correct operation with devices at the higher and lower ends of the maximum duty-ratio, the spreadsheet provides calculations assuming tolerance limits.

Referring to Figure 8, the parameters with MIN correspond to the parameters for the low-end tolerance part. Duty-ratios corresponding dropout voltage, low-line input voltage and high line input voltages are listed. These duty-ratios at the corresponding voltages define the lower limit curves for the maximum duty-cycle reduction circuit. This curve should be above the $D_{ACTUAL}$ curve.
$DXDO_{MIN}$ = 0.70 **(DXDO MIN, F146)**
$DXLL_{MIN}$ = 0.55 **(DXLL MIN, F150)**
$DXHL_{MIN}$ = 0.24 **(DXHL MIN, F155)**

**Max duty ratio (High-end tolerance part) parameters:** $DXDO_{MIN}, DXLL_{MIN}, DXHL_{MIN}$
Again, referring to Figure 8, the parameters with subscripts MAX correspond to the parameters for the high-end tolerance part. Duty-ratios corresponding dropout voltage, low-line input voltage and high line input voltages are listed. These duty-ratios at the corresponding voltages define the higher limit curves for the maximum duty-cycle reduction circuit. This curve should be below the $D_{RESET}$ curve.
$DXDO_{MAX}$ = 0.79 **(DXDO MAX, F147)**
$DXLL_{MAX}$ = 0.67 **(DXLL MAX, F151)**
$DXHL_{MAX}$ = 0.35 **(DXHL MAX, F156)**

To guarantee smooth operation, these 4 curves namely the regulation duty cycle ($D_{ACTUAL}$) curve, the low-end tolerance part ($D_{MIN}$) curve, the high-end tolerance part ($D_{MAX}$) curve and the core reset ($D_{RESET}$) curve should never intersect each other. This guarantees that the power supply will not drop out of regulation and also ensures that there will be no transformer saturation. In the EP-12 example, the parameter $DXDO_{MAX}$ exceeds parameter $DMAX_{RESET}$. This could POSSIBLY cause transformer saturation ONLY during load transients or during shut down of the converter, which is NOT hazardous.

**Regulating duty-ratio parameters:** $DMAX_{ACTUAL}, DLL_{ACTUAL}, DHL_{ACTUAL}$
Referring to Figure 8, these three parameters correspond to the operating duty-ratio at dropout, low line input and high line input respectively.
$DMAX_{ACTUAL}$ = 0.69 **(DMAX ACTUAL, F144)**
$DLL_{ACTUAL}$ = 0.40 **(DLL ACTUAL, F149)**
$DHL_{ACTUAL}$ = 0.23 **(DHL ACTUAL, F154)**

**Step (n)-Step (p). Calculation of RMS Ripple currents in output capacitors, parameters for the coupled inductor and stresses on the rectifier diodes.**

**Calculations of RMS Ripple currents in output capacitors:** $I_{RMS\ MAIN}$, $I_{RMS\ MAINMA}$, $I_{RMS\ AUX1}$
The RMS currents in the output capacitors, for each individual output is calculated by the spreadsheet. The values for EP-12 supply are as follows:

$I_{RMS\ MAIN}$ = 0.52 *A* **(IRMSMAIN, F108)**
$I_{RMS\ MAINMA}$ = 0.52 *A* **(IRMSMAINMA, F109)**
$I_{RMS\ AUX1}$ = 0.17 *A* **(IRMSAUX1, F110)**

For the auxiliary output this ripple current calculation is only an estimate. This value varies with the coupling co-efficient, parasitic voltage drops and other quantities which are difficult to predict.

Choose output capacitors to meet the above ripple current requirements.

**Parameters for the coupled output inductor, and mag-amp inductance:** $L_{MAIN}$, $L_{MAINMA}$
The turn's-ratio for the coupled choke is the same as that of the transformer.

$$\frac{N_{LMAIN}}{N_{LAUX}} = \frac{3}{4}$$

The inductor is computed by the spreadsheet $L_{MAIN}$ = 10.1 $\mu H$ **(LMAIN, F68)**

An inductor value of 10.2 $\mu H$ was tried in the EP-12 design. Bench evaluation of the prototype for fine adjustment led to satisfactory performance with this value for the inductor.

The mag-amp inductance is calculated by spreadsheet. This is calculated as 12.4 $\mu H$ .

LMAINMA = 12.4 $\mu H$ **(LMAINMA, B90)**

First select the closest standard value. If performance is not satisfactory, a more accurate inductor should be wound. For the EP-12 design a standard 15 $\mu H$ inductor was found to be satisfactory.

**PIV stress on Rectifier diodes:** *VPIVMAIN, VPIVMAINMA, VPIVAUX1, VPIVB*
The spreadsheet calculates the peak inverse voltage that is imposed on the rectifier diodes.

Main output rectifier peak inverse voltage = 29.5 V **(VPIVMAIN, F114)**
MagAmp output rectifier peak inverse voltage = 29.5 V **(VPIVMAINMA, F115)**
Auxiliary output rectifier peak inverse voltage = 34.9 V **(VPIVAUX1, F116)**
Bias winding output rectifier peak inverse voltage = 102.1 V **(VPIVB, F118)**

Choose rectifier diodes with PIV ratings typically 120% of the ratings calculated above.

### Optional Under-Voltage Lockout Circuit: $R_{UVA}$, $R_{UVB}$, $R_{UVC}$

The external under-voltage lockout circuit is shown in Figure 9. The circuit sets the minimum input voltage that should be present before the *TOPSwitch-GX* is enabled. The circuit also sets the voltage at which the converter is shut off during power down.

**Step (q). Selection of $R_{UVA}$ $R_{UVB}$ & $R_{UVC}$:**

Under worst-case input voltage conditions power dissipation in $R_{UVA}$ must not exceed 150 mW. The spreadsheet calculates the value of this resistor. In EP-12 this resistor is:

$R_{UVA}$ = 2.23 *MΩ* **(RUVA, F126)**

Choose closest standard value; $R_{UVA}$ = 2.2 *MΩ, 0.5 W*

Choose $V_{ACUVL}$ and $V_{ACUV}$ and select $R_{UVB}$ & $R_{UVC}$:
Choose a value for $V_{ACUVL}$ and $V_{ACUV}$ such that
$V_{ACUVL} < V_{ACUVX} < V_{ACUV}$

where $V_{ACUVX}$ is the voltage at which the external under-voltage lockout circuit enables the *TOPSwitch-GX* during start-up. This value is automatically calculated by the spreadsheet.

Set the voltage at which the converter shuts off with the external UVLO circuit, $V_{ACUVL}$ = 67 *V*.

Enter the voltage at which the converter should begin its steady state operation $V_{ACUV}$ = 80 *V*.

This means that the voltage at which the external UVLO circuit enables the *TOPSwitch-GX* while the input voltage is rising, $V_{ACUVX}$ must lie within the limits 67 *V* < $V_{ACUVX}$ < 80 *V*.
The spreadsheet returns a value for voltages $V_{ACUVX}$ and $V_{ACUVL}$. Check that these values are within acceptable limits.

The spreadsheet returns the following values for resistors $R_{UVB}$ & $R_{UVC}$.
$R_{UVB}$ = 523.73 *kΩ* **(RUVB, F127)**
$R_{UVC}$ = 75.91 *kΩ* **(RUVC, F128)**

If the calculated value of the resistors is unavailable, use closest available standard values. Back calculate for $V_{ACTUAL}$ and $V_{ACUVX}$ and check that they are within acceptable limits.

For EP-12 the values of resistors are as follows
$R_{UVB}$ = 560 *kΩ*
$R_{UVC}$ = 75 *kΩ*
Back calculating to check for $V_{ACUVL}$ and $V_{ACUVX}$ we have
$V_{ACUVL}$ = 67.5 *V* **(VACUVL ACTUAL, F130)**
$V_{ACUVX}$ = 70.36 *V* **(VACUVX ACTUAL, F131)**
both within reasonable limits.

### Circuit for Reduction of Maximum Duty Ratio

Figure C1 shows the external circuit for limiting the maximum duty cycle of the *TOPSwitch-GX*.

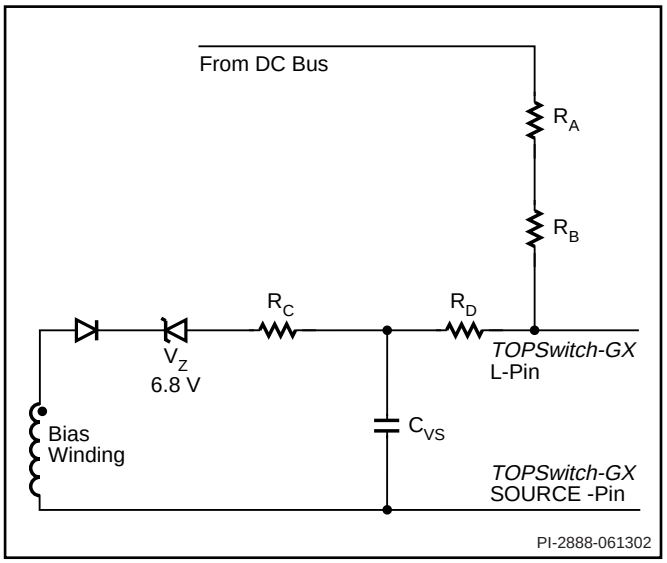



*Figure C1: Components that make up external duty-ratio limiting circuit.*

**Step (r). Selection of duty-cycle limiting circuit components:** $R_A$, $R_B$, $R_C$, $R_D$, $V_Z$, $C_{VS}$
**Selection of** $R_A$, $R_B$
These resistors provide L pin current that is proportional to the input voltage. The calculation formula for these resistors is as in Equation (35) of AN-30. $R_A = R_B = 2.25\ M\Omega$.
Selecting closest standard values:
Select $R_A = 2.26\ M\Omega$, 0.5 *W* **(RA, F137)**
Select $R_B = 2.26\ M\Omega$, 0.5 *W* **(RB, F138)**

**Selection of Zener:** $V_Z$
The Zener diode increases the dynamic range of operation by allowing the low line duty-ratio to be a higher value, while still avoiding saturation.

The Zener diode should be used only in designs that operate over a very wide range of duty-cycle. Whenever needed, a 4 V-9 V Zener diode should be used. In EP-12 this value is set at 6.8 V, as this is the maximum value of the Zener that avoids core saturation at low line, while allowing extended operating range. Choose any standard low power (500 mW) Zener diode.

Choose 6.8 V Zener diode BZX79-C6V8, VZ = 6.8 V **(VZ F134)**

**Selection of Duty-Ratio limits:** $D_{XDO}$, $D_{XHL}$
Note that the spreadsheet takes default inputs corresponding to $D_{XDO}$ and $D_{XHL}$. These values are based on the low-end parts. It can be seen by looking at the curves for core saturation ($D_{RESET}$) and the operating duty cycle ($D$), that the attempt here is to place the maximum limiting duty-ratio ($D_{MAX}$) curve approximately mid-way these two limit curves.

Figure C2 shows an example curve taken from the design spreadsheet where the $D_{RESET}$ limit is violated. Figure C3 shows an example where the regulation limit, $D_{ACTUAL}$ is violated.

**Selection of Overvoltage onset level VOV**
This determines the voltage at which frequency reduction commences. In EP-12 the default value was used.
*VOV* = 380 **(VOV, F135)**

| | | | | | | |
|---|---|---|---|---|---|---|
| 143 | **DUTY CYCLE PARAMETERS (see graph)** | | | | | *Dropout Duty-Cycle Parameters* |
| 144 | DMAX ACTUAL | | | 0.67 | | Operating Duty cycle at DC Bus dropout voltage |
| 145 | DMAX RESET | | | 0.79 | | Transformer Reset Minimum duty cycle at DC Bus dropout voltage |
| 146 | DXDO MIN | | | 0.68 | | Device Min Duty cycle limit at DC Bus dropout voltage |
| 147 | DXDO MAX | | | 0.78 | | Device Max Duty cycle limit at DC Bus dropout voltage |
| 148 | | | | | | |
| 149 | DLL ACTUAL | | | 0.46 | | Duty cycle at minimum DC Bus voltage |
| 150 | **DXLL MIN** | | | **0.52** | | Duty cycle minimum limit at minimum DC Bus voltage |
| 151 | DXLL MAX | | | 0.64 | | Duty cycle maximum limit at minimum DC Bus voltage |
| 152 | DLL RESET | | | 0.69 | | Minimum duty cycle to reset transformer at low line |
| 153 | | | | | | *High Line Duty-Cycle Parameters* |
| 154 | DHL ACTUAL | | | 0.23 | | Duty cycle at minimum DC Bus voltage |
| 155 | DXHL MIN | | Warning | 0.13 | | !!! < 103% of operating duty cycle at max DC Bus voltage: increase DXHL MIN, decre |
| 156 | **DXHL MAX** | | | **0.24** | | Duty cycle maximum limit at maximum DC Bus voltage |
| 157 | DHL RESET | | | 0.36 | | Minimum duty cycle to reset transformer at high line |
| 158 | | | | | | |

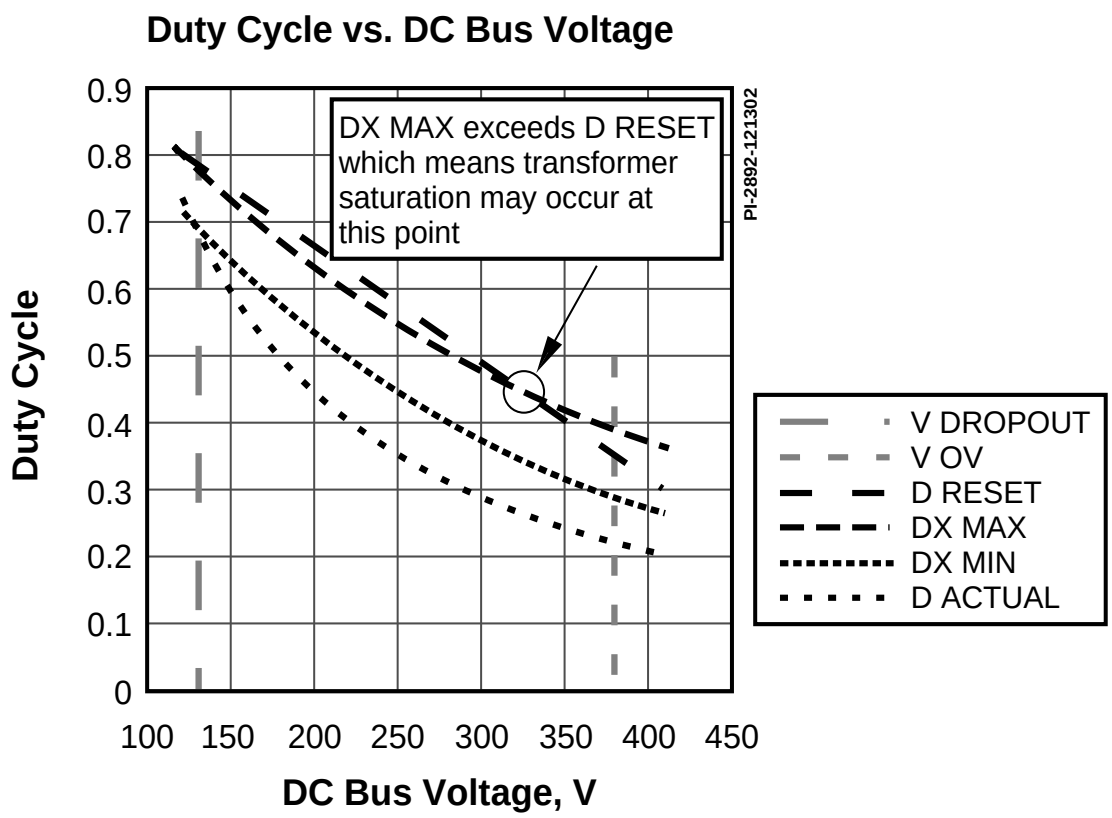



*Figure C2. Example of $D_{RESET}$ Limit Violation.*

| | | | | | | |
|---|---|---|---|---|---|---|
| 143 | **DUTY CYCLE PARAMETERS (see graph)** | | | | | *Dropout Duty-Cycle Parameters* |
| 144 | DMAX ACTUAL | | | 0.67 | | Operating Duty cycle at DC Bus dropout voltage |
| 145 | DMAX RESET | | | 0.79 | | Transformer Reset Minimum duty cycle at DC Bus dropout voltage |
| 146 | DXDO MIN | | | 0.69 | | Device Min Duty cycle limit at DC Bus dropout voltage |
| 147 | DXDO MAX | | | 0.78 | | Device Max Duty cycle limit at DC Bus dropout voltage |
| 148 | | | | | | |
| 149 | DLL ACTUAL | | | 0.46 | | Duty cycle at minimum DC Bus voltage |
| 150 | **DXLL MIN** | | | **0.56** | | Duty cycle minimum limit at minimum DC Bus voltage |
| 151 | DXLL MAX | | | 0.66 | | Duty cycle maximum limit at minimum DC Bus voltage |
| 152 | DLL RESET | | | 0.69 | | Minimum duty cycle to reset transformer at low line |
| 153 | | | | | | *High Line Duty-Cycle Parameters* |
| 154 | DHL ACTUAL | | | 0.23 | | Duty cycle at minimum DC Bus voltage |
| 155 | DXHL MIN | | | 0.30 | | Duty cycle minimum limit at maximum DC Bus voltage |
| 156 | **DXHL MAX** | | **Warning** | **0.39** | | !!! > reset duty cycle at VMAX : decrease DXHL MAX, increase VDSOP |
| 157 | DHL RESET | | | 0.36 | | Minimum duty cycle to reset transformer at high line |
| 158 | | | | | | |

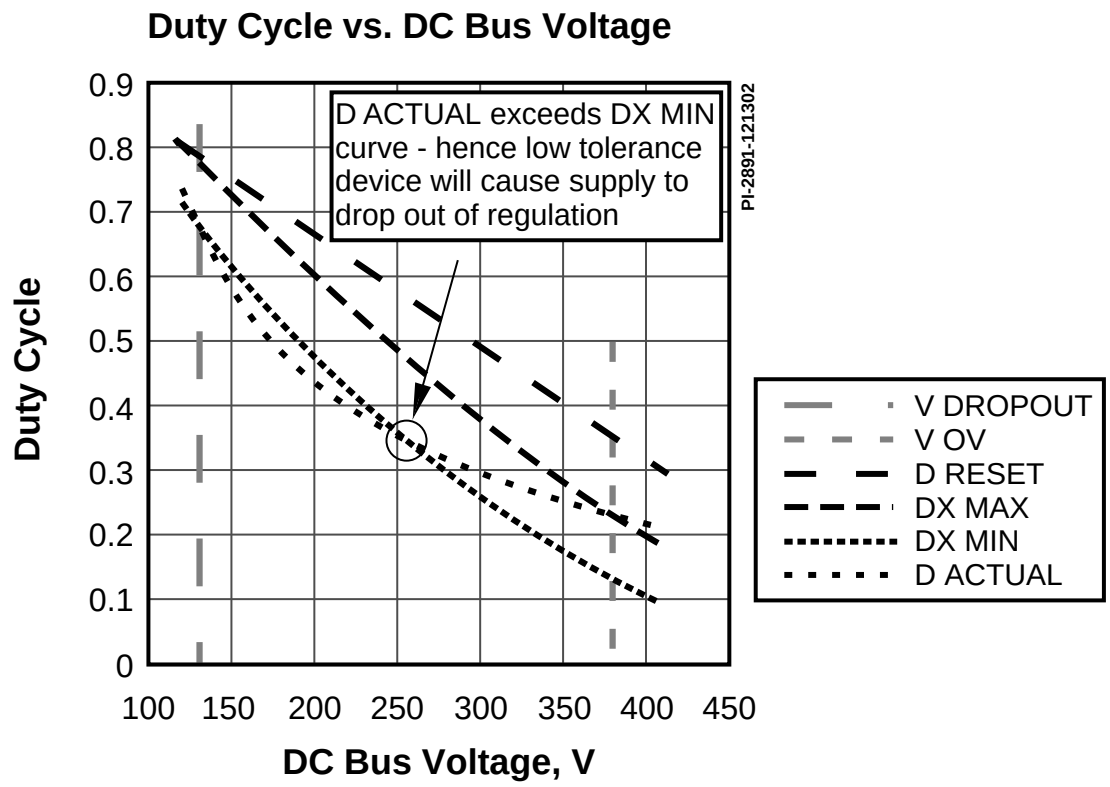



*Figure C3. Example of $D_{ACTUAL}$ (Regulation) Limit Violation.*

**Selection of $R_C$**

The value of $R_C$ is calculated by the spreadsheet. In EP-12 this value is calculated as:
$R_C$ = 40.26 *kΩ* **(RC, F139)**

Choose closest standard available value, $R_C$ = 43.2 *kΩ*, 0.125 *W*

**Selection of $R_D$**
The value of $R_D$ is automatically calculated by the spreadsheet. In EP-12 this value is calculated as:
$R_D$ = 126.70 *kΩ* **(RD, F143)**

Choose closest standard available value, $R_D$ = 130 *kΩ*, 0.125 *W*

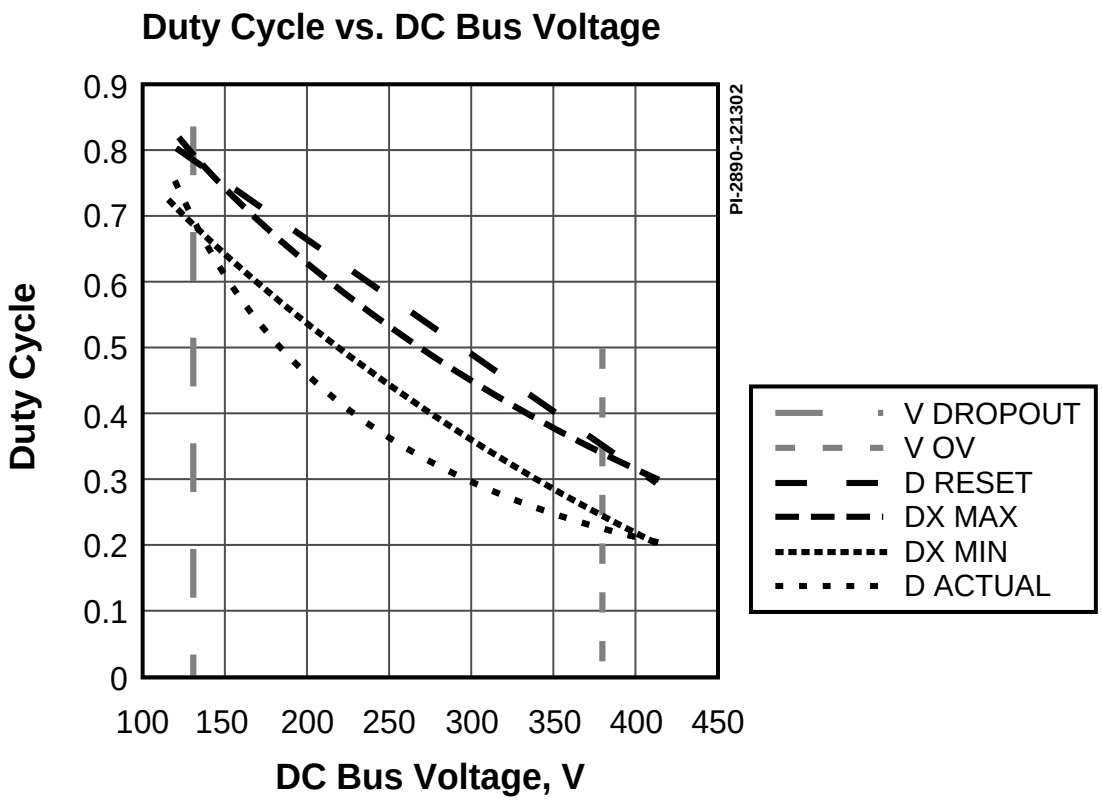
**Selection of Capacitor $C_{VS}$**
The capacitor $C_{VS}$ is also estimated by the spreadsheet. For EP-12, the value from the equation is approximately 93 pF.

If the calculated value is unavailable choose next higher standard available value.
Choose $C_{VS}$ = 100 *pF*, 100 *V* **(CVS, F141)**

# Spreadsheet

| | A | B | D | F | G | I |
|---|---|---|---|---|---|---|
| 1 | ACDC_TOPGXForward_Rev_1.03_061802 Copyright Power Integrations Inc. 2002 | INPUT | INFO | OUTPUT | UNIT | ACDC_TOPGXFwd_061802_r103.xls: TOPSwitch-GX Forward Transformer Design Spreadsheet |
| 2 | **OUTPUT VOLTAGE AND CURRENT** | | | | | **EP12 PC Main power supply** |
| 3 | VMAIN | 5 | | | Volts | Main output voltage |
| 4 | IMAIN | 12 | | | Amps | Main output current |
| 5 | VMAINMA | 3.3 | | | Volts | Magamp output voltage |
| 6 | IMAINMA | 12 | | | Amps | Magamp output current |
| 7 | VAUX1 | 12 | | | Volts | Auxiliary output voltage |
| 8 | IAUX1 | 4 | | | Amps | Auxiliary output current |
| 9 | VIND1 | | | | Volts | Independant output voltage |
| 10 | IND1 | | | | Amps | Independent output current |
| 11 | **PO** | | | **147.6** | Watts | Total output power |
| 12 | | | | | | |
| 13 | **ENTER APPLICATION VARIABLES** | | | | | |
| 14 | VACMIN | 90 | | | AC volts | Minimum AC input voltage. Input voltage doubler circuit is assumed. |
| 15 | VACMAX | 132 | | | AC volts | Maximum AC input voltage. Input voltage doubler circuit is assumed. |
| 16 | VMIN | | | 188 | Volts | Minimum DC Bus voltage at low line input |
| 17 | VMAX | | | 373 | Volts | Maximum DC Bus voltage at high line input |
| 18 | CIN | 165 | | | uFarads | Equivalent bulk input capacitance. Input voltage doubler circuit is assumed. |
| 19 | fL | 50 | | | Hz | Input AC line frequency |
| 20 | tc | 3.0 | | | mSeconds | Estimate input bridge diode conduction time |
| 21 | th | 16.0 | | | mSeconds | Minimum required hold-up time from VDROPOUT to VHOLDUP |
| 22 | EFF | 0.75 | | | | Efficiency estimate to determine minimum DC Bus voltage |
| 23 | VHOLDUP | | | 188 | Volts | DC Bus voltage at start of hold-up time (default VMIN) |
| 24 | VDROPOUT | 132 | | 132 | Volts | DC Bus Voltage at end of hold-up time |
| 25 | DMAX GOAL | 0.7 | | 0.70 | | Maximum duty cycle at DC dropout voltage |
| 26 | VDSOP | | | 580 | Volts | Maximum operating drain voltage |
| 27 | KDI | | | 0.15 | | Maximum output current ripple factor at maximum DC Bus voltage |
| 28 | REF AUX1 | 1 | | DC Stack | | Enter one ('1') for DC stacked , zero ('0') Independent winding |
| 29 | | | | | | |
| 30 | **ENTER TOPSWITCH VARIABLES** | | | | | |
| 31 | **TOPSwitch** | **top247** | | | *Universal* | *Doubled 115V/230V* |
| 32 | *Chosen Device* | *TOP247* | | *Power Out* | - | 165W |
| 33 | ILIMIT | *3.348* | *3.852* | | Amps | From TOPSwitch-GX datasheet |
| 34 | fS | *124000* | *132000* | | Hertz | From TOPSwitch-GX+H76 datasheet |
| 35 | KI | 0.81 | | | | Ilimit reduction (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT) |
| 36 | RX | | | 7.78 | kOhm | Maximum current limit resistance to ensure KI >= 0.81 setting |
| 37 | ILIMITEXT | | | 2.712 | Amps | External current limit |
| 38 | VDS | | | 8.1 | Volts | TOPSwitch-GX average on-state Drain to Source Voltage |
| 39 | | | | | | |
| 40 | **DIODE Vf SELECTION** | | | | | |
| 41 | VDMAIN | | | 0.5 | Volts | Main output rectifiers forward voltage drop (Schottky) |
| 42 | VDMAINMA | | | 0.5 | Volts | Magamp output rectifiers forward voltage drop (Schottky) |
| 43 | VDAUX1 | | | 0.7 | Volts | Auxiliary output rectifiers forward voltage drop (Ultrafast) |
| 44 | VDIND1 | | | 0 | Volts | Independent output rectifiers forward voltage drop (Schottky) |
| 45 | VDB | | | 0.7 | Volts | Bias output rectifier conduction drop |
| 46 | | | | | | |
| 47 | | | | | | |
| 48 | **BRIDGE RECTIFIER DIODE SELECTION** | | | | | |
| 49 | VPIVAC | | | 467 | Volts | Maximum voltage across Bridge rectifier diode |
| 50 | IDAVBR | | | 0.773 | Amps | Average Bridge Rectifier Current |
| 51 | | | | | | |
| 52 | **TRANSFORMER CORE SELECTION** | | | | | |
| 53 | **Core Type** | **eer28l** | | | | |
| 54 | *Core* | | *EER28L* | | P/N: | PC40EER28L-Z |
| 55 | *Bobbin* | | *EER28L_BC* | | P/N: | BEER-28L-1112CPH |
| 56 | AE | | | 0.814 | cm^2 | Core Effective Cross Sectional Area |
| 57 | LE | | | 7.55 | cm | Core Effective Path Length |
| 58 | AL | | | 2520 | nH/T^2 | Ungapped Core Effective Inductance |
| 59 | BW | | | 21.8 | mm | Bobbin Physical Winding Width |
| 60 | LG MAX | | | 0.02 | mm | Maximum actual gap when zero gap specified |
| 61 | R FACTOR | 9% | | 9% | % | Percentage of total PS losses lost in transformer windings; default 10% |
| 62 | M | 3.0 | | | mm | Transformer margin |
| 63 | L | 0.80 | | | | Transformer primary layers |
| 64 | NMAIN | | | 3 | | Main rounded turns |
| 65 | | | | | | |
| 66 | **TRANSFORMER DESIGN PARAMETERS** | | | | | |
| 67 | NP | 45 | | 45 | | Primary rounded turns |
| 68 | NB | | | 6 | | Bias turns to maintain 8V minimum input voltage, light load |
| 69 | NAUX1 | | | 4 | | Auxiliary rounded turns (DC stacked on Main winding) |
| 70 | VAUX1 ACTUAL | | | 11.63 | Volts | Approx. Aux output voltage with NAUX1 = 4 Turns and DC stack |
| 71 | NIND1 | | | 0 | | Independent rounded turns (separate winding) |
| 72 | VIND1 ACTUAL | | | 0.00 | Volts | Approximate Independent output voltage with NIND1 = 0 turns |
| 73 | | | | | | |
| 74 | **BM** | | | **1816** | Gauss | Maximum operating flux density at minimum switching frequency |
| 75 | **BP** | | | **2884** | Gauss | Maximum peak flux density at minimum switching frequency |
| 76 | LP MIN | | | 3.419 | mHenries | Minimum primary magnetizing inductance (assumes LGMAX=20um) |
| 77 | IMAG | | | **0.189** | Amps | Peak magnetizing current at minimum input voltage |

| | A | B | D | F | G | I |
|---|---|---|---|---|---|---|
| 78 | OD_P | | | 0.33 | mm | Primary wire outer diameter |
| 79 | AWG_P | | | **28** | AWG | Primary Wire Gauge (rounded to maximum AWG value) |
| 80 | | | | | | |
| 81 | **CURRENT WAVESHAPE PARAMETERS** | | | | | |
| 82 | **IP** | | | **2.451** | Amps | Maximum peak primary current at maximum DC Bus voltage |
| 83 | IPRMS | | | 1.460 | Amps | Maximum primary RMS current at minimum DC Bus voltage |
| 84 | | | | | | |
| 85 | **INDUCTOR OUTPUT PARAMETERS** | | | | | |
| 86 | LMAIN | | | 10.0 | uHenries | Main / Auxiliary coupled output inductance (referred to Main winding) |
| 87 | WLMAIN | | | 2286 | uJoules | Main / Auxiliary coupled output inductor full-load stored energy |
| 88 | KDIMAIN | | | 0.150 | | Current ripple factor of combined Main and Aux1 outputs |
| 89 | | | | | | |
| 90 | LMAINMA | | | 12.3 | uHenries | Magamp output inductance |
| 91 | WLMAINMA | | | 888 | uJoules | Magamp output inductor full-load stored energy |
| 92 | KDIMAINMA | | | 0.150 | | Current ripple factor for Magamp output |
| 93 | | | | | | |
| 94 | LIND1 | | | 0.0 | uHenries | Independent output inductance |
| 95 | WLIND1 | | | 0.0 | uJoules | Independent output inductor full-load stored energy |
| 96 | KDIIND1 | | | 0.000 | | Current ripple factor for Independent output |
| 97 | | | | | | |
| 98 | **SECONDARY OUTPUT PARAMETERS** | | | | | |
| 99 | ISMAINRMSLL | | | 15.61 | Amps | Maximum transformer secondary RMS current (DC Stack) |
| 100 | ISAUX1RMSLL | | | 2.42 | Amps | Maximum transformer secondary RMS current (DC Stack) |
| 101 | ISIND1RMSDLL | | | 0.00 | Amps | Maximum transformer secondary RMS current |
| 102 | | | | | | |
| 103 | IDAVMAIN | | | 12.3 | Amps | Maximum average current, Main rectifier (single device rating) |
| 104 | IDAVMAINMA | | | 9.3 | Amps | Maximum average current, Magamp rectifier (single device rating) |
| 105 | IDAVAUX1 | | | 3.1 | Amps | Maximum average current, Auxiliary rectifier (single device rating) |
| 106 | IDAVIND1 | | | 0.0 | Amps | Maximum average current, Independent rectifier (single device rating) |
| 107 | | | | | | |
| 108 | IRMSMAIN | | | 0.52 | Amps | Maximum RMS current, Main output capacitor |
| 109 | IRMSMAINMA | | | 0.52 | Amps | Maximum RMS current, Magamp output capacitor |
| 110 | IRMSAUX1 | | | 0.17 | Amps | Maximum RMS current, Auxiliary output capacitor |
| 111 | IRMSIND1 | | | 0.00 | Amps | Maximum RMS current, Independent output capacitor |
| 112 | | | | | | |
| 113 | **DIODE PIV** | | | | | *No derating* |
| 114 | VPIVMAIN | | | 29.5 | Volts | Main output rectifiers peak-inverse voltage |
| 115 | VPIVMAINMA | | | 29.5 | Volts | Magamp output rectifiers peak-inverse voltage |
| 116 | VPIVAUX1 | | | 34.9 | Volts | Auxiliary output rectifiers peak-inverse voltage |
| 117 | VPIVIND1 | | | 0.0 | Volts | Independent output rectifiers peak-inverse voltage |
| 118 | VPIVB | | | 102.1 | Volts | Bias output rectifier peak-inverse voltage |
| 119 | | | | | | *Optocoupler* |
| 120 | VCEO OPTO | | | 49.8 | Volts | Maximum optocoupler collector-emitter voltage |
| 121 | | | | | | |
| 122 | **UNDER-VOLTAGE LOCKOUT CIRCUIT PARAMETERS** | | | | | |
| 123 | VACUVL | | | 68 | AC volts | AC undervoltage lockout voltage; On-Off transition |
| 124 | VACUV | | | 78 | AC volts | AC undervoltage lockout voltage; Off-On transition |
| 125 | VACUVX | | | 68 | | |
| 126 | RUVA | | | 2.23 | MOhm | Resistor RUVA value |
| 127 | RUVB | | | 523.73 | kOhm | Resistor RUVB value |
| 128 | RUVC | | | 75.91 | kOhm | Resistor RUVC value |
| 129 | | | | | | |
| 130 | VACUVL ACTUAL | | | 67.50 | AC volts | Actual AC undervoltage lockout voltage; On-Off transition |
| 131 | VACUVX ACTUAL | | | 70.36 | AC volts | Actual AC undervoltage lockout voltage; Off-On transition |
| 132 | | | | | | |
| 133 | **DUTY CYCLE LIMIT CIRCUIT PARAMETERS** | | | | | |
| 134 | VZ | | | 6.80 | Volts | Zener voltage used within DLIM circuit |
| 135 | **VOV** | | | **380** | Volts | Approximate frequency reduction voltage (determines CVS value) |
| 136 | | | | | | |
| 137 | RA | | | 2.20 | MOhm | Resistor RA value |
| 138 | RB | | | 2.20 | MOhm | Resistor RB value |
| 139 | RC | | | 40.26 | kOhm | Resistor RC value |
| 140 | RD | | | 126.70 | kOhm | Resistor RD value |
| 141 | CVS | | | 92.98 | pF | Capacitor CVS value |
| 142 | | | | | | |
| 143 | **DUTY CYCLE PARAMETERS (see graph)** | | | | | *Dropout Duty-Cycle Parameters* |
| 144 | DMAX ACTUAL | | | 0.69 | | Operating Duty cycle at DC Bus dropout voltage |
| 145 | DMAX RESET | | | 0.79 | | Transformer Reset Minimum duty cycle at DC Bus dropout voltage |
| 146 | DXDO MIN | | | 0.70 | | Device Min Duty cycle limit at DC Bus dropout voltage |
| 147 | DXDO MAX | | Caution | 0.79 | | !!! >DMAXRESET from VMIN to VDROPOUT. NOT hazardous |
| 148 | | | | | | |
| 149 | DLL ACTUAL | | | 0.47 | | Duty cycle at minimum DC Bus voltage |
| 150 | **DXLL MIN** | | | **0.55** | | Duty cycle minimum limit at minimum DC Bus voltage |
| 151 | DXLL MAX | | | 0.67 | | Duty cycle maximum limit at minimum DC Bus voltage |
| 152 | DLL RESET | | | 0.69 | | Minimum duty cycle to reset transformer at low line |
| 153 | | | | | | *High Line Duty-Cycle Parameters* |
| 154 | DHL ACTUAL | | | 0.23 | | Duty cycle at minimum DC Bus voltage |
| 155 | DXHL MIN | | | 0.24 | | Duty cycle minimum limit at maximum DC Bus voltage |
| 156 | **DXHL MAX** | | | **0.35** | | Duty cycle maximum limit at maximum DC Bus voltage |
| 157 | DHL RESET | | | 0.36 | | Minimum duty cycle to reset transformer at high line |


Duty Cycle vs. DC Bus Voltage
Duty Cycle
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
100
150
200
250
300
350
400
450
DC Bus Voltage, V
PI-2890-121302
V DROPOUT
V OV
D RESET
DX MAX
DX MIN
D ACTUAL

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**WORLD HEADQUARTERS AMERICAS**
Power Integrations, Inc.
5245 Hellyer Avenue
San Jose, CA 95138 USA
Main: +1 408-414-9200
Customer Service:
Phone: +1 408-414-9665
Fax: +1 408-414-9765
*e-mail: usasales@powerint.com*

**EUROPE & AFRICA**
Power Integrations (Europe) Ltd.
Centennial Court
Easthampstead Road
Bracknell
Berkshire, RG12 1YQ
United Kingdom
Phone: +44-1344-462-300
Fax: +44-1344-311-732
*e-mail: eurosales@powerint.com*

**SINGAPORE**
Power Integrations, Singapore
51 Goldhill Plaza #16-05
Republic of Singapore 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
*e-mail: singaporesales@powerint.com*

**TAIWAN**
Power Integrations
International Holdings, Inc.
17F-3, No. 510
Chung Hsiao E. Rdl,
Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
*e-mail: taiwansales@powerint.com*

**CHINA**
Power Integrations
International Holdings, Inc.
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu
Shenzhen Guangdong, 518031
China
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
*e-mail: chinasales@powerint.com*

**KOREA**
Power Integrations
International Holdings, Inc.
Rm# 402, Handuk Building
649-4 Yeoksam-Dong, Kangnam-Gu,
Seoul, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
*e-mail: koreasales@powerint.com*

**JAPAN**
Power Integrations, K.K.
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama 2-Chome
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
*e-mail: japansales@powerint.com*

**INDIA (Technical Support)**
Innovatech
#1, 8th Main Road
Vasanthnagar
Bangalore, India 560052
Phone: +91-80-226-6023
Fax: +91-80-228-9727
*e-mail: indiasales@powerint.com*

**APPLICATIONS HOTLINE**
World Wide +1-408-414-9660

**APPLICATIONS FAX**
World Wide +1-408-414-9760