Synchronous Buck PWM and Linear Controller

Features

- Provide Two Regulated Voltages
  - Synchronous Rectified Buck PWM Controller
  - Linear Controller
- Fast Transient Response
  - 0~85% Duty Ratio
- Excellent Output Voltage Regulation
  - 0.8V Internal Reference
  - ±1% Over Line Voltage and Temperature
- Over Current Protection
  - Sense Low-Side MOSFET's $R_{DS(ON)}$
- Under Voltage Lockout
- Small Converter Size
  - 250KHz Free-Running Oscillator
  - Programmable From 70kHz to 800kHz
- 14-Lead SOIC Package
- Lead Free Available (RoHS Compliant)

Applications

- Graphic Cards
- Memory Power Supplies
- DSL or Cable MODEMs
- Set Top Boxes
- Low-Voltage Distributed Power Supplies

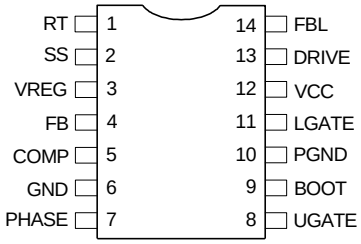
General Description

The APW7063 integrates PWM and linear controller, as well as the monitoring and protection functions into a single package. The synchronous PWM controller which drives dual N-channel MOSFETs, which provides one controlled power outputs with under-voltage and over-current protections. Linear controller drives an external N-channel MOSFET with under-voltage protection.

APW7063 provides excellent regulation for output load variation. An internal 0.8V temperature-compensated reference voltage is designed to meet the various low output voltage applications. APW7063 includes a 250kHz free-running triangle-wave oscillator that is adjustable from below 70KHz to over 800KHz.

A power-on-reset (POR) circuit limits the VCC minimum opearting supply voltage to assure the controller working well. Over current protection is achieved by monitoring the voltage drop across the low side MOSFET, eliminating the need for a current sensing resistor and short circuit condition is detected through the FB pin. The over-current protection triggers the soft-start function until the fault events be removed, but Under-voltage protection will shutdown IC directly.

Pull the COMP pin below 0.4V will shutdown the controller, and both gate drive signals will be low.

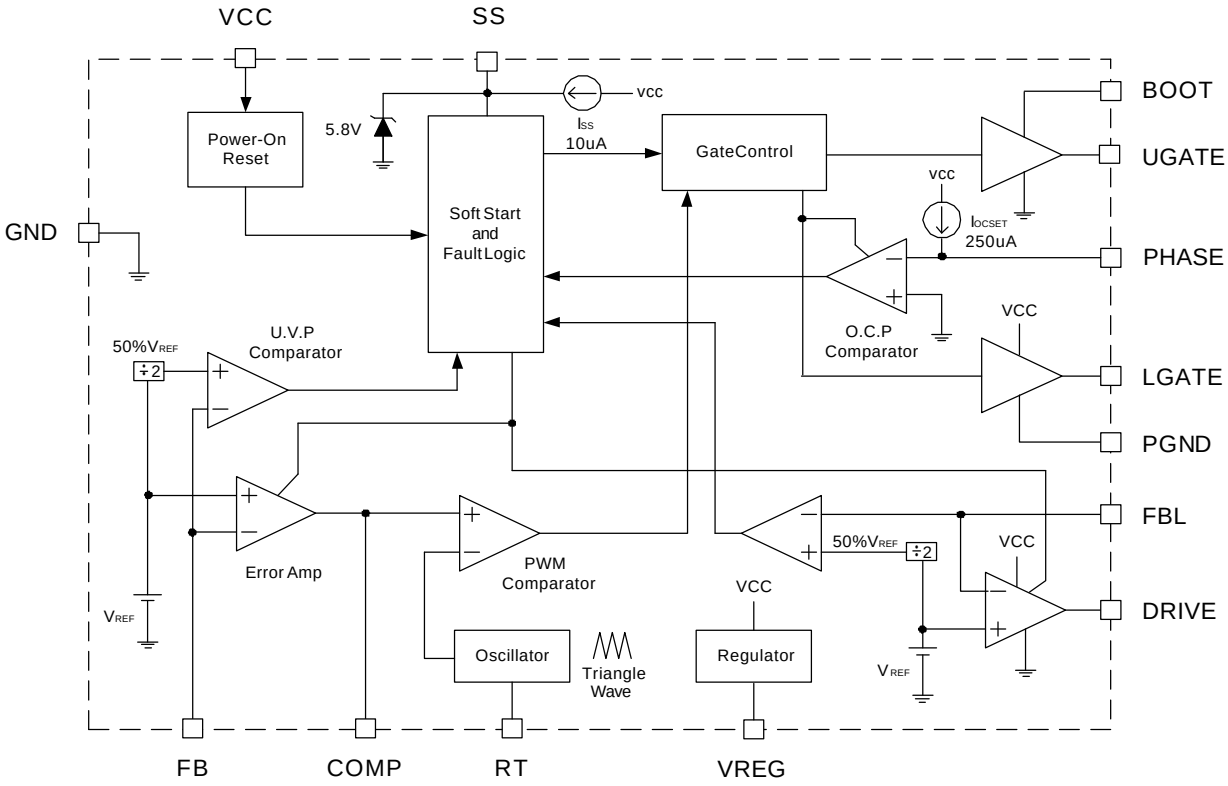


Ordering and Marking Information

APW7063 □□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code K : SOP - 14 Operating Ambient Temp. Range C : 0 to 70°C Handling Code TU : Tube TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Original Device
APW7063 K : APW7063 XXXXX	XXXXX - Date Code

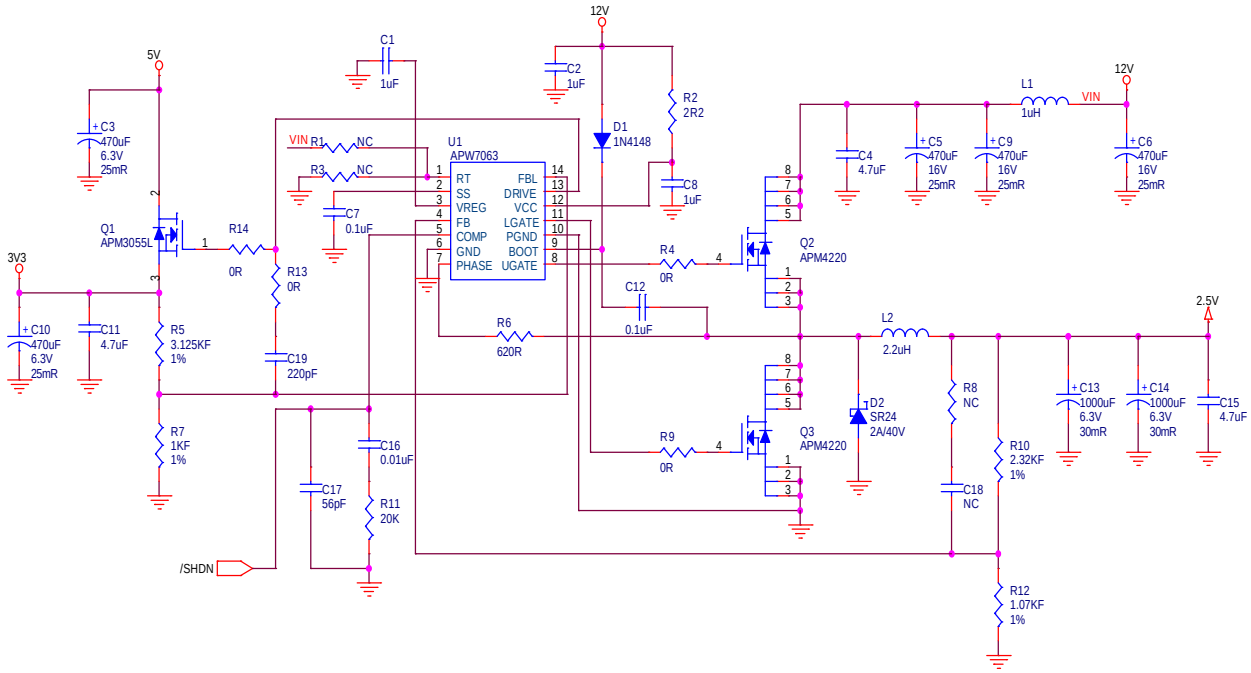
Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Block Diagram

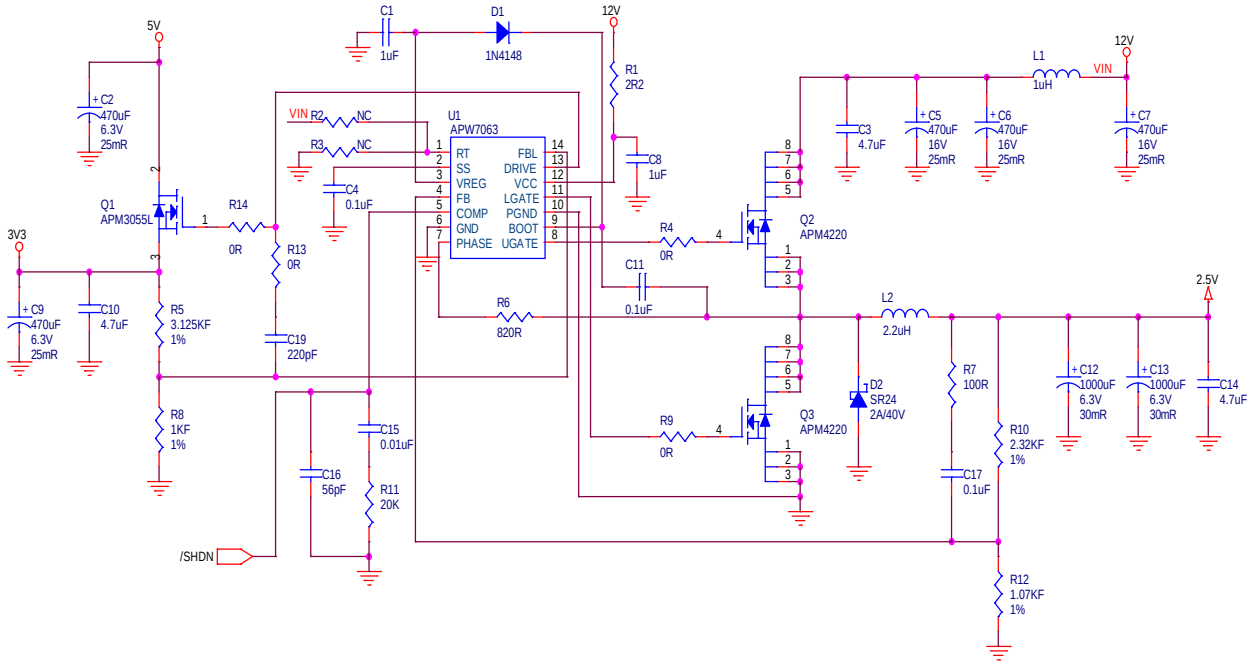


Application Circuit

1. Boot-Strap - Use Internal Regulator



2. Boot-Strap - Use External Power



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	VCC to GND	30	V
LGATE	LGATE to GND	30	V
DRIVE	DRIVE to GND	30	V
UGATE	UGATE to GND	30	V
V_{BOOT}	BOOT to GND	30	V
	PHASE to GND	30	V
	Operating Junction Temperature	0~150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature (10 Seconds)	300	°C
V_{ESD}	Minimum ESD Rating	±2	KV

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
V_{CC}	Supply Voltage	7	12	19	V
V_{BOOT}	Boot Voltage			26	V

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction to Ambient Resistance in free air (SOP-14)	160	°C/W

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC} = 12V, V_{BOOT} = 12V, R_T = OPEN and T_A = 0 ~ 70°C. Typlcal values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7063			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{CC}	VCC Nominal Supply	UGATE and LGATE Open		3		mA
POWER-ON-RESET						
	Rising V_{CC} Threshold		7.0	7.2	7.4	V
	Falling V_{CC} Threshold		6.6	6.8	7.0	V
OSCILLATOR						
	Free Running Frequency	R_T = OPEN, V_{CC} = 12V	220	250	280	kHz
	Total Variation	6KΩ < R_T to GND < 200KΩ	-15		+15	%
	Ramp Amplitude	R_T = OPEN		1.7		V_{P-P}

Electrical Characteristics (Cont.)

Unless otherswise specified, these specifications apply over V_{CC} = 12V, V_{BOOT} = 12V, R_T = OPEN and T_A = 0 ~ 70°C. Typlcal values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	APW7063			Unit
			Min	Typ	Max	
REFERENCE						
V_{REF}	Reference Voltage			0.80		V
	Reference Voltage Tolerance		-1		+1	%
PWM EEEOR AMPLIFIER						
	DC Gain			75		dB
	UGATE Duty Range		0		85	%
	FB Input Current				0.1	uA
GATE DRIVERS						
I_{UGATE}	Upper Gate Source	V_{BOOT} = 12V, V_{UGATE} = 6V	650	800		mA
R_{UGATE}	Upper Gate Sink	I_{UGATE} = 0.3A		4	8	Ω
I_{LGATE}	Lower Gate Source	V_{CC} = 12V, V_{LGATE} = 6V	550	700		mA
R_{LGATE}	Lower Gate Sink	I_{LGATE} = 0.3A		4	8	Ω
T_D	Dead Time			50		nS
LINEAR REGULATOR						
	Reference Voltage			0.8		V
	Regulation			2		%
	Output Drive Current	V_{DRIVE} = 4V	8	10	12	mA
PROTECTION						
	FB Under Voltage Level			50		%
	FBL Under Voltage Level			50		%
	OCSET Source Current			250		µA
VREG						
V_{REG}	Output Voltage Accuracy	$V_{CC} \geq$ 12V	5.5	6	6.5	V
I_{OUT}	Output Current Capacity	V_{CC} = 12V		20		mA
SOFT START and SHUTDOWN						
T_{SS}	Internal Soft-Start Interval	C_{SS} = 0uF		2		mS
I_{SS}	Soft-Start Charge Current		8	10	12	uA
	Shutdown Threshold	COMP Falling		0.4		V
	Shutdown Hysteresis			50		mV

Functional Pin Description

RT (Pin 1)

This pin can adjust the switching frequency. Connect a resistor from RT to V_{CC} for decreasing the switching frequency, Conversely, connect a resistor from RT to GND for increasing the switching frequency (see Typical Characteristics).

SS (Pin 2)

Connect a capacitor from this pin to GND to set the soft-start interval of the converter. An internal 10μA current source charges this capacitor to 5.2V. The SS voltage clamps the reference voltage to the SS voltage, and Figure1 shows the soft-start interval. At t0, the internal source current starts to charge the capacitor and the internal 0.8V reference also starts to rise and follows the SS. Until the internal reference reaches to 0.8V at t2, the soft-start interval is completed. This method provides a rapid and controlled output voltage rise. The way of the Soft-Start of the output2 is the same as the output1, but it starts from the SS at 2.2V to 3.0V. The APW7063 also provides the internal Soft-Start which is fixed to 2ms (t0 to t1). If the external Soft-Start interval is slower than the internal Soft-Start interval (C_{SS}<0.025uF) or no external capacitor, the Soft-Start will follow the internal Soft-Start.

$$T_{Soft\text{-}Start} = t1 - t0 = \frac{C_{SS}}{I_{SS}} \times 0.8V$$

$$t3 = t2 + \frac{C_{SS}}{I_{SS}} \times 0.8V$$

Where:

C_{SS} = external Soft-Start capacitor

I_{SS} = Soft-Start current = 10μA

$$t2 = \frac{C_{SS}}{I_{SS}} \times 2.2V$$

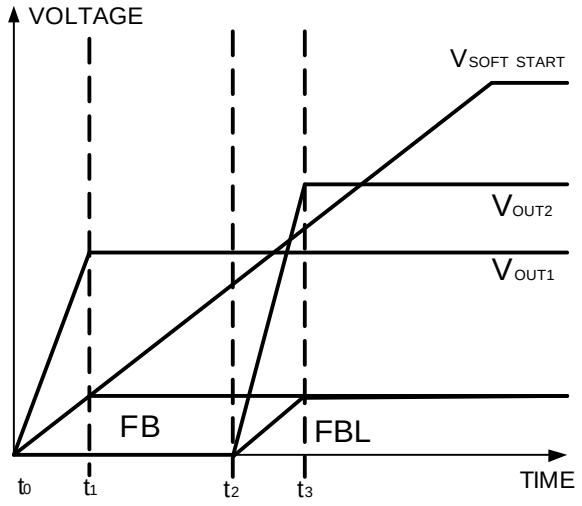


Figure 1. Soft-Start Interval

VREG (Pin 3)

An internal regulator will supply 6V for boost voltage, a 1uF capacitor to GND is recommended for stability. If the VREG voltage has variation by other interference, the IC can not work normally. When the VCC<8V, don't use the VREG for BOOST voltage.

FB (Pin 4)

FB pin is the inverting input of the error amplifier, and it receives the feedback voltage from an external resistive divider across the output (V_{OUT}). The output voltage is determined by :

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where R_{OUT} is the resistor connected from V_{OUT} to FB, and R_{GND} is the resistor connected from FB to GND.

When the FB voltage is under 50% Vref, it will cause the under voltage protection, and shutdown the device. Remove the condition and restart the VCC voltage or pull the COMP from low to high once, will enable the device again.

Functional Pin Description (Cont.)

COMP (Pin 5)

This pin is the output of the error amplifier. Add an external resistor and capacitor network to provide the loop compensation for the PWM converter (see Application Information).

Pull this pin below 0.4V will shutdown the controller, forcing the UGATE and LGATE signals to be 0V. A soft start cycle will be initiated upon the release of this pin.

GND (Pin 6)

Signal ground for the IC.

PHASE (Pin 7)

A resistor (R_{OCSET}) is connected between this pin and the drain of the low-side MOSFET will determine the over current limit. An internally generated 250uA current source will flow through this resistor, creating a voltage drop. This voltage will be compared with the voltage across the low-side MOSFET. The threshold of the over current limit is therefore given by :

$$R_{OCSET} = \frac{I_{LIMIT} \times R_{DS(ON)}}{250uA}$$

An over current condition will cycle the soft start function until the over current condition is removed. Because of the comparator delay time, so the on time of the low-side MOSFET must be longer than 800ns to have the over current protection work.

UGATE (Pin 8)

This pin provides gate drive for the high-side MOSFET.

BOOT (Pin 9)

This pin provides the supply voltage to the high side MOSFET driver. For driving logic level N-channel MOSEFT, a bootstrap circuit can be use to create a suitable driver's supply.

PGND (Pin 10)

Power ground for the gate diver. Connect the lower MOSFET source to this pin.

LGATE (Pin 11)

This pin provides the gate drive signal for the low side MOSFET.

VCC (Pin 12)

This pin provides a supply voltage for the device, when VCC is above the rising threshold 4.2V, It turns on the device is turned on, and conversely, VCC is below the falling threshold 3.9V, the device is turned off. A 1uF decoupling capacitor to GND is recommended.

DRIVE (Pin 13)

Connect this pin to the gate of an external N-channel MOSFET transistor. This pin provides the gate voltage for the linear regulator pass transistor. It also provides a means of compensating the linear controller for applications where the user needs to optimize the regulator transient response.

FBL (Pin 14)

Connect this pin to the output of the linear regulator via a proper sized resistor divider. The voltage at this pin is regulated to 0.8V and the output voltage is determined using the following formula :

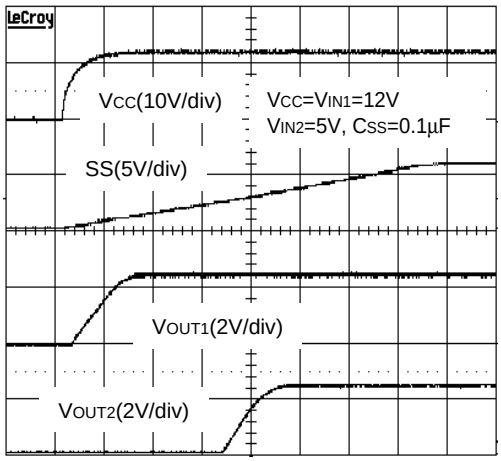
$$V_{OUT} = 0.8V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where R_{OUT} is the resistor connected from V_{OUT} to FBL, and R_{GND} is the resistor connected from FBL to GND.

This pin also monitores the under-voltage events, if the linear regulator is not used, tie the FBL to VREG.

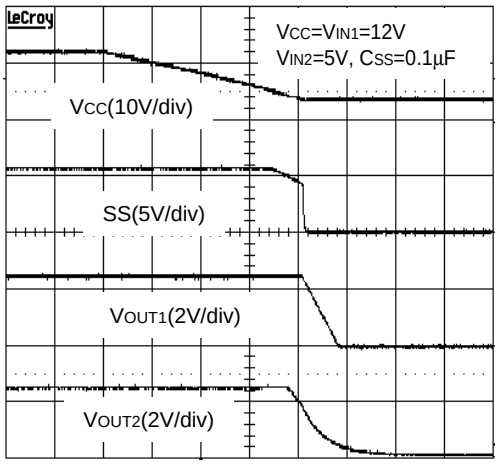
Typical Characteristics

Power Up



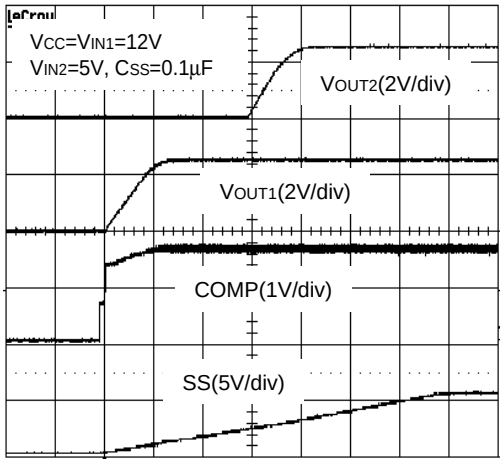
Time (10ms/div)

Power Down



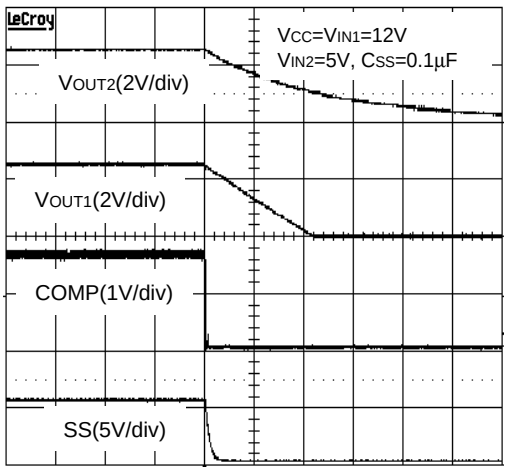
Time (10ms/div)

Enable (COMP is left open)



Time (10ms/div)

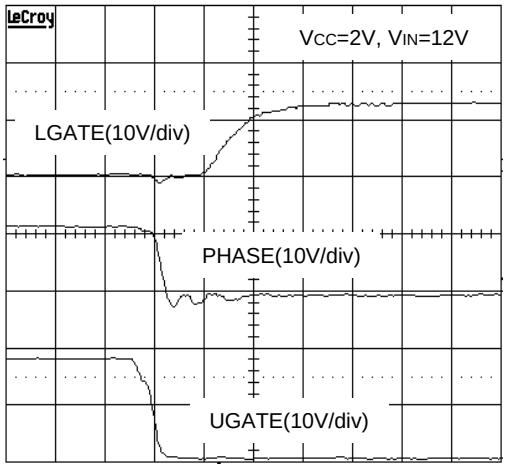
Shutdown (COMP is pulled to GND)



Time (2ms/div)

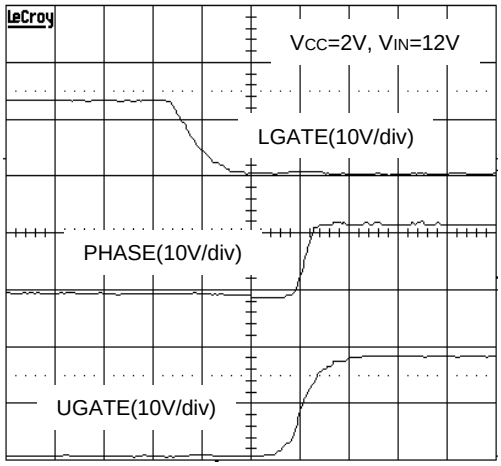
Typical Characteristics (Cont.)

UGATE Falling



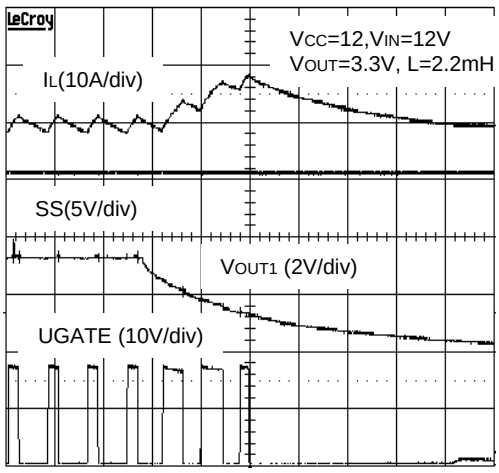
Time (50ns/div)

UGATE Rising



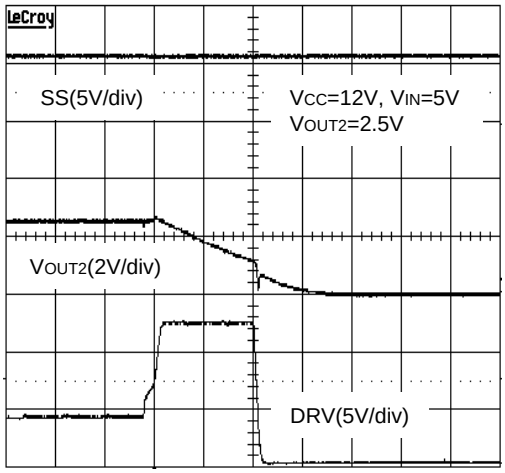
Time (50ns/div)

Under Voltage Protection (PWM)



Time (5us/div)

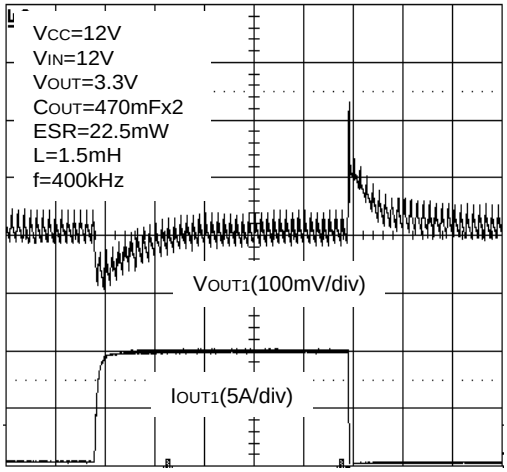
Under Voltage Protection (Linear)



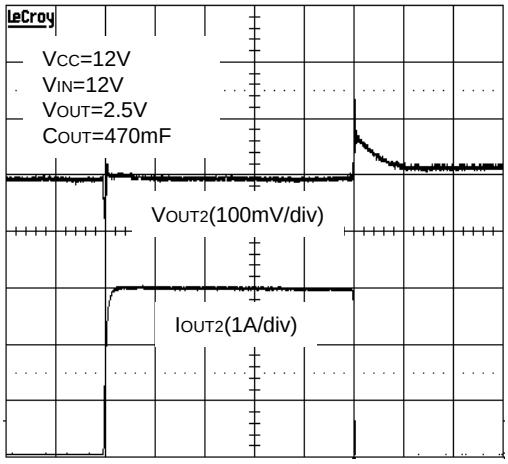
Time (5us/div)

Typical Characteristics (Cont.)

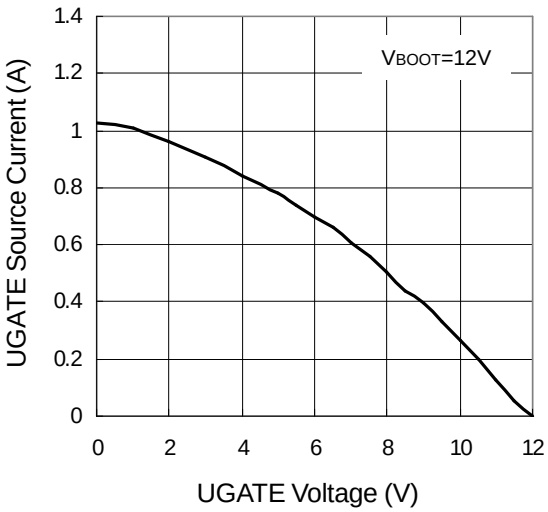
PWM Load Transient



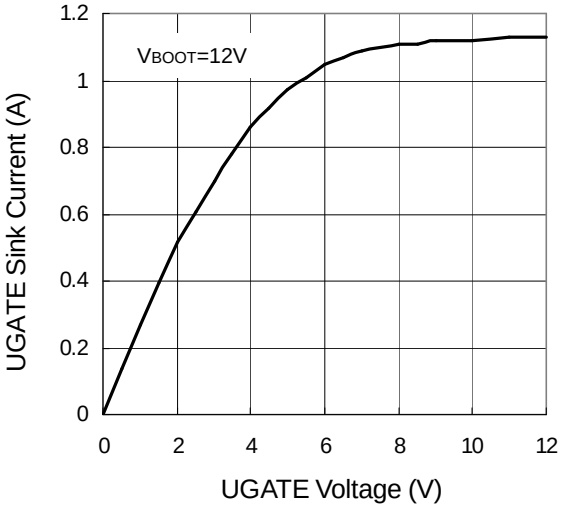
Linear Load Transient



UGATE Source Current vs. UGATE Voltage

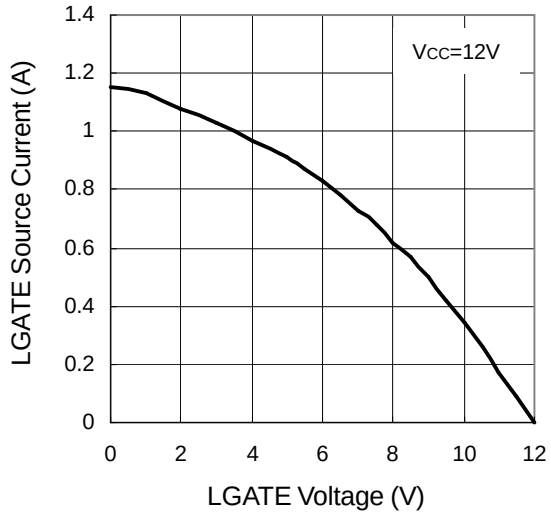


UGATE Sink Current vs. UGATE Voltage

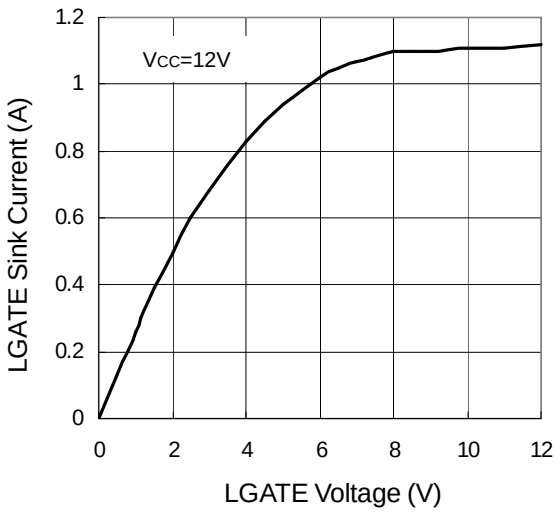


Typical Characteristics (Cont.)

LGATE Source Current vs. LGATE Voltage

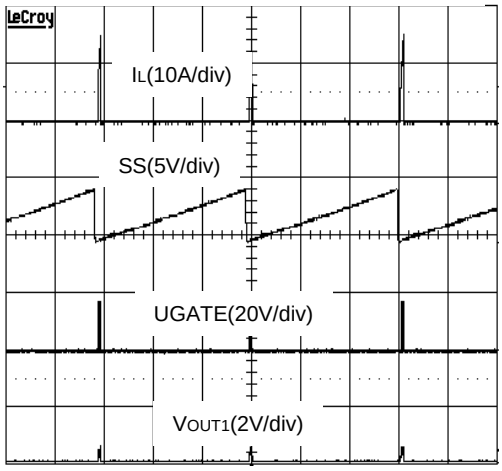


LGATE Sink Current vs. LGATE Voltage

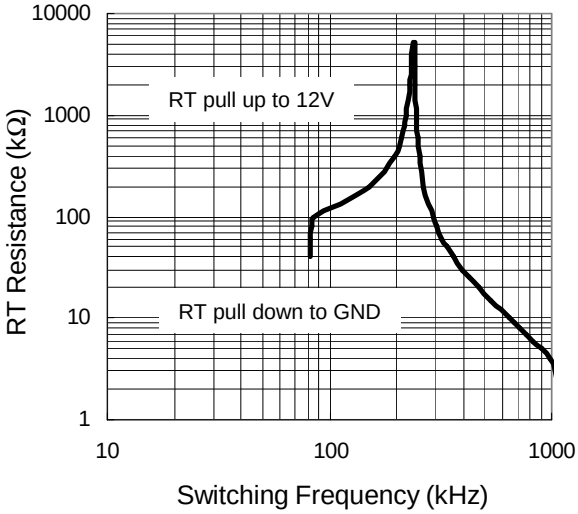


Over Current Protection

Vcc=12V,Vin=12V, Vout=2.5V, Rocset=1kW
Rds(on)=16mW, L=2.2mH, Iout=15A

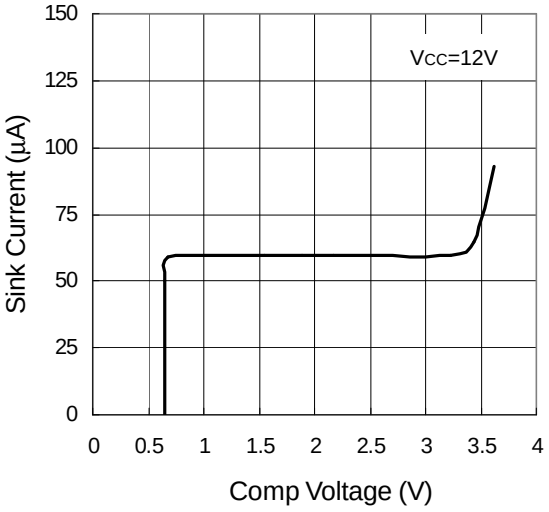


Switching Frequence vs. RT Resistance

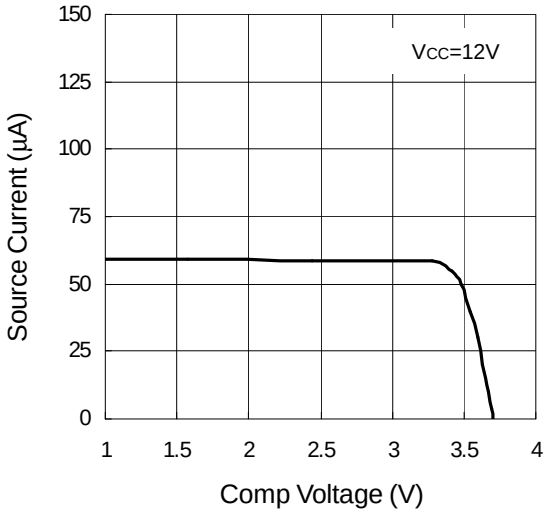


Typical Characteristics (Cont.)

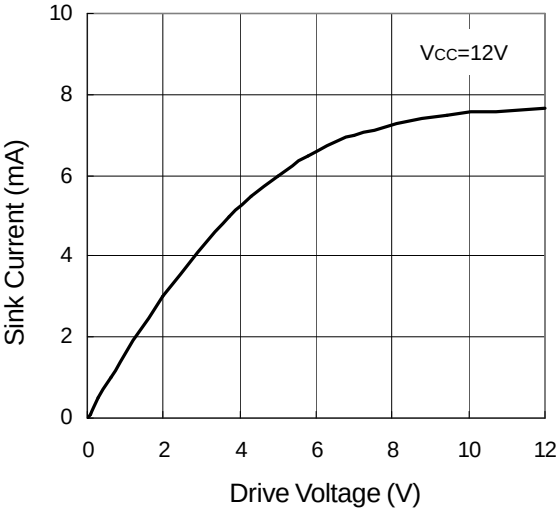
Comp Sink Current vs. Comp Voltage



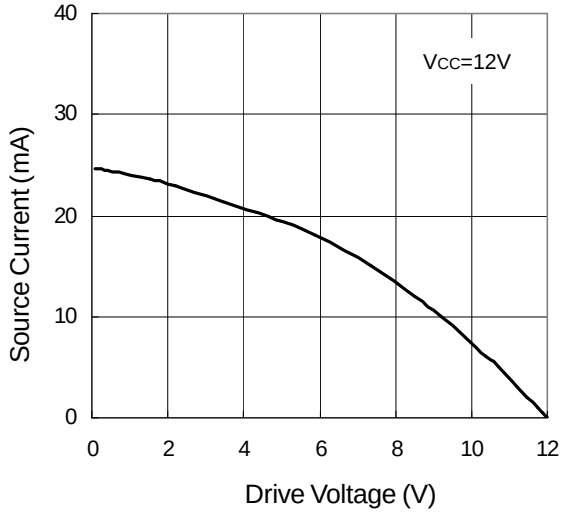
Comp Source Current vs. Comp Voltage



Drive Sink Current vs. Drive Voltage

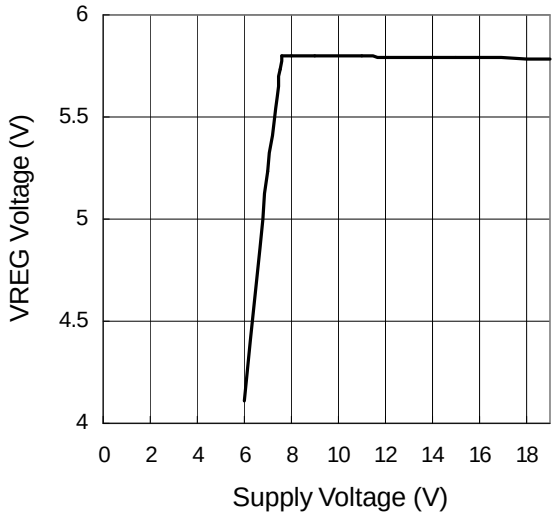


Drive Source Current vs. Drive Voltage

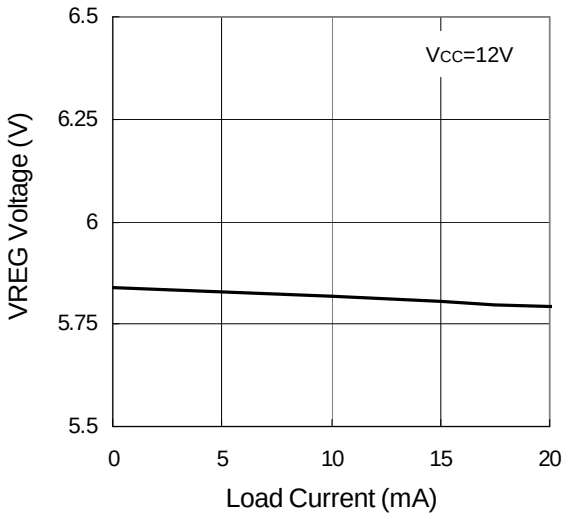


Typical Characteristics (Cont.)

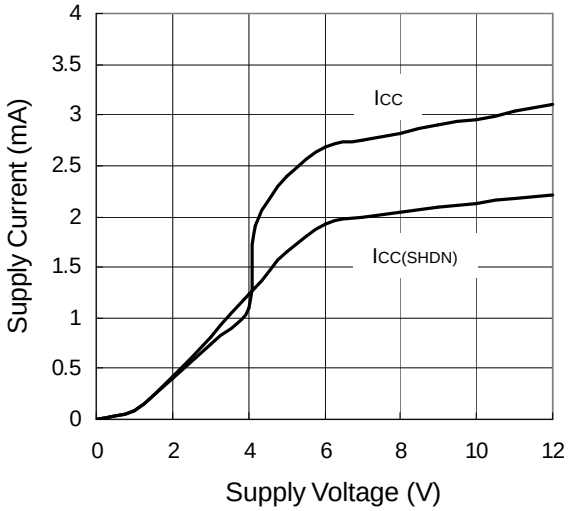
VREG Voltage vs. Supply Voltage



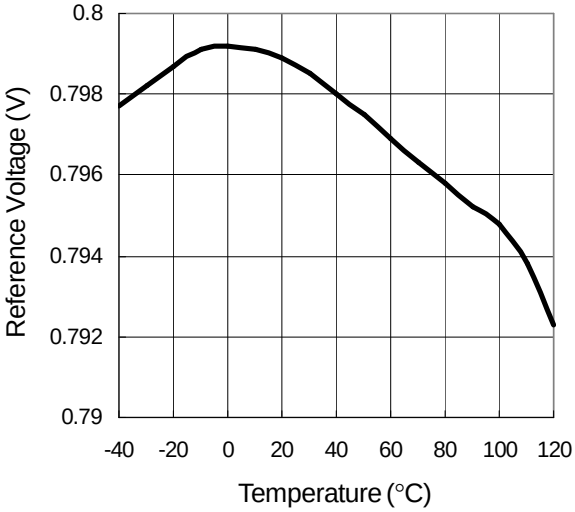
VREG Voltage vs. Load Current



Supply Current vs. Supply Voltage



Reference Voltage vs. Temperature



Application Information

Component Selection Guidelines

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be paralled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1uF to 1uF can be connected between V_{CC} and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

There is a tradeoff exists between the inductor's ripple current and the regulator load transient response time A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some type of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with –40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP pin and ground should be added. The simplest loop compensation network is shown in Fig. 5.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

Application Information (Cont.)

Compensation (Cont.)

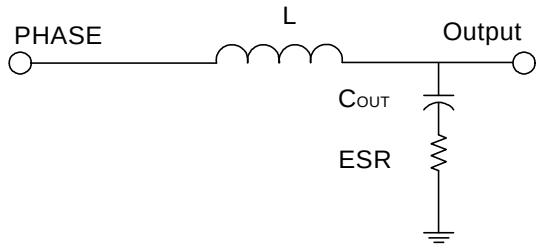


Figure 2. The Output LC Filter

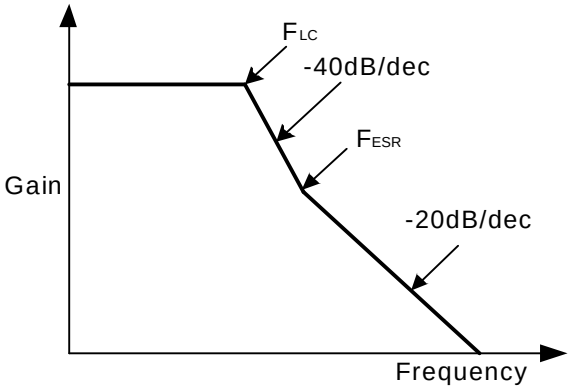


Figure 3. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure. 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

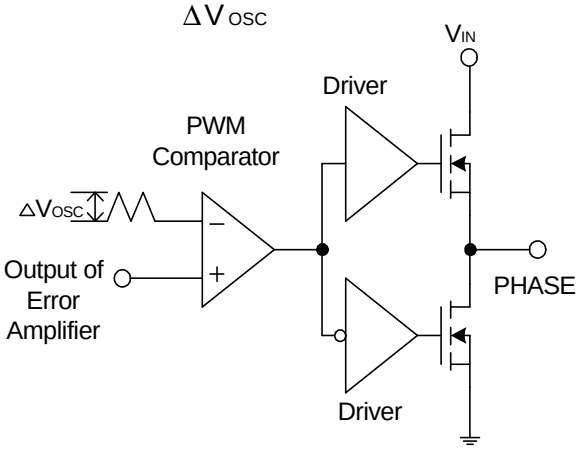


Figure 4. The PWM Modulator

The compensation circuit is shown in Figure 5. R3 and C1 introduce a zero and C2 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Zo = gm \times \left[\left(R3 + \frac{1}{sC1}\right) // \frac{1}{sC2}\right]$$

$$= gm \times \frac{\left(s + \frac{1}{R3 \times C1}\right)}{s \times \left(s + \frac{C1 + C2}{R3 \times C1 \times C2}\right) \times C2}$$

The pole and zero of the compensation network are:

$$F_P = \frac{1}{2 \times \pi \times R3 \times \frac{C1 \times C2}{C1 + C2}}$$

$$F_Z = \frac{1}{2 \times \pi \times R3 \times C1}$$

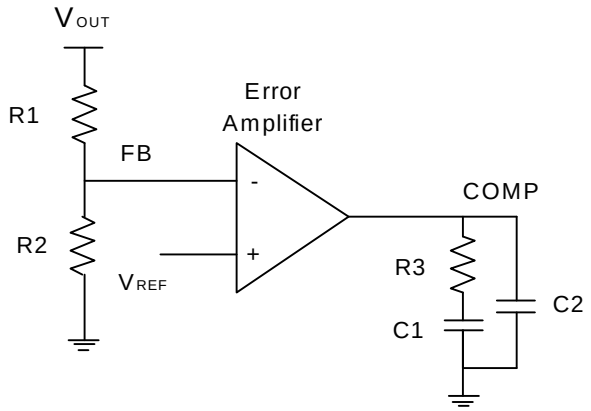


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R2}{R1 + R2} \times GAIN_{AMP}$$

Figure 6 shows the converter gain and the following guidelines will help to design the compensation network.

1.Select the desired zero crossover frequency F_O:

$(1/5 \sim 1/10) \times F_S > F_O > F_Z$

Use the following equation to calculate R3:

Application Information (Cont.)

Compensation (Cont.)

$$R3 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R1+R2}{R2} \times \frac{F_O}{gm}$$

Where:

gm = 900uA/V

2.Place the zero F_Z before the LC filter double poles F_{LC}:

$F_Z = 0.75 \times F_{LC}$

Calculate the C1 by the equation:

$$C1 = \frac{1}{2 \times \pi \times R1 \times 0.75 \times F_{LC}}$$

3. Set the pole at the half the switching frequency:

$F_P = 0.5 \times F_S$

Calculate the C2 by the equation:

$$C2 = \frac{C1}{\pi \times R3 \times C1 \times F_S - 1}$$

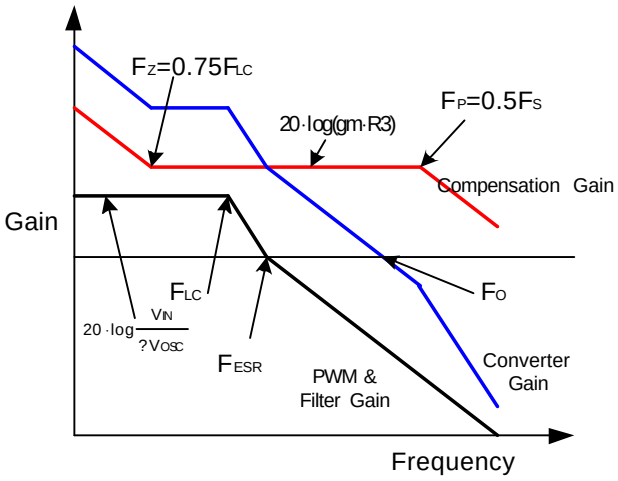


Figure 6. Converter Gain & Frequency

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following :

$$P_{UPPER} = I_{out}^2(1+TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_S$$

$$P_{LOWER} = I_{out}^2(1+TC)(R_{DS(ON)})(1-D)$$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching internal, t_{sw}, is a function of the reverse transfer capacitance C_{RSS}. Figure 7 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Linear Regulator Input/Output Capacitor Selection

The input capacitor is chosen based on its voltage rating. Under load transient condition, the input capacitor will momentarily supply the required transient current. A 1uF ceramic capacitor will be sufficient inmost applications.

The output capacitor for the linear regulator is chosen to minimize any droop during load transient condition. In addition, the capacitor is chosen based on its voltage rating.

Linear Regulator MOSFET Selection

The maximum DRIVE voltage is determined by the V_{CC}. Since this pin drives an external N-channel MOSFET, therefore the maximum output voltage of the linear regulator is dependent upon the V_{GS}.

Application Information (Cont.)

MOSFET Selection (Cont.)

$V_{OUT2MAX} = V_{CC} - V_{GS}$

Another criteria is its efficiency of heat removal. The power dissipated by the MOSFET is given by:

$Pdiss = Iout * (V_{IN} - V_{OUT2})$

where Iout is the maximum load current

V_{out2} is the nominal output voltage

In some applications, heatsink maybe required to help maintain the junction temperature of the MOSFET below its maximum rating.

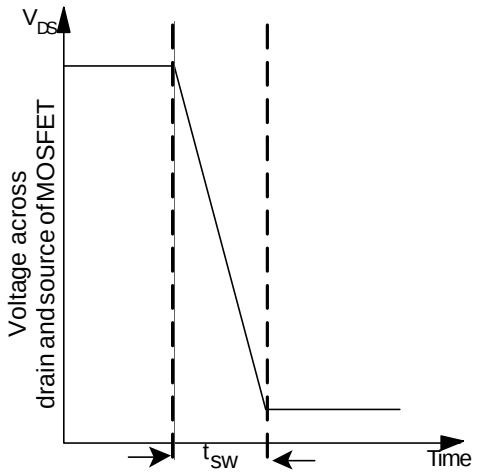


Figure 7. Switching waveform across MOSFET

Layout Considerations

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 8 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

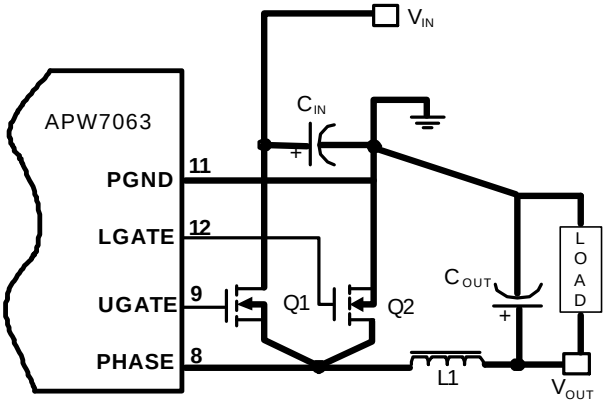
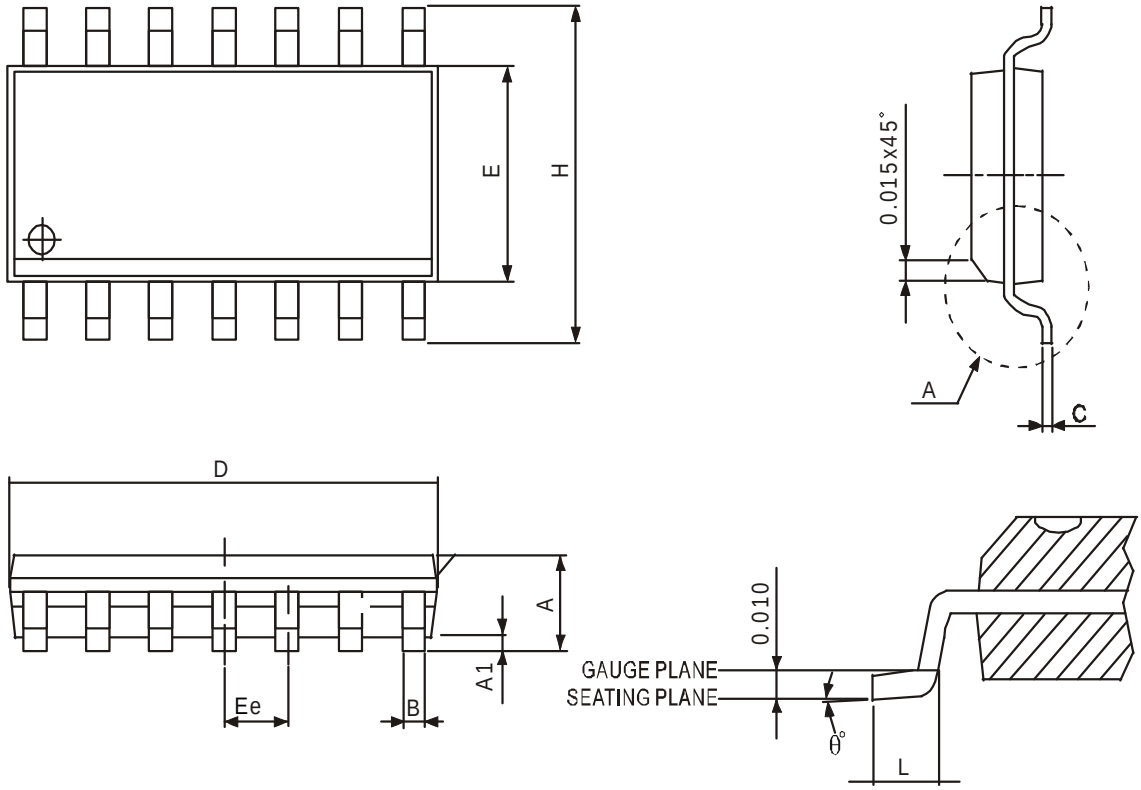


Figure 8. Recommended Layout Diagram

- Keep the switching nodes (UGATE, LGATE and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore keep traces to these nodes as short as possible.
- The ground return of C_{IN} must return to the combine C_{OUT} (-) terminal.
- Capacitor C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.

Package Information

SOP – 14 (150mil)

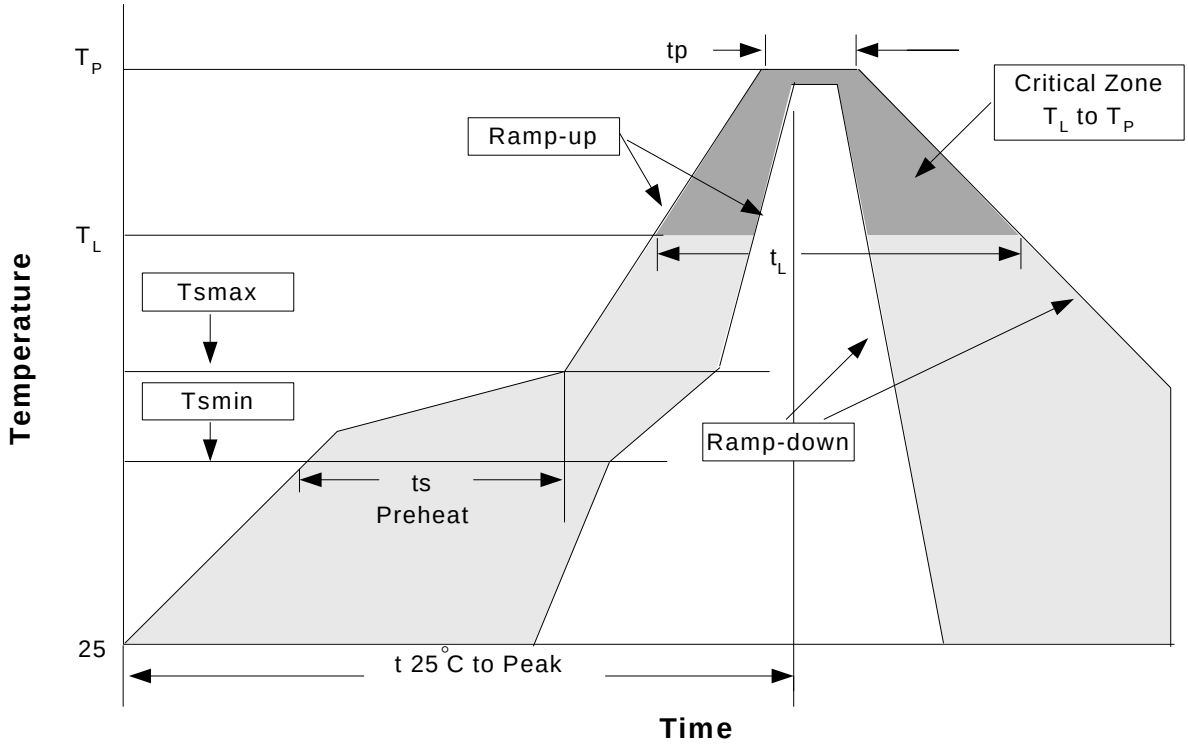


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.477	1.732	0.058	0.068
A1	0.102	0.255	0.004	0.010
B	0.331	0.509	0.013	0.020
C	0.191	0.2496	0.0075	0.0098
D	8.558	8.762	0.336	0.344
E	3.82	3.999	0.150	0.157
e	1.274		0.050	
H	5.808	6.215	0.228	0.244
L	0.382	1.274	0.015	0.050
θ°	0°	8°	0°	8°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

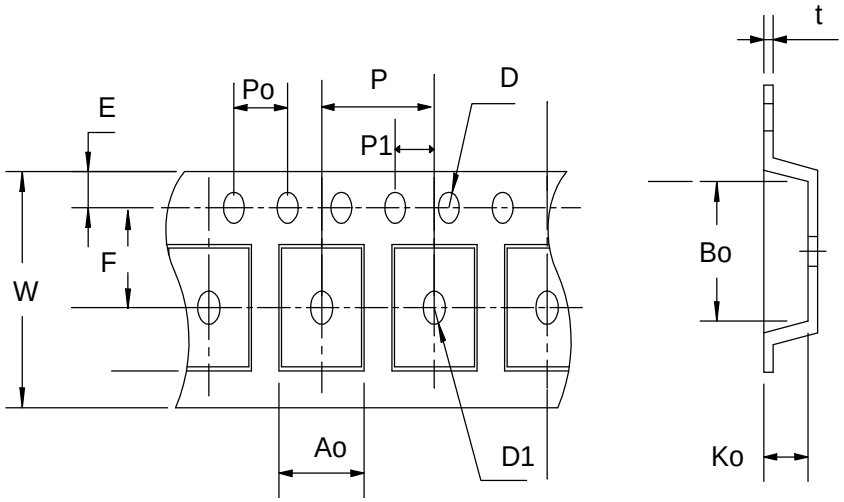
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

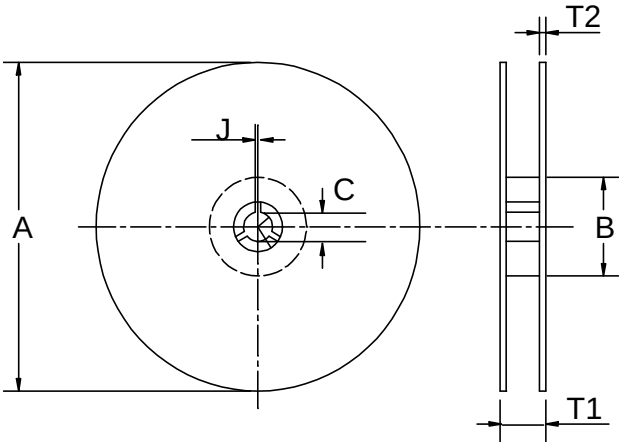
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C,5 SEC
HOLT	MIL-STD 883D-1005.7	1000 Hrs Bias @ 125°C
PCT	JESD-22-B, A102	168 Hrs, 100% RH, 121°C
TST	MIL-STD 883D-1011.9	-65°C ~ 150°C, 200 Cycles

Carrier Tape & Reel Dimensions



Carrier Tape & Reel Dimensions(Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOP-14 (150mil)	330REF	100REF	13.0 + 0.5 - 0.2	2 ± 0.5	16.5REF	2.5 ± 025	16.0 ± 0.3	8	1.75
	F	D	D1	Po	P1	Ao	Ko	t	
	7.5	ϕ0.50 + 0.1	ϕ1.50 (MIN)	4.0	2.0	6.5	2.10	0.3±0.05	

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 14	24	21.3	2500

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