FEATURES

- Drives both high-side and low-side MOSFETs in a synchronous buck configuration
- Large drivers designed to drive 6nF server class FETs
  - Low side driver - 4.0A source / 6A sink
  - High side driver – 3A source / 4A sink
  - Transitions times & Propagation delays < 20ns
- Independent variable gate voltage for both high and low side drivers from 4.5V to 13.2V
  - Improves efficiency
  - Compatible with CHiL controller VGD feature
- Integrated bootstrap diode
  - Reduces external component count
- Capable of high switching frequencies up to 1MHz
- Configurable PWM modes of operation
  - CHiL Active Tri-Level (ATL), disables both MOSFETs in 30ns with no hold-off time
  - Generic tristate PWM with hold-off
- Adaptive non-overlap protection minimizes diode conduction time
- Input supply under voltage protection
- Thermally enhanced 10 pin DFN package
- Lead free RoHS compliant package, MSL level 1

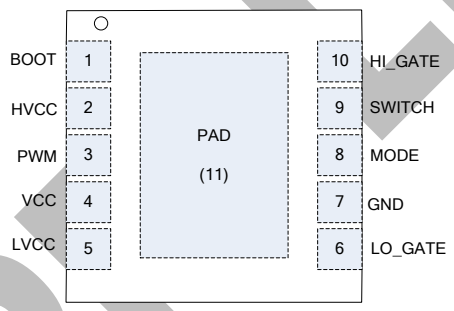

Figure 1. CHL8510 10 pin DFN Package

DESCRIPTION

The CHL8510 MOSFET is a high efficiency gate driver which can switch both high-side and low-side N-channel external MOSFETs in a synchronous buck converter. It is intended for use with CHiL Digital PWM controllers to provide a total voltage regulator (VR) solution for today's advanced computing applications.

The CHL8510 low side driver is capable of rapidly switching large MOSFETs with low R_{dson} and large input capacitance used in high efficiency designs.

The CHL8510 features individual control of both the high- and low-side gate drive voltages from 4.5V to 13.5V. This enables the optimization of switching and conduction losses in the external MOSFETs. When used with CHiL's proprietary Variable Gate Drive (VGD) technology, a significant improvement in efficiency is observed across the entire load range.

The CHL8510 can be configured to drive both the high and low side switches from the unique CHiL fast Active Tri-Level (ATL) PWM signal or a generic tri-state PWM mode. The CHiL ATL mode allows the controller to disable the high and low side FETS in less than 30ns without the need for a dedicated disable pin. This improves VR transient performance, especially during load release.

The integrated boot diode reduces external component count. The CHL8510 also features an adaptive non-overlap control for shoot-through protection. This prevents cross conduction of both high-side and low-side MOSFETs and minimizes body diode conduction time to provide best in class efficiency.

APPLICATIONS

- Multiphase synchronous buck converter for Server and desktop computers using Intel® VR11.x and AMD® microprocessors
- High efficiency and compact VRM
- High current DC/DC Converters

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FUNCTIONAL BLOCK DIAGRAM

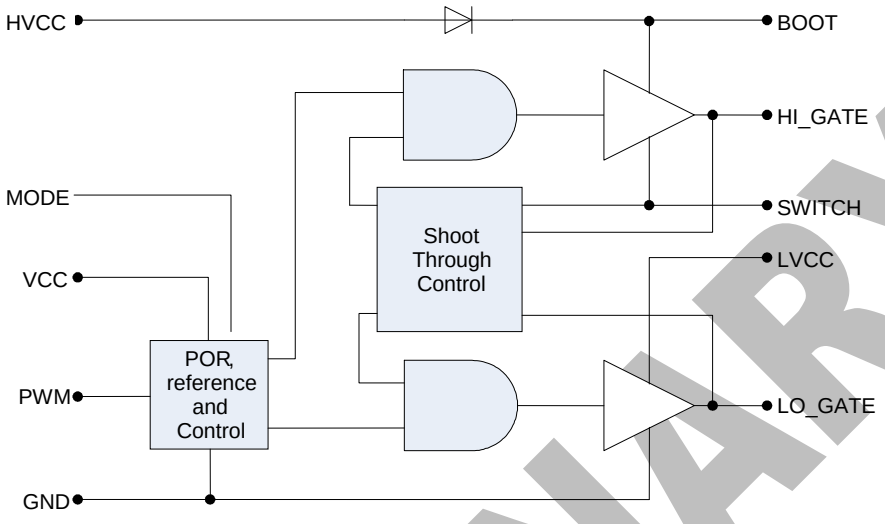


Figure 2. Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	FUNCTION
1	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the SWITCH pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
2	HVCC	Connect this pin to VCC (12V) or to a separate supply between 4.5V and 12V to provide a lower gate drive voltage on the high-side MOSFETS. This is the anode of the internal bootstrap diode. Place a high quality low ESR ceramic capacitor from this pin to GND.
3	PWM	The PWM signal is the control input for the driver from a 1.8V PWM signal. The PWM signal can enter three distinct states during operation; see the three-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
4	VCC	Connect this pin to a +12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
5	LVCC	Connect this pin to Vcc (12V) or a separate supply voltage between 4.5V and 12V to vary the drive voltage on the low-side MOSFETs. Place a high quality low ESR ceramic capacitor from this pin to GND.
6	LO_GATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
7	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
8	MODE	This pin allows selection of the PWM signal voltage for 1.8V or 3.3V normal operation. Floating this pin configures the driver for CHiL Active Tri-Level (ATL) at 1.8V PWM and connecting this pin to ground configures the driver for generic active tri-state operation using 3.3V PWM.
9	SWITCH	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
10	HI_GATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
PAD(11)	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.

TYPICAL APPLICATION

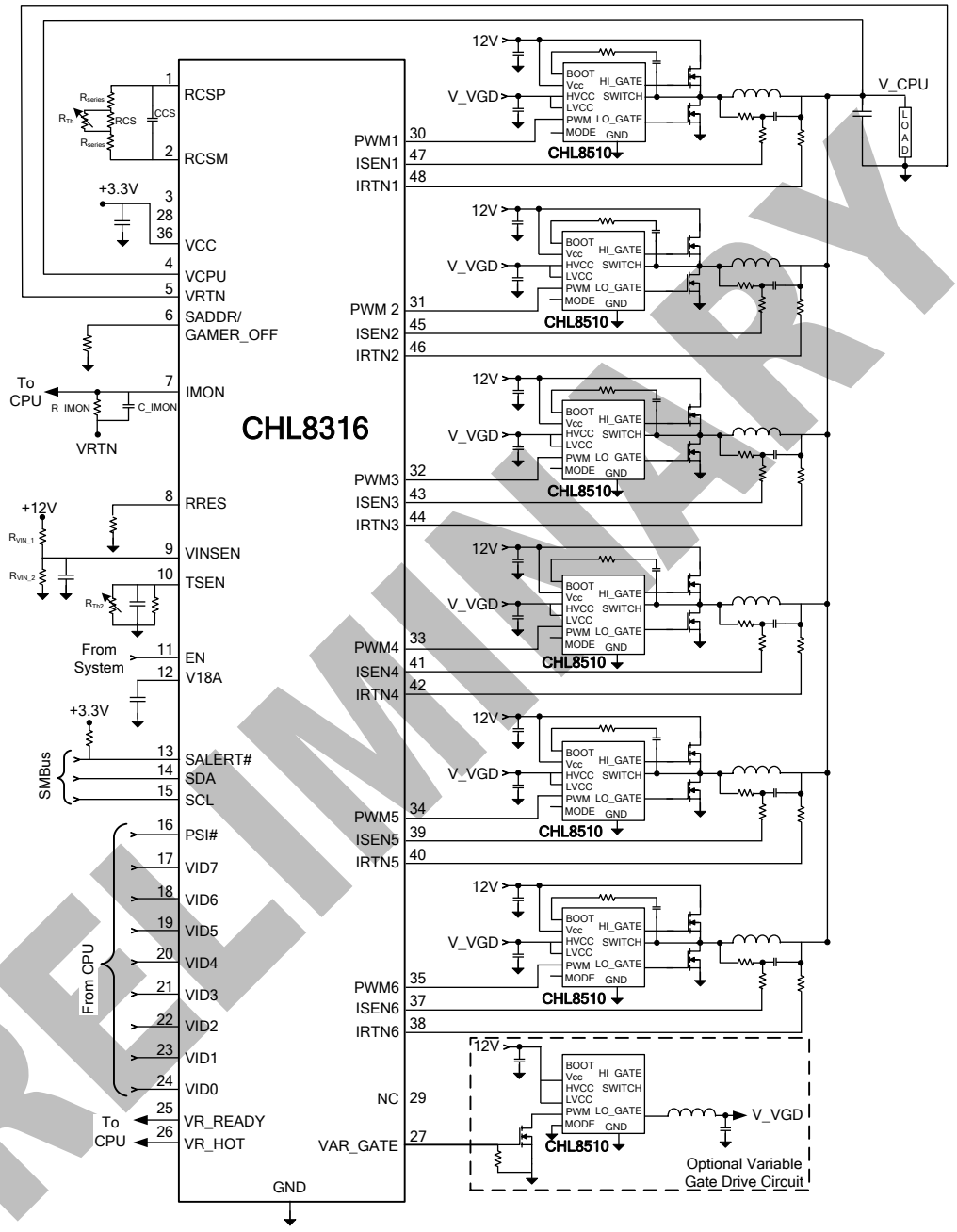


Figure 3. 6-Phase VRD using CHL8510 MOSFET drivers & CHL8316 Controller

ORDERING INFORMATION

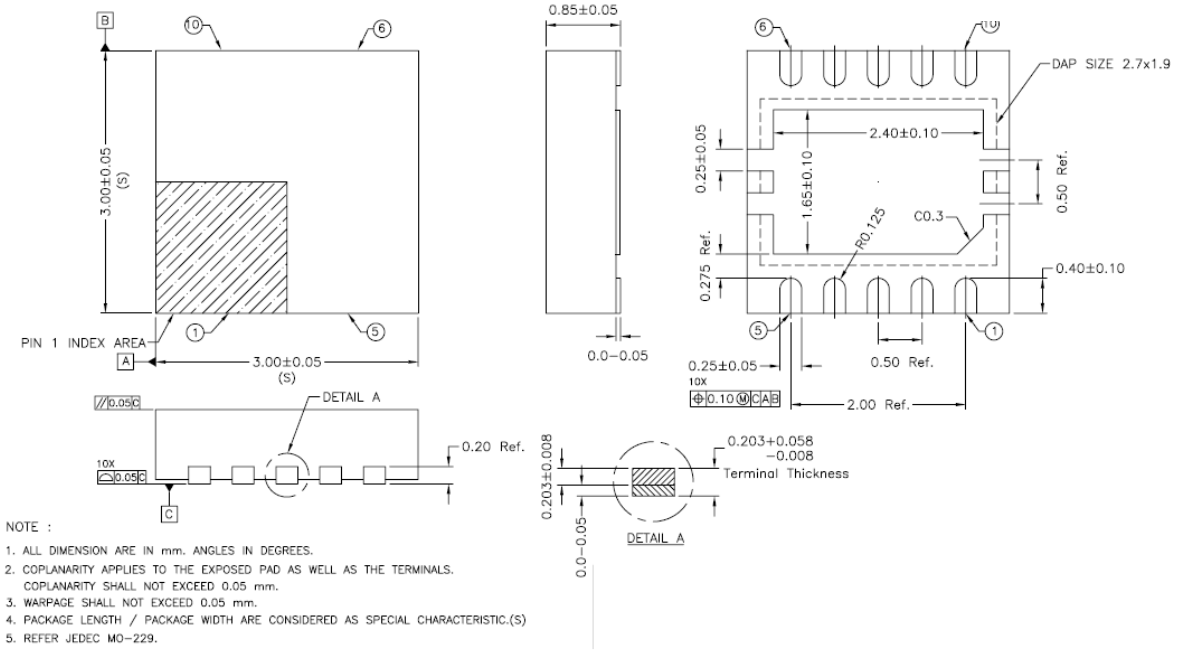
CHL8510 □ □ □

- T: Tape & Reel
- Package type
  R: DFN
- Operating Temperature Range
  C: Commercial Standard

Package	Tape & Reel Qty	Part Number
DFN	3000	CHL8510CRT

PACKAGE INFORMATION

10 pin DFN package



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. REFER JEDEC MO-229.