Features

- Maximum 1.2A Low-Dropout Voltage Regulator
- Ultra Low Dropout Voltage
  Typically 400mV at 1A Output Current
- High Output Accuracy over Line, Load and Temperature
- Build-In Soft-Start
- Excellent startup under load from 0 to 1.2A
- Power-On-Reset Monitoring on V_{DD} Pin
- Foldback over Current Protection and Thermal shutdown
- Low ESR Output Capacitor(Multi-layer Chip Capacitors (MLCC)) Applicable
- SOT-223, SOT-89-5,TO-252,TO-263 and PSOP-8 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Notebook PC Applications
- Motherboard Applications
- LCD Monitor
- Telecom Equipment
- Graphic Cards
- DVD-video Player

General Description

The GS7112 is a three-terminal regulator which can deliver up to 1A of continuous output current with a typical dropout voltage of only 400mV using internal p-channel MOSFETs.

The GS7112 allows the use of low-ESR ceramic capacitor as low as 4.7uF. Moreover the IC provides good performance on both line transient response and load transient response.

The GS7112 provides foldback over current limit and thermal shutdown to prevent the linear regulator from damage. Built-in soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up.

The GS7112 is available in the SOT-223, SOT-89-5,TO-252,TO-263 and PSOP-8 package.

Typical Application

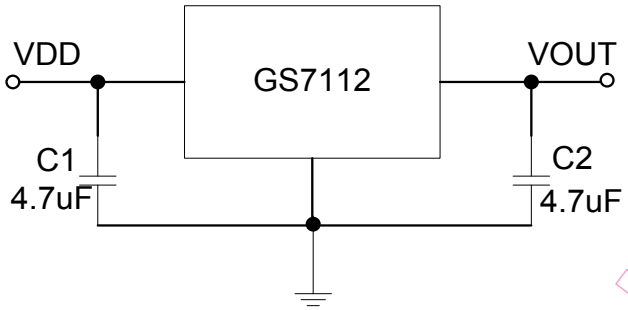


Figure 1a Typical Application of GS7112 (non EN)

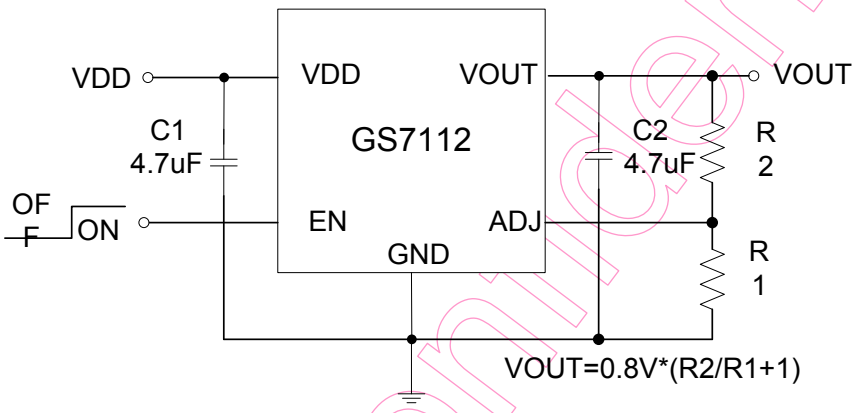


Figure 1b Typical Application of GS7112(ADJ)

Function Block Diagram

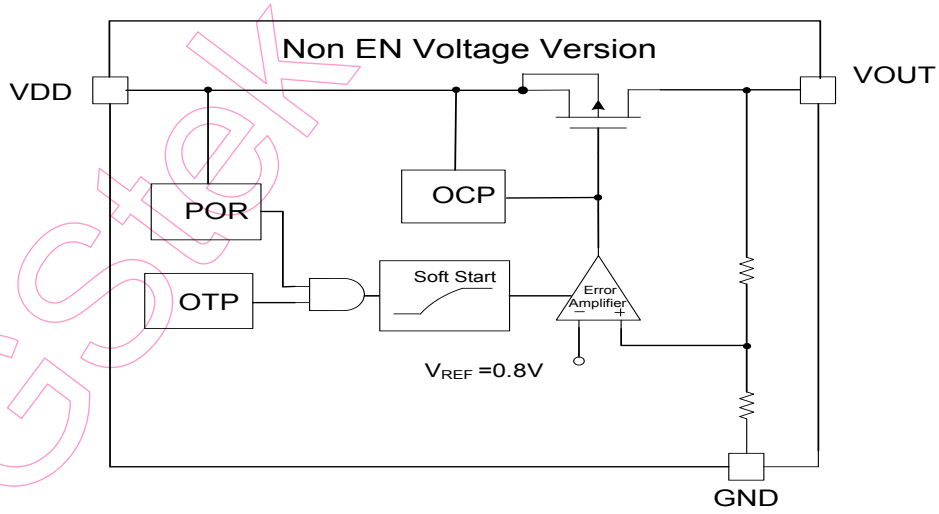


Figure 2a Function Block Diagram (non EN)

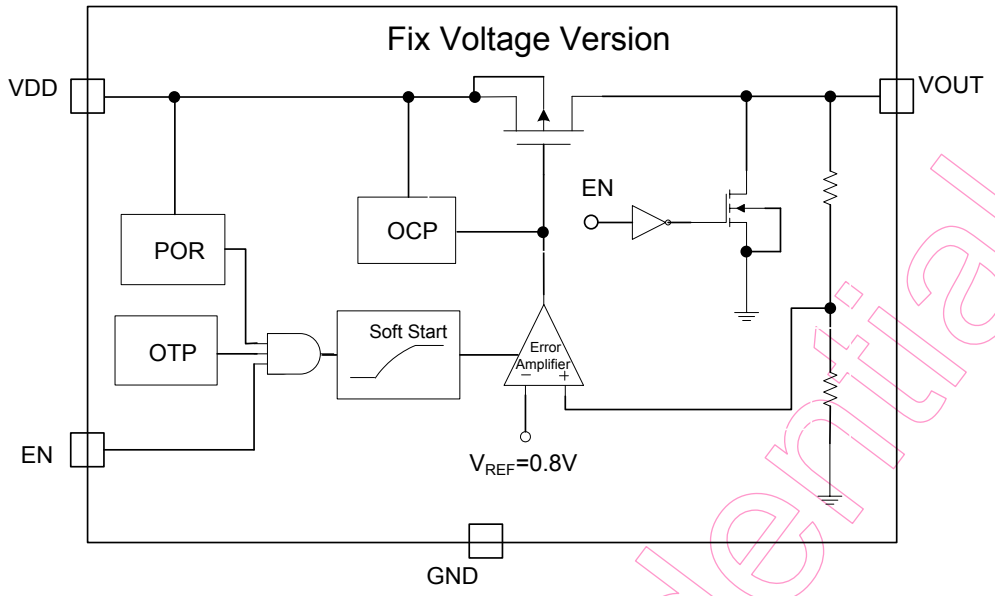


Figure 2b Function Block Diagram (Fix)

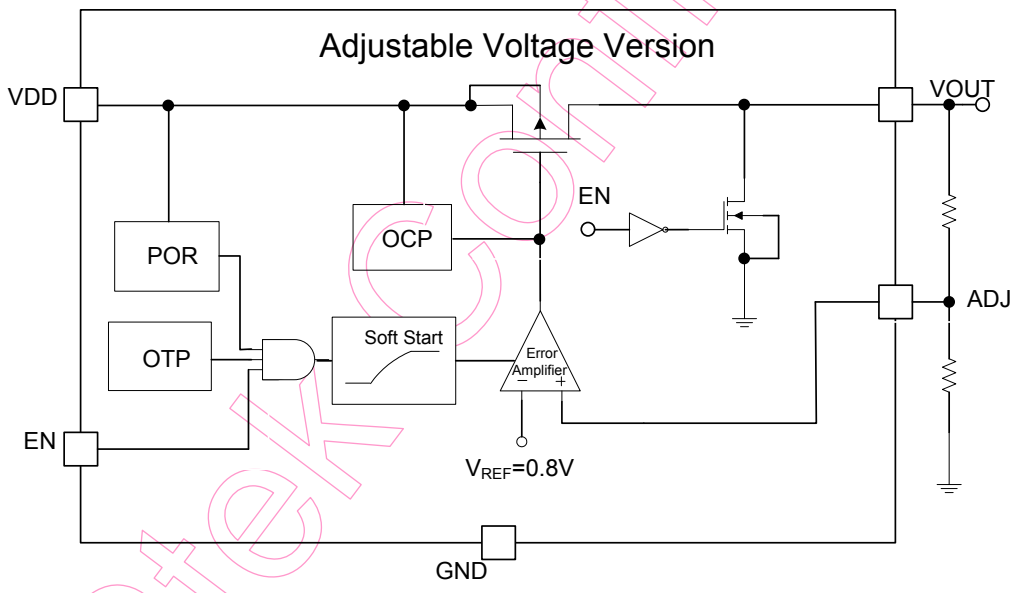
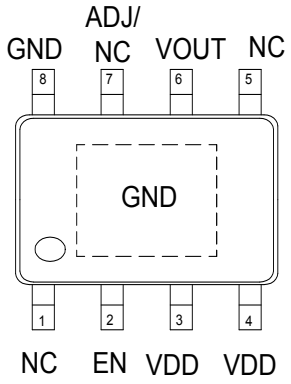
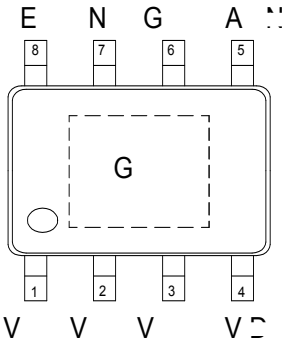


Figure 2c Function Block Diagram (ADJ)

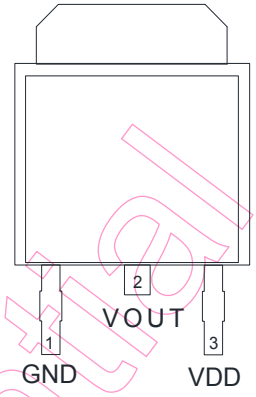
Pin Configuration



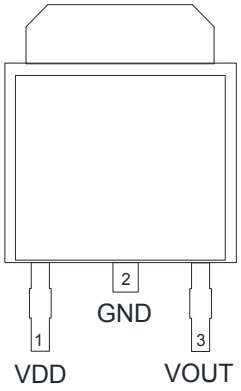
PSOP-8(SO) package



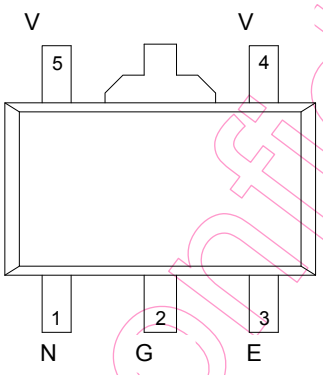
PSOP-8*(SP) package



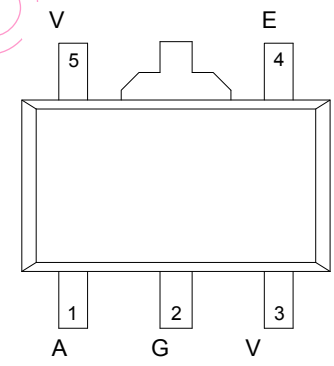
TO-252(D0) package



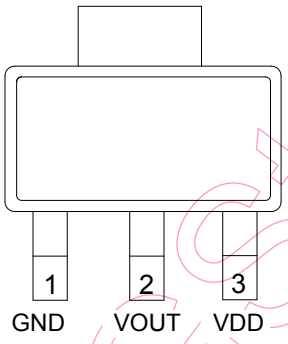
TO-252*(T1) package



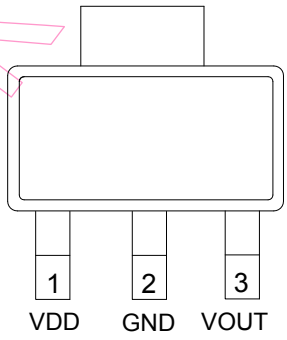
SOT-89-5(F1) package



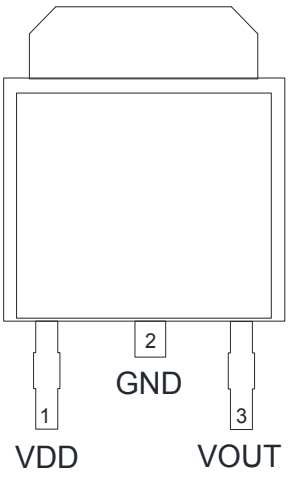
SOT-89-5*(F2) package



SOT-223*(S2) package



SOT-223(S3) package

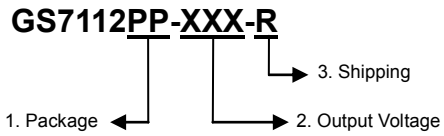


TO-263 package

Pin Descriptions

No.								Name	I/O type	Description
SOT-223*	SOT-223	SOT-89-5	SOT-89-5*	PSOP-8		PSOP-8*	TO-252	TO-252*/ TO-263			
1	2	2	2	8		6	1	2	GND	I/O	Ground pin
2	3	5	3	6		3、4	2	3	VOUT	O	Output Voltage
3	1	4	5	3、4		1、2	3	1	VDD	I/O	Supply voltage
		3	4	2		8			EN	I	Enable input (active high)
		1		1、5	7	7			NC		Not connected
			1			5			ADJ	I	Adjustable input. Feedback pin connect to resistor divider.

Ordering Information



No	Item	Contents
1	Package	S2: SOT-223* S3: SOT-223 F1: SOT-89-5 F2: SOT-89-5* SO:PSOP-8 SP:PSOP-8* D0:TO-252 T1:TO-252* TO:TO-263
2	Output Voltage	ADJ: 0.8V to 5.0V 2P5: 2.5V, 2P8: 2.8V, 285: 2.85V, 3P0: 3.0V, 3P3: 3.3V, 5P0: 5.0V
3	Shipping	R: Tape & Reel, T: Tube

Example: GS7112 PSOP-8 3.3V Tape & Reel ordering information is “GS7112SO-3P3-R”

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Maximum	Units
Control Voltage	V_{DD}	7	V
Package Power Dissipation at $T_A \leqq 25°C$	$P_{D\_SOT-223}$	741	mW
Package Power Dissipation at $T_A \leqq 25°C$	$P_{D\_SOT-89-5}$	500	mW
Package Power Dissipation at $T_A \leqq 25°C$	P_{D_PSOP-8}	1333	mW
Package Power Dissipation at $T_A \leqq 25°C$	P_{D_TO-252}	1333	mW
Package Power Dissipation at $T_A \leqq 25°C$	P_{D_TO-263}	1600	mW
Junction Temperature	T_J	- 45 ~ 150	℃
Storage Temperature	T_{STG}	- 65 ~ 150	℃
Lead Temperature (Soldering) 10S	T_{LEAD}	260	℃
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	$\theta_{JA\_SOT-223}$	135	°C/W
Thermal Resistance Junction to Ambient	$\theta_{JA\_SOT-89-5}$	200	°C/W
Thermal Resistance Junction to Ambient	θ_{JA_PSOP-8}	75	°C/W
Thermal Resistance Junction to Ambient	θ_{JA_TO-252}	75	°C/W
Thermal Resistance Junction to Ambient	θ_{JA_TO-263}	62.5	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
Control Voltage	V_{DD}	$(V_{OUT}+ V_{DROPOUT}) < VDD < 6.5$	V
Junction Temperature	T_J	-40 ~ 125	℃
Ambient Temperature	T_A	-40 ~ 85	℃

Electrical Characteristics

V_{IN}=V_{OUT}+1V, I_{OUT}=0.1mA, C_{VDD}=4.7μF, C_{OUT}=4.7μF, T_A =25°C, unless otherwise specified.

Parameter		Symbol	Test Conditions		Min	Typ.	Max	Units
Input Voltage		V_{DD}			V_{OUT}+$V_{DROPOUT}$ (V_{DD} must≧2.3V)		6.5	V
Output Voltage accuracy		V_O			-2		2	%
Adjustable input voltage(Note 5, 9)		V_{ADJ}	I_{OUT}=0.1mA		0.784	0.8	0.816	V
Dropout Voltage (Note 6)		V_{DROP}	I_O=1000mA,V_O=3.3V			400	550	mV
			I_O=1200mA,V_O=3.3V			500	650	mV
Current limit		I_{LIMIT}				1.6		A
Short current limit (Note 7)		I_{SC}	V_O <0.2			100		mA
Quiescent Current		I_Q				85	120	uA
Line Regulation		V_{R-LINE}	I_O=1mA, V_{DD} = V_O +1V to 6.5V		-0.2		0.2	%/V
Load Regulation		V_{R-LOAD}	I_O=1mA to 1000mA			60	80	mV
POR threshold						2.1		V
EN Threshold (Note 8,9)	Logic-Low Voltage	V_{EN-L}					0.4	V
	Logic-High Voltage	V_{EN-H}			1.4			
EN Input Bias Current (Note 9)		I_{EN}	V_{EN}=5V			0.3	1	uA
Over temperature shutdown		T_{SD}				160		℃
Return temperature						130		℃
Power supply rejection		PSRR	I_O=100mA	f=1kHz		50		dB
				f=20KHz		22		

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A=25℃ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. SOT-89-5*, PSOP-8 and PSOP-8* Package.

Note 6. The Dropout voltage is defined as V_{IN}-V_{OUT}, which is measured when V_{OUT} is 0.98*$V_{OUT(NORMAL)}$.

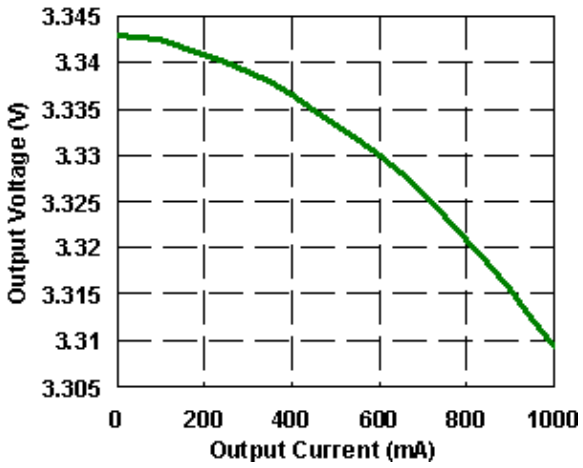
Note 7. If V_{OUT} is detected as <0.2V, then Io is restricted to typical 100mA.

Note 8. SOT-89-5, SOT-89-5*, PSOP-8 and PSOP-8* Package.

Note 9. 5 Pin application.

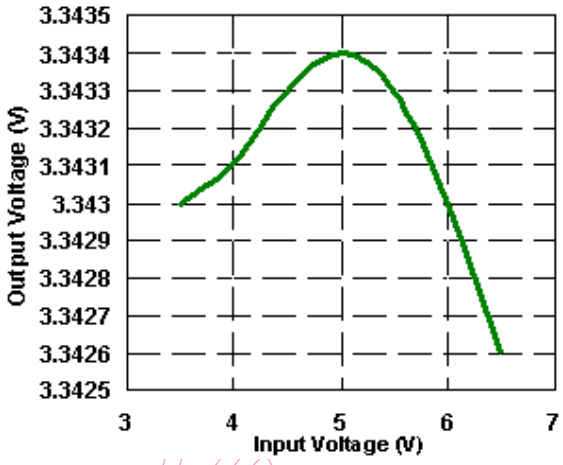
Typical Characteristics

Load Regulation

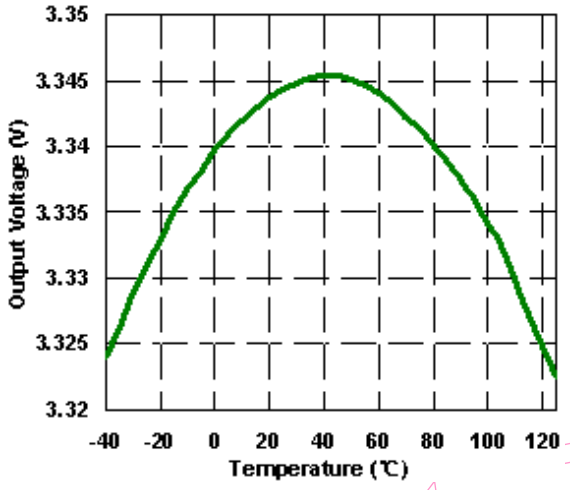


Output Voltage vs. Temperature

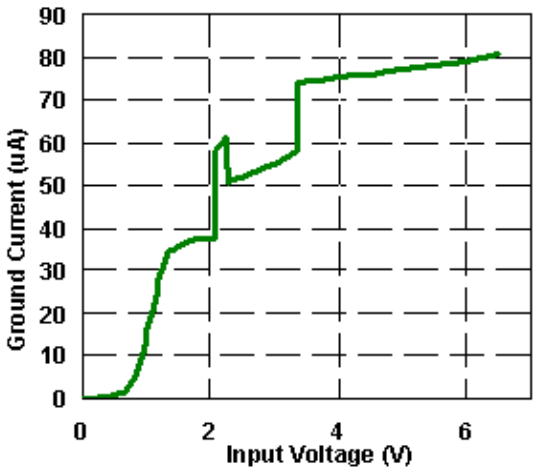
Line Regulation



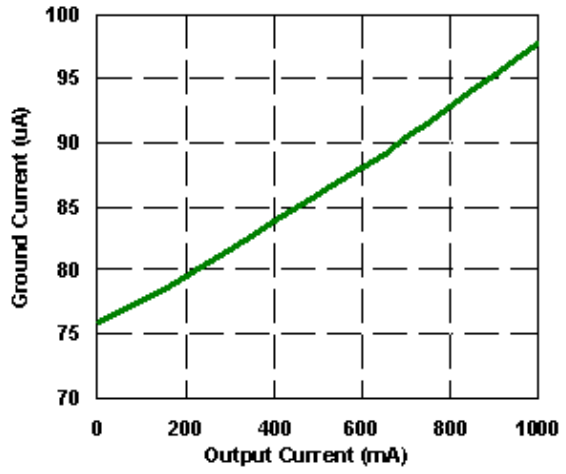
Ground Current vs. Input Voltage



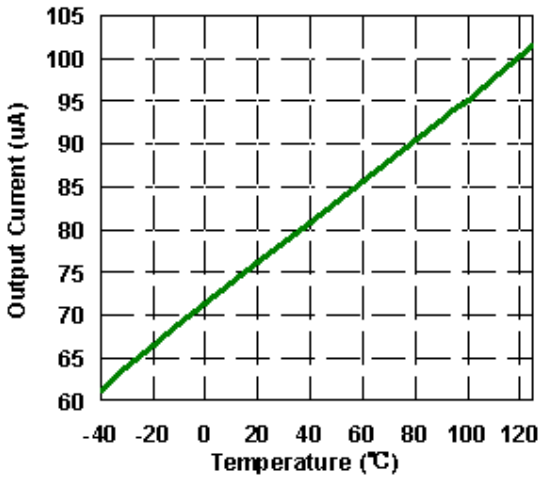
Ground Current vs. Load Current



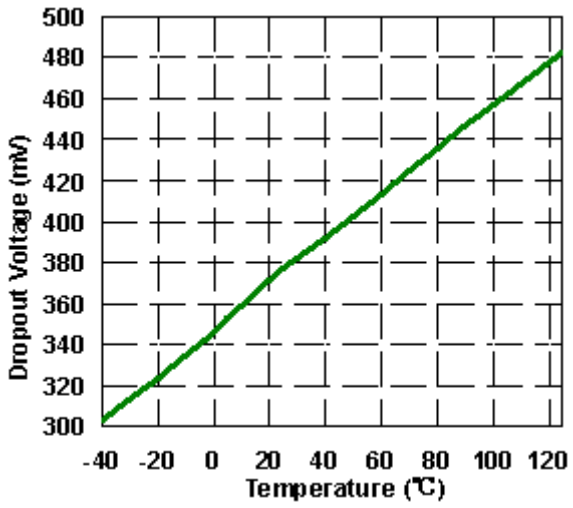
Ground Current vs. Temperature



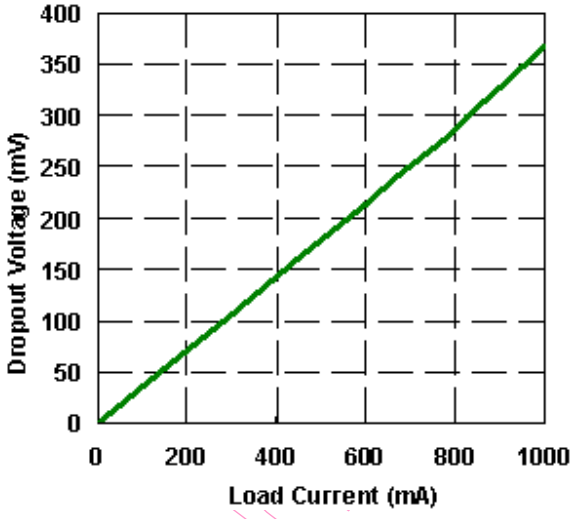
Dropout vs. Temperature



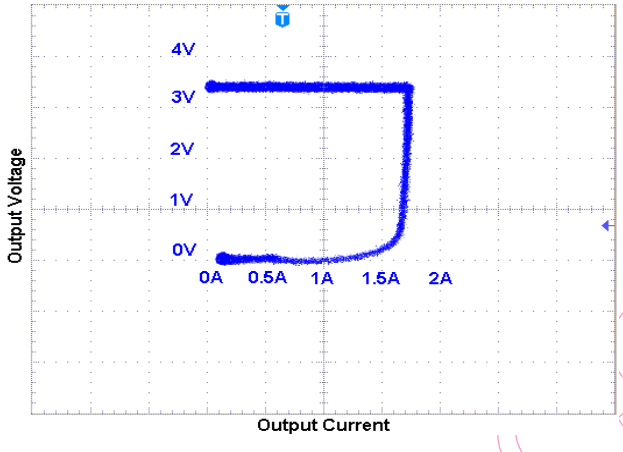
Dropout vs. Load Current



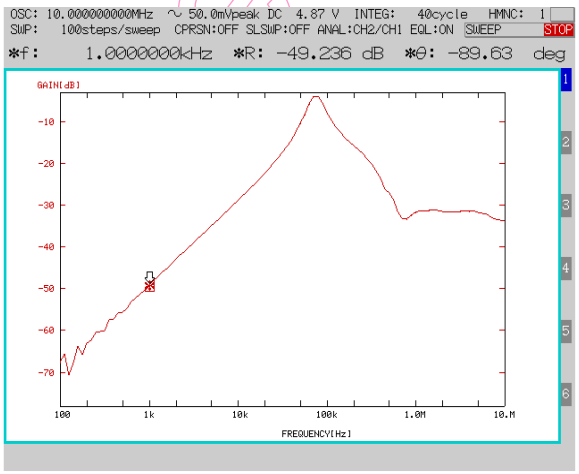
Circuit Current vs. Input Voltage



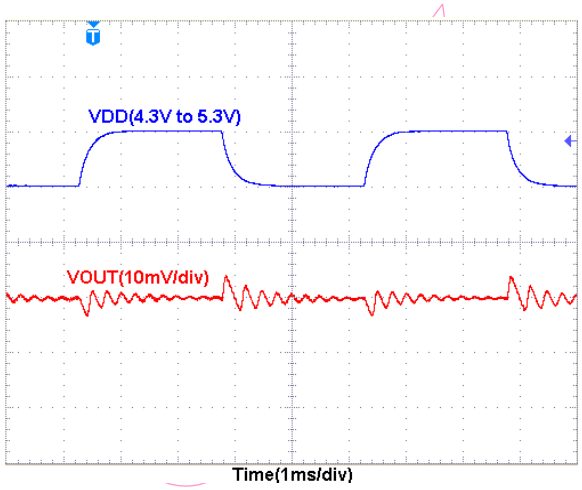
PSRR vs. Frequency



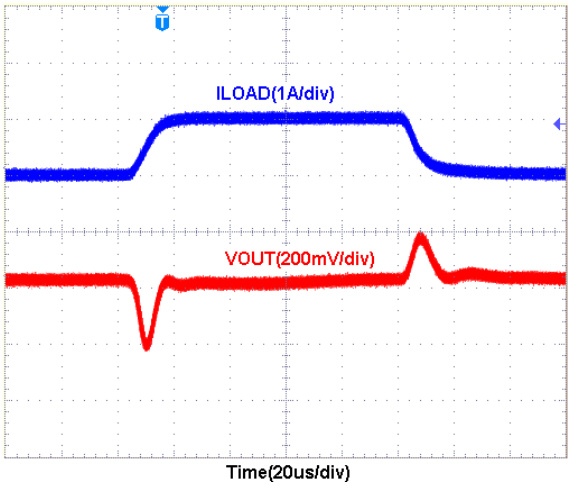
Line Transient Response



Load Transient Response



V_{OUT} =3.3V, I_{OUT} =0.1mA



V_{OUT} =3.3V,V_{DD}=4.3V

Application Information

Power-on-Reset

The GS7112 features a power-on-reset control through monitor the supply voltage to prevent wrong operation. Only after the supply voltage exceed its rising POR threshold voltage, the regulator is to be initiated and starts up.

Build-In Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 0.5mS.

Current Limit

The GS7112 contains a foldback over current protection function. It allows the output current to reach the maximum value of 1.6A. Then further decreases in the load resistance reduce both the load current and the load voltage. The main advantage of foldback limiting is less power dissipation in the pass transistor under shorted-load conditions. During startup, the current limit value is set to high, thus GS7112 can operate in full load condition. After startup, the current limit value is set to normal value, so the pass transistor is protected well.

Thermal-Shutdown Protection

Thermal Shutdown protects GS7112 from excessive power dissipation. If the die temperature exceeds 160℃, the pass transistor is shut off.30℃ of hysteresis prevents the regulator from turning on until the die temperature drops to 130℃.

Output Capacitor selection

The GS7112 is specifically designed to employ ceramic output capacitor as low as 4.7uF. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Input Capacitor selection

Bypass VDD to ground with a 4.7uF or greater capacitor. Ceramic, tantalum or aluminum electrolytic capacitors may be selected for input capacitor. However ceramic capacitors are recommended due to their significant cost and space savings. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Power Dissipation and Layout Considerations

Although internal thermal limiting function is integrated in GS7112, continuously keeping the junction near the thermal shutdown temperature may possibly affect device reliability. For continuous operation, it is highly recommended to keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The power dissipation definition in device is:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{DD} \times I_Q$

The maximum power dissipation can be calculated as:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The thermal resistance θ_{JA} for PSOP-8 package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.33W (SOP-8 Exposed Pad on the minimum layout)

The thermal resistance θ_{JA} of PSOP-8 is determined by the package design and the PCB design. Copper plane under the exposed pad is an effective heat sink and is useful for improving thermal conductivity. As shown in Figure 3, the amount of copper area to which the PSOP-8 is mounted affects thermal performance. When mounted to the standard PSOP-8 pad (Figure 3a), θ_{JA} is 75°C/W. Adding copper area of pad under the PSOP-8 Figure 3b) reduces the θ_{JA} to 54°C/W. Even further, increasing the copper area of pad to 70mm2 (Figure 3c) reduces the θ_{JA} to 49°C/W.

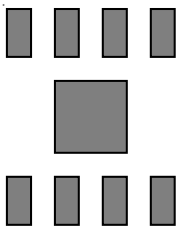


Figure 3 (a) Minimum Footprint, θ_{JA} = 75°C/W

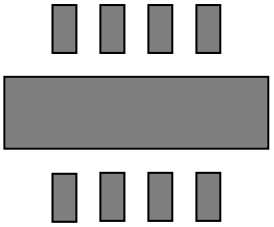


Figure 3 (b) Copper Area = 30mm², θ_{JA} = 54°C/W

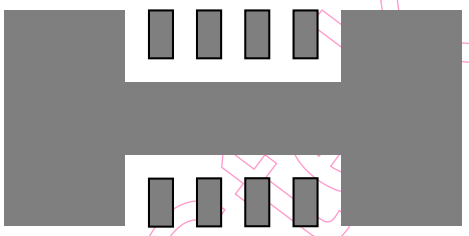


Figure 3 (c) Copper Area = 70mm², θ_{JA} = 49°C/W

Figure 3 θ_{JA} vs. Different Cooper Area Layout Design

And Figure 4 shows a curve for the θ_{JA} of the PSOP-8 package for different copper area sizes using a typical PCB with 2oz copper in still air.

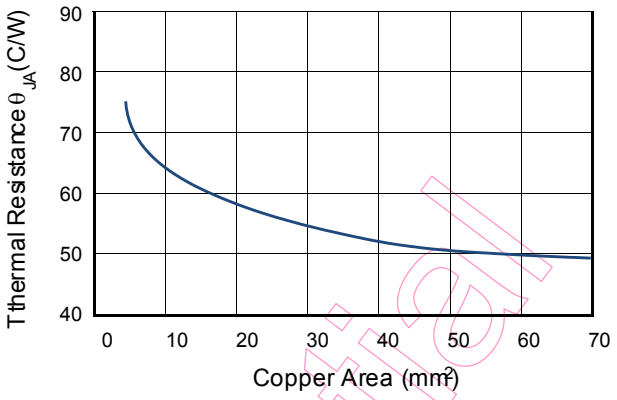


Figure 4 θ_{JA} vs. Copper Area

The maximum power dissipation depends on operating ambient temperature or fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For GS7112 packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

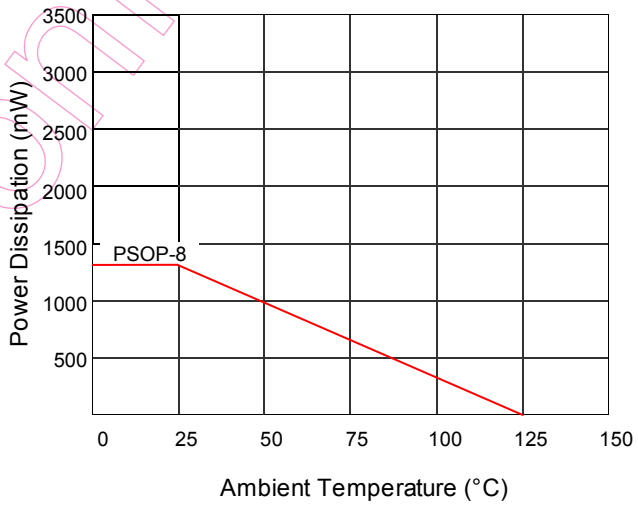
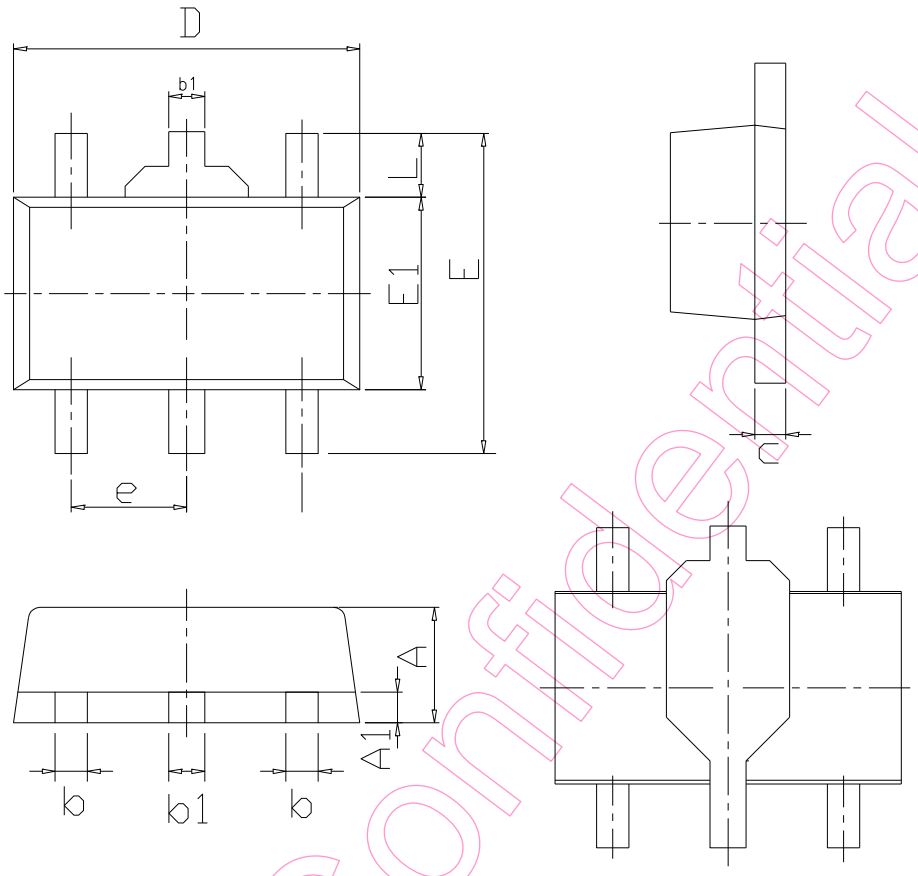


Figure 5 Derating Curve for Packages

Package Dimensions, SOT-89-5



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.40	1.60
A1	0.30	0.50
b	0.36	0.48
b1	0.41	0.53
C	0.38	0.43
D	4.40	4.60
E	--	4.25
E1	2.40	2.60
e	1.50 REF.	
L	0.80	--

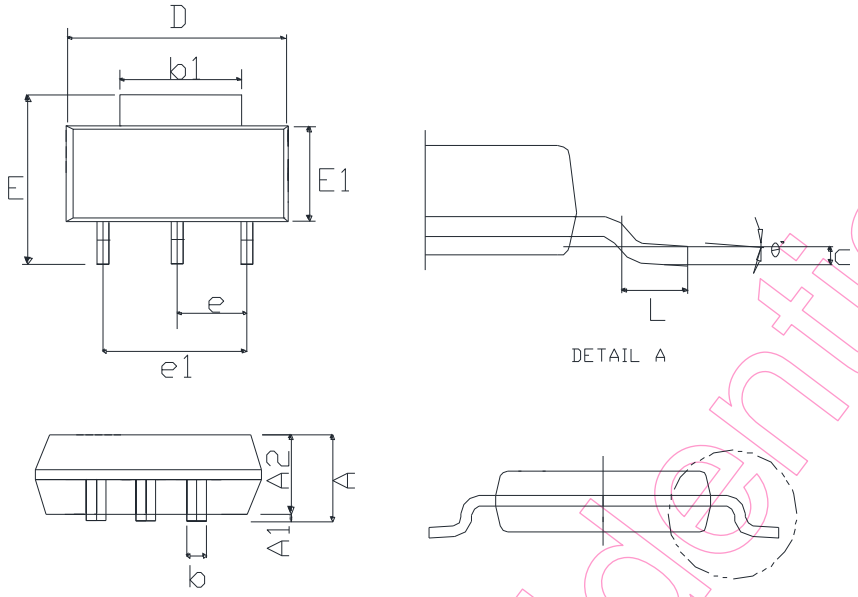
Note

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, SOT-223

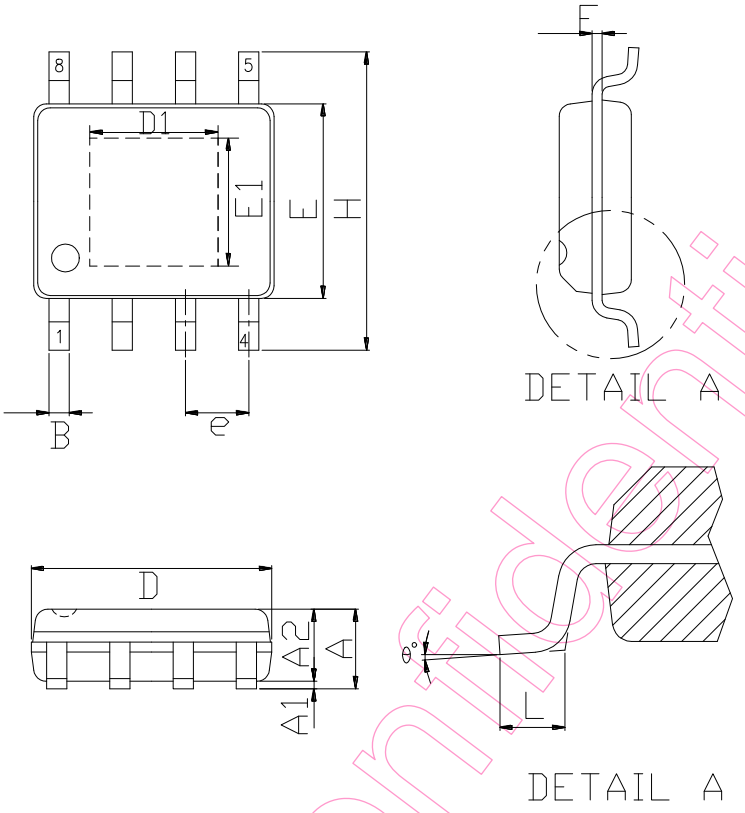


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	--	1.80
A1	0.00	0.10
A2	1.50	1.70
b	0.65	0.82
b1	2.90	3.10
D	6.20	6.60
c	0.25	0.35
E	6.80	7.20
E1	3.30	3.70
e	2.30 REF.	
e1	4.60 REF.	
L	0.80	1.20
θ	0^{o}	10^{o}

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

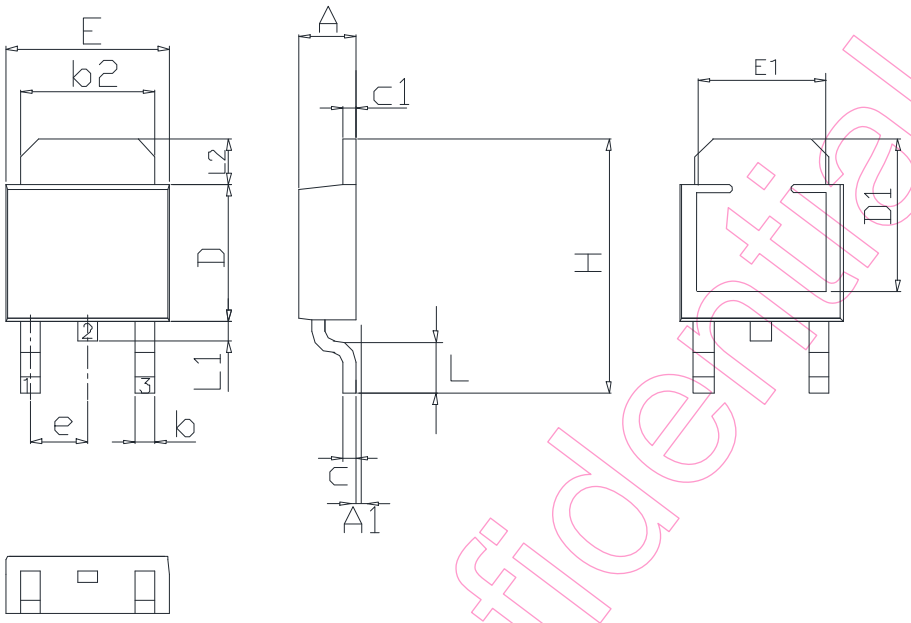
Package Dimensions, PSOP-8(S)



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.30	1.80
A1	-	0.15
A2	1.24	-
B	0.31	0.51
D	4.70	5.10
E	3.80	4.00
D1	2.00	2.30
E1	2.00	2.30
e	1.27 REF.	
F	0.17	0.25
H	5.80	6.20
L	0.40	1.27
θ	0^{o}	8^{o}

Note
1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TO-252

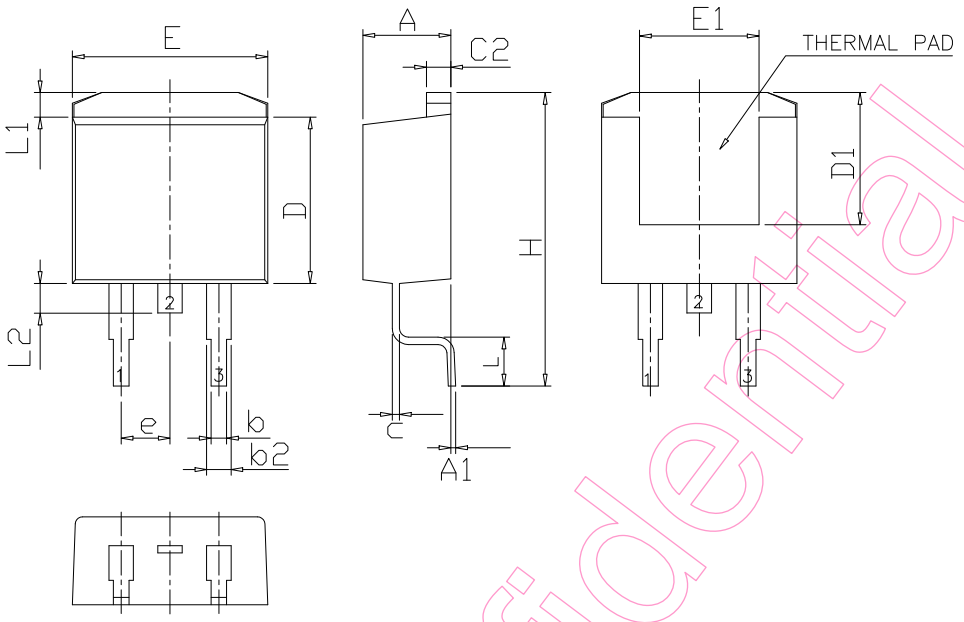


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.15
b	0.50	0.70
b2	5.20	5.50
c	0.43	0.60
c1	0.43	0.58
D	5.40	6.20
E	6.35	6.80
D1	4.57	--
E1	3.80	--
e	2.30 REF.	
H	9.40	10.40
L	1.40	1.78
L1	0.35	1.20
L2	0.89	1.65

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TO-263



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	4.06	4.82
A1	0.00	0.25
b	0.70	1.00
b2	1.17	1.47
c	0.31	0.53
c2	1.17	1.45
D	8.50	9.25
D1	6.60 REF.	
E	9.80	10.40
E1	7.80 REF.	
e	2.54 REF.	
H	14.6	15.8
L	2.00	2.80
L1	1.27 REF.	
L2	1.50 REF.	

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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