NEXSEM

SINGLE CHANNEL MOBILE PWM CONTROLLER WITH PFM AND PWM MODE

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2130 controller IC is a compact Buck controller IC with 16 lead MLPQ package designed for step down DC to DC converter in portable applicaitons. It can be selected to operate in synchronous mode for continuous fixed PWM or non-synchronous mode to improve the efficiency at light load.Voltage feedforward provides fast response, good line regulation and nearly constant power stage gain under wide voltage input range. The NX2130 controller is optimized to convert single supply up to 24V bus voltage to as low as 0.8V output voltage. Internal UVLO keeps the regulator off until the supply voltage exceeds 4.5V where internal digital soft starts get initiated to ramp up output. Over current protection and FB UVLO followed by latch off feature. Other features includes: 5V gate drive capability, power good indicator, over voltage protection, output and adaptive dead band control.

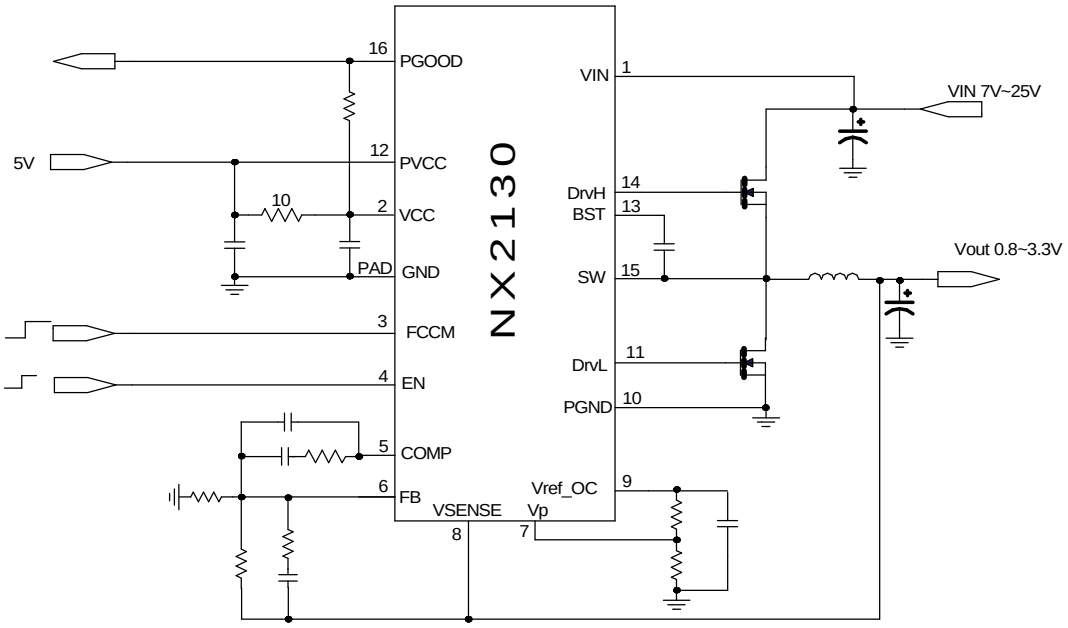
FEATURES

- Bus voltage operation from 7V to 25V
- Less than 1uA shutdown current with Enable low
- Excellent dynamic response with input voltage feed-forward and voltage mode control-PFM mode
- Selectable between Synchronous CCM and PWM/ PFM mode to improve efficiency at light load
- Fixed 300kHz switching frequency
- Internal Digital Soft Start Function
- Programmable current limit with latch off
- Over voltage protection with latch off
- FB UVLO with latch off
- Power Good indicator available
- Pb-free and RoHS compliant
- Output soft discharge
- Internal BST schottky diode

APPLICATIONS

- Notebook PCs and Desknotes
- Tablet PCs/Slates
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Hand-held portable instruments

TYPICAL APPLICATION



PATENT PENDING

Figure1 - Typical application of NX2130

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2130CMTR	-10° C to 100° C	MLPQ-16L	300kHz	Yes

ABSOLUTE MAXIMUM RATINGS

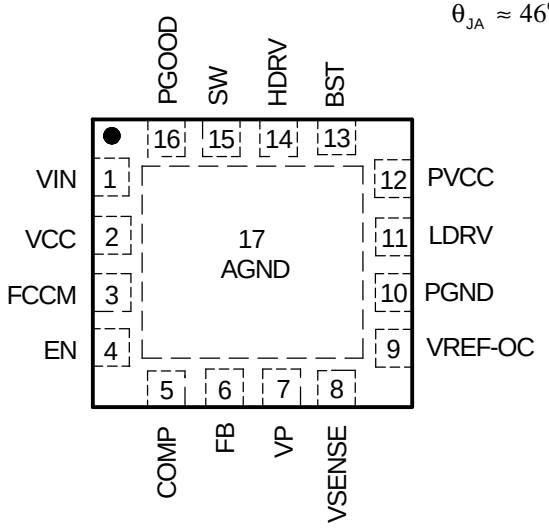
VCC,PVCC to GND & BST to SW voltage ..... -0.3V to 6.5V
VIN to GND ..... -0.3V to 25V
HDRV to SW Voltage ..... -0.3V to 6.5V
SW to GND ..... -2V to 30V
All other pins ..... VCC+0.3V
Storage Temperature Range .....-65°C to 150°C
Operating Junction Temperature Range .....-40°C to 125°C
ESD Susceptibility 2kV

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

16-LEAD PLASTIC MLPQ

$\theta_{JA} \approx 46^{o}C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =5V, VIN=15V and T_A = 0 to 70°C. Typical values refer to T_A = 25°C.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.75		5.25	V
Operating quiescent current	I_Q	EN=HIGH		2		mA
V_{CC} Shut down current	I_{SD}	EN=LOW			1	uA
Vcc UVLO						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4.4		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Supply Voltage(Vin)						
V_{in} Voltage Range	V_{in}		5.5		24	V
Input Voltage Current		Vin=24V		24		uA
V_{in} Shut Down Current		EN=LOW			1	uA
Vin UVLO						
V_{in}-Threshold	V_{in}_UVLO	V_{CC} Rising		4.5		V
V_{in}-Hysteresis	V_{in}_Hyst	V_{CC} Falling		0.2		V
Oscillator (Rt)						
Frequency	F_S			300		KHz
Ramp Offset				0.5		V
Ramp/Vin Gain				0.4		V/V
Max Duty Cycle				90		%
Min on time					150	nS
Error Amplifiers						
open loop gain				70		DB
Input Bias Current	Ib				100	nA
maximum soucring current		FB=GND		2		mA
maximum sinking current		FB=VCC		300		uA
offset voltage				0		mV
COMP High voltage		FB=0.4, Vp=0.8V, sink 40uA		3.5		V
COMP low voltage		source 80uA		0.1		V
Vref and Soft Start						
Internal Reference voltage				3		V
reference accuracy			-1		1	%
Soft Start time	Tss			1.6		mS
SW zero cross comparator						
offset voltage				5		mV
Enable						
Enable input high			1.4			V
Enalble input low					0.4	V
FCCM						
Logic input high			1.4			V
Logic input low					0.4	V
High Side						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		0.8		ohm
Rise Time	THdrv(Rise)	10% to 90%		50		ns
Fall Time	THdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		30		ns

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Low Side Driver						
Output Impedance, Sourcing	R_{source}(Ldrv)	I=200mA		1		ohm
Output Impedance, Sinking	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Rise Time	TLdrv(Rise)	10% to 90%		50		ns
Fall Time	TLdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		10		ns
Power Good(Pgood)						
Threshold Voltage as % of Vref		FB ramping up		90		%
Hysteresis				5		%
FB Under Voltage						
FB Threshold				70		%*Vp
Time Delay				3		cycle
Current Limit						
Ocset setting current		100k from VREF_OC to GND		30		uA
Over Voltage						
Over Voltage Trip Point				120		%Vref
Hysteresis				8		%Vref
Over Voltage Delay				2		cycle
Over temperature						
Threshold				150		°C
Hysteresis				20		°C

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VCC	This pin supplies the internal 5V bias circuit. A 1uF ceramic capacitor is placed as close as possible to this pin and ground pin.
BST	This pin supplies voltage to high side FET driver. A high freq minimum 0.1uF ceramic capacitor is placed as close as possible to and connected to this pin and SW pin.
PGND	Power ground.
FB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop.
SW	This pin is connected to source of high side FETs and provide return path for the high side driver. It is also used to hold the low side driver low until this pin is brought low by the action of high side turning off.
HDRV	High side gate driver output.
LDRV	Low side gate driver output.
EN	Pull up this pin to Vcc for normal operation. Pulling this pin down below 0.4V shuts down the controller and resets the soft start.
VIN	Bus voltage input provides power supply to oscillator and VIN UVLO signal.
PGOOD	An open drain output that requires a pull up resistor to Vcc or a voltage lower than Vcc. When FB pin reaches 90% of the reference voltage PGOOD transitions from LO to HI state.
FCCM	Forced CCM operation. Pull this pin high will force step down converter works at synchronous mode. Pull this pin low, the PWM controller with work at either synchronous PWM mode or Pulse frequency modulation (PFM) mode depending on the load condition.
VSENSE	Voltage sensing pin.
VREF_OC	Reference output voltage. A resistor from this pin to ground also set the current limit threshold.
VP	Output voltage indicator. This pin should set to be half of the desired output voltage.
PVCC	Provide the voltage supply to the lower MOSFET drivers.
AGND	Analog ground.

BLOCK DIAGRAM

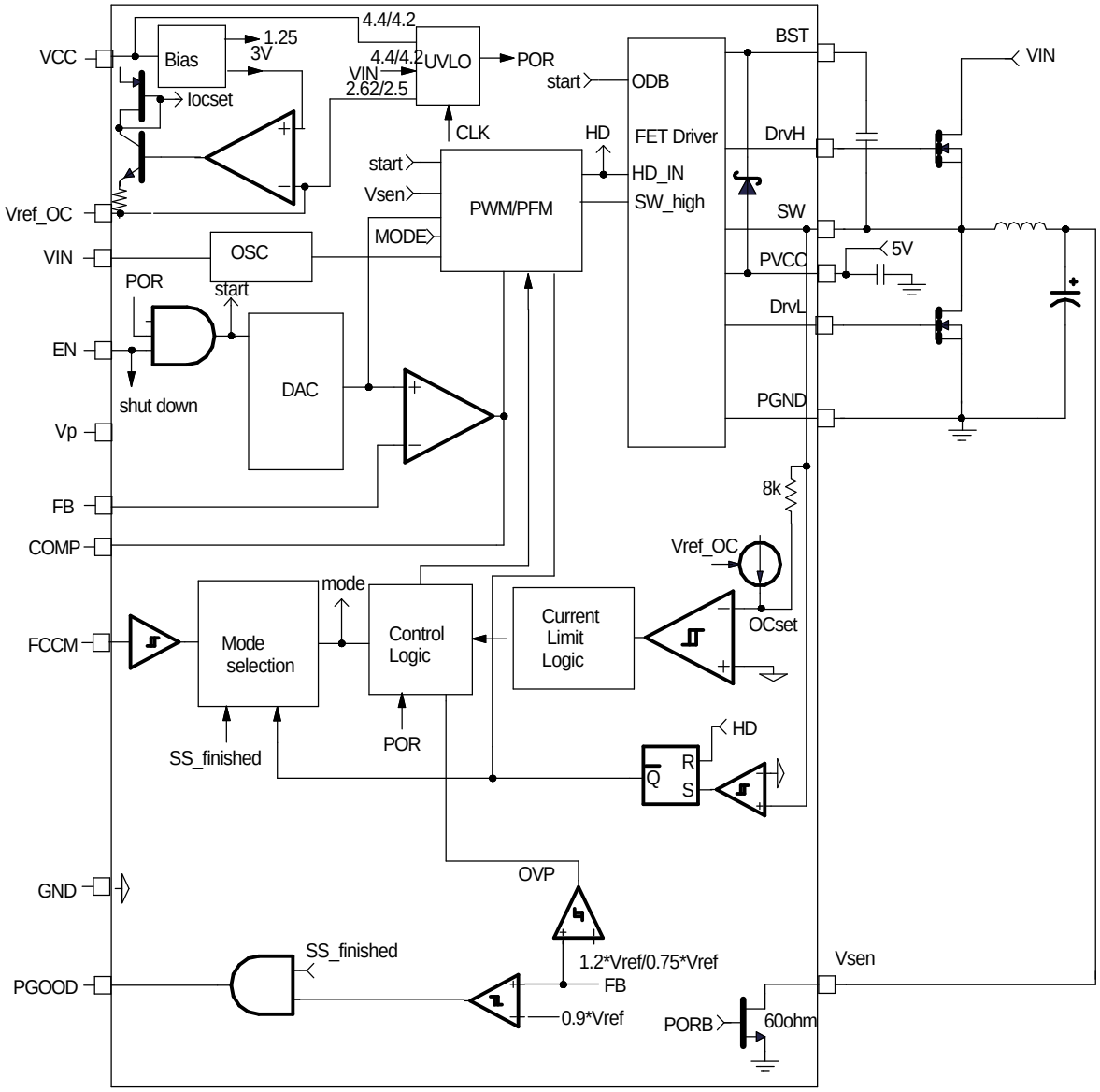


Figure 2 - Simplified block diagram of the NX2130

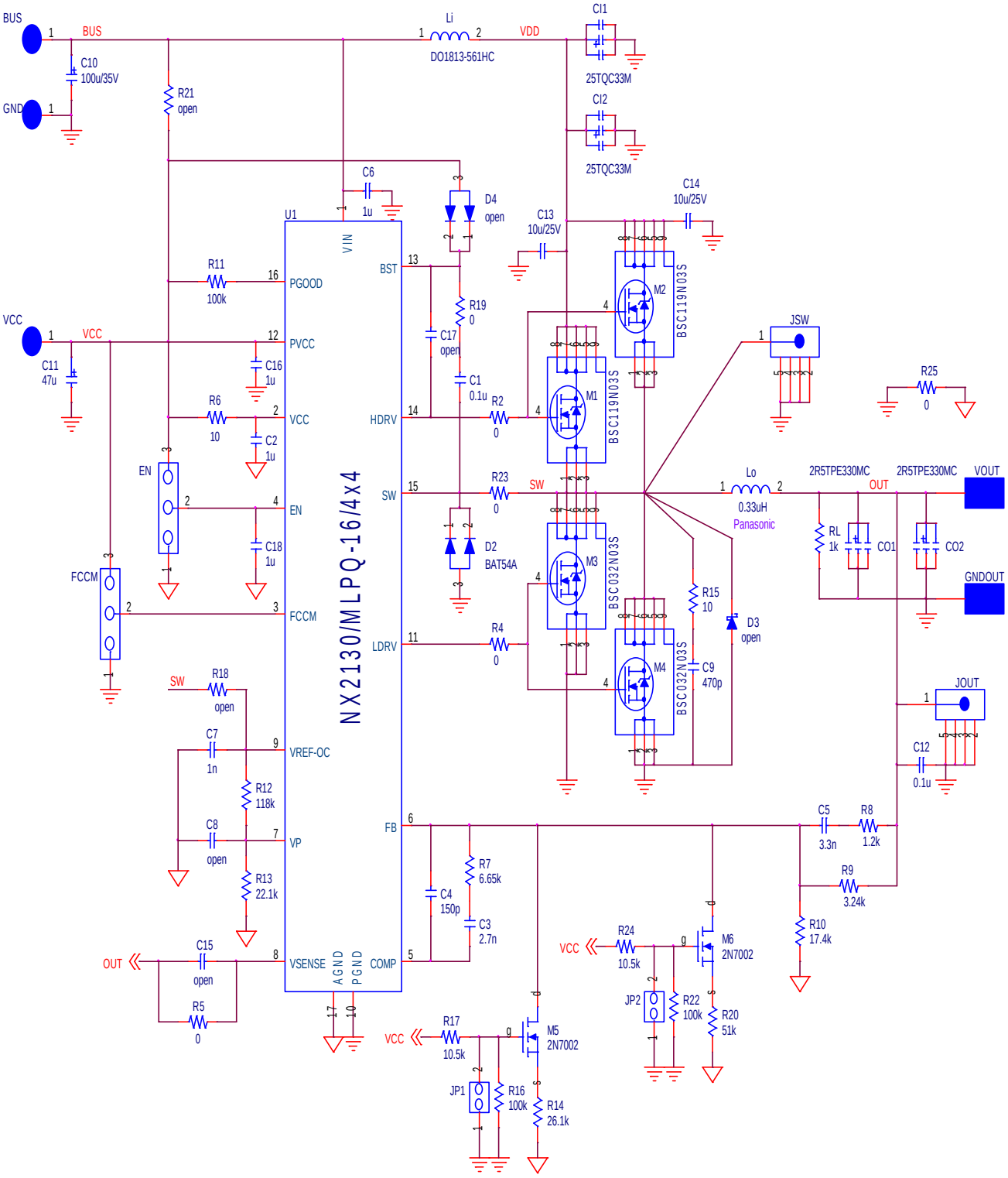


Figure 3- Demo board schematic based on ORCAD (VIN=7V to 20V,VOUT=1.1,IOUT=30A)

Bill of Materials

Item	Quantity	Reference	Value	Manufacture
1	2	CI1,CI2	25TQC33M	SANYO
2	2	CO1,CO2	2R5TPE330MC	SANYO
3	2	C1,C12	0.1u	
4	4	C2,C6,C16,C18	1u	
5	1	C3	2.7n	
6	1	C4	150p	
7	1	C5	3.3n	
8	1	C7	1n	
9	1	C9	470p	
10	1	C10	100u/35V	
11	1	C11	47u	
12	2	C13,C14	10u/25V	
13	1	Li	DO1813-561HC	COILCRAFT
14	1	Lo	0.33uH	PANASONIC
15	2	M1,M2	BSC119N03S	INFINEON
16	2	M3,M4	BSC032N03S	INFINEON
17	2	M5,M6	2N7002	
18	1	RL	1k	
19	6	R2,R4,R5,R19,R23,R25	0	
20	2	R6,R15	10	
21	1	R7	6.65k	
22	1	R8	1.2k	
23	1	R9	3.24k	
24	1	R10	17.4k	
25	3	R11,R16,R22	100k	
26	1	R12	118k	
27	1	R13	22.1k	
28	1	R14	26.1k	
29	2	R17,R24	10.5k	
30	1	R20	51k	
31	1	U1	NX2130/MLPQ-16	NEXSEM INC.

Demoboard waveforms

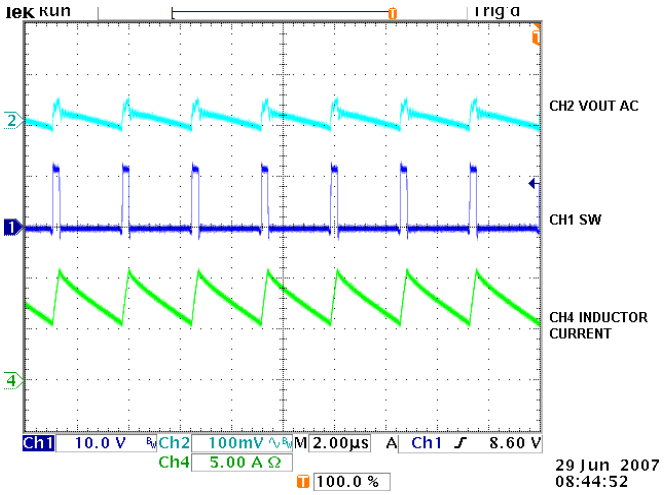


Figure 4 - PWM mode

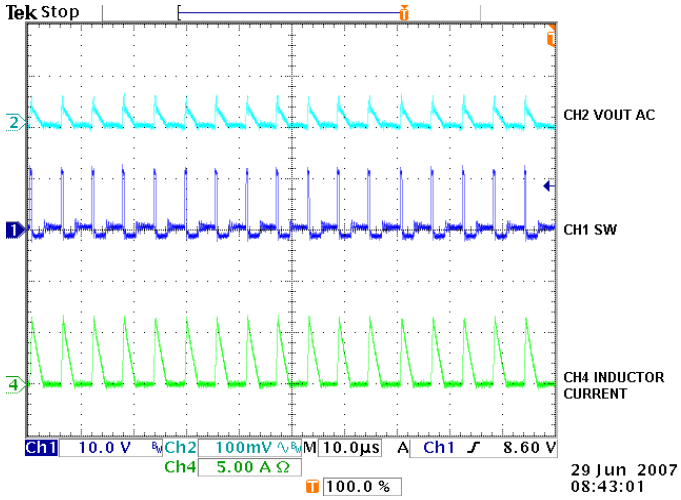


Figure 5 - PFM mode

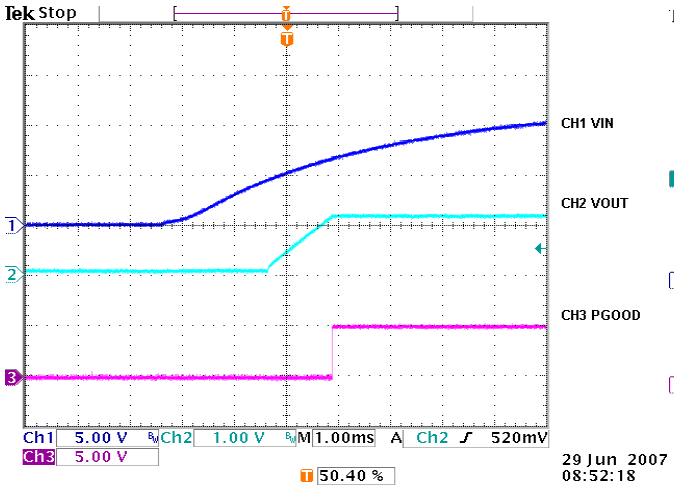


Figure 6 - Soft start

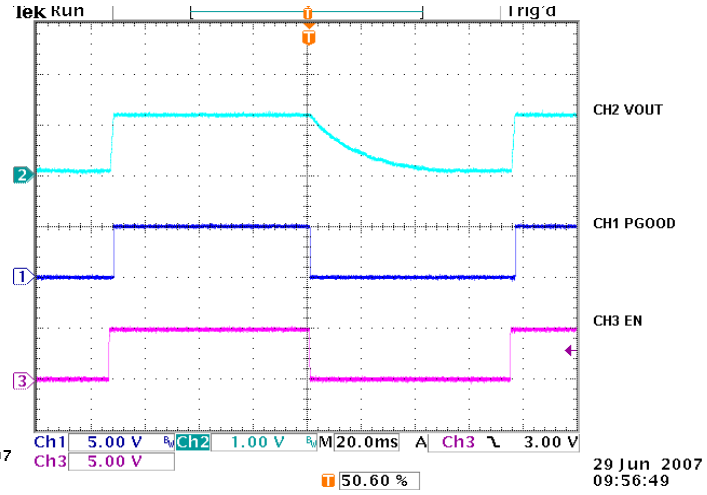


Figure 7 - Soft shutdown

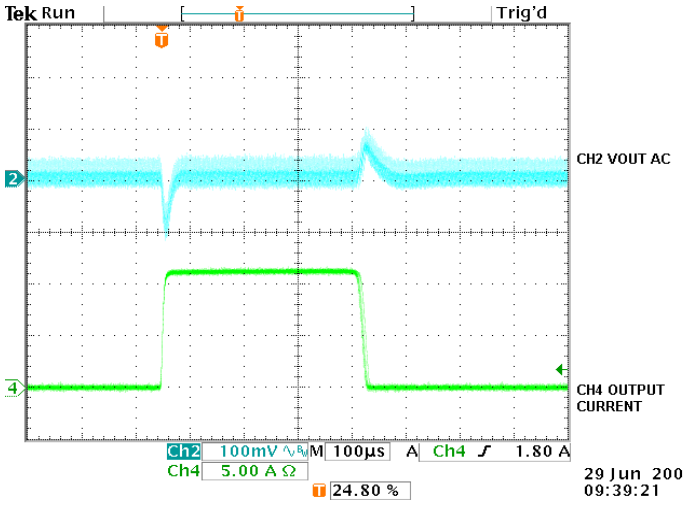


Figure 8 - Step response(PWM mode)

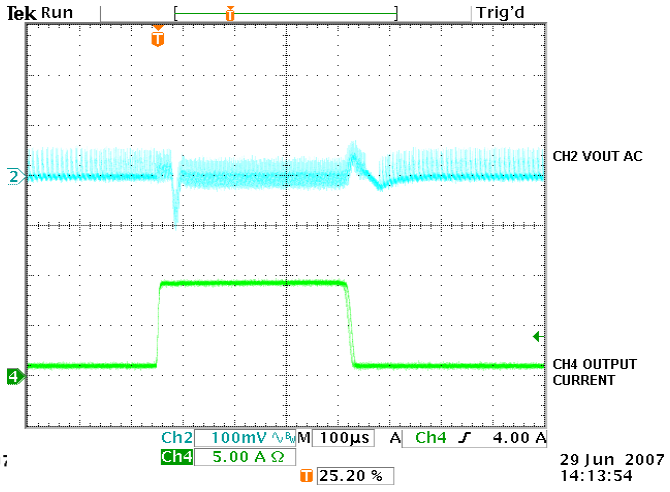


Figure 9 - Step response(PFM and PWM transition)

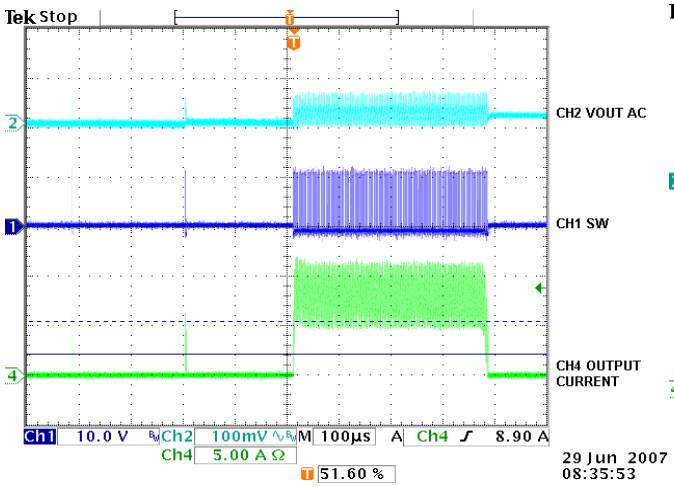


Figure 10 - Step Response(PFM only)

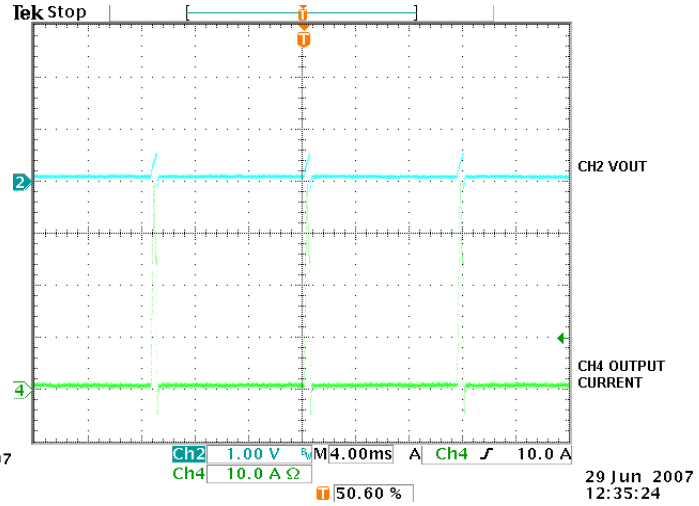


Figure 11 - Over Current Protection

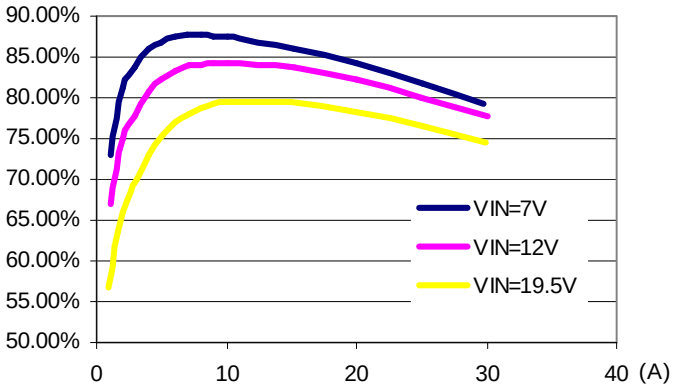


Figure 12 - Efficiency vs IOUT @ PWM mode (VOUT=1.1V)

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Switching frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

Power stage design requirements:
V_{IN}=12V
V_{OUT}=1.1V
I_{OUT} =30A
ΔV_{TRAN}<=50mV @ 5A step
F_S=300kHz

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \quad ...(1)$$
$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.25, then

$$L_{OUT}=\frac{12V-1.1V}{0.4\times 30A}\times\frac{1.1V}{12V}\times\frac{1}{300kHz}$$
$$L_{OUT}=0.28uH$$

Choose L_{OUT}=0.33uH.
Current Ripple is calculated as

$$I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$
$$=\frac{12V-1.1V}{0.33uH}\times\frac{1.1V}{12V}\times\frac{1}{300kHz}=10A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire}=\frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}}=\frac{20mV}{10A}=2m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 50mV output ripple, POSCAP 2R5TPE330MC with 12mΩ are chosen.

$$N=\frac{ESR_E\times\Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N=\frac{12m\Omega\times 10A}{50mV}$$

N =2.4

The number of capacitor has to be round up to a integer. Choose N =2.

If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as

$\Delta V_{droop} < \Delta V_{tran}$ @step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One section is dependent on the ESR of capacitor, the other section is

a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where t is the a function of capacitor,etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is mostly like to dependent on the ESR of capacitor.

Most case, the output capacitor is multiple capacitor in parallel. The number of capacitor can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 50mV for 5A load step.

If the POSCAP 2R5TPE330MC(330uF, 12mohm ESR) is used, the crticial inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{12m\Omega \times 330\mu F \times 1.1V}{5A} = 0.6\mu H$$

The selected inductor is 0.33uH which is smaller than critical inductance. In that case, the output voltage transient only dependent on the ESR.

number of capacitor is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E = \frac{0.33\mu H \times 5A}{1.1V} - 12m\Omega \times 330\mu F = -1.86us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 = \frac{12m\Omega \times 5A}{50mV} + \frac{1.1V}{2 \times 0.33\mu H \times 330\mu F \times 50mV} \times (0)^2 = 1.82$$

The number of capacitors has to satisfy both ripple and transient requirement. Overall, we choose N=2.

It should be considered that the proposed equa-

tion is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, forhigh frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

Voltage feedforward compensation is used in NX2130 to compensate the output voltage variation caused by input voltage changing. The feedforward funtion is realized by using VIN pin voltage to program the oscillator ramp voltage V_{OSC} at about 4/10 of V_{IN} voltage, which provides nearly constant power stage gain under wide voltage input range.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator.

The transfer function of type III compensator amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1}{sR_2\times(C_2+C_1)}\times\frac{(1+sR_4\times C_2)\times[1+s(R_2+R_3)\times C_3]}{(1+sR_4\times\frac{C_2\times C_1}{C_2+C_1})\times(1+sR_3\times C_3)}$$

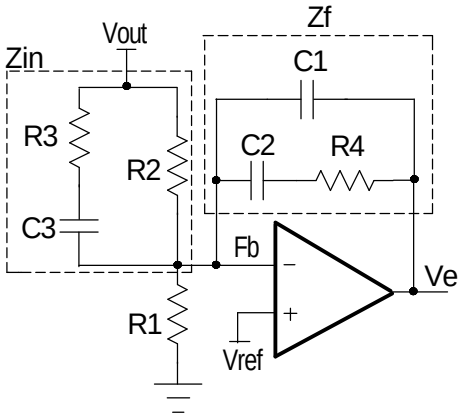


Figure 13 - Type III compensator

Case 1: $F_{LC}<F_O<F_{ESR}$(for most ceramic or low ESR POSCAP, OSCON)

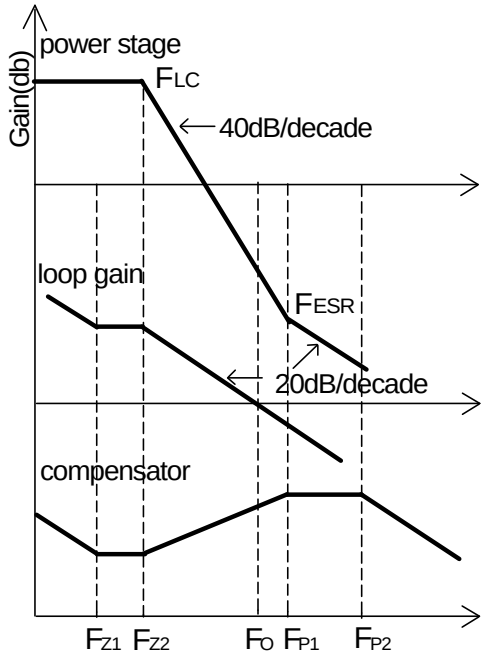


Figure 14 - Bode plot of Type III compensator ($F_{LC}<F_O<F_{ESR}$)

Typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_O<F_{ESR}$ and $F_O<=1/10~1/5F_s$ is shown as the following steps.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{0.33uH\times 660uF}}$$
$$=10.8kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 12m\Omega\times 660uF}$$
$$=40.2kHz$$

2. Set R_2 equal to 3.24kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{3.24k\Omega\times 0.8V}{1.1V-0.8V}=8.64k\Omega$$

Choose R_1=8.66kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$, calculate C_3.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)$$
$$=\frac{1}{2\times\pi\times 10k\Omega}\times\left(\frac{1}{10.8kHz}-\frac{1}{40.2kHz}\right)$$
$$=3.33nF$$

Choose C_3=3.3nF.

4. Calculate R_4 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=40kHz.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}$$
$$=\frac{4}{10}\times\frac{2\times\pi\times 40kHz\times 0.33uH}{3.3nF}\times 660uF$$
$$=6.63k\Omega$$

Choose R_4=6.65kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}$$
$$=\frac{1}{2\times\pi\times 0.75\times 10.8kHz\times 6.65k\Omega}$$
$$=2.9nF$$

Choose C_2=2.7nF.

6. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}$$
$$=\frac{1}{2\times\pi\times 6.65k\Omega\times 150kHz}$$
$$=160pF$$

Choose C_1=150pF.

7. Calculate R_3 by equation (13) with $F_{p1}=F_{ESR}$.

$$R_3 = \frac{1}{2\times\pi\times F_{P1}\times C_3}$$
$$= \frac{1}{2\times\pi\times 40.2kHz\times 3.3nF}$$
$$= 1.2k\Omega$$

Choose R_3 =1.2kΩ.

Case 2: $F_{LC}<F_{ESR}<F_O$(for electrolytic capacitors)

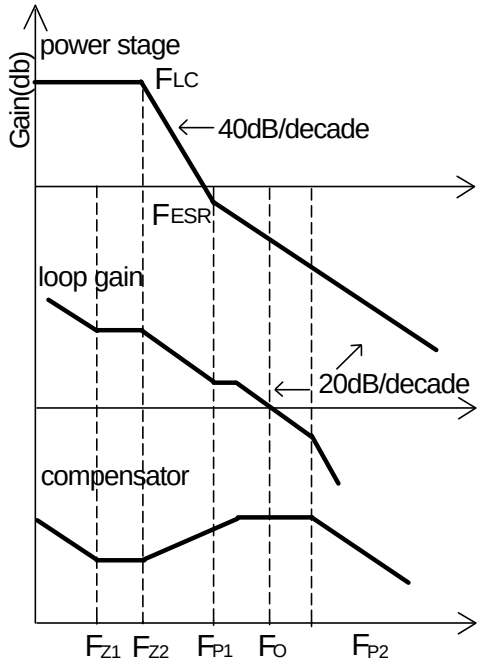


Figure 15 - Bode plot of Type III compensator ($F_{LC}<F_{ESR}<F_O$)

If electrolytic capacitors are used as output capacitors, typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_{ESR}<F_O$ and $F_O<=1/10\sim1/5F_s$ is shown as the following steps. Here two SANYO MV-WG1000 with 30 mΩ is chosen as output capacitor, output inductor is 2.2uH.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$= \frac{1}{2\times\pi\times\sqrt{2.2uH\times 2000uF}}$$
$$= 1.8kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$= \frac{1}{2\times\pi\times 15m\Omega\times 2000uF}$$
$$= 5.3kHz$$

2. Set R_2 equal to 15kΩ.

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}} = \frac{15k\Omega\times 0.8V}{1.8V-0.8V} = 12k\Omega$$

Choose R_1=12kΩ.

3. Set zero $F_{Z2} = F_{LC}$ and $F_{p1} = F_{ESR}$.

4. Calculate C_3.

$$C_3 = \frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)$$
$$= \frac{1}{2\times\pi\times 15k\Omega}\times\left(\frac{1}{1.8kHz}-\frac{1}{5.3kHz}\right)$$
$$= 2.4nF$$

Choose C_3=2.7nF.

5. Calculate R_3.

$$R_3 = \frac{1}{2\times\pi\times F_{P1}\times C_3}$$
$$= \frac{1}{2\times\pi\times 5.3kHz\times 2.7F}$$
$$= 11.1k\Omega$$

Choose R_3 =11kΩ.

6. Calculate R_4 with F_O=30kHz.

$$R_4 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times\frac{R_2\times R_3}{R_2+R_3}$$
$$= 0.1\times\frac{2\times\pi\times 30kHz\times 2.2uH}{15m\Omega}\times\frac{15k\Omega\times 11k\Omega}{15k\Omega+11k\Omega}$$
$$= 16k\Omega$$

Choose R_4=16kΩ.

7. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2 = \frac{1}{2\times\pi\times F_{Z1}\times R_4}$$
$$= \frac{1}{2\times\pi\times 0.75\times 1.8kHz\times 16k\Omega}$$
$$= 4.2nF$$

Choose C_2=4.7nF.

8. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1 = \frac{1}{2\times\pi\times R_4\times F_{P2}}$$
$$= \frac{1}{2\times\pi\times 16k\Omega\times 150kHz}$$
$$= 66pF$$

Choose C_1=68pF.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10~1/5F_s$.

Case 1:

Type II compensator can be realized by simple RC circuit as shown in figure 17. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=\frac{R_3}{R_2} \quad \text{... (15)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

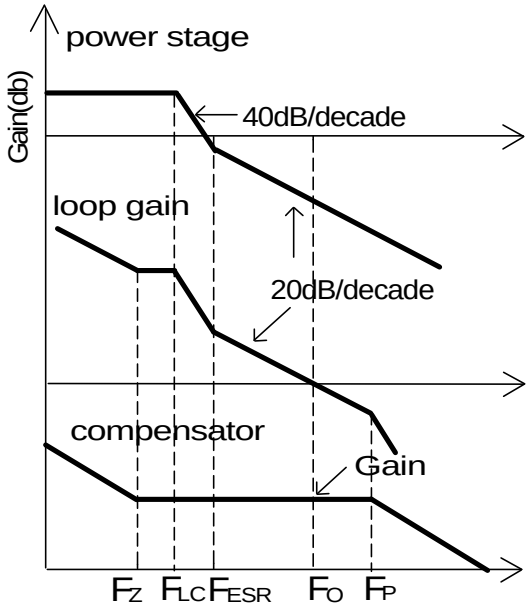


Figure 16 - Bode plot of Type II compensator

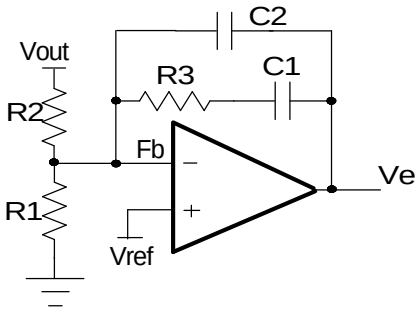


Figure 17 - Type II compensator

The following parameters are used as an example for type II compensator design, three 1500uF with 19mohm Sanyo electrolytic CAP 6MV1500WGL are used as output capacitors. Coilcraft DO5010P-152HC 1.5uH is used as output inductor. The power stage information is that:V_{IN}=12V, V_{OUT}=1.2V, I_{OUT} =12A, F_S=300kHz.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$= \frac{1}{2\times\pi\times\sqrt{1.5uH\times 4500uF}}$$
$$= 1.94kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$= \frac{1}{2\times\pi\times 6.33m\Omega\times 4500uF}$$
$$= 5.6kHz$$

2.Set crossover frequency F_O=30kHz>>F_{ESR}.

3. Set R_2 equal to10kΩ. Based on output voltage, using equation 21, the final selection of R_1 is 20kΩ.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times R_2$$
$$= \frac{1}{10}\times\frac{2\times\pi\times 30kHz\times 1.5uH}{6.33m\Omega}\times 10k\Omega$$
$$= 40.6k\Omega$$

Choose R_3 =40.2kΩ.

5. Calculate C_1 by setting compensator zero F_z at 75% of the LC double pole.

$$C_1 = \frac{1}{2\times\pi\times R_3\times F_z}$$
$$= \frac{1}{2\times\pi\times 37.4k\Omega\times 0.75\times 1.94kHz}$$
$$= 2.7nF$$

Choose C_1=2.7nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi\times R_3\times F_s}$$
$$= \frac{1}{\pi\times 37.4k\Omega\times 300kHz}$$
$$= 27pF$$

Choose C_2=27pF.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation applies to figure 18, which shows the relationship between V_{OUT} , V_{REF} and voltage divider.

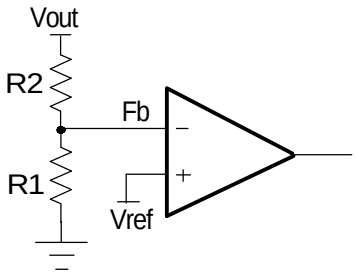


Figure 18 - Voltage divider

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT}\times\sqrt{D}\times\sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{INMIN}} \quad ...(19)$$

V_{INMIN} = 8V, V_{OUT}=1.05V, I_{OUT}=10A, the result of input RMS current is 3.4A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo OSCON CAP 25SVP56M

25V 56uF 28mΩ with 3.8A RMS rating are chosen as input bulk capacitors.

Power MOSFETs Selection

The NX2130 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. For example, two IRF7822 are used. They have the following parameters: V_{DS}=30V, I_D=18A,R_{DSON} =5mΩ,Q_{GATE} =44nC.

There are two factors causing the MOSFET power loss:conduction loss, switching loss.

Conduction loss is simply defined as:

$$P_{HCON}=I_{OUT}^2\times D\times R_{DS(ON)}\times K$$
$$P_{LCON}=I_{OUT}^2\times(1-D)\times R_{DS(ON)}\times K \quad ...(22)$$
$$P_{TOTAL}=P_{HCON}+P_{LCON}$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K approximately equals to 1.4 at 125°C according to datasheet. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW}=\frac{1}{2}\times V_{IN}\times I_{OUT}\times T_{SW}\times F_S \quad ...(23)$$

where I_{OUT} is output current, T_{SW} is the sum of T_R and T_F which can be found in mosfet datasheet, and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Also MOSFET gate driver loss should be considered when choosing the proper power MOSFET. MOSFET gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits.It is proportional to frequency and is defined as:

$$P_{gate}=(Q_{HGATE}\times V_{HGS}+Q_{LGATE}\times V_{LGS})\times F_S \quad ...(24)$$

where Q_{HGATE} is the high side MOSFETs gate charge,Q_{LGATE} is the low side MOSFETs gate charge,V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

This power dissipation should not exceed maximum power dissipation of the driver device.

Over Current Limit Protection

Over current Limit for step down converter is achieved by sensing current through the low side MOSFET. Inside NX2130, current limit I_{OCP} is set by the resistance Rocset from pin Vref_OC to ground and Vref_OC voltage. The current generated by 3V/Rocset is mirrored to a current source, which injects to SW node through a internal 8kohm resistor. This current I_{OCP} will determine the current limit threshold.

This current is very accurate and does not change with silicon process and temperature, the over current limit tripping point can be set more accurate than traditional current source. When synchronous FET is on, the voltage at node SW is given as

$$V_{SW}=I_{OCP}\times 8k\Omega - I_L\times R_{DSON}$$

When the voltage is below zero, the over current occurs. The over current limit can be set by the following equation

$$I_{SET}=3V/R_{ocset}\times 8k\Omega/R_{DSON}$$

For example, For 20A current limit and 9mohm Rdson for IRFR3706, the OCP set resistor is calculated as

$$Rocset=\frac{3V}{I_{SET}\times R_{DSON}\times 1.4}\times 8k\Omega$$
$$=\frac{3V}{20A\times 9mohm\times 1.4}\times 8k\Omega$$
$$=95kohm$$

Select Vref_OC pin to ground resistance Rocset=102kohm.

Vp voltage setup

The input of Vp voltage should be set at Vout/2 and can be derived by resistor divider from Vref_OC to ground. For example when Vout is 5V, the bottom resistor of divider is

$$R_{OC\_BOT} = \frac{Vout/2}{V_{REF\_OC}} \times R_{OCSET}$$
$$= \frac{5V/2}{3V} \times 102kohm$$
$$= 85kohm$$

Choose R_{OC_BOT} =86.6kohm.

$$R_{OC\_TOP} = \frac{V_{REF\_OC} - Vout/2}{Vout/2} \times R_{OC\_BOT}$$
$$= \frac{3V - 5V/2}{5V/2} \times 86.6kohm$$
$$= 17.3kohm$$

Choose R_{OC_TOP} =17.4kohm.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

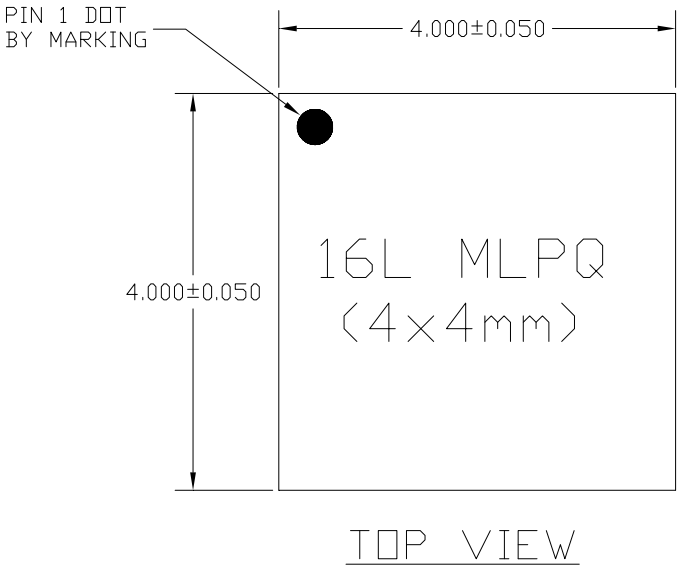
8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

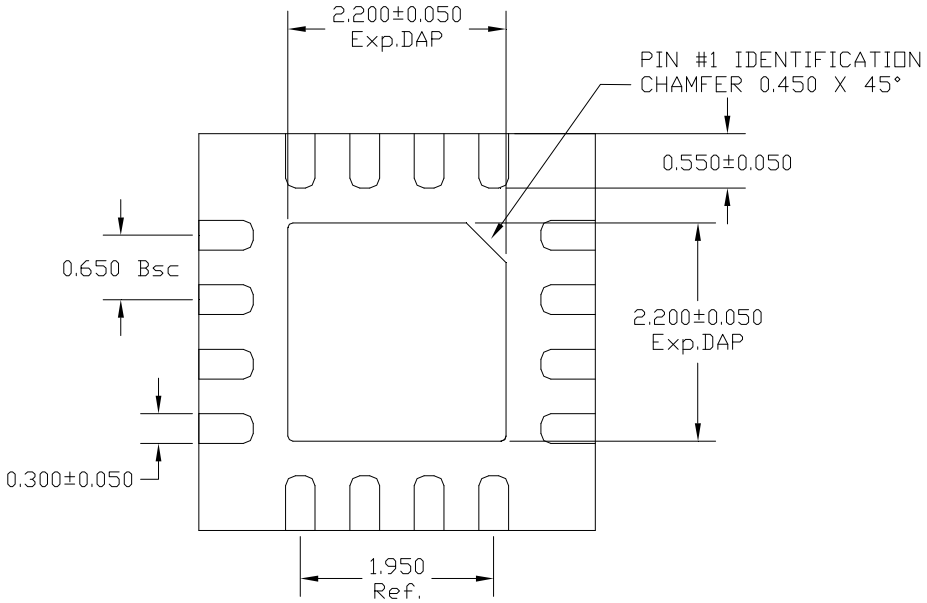
10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

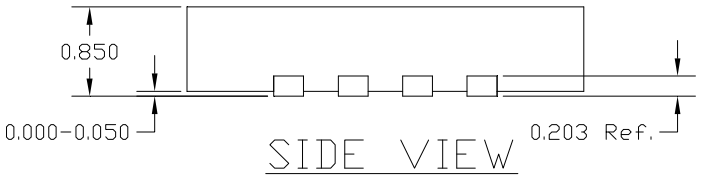
4x4 16 PIN MLPQ OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE: ALL DIMENSIONS ARE DISPLAYED IN MILLIMETERS.