NEXSEM

NX2201

HIGH FREQUENCY SYNCHRONOUS PWM & LDO CONTROLLER

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2201 controller is a combination synchronous Buck controller and LDO controller IC designed for step down DC to DC converter applications. This device can generate two low cost supply from a single 5V input voltage or a 12V bus voltage with a separate 5V for IC biasing. The NX2201offers an Enable pin that can be used to program the converter's start voltage using an external divider from bus voltage. The LDO controller has an internal 16V drive capability which allows an easy control of the gate voltage for the linear regulator's external Nch MOSFET. The NX2201 can operate up to 1MHz switching frequency, making it ideal for applications requiring ceramic output capacitor. Other features of the part are; Power Good function, less than 50 nS of dead band which increases efficiency at higher frequencies, Internal digital soft start; Vcc undervoltage lock out; Output undervoltage protection with digital filter and shutdown capability via the enable pin.

FEATURES

- <1ohm Driver keeps High Capacitance Synchronous MOSFET off during SW node transition
- LDO Controller allows a Low Cost Linear Supply
- Bus voltage operation from 4V to 25V
- Power Good indicator
- Adjustable frequency up to 1MHz
- Internal Digital Soft Start Function
- Less than 50 nS adaptive deadband
- Enable pin allows BUS voltage UVLO programmability
- Short protection with feedback UVLO
- Pb-free and RoHS compliant

APPLICATIONS

- FPGA High Freqency Supply
- ADSL Modem Power
- On board DC to DC such as 12V to 3.3V, 2.5V or 1.8V
- Memory Vddq Supply

TYPICAL APPLICATION

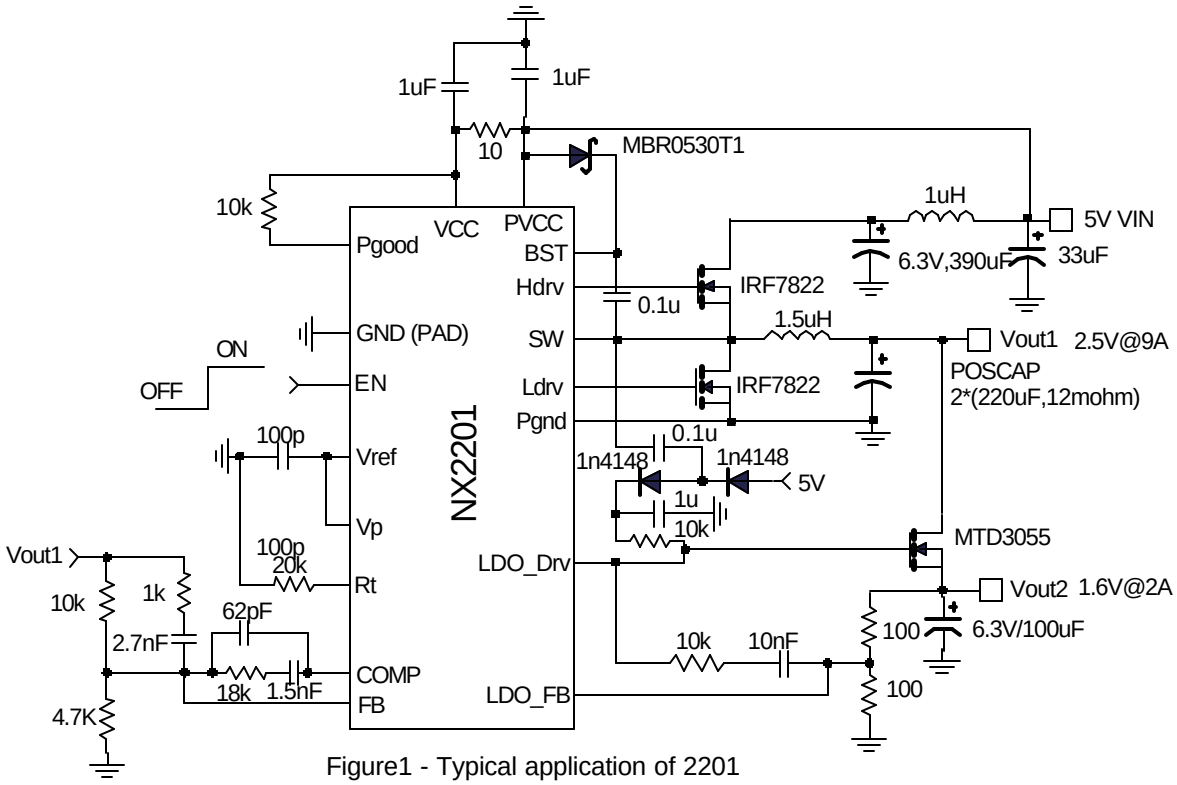


Figure1 - Typical application of 2201

ORDERING INFORMATION

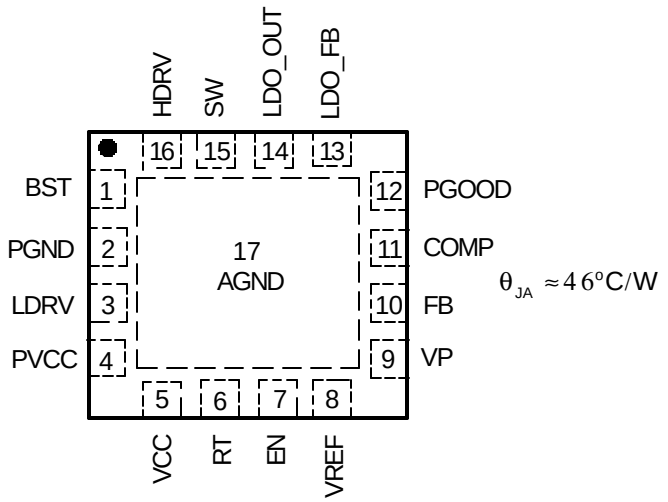
Device	Temperature	Package	Pb-Free
NX2201CMTR	0 to 70°C	MLPQ-16L	Yes

ABSOLUTE MAXIMUM RATINGS(NOTE1)

Vcc to GND & BST to SW voltage 6.5V
BST to GND Voltage 35V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

PACKAGE INFORMATION

16-LEAD PLASTIC MLPQ



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, and T_A= 0 to 70°C. Typical values refer to Ta = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Feedback Voltage						
FB Voltage	V_{REF}	4.5 < Vcc < 5.5		0.800		V
FB Voltage Line Regulation				0.2		%
Vcc supply voltage						
UVLO Threshold - Vcc	V_{CC}	Supply Ramping Up		4.1		V
UVLO Hysteresis - Vcc	V_{CC_Hyst}			0.22		V
UVLO Threshold - BST	V_{BST}	Supply Ramping Up		2.4		V
UVLO Threshold - FB		FB Ramping Down		0.4		V
Supply Current						
Vcc Dynamic Supply Current	I_{CC_DYN}	Freq =300KHz, Cl = 3300pF		5		mA
BST Dynamic Supply Current	I_{BST_DYN}	Freq = 300KHz, Cl = 3300pF		5		mA
Vcc Static Supply Current	I_{CC_STA}			3		mA
BST Static Supply Current	I_{BST_STA}			0.1		mA
Soft Start Section						
Soft start time	T_{ss}	Fsw=300Khz, 2211 Fsw=1Mhz, 2210		3.4 1.02		mS mS
Error Amp						
Transconductance	g_m			2500		umho

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Oscillator						
Frequency	F_S	NX2211		600		KHz
		NX2210		1000		KHz
Ramp Amplitude	V_{RAMP}			2		Vpp
Output Drivers						
HDRV source impedance		I=200mA		0.9		ohm
HDRV sink impedance		I=200mA		0.65		ohm
LDRV source impedance		I=200mA		0.9		ohm
LDRV sink impedance		I=200mA		0.5		ohm
Rise Time	T_{RISE}	Cload = 1500pF		50		nS
Fall Time	T_{FALL}	Cload = 1500pF		50		nS
Dead Band Time	T_{dead}	LDRV Low to HDRV High		30		nS
Max Duty Cycle	D_{max}	FB = 0.6V		95		%
Min Duty Cycle	D_{min}	FB = 1V			0	%
EN						
Enable Threshold Voltage		Enable ramp up		1.6		V
Enable Hysterises				0.1		V
Power Good						
Threshold				$0.9V_{REF}$		V
Hysteresis				$0.05V_{REF}$		V
PGood Voltage Low				0.2		V
LDO Controller						
LDO FB voltage		LDO OUT=LDO FB		0.8		V
LDO FB Bias Current			-0.2	0	0.2	uA
LDO OUT drive Vsat voltage		I=10mA		0.4		V

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
16	HDRV	High side MOSFET gate driver.
2	PGnd	Power ground pin. This pin must be connected directly using a via to ground plane.
3	LDRV	Low side MOSFET gate driver.
5	Vcc	Voltage supply for the internal circuit. A 1uF high frequency ceramic capacitor must be connected from this pin to ground plane using a via. A resistor of 10ohm can be placed from this pin to PVcc pin to form a low pass filter for further noise reduction.
6	Rt	Add resistor to this pin for adjustable frequency which is from 2kHz to 1MHz
7	EN	Pull up this pin to Vcc for normal operation. Pulling this pin down below 1.25V shuts down the controller and resets the soft start. This pin can also be used as a UVLO detector for the bus voltage via a resistor divider.
10	FB	FB pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below 0.4V, both HDRV and LDRV outputs are latched off.
11	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin.
15	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.
12	PGood	This is an open drain output and it is pulled low if the FB voltage is below 90% of the Vref. If not used it may be left floating.
13	LDO_FB	LDO controller feedback input.
14	LDO OUT	LDO controller output. This pin is an open drain output controlling the gate of an external NCH MOSFET thru a pull up resistor to a voltage higher than the drain by at least 5V. The maximum rating of this pin is 16V.
8	Vref	Output of the internal reference voltage. A capacitor of 100pF to 1000pF may be placed from this pin to Gnd to reduce high frequency noise.
9	Vp	This pin is the error amplifier noninverting input. It should be connected to the Vref pin.
4	Pvcc	Voltage supply for the low side MOSFET gate driver. A 1uF high frequency ceramic capacitor must be connected from this pin to ground plane using a via.
PAD	AGnd	Analog ground pin. This pin must be connected directly using via to ground plane.