NEXSEM

NX3101

HIGH SPEED 5V SYNCHRONOUS MOSFET DRIVER

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX3101 is a high frequency MOSFET driver designed to drive two N-Channel MOSFETs in a synchronous rectified Step Down(BUCK) regulator topology. This driver combined with other NEXSEM controllers such as NX2511 or NX2517 2 to 4 phase controller ICs makes a high efficiency high performance Multiphase regulator designed for latest Microprocessor Vcore power as well as other high current regulator applications. The IC is powered by a single 5V supply and its ultra low resistance drivers minimizes switching losses for high frequency applications using high gate capacitance MOSFETs. The NX3101 features 0.44 ohm sink resistance for the lower gate driver capable of holding the lower MOSFET gate off during SW node fast dv/dt rise time, preventing shoot through power loss.

FEATURES

- Bus voltage operation from 3V to 25V
- High Peak Current Drive Capability (Lower Driver Sink Resistance 0.44 ohm)
- High Frequency Operating Range(up to 2MHz)
- Minimal Propagation Delay
- Adaptive Non-overlap Control
- Output disable(ODB) signal turns both outputs off
- Pb-free and RoHS compliant

APPLICATIONS

- Desktop and Notebook Microprocessor Vcore regulator applications
- High Current Multiphase Converter
- High Efficiency / High Current Graphic Vcore

TYPICAL APPLICATION

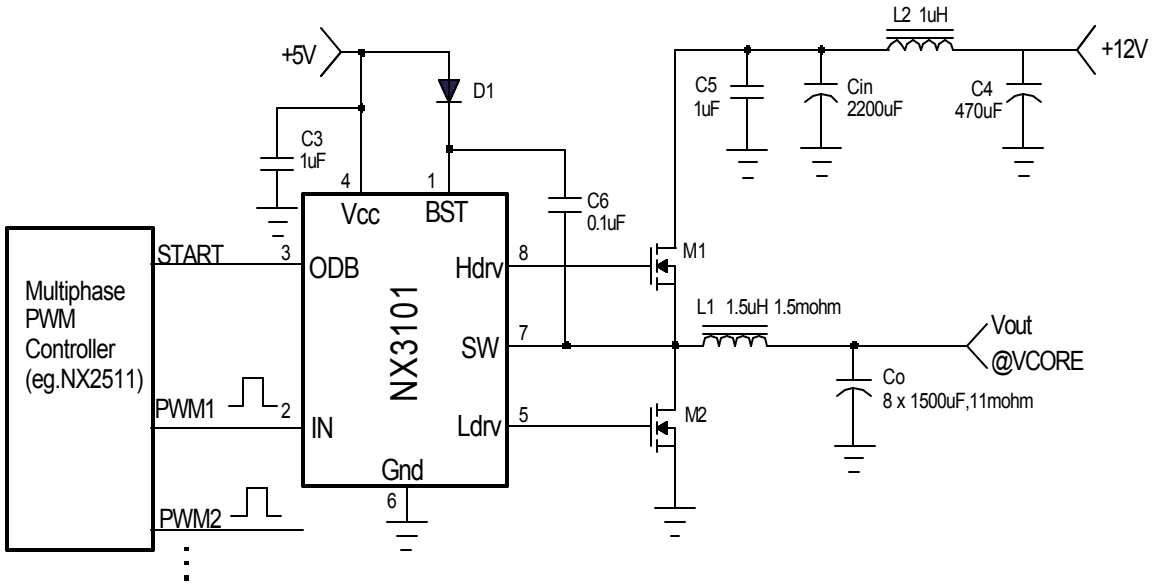


Figure1 - Typical application of 3101

ORDERING INFORMATION

Device	Temperature	Package	Pb-Free
NX3101CSTR	0 to 70°C	SOIC-8L	Yes

ABSOLUTE MAXIMUM RATINGS

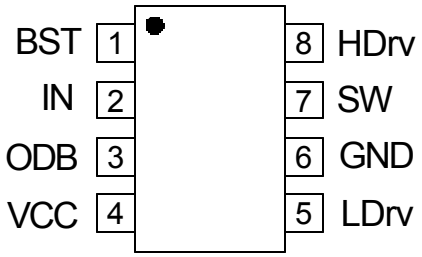
Vcc to GND & BST to SW Voltage 6.5V
BST to GND Voltage 35V
SW to GND Voltage 35V
ODB & IN to GND Voltage 6.5V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

Caution: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

8-PIN PLASTIC SOIC (S)

$\theta_{JA} \approx 130°C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over VCC =BST= 5V, SW=GND=0V, ODB=VCC, and T_A = 0 to 125°C. Typical values refer to T_A = 25°C.

PARAMETERS	SYM	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Vcc Supply						
Vcc Quiescent Current Operating Mode	Iq	VBST=12V, IN=0V		0.5	2	mA
		VBST=12V, IN=5V		0.5	2	
		IN=Swch at 500Khz, 50% DC, CL=0		TBD		
		IN=Swch at 500Khz, 50% DC, CL=3nF		TBD		
Vcc Quiescent Current Shutdown Mode	Iqsd	ODB=0V		0.5	2	uA
ODB						
ODB Threshold (High)	ODB(H)		2.4			V
ODB Threshold (Low)	ODB(L)				0.8	V
ODB Current	Ienb		-2		2	uA
Propagation delay time	Tprop			15		ns
IN						
Input voltage High	IN (H)		2.4			V
Input Voltage low	IN(L)				0.8	V
Input Current	$I_{bias-ODB}$		-2		2	uA

PARAMETERS	SYM	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High Side driver(CL=3300pF) Output Impedance, Sourcing Current	R_{source}(Hdrv)			0.85		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)			0.65		ohm
Rise Time	THDrv(Rise)	10% to 90%		25		ns
Fall Time	THDrv(Fall)	90% to 10%		20		ns
Deadband Time	Tdead(L to H)	LDRV going Low to HDRV going High, 10% to 10%		30		ns
Propagation Delay	Tdelay(H)	IN going HI to LDRV going Low		10		ns
Low Side Driver(CL=3300pF) Output Impedance, Sourcing Current	R_{source}(Ldrv)			0.85		ohm
Output Impedance , Sinking Current	R_{source}(Ldrv)			0.5		ohm
Rise Time	TLDrv(Rise)	10% to 90%		25		ns
Fall Time	TLDrv(Fall)	90% to 10%		20		ns
Deadband Time	Tdead(H to L)	SW going Low to LDRV going High, 10% to 10%		20		ns
Propagation Delay	Tdelay(L)	IN going Low to LDRV going High		10		ns

PIN DESCRIPTIONS

Pin#	Pin Symbol	Pin Description
1	BST	Bootstrap Pin. A capacitor is connected between BST and SW pins to generate the floating bootstrap voltage for High-side Driver. The capacitor value is typically between 0.1uf to 1uF.
2	IN	PWM input signal to the MOSFET drivers.
3	ODB	Output disable pin. When high the internal circuitry is enabled. When low both high side and low side drivers are turned off.
4	VCC	Biasing supply both for the IC and low side driver, a minimum of 1uF ceramic cap should be connected between this pin and PGND.
5	LDRV	Output driver for low side MOSFET.
6	GND	Power ground.
7	SW	Switching point, this pin connects to the junction of external high-side and low-side MOSFETs.
8	HDRV	Output drive for high-side MOSFET.

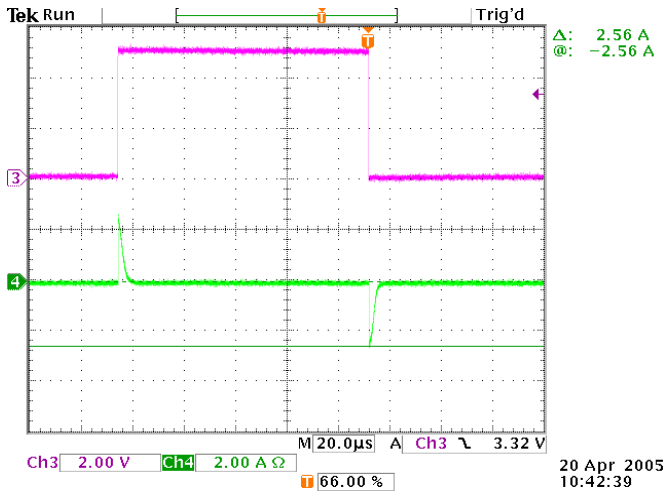


Figure 2 - Hdrv peak current

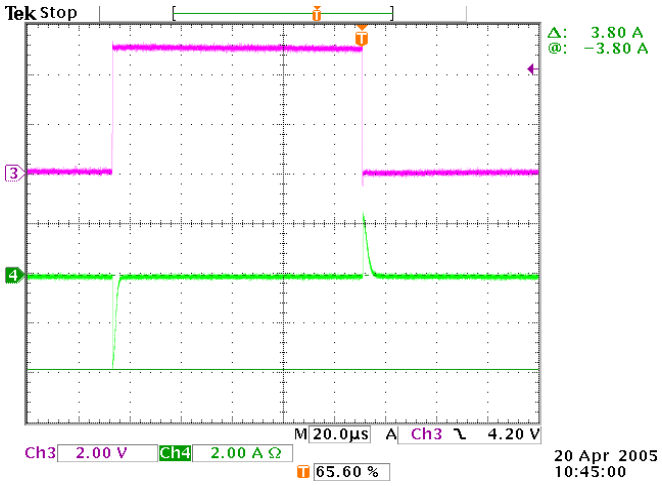


Figure 3 - Ldrv peak current