NEXSEM

NX9811A

13A SYNCHRONOUS BUCK SWITCHING REGULATOR WITH 600kHz OPERATION FREQUENCY

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX9811A is synchronous buck switching converter in multi chip module designed for step down DC to DC converter applications. They are optimized to convert bus voltages from 2V to 25V to as low as 0.8V output voltage. The output current can be up to 13A. The NX9811A offers an enable pin that can be used to program the converter's start up. NX9811A operates at fixed internal frequency of 600kHz and employ loss-less current limiting protection by sensing the Rdson of synchronous MOSFET followed by latch out feature. Feedback under voltage protection triggers hiccup.
Other features are: Internal digital soft start; Vcc undervoltage lock out and shutdown capability via the enable pin or comp pin. NX9811A is available in 8x8 MCM package.

FEATURES

- Switching Controller and MOSFETs in one package
- Bus voltage operation from 2V to 25V
- Fixed 600kHz
- Internal Digital Soft Start Function
- Output current up to 13A
- Enable pin to program BUS UVLO
- Programmable current limit triggers latch out by sensing Rdson of Synchronous MOSFET
- No negative spike at Vout during startup and shutdown
- Pb-free and RoHS compliant

APPLICATIONS

- Graphic Card on board converters
- On board DC to DC such as 12V to 5V, 3.3V or 1.2V
- Point of load applications
- Area constrained DC to DC step down applications

TYPICAL APPLICATION

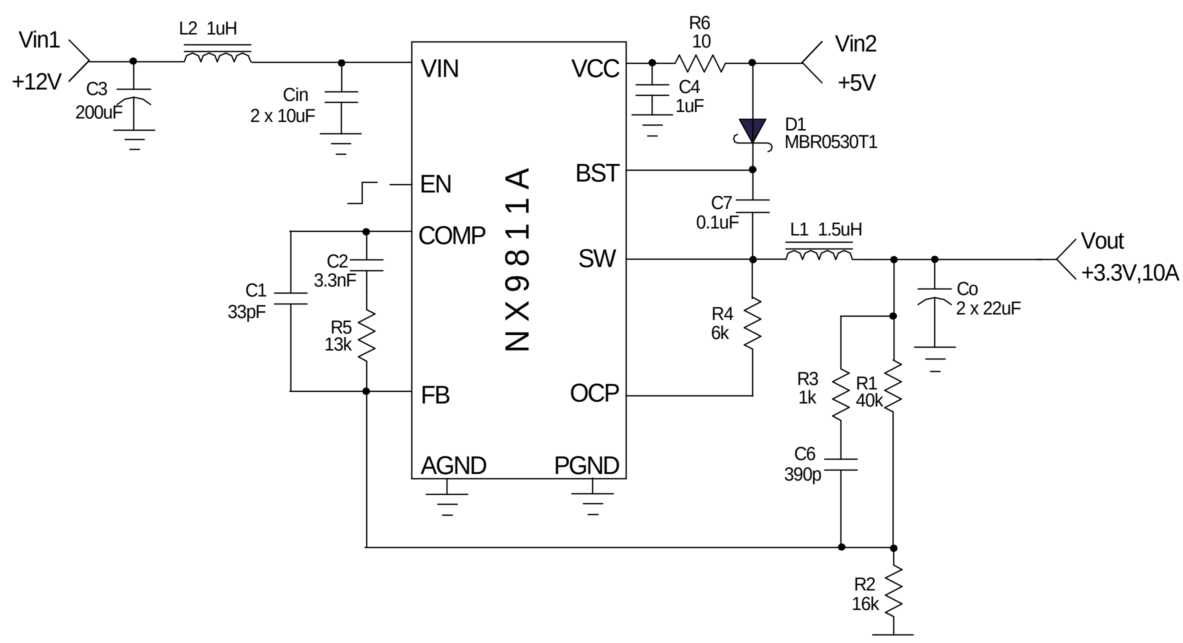


Figure 1 - Typical application of 9811A

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX9811ACMTR	0 to 70°C	8X8 MCM-56L	600kHz	Yes

ABSOLUTE MAXIMUM RATINGS

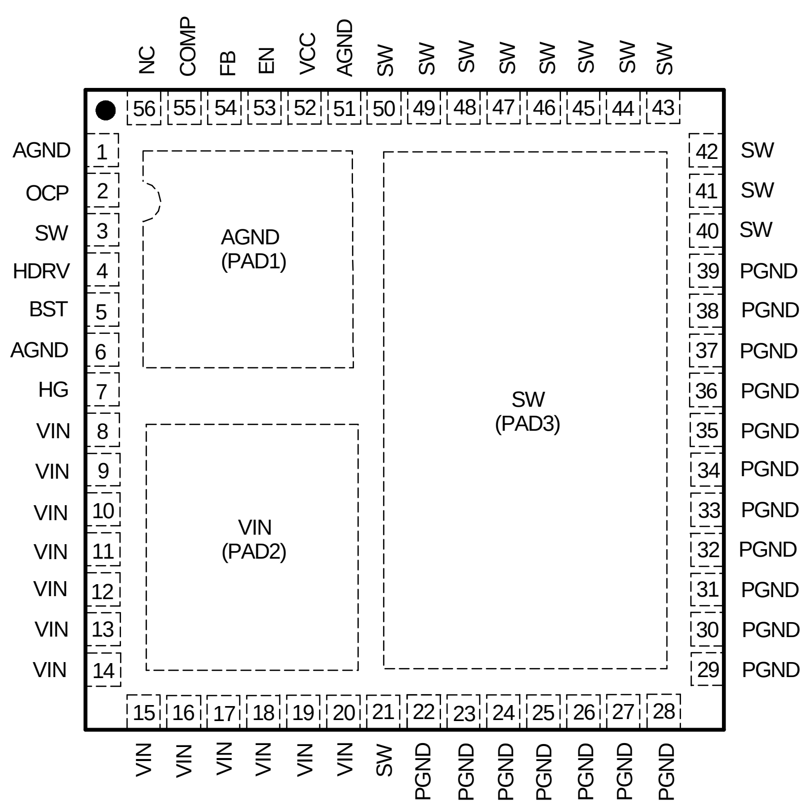
VCC to GND & BST to SW voltage .... -0.3V to 6.5V
VIN to GND 25V
BST to GND Voltage .... -0.3V to 35V
SW to GND .... -2V to 35V
All other pins .... -0.3V to VCC+0.3V or 6.5V
Storage Temperature Range .... -65°C to 150°C
Operating Junction Temperature Range .... -40°C to 125°C
ESD Susceptibility 2kV
Power Dissipation .... TBD(Note1)

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note1: Under room temperature, this module can dissipate up to 5.5W on a four layer PCB board with 1ounce copper.

PACKAGE INFORMATION

56-LEAD PLASTIC MCM 8 x 8



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, V_{IN} = 12V and T_A= 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}			0.8		V
Ref Voltage line regulation				0.2		%
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.5	5	5.5	V
V_{CC} Supply Current (Static)	I_{CC} (Static)	Outputs not switching		3		mA
V_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)			TBD		mA
Supply Voltage(V_{BST})						
V_{BST} Supply Current (Static)	I_{BST} (Static)	Outputs not switching		TBD		mA
V_{BST} Supply Current (Dynamic)	I_{BST} (Dynamic)			TBD		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising	3.8	4	4.2	V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.2		V
Oscillator						
Frequency	F_S			600		kHz
Ramp-Amplitude Voltage	V_{RAMP}			1.5		V
Max Duty Cycle				95		%
Min Duty Cycle					0	%
Error Amplifiers						
Transconductance				2000		umho
Input Bias Current	Ib			10		nA
EN & SS						
Soft Start time	Tss			3.4		mS
Enable HI Threshold				1.25		V
Enable Hysterises				150		mV
Ouput Stage						
High Side MOSFET R_{DSON}				15		mohm
Low Side MOSFET R_{DSON}				15		mohm
Maximum Output Current				13		A
OCP Adjust						
OCP current				40		uA
FB Under Voltage Protection						
FB Under Voltage Threshold				0.48		V

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1,6,51	AGND	Analog ground.
2	OCP	This pin is connected to the drain of the external low side MOSFET via resistor and is the input of the over current protection(OCP) comparator. An internal current source 40uA is flown to the external resistor which sets the OCP voltage across the Rdson of the low side MOSFET. Current limit point is this voltage divided by the Rds-on. Once this threshold is reached the Hdrv and Ldrv pins are latched out.
3,21 40-50	SW	These pins are connected to source of high side FET and provides return path for the high side driver. It is also used to hold the low side driver low until this pin is brought low by the action of high side turning off. LDRV can only go high if SW is below 1V threshold .
4	HDRV	High side MOSFET gate driver output
5	BST	This pin supplies voltage to high side FET driver. A high freq 0.1uF ceramic capacitor is placed as close as possible to and connected to this pin and SW pin.
7	HG	High side MOSFET gate pin out which is needed to connected HDRV pin.
8-20	VIN	Bus input which is connected to high side MOSFET's drain.
22-39	PGND	Source of low side MOSFET and ground of switching converter.
52	VCC	Power supply voltage. A high freq 1uF ceramic capacitor is placed as close as possible to and connected to this pin and ground pin. The maximum rating of this pin is 5V.
53	EN	A resistor divider is connected from the respective switcher BUS voltages to these pins that holds off the controller's soft start until this threshold is reached. An external low cost transistor can be connected to this pin for external enable control.
54	FB	This pin is the error amplifier inverting input. It is connected via resistor divider to the output of the switching regulator to set the output DC voltage. When FB pin voltage is lower than 0.6V, hiccup circuit starts to recycle the soft start circuit after 2048 switching cycles.
55	COMP	This pin is the output of error amplifier and is used to compensate the voltage control feedback loop. This pin can also be used to perform a shutdown if pulled lower than 0.3V.
56	NC	

BLOCK DIAGRAM

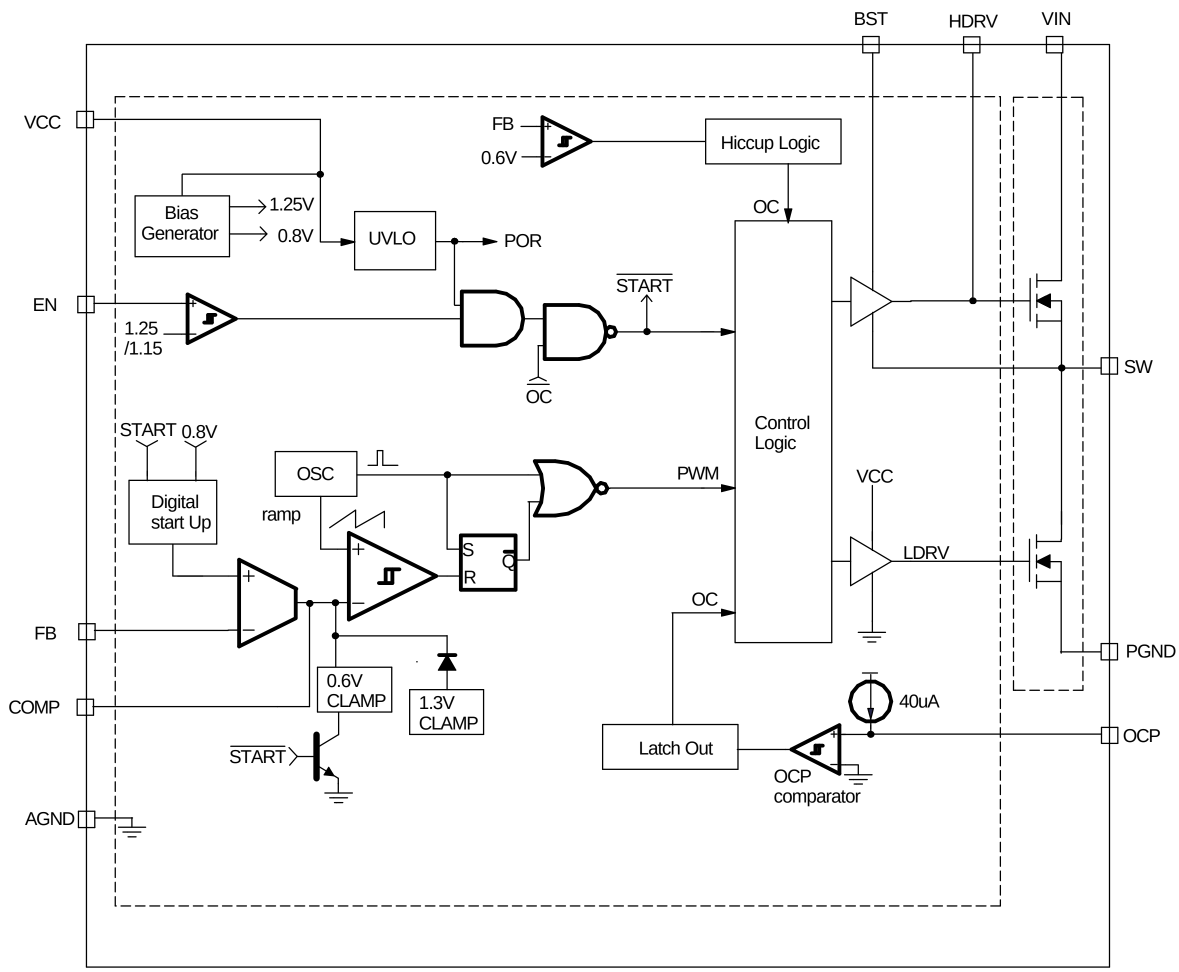


Figure 2 - Simplified block diagram of the NX9811A

Demoboard schematic

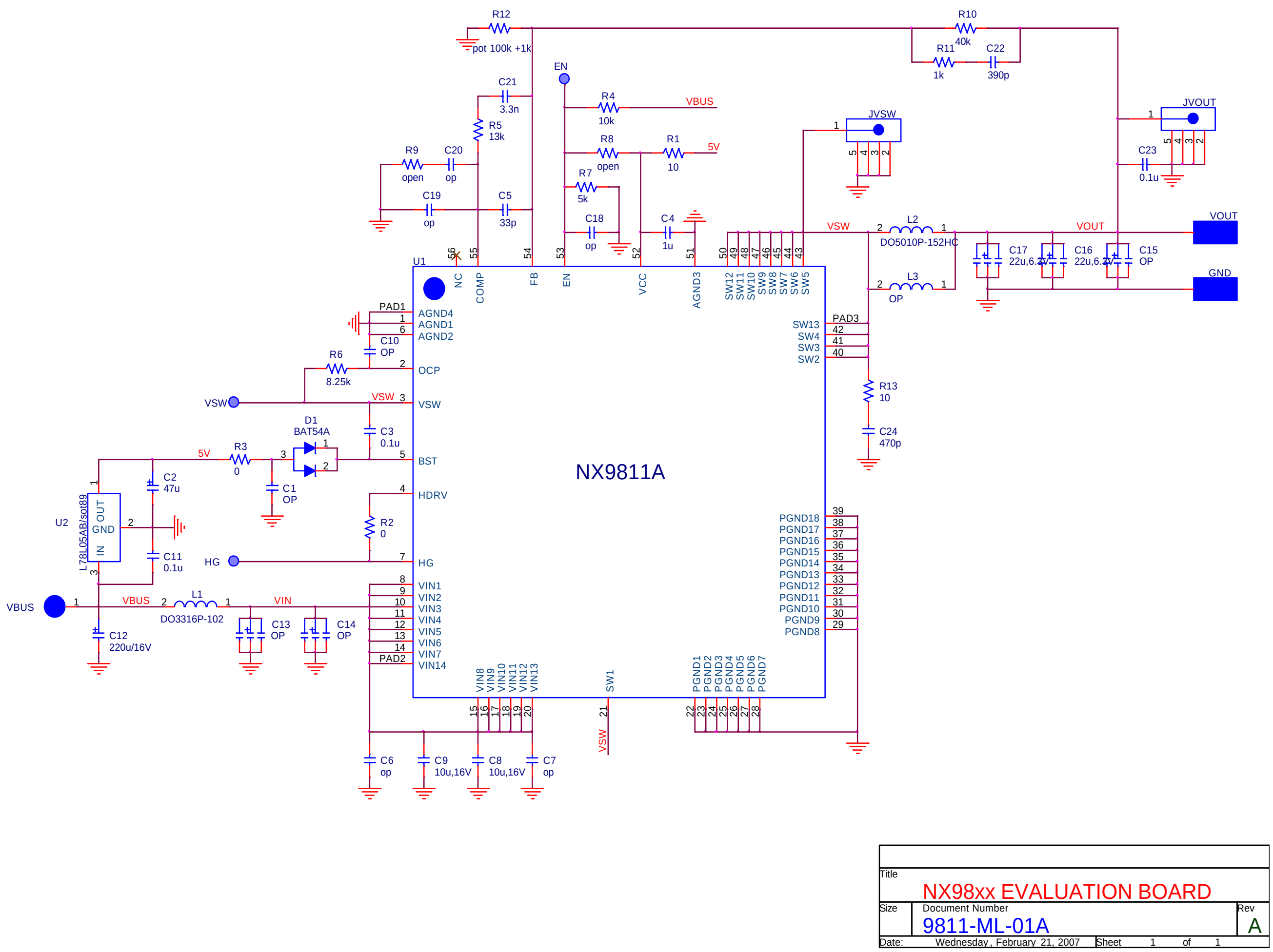


Figure 3- Demo board schematic based on ORCAD

Bill of Materials

Item	Quantity	Reference	Value	Manufacture
1	1	C2	47u,electricial	
2	3	C3,C11,C23	0.1u	
3	1	C4	1u	
4	1	C5	33p	
5	2	C8,C9	10u/16V ceramic	
6	1	C12	220u/16V,electrical	
7	2	C16,C17	22u/6.3V, ceramic	
8	1	C21	3.3n	
9	1	C22	390p	
10	1	C24	470p	
11	1	D1	BAT54A	
12	1	L1	DO3316P-102	Coilcraft
13	1	L2	DO5010P-152HC	Coilcraft
14	2	R1,R13	10	
15	2	R2,R3	0	
16	1	R4	10k	
17	1	R5	13k	
18	1	R6	8.25k	
19	1	R7	5k	
20	1	R10	40k	
21	1	R11	1k	
22	1	R12	100k pot	
23	1	U1	NX9811A	NEXSEM INC.
24	1	U2	L78L05AB/sot89	

Demoboard waveforms

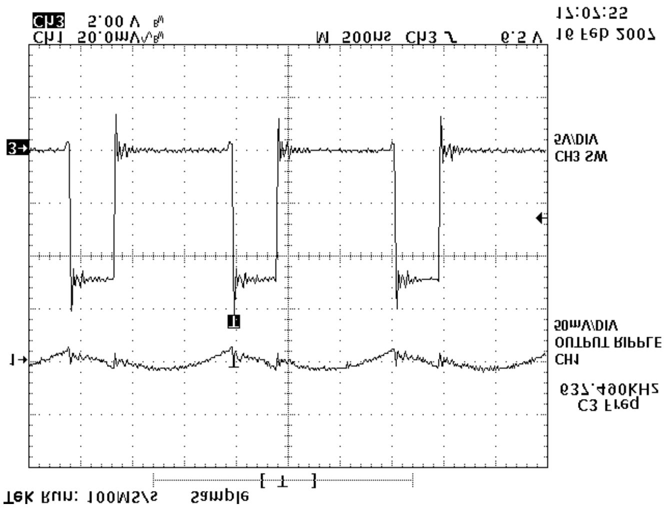


Figure 4 - Output ripple @ VOUT=3.3V

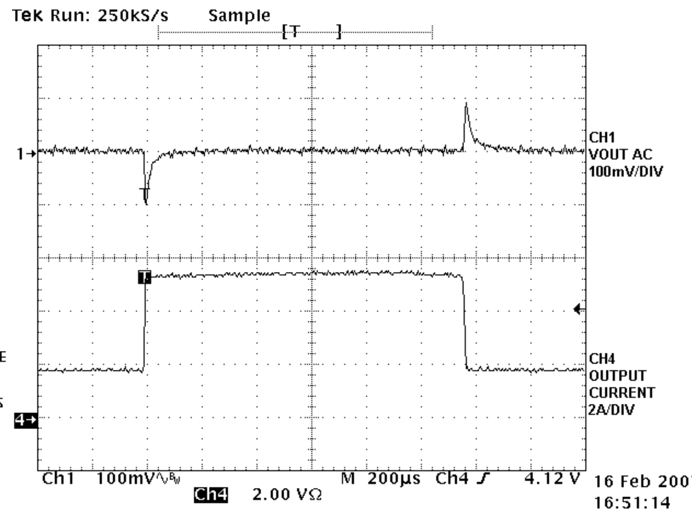


Figure 5 - Output voltage transient response @VOUT=1.2V

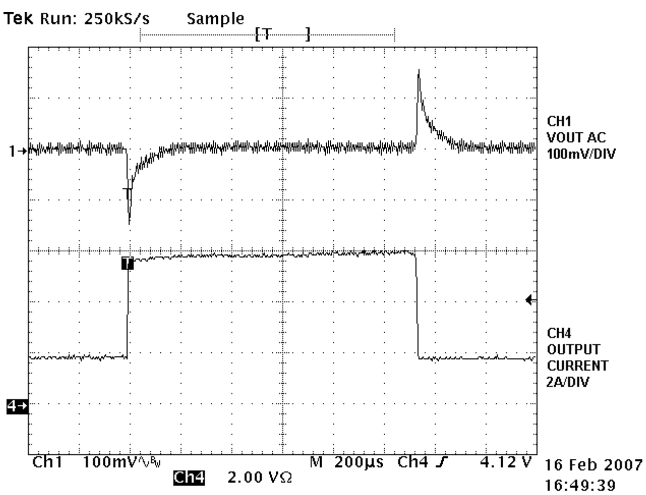


Figure 6 - Output voltage transient response @VOUT=5V

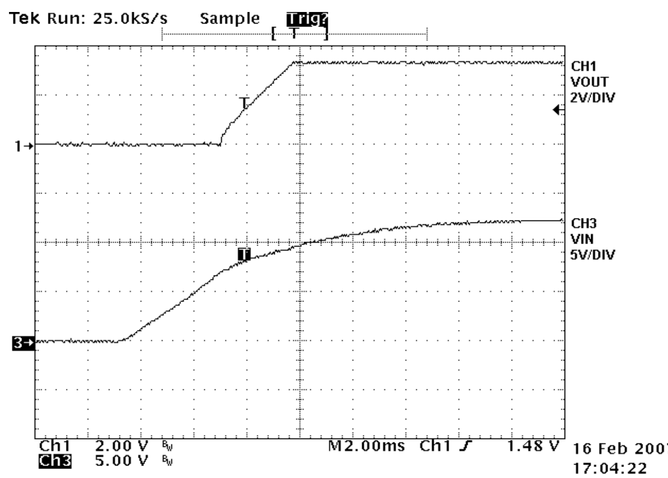


Figure 7 - Startup @VOUT=3.3V

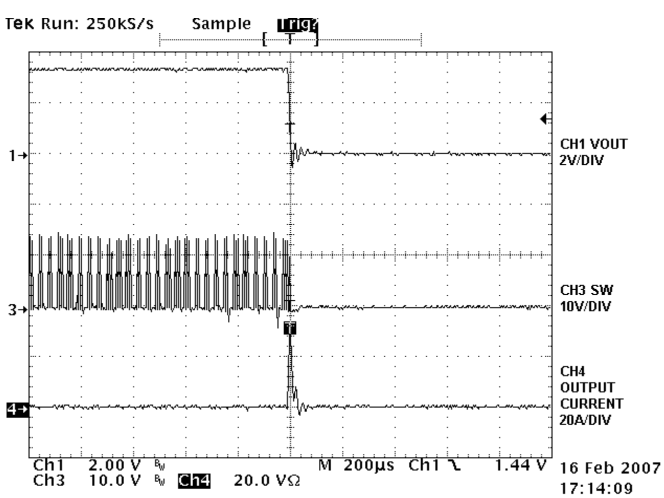


Figure 8 - Short circuit protection

Demoboard waveforms(Cont'd)

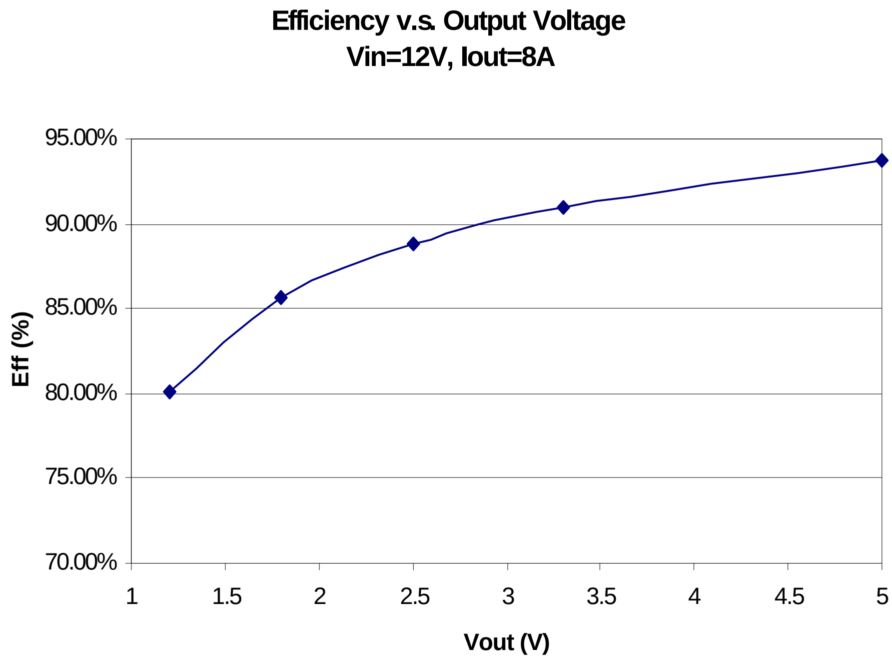


Figure 9 - Efficiency chart

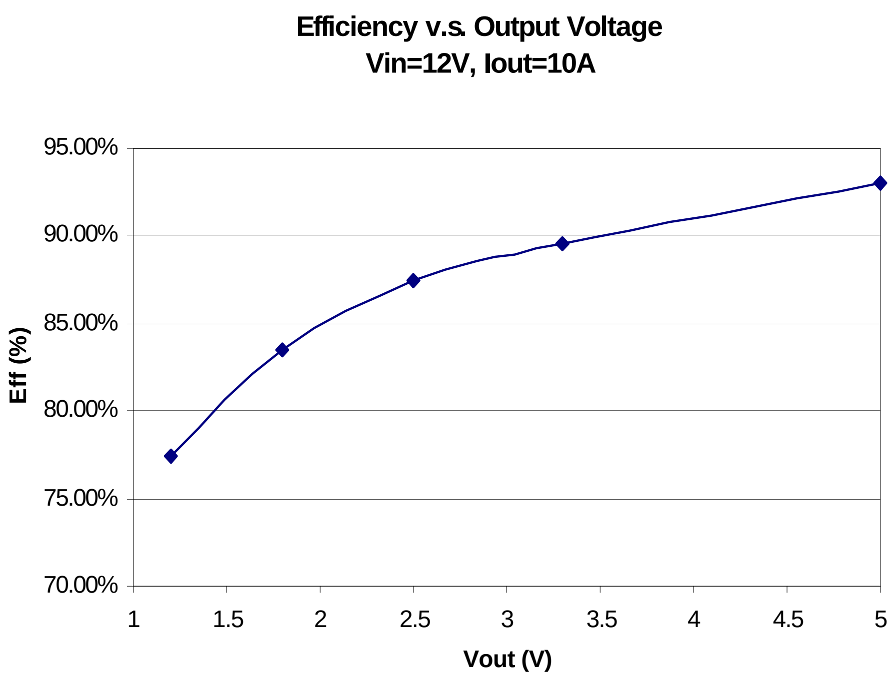


Figure 10 - Efficiency chart

Demoboard waveforms(Cont'd)

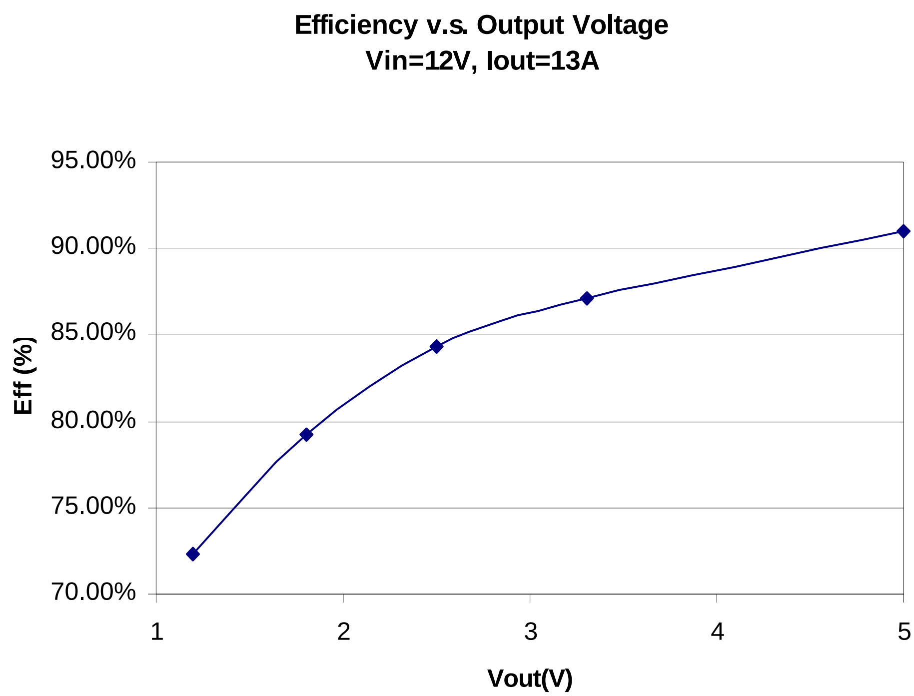


Figure 11 - Efficiency chart

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage

V_{OUT} - Output voltage

I_{OUT} - Output current

ΔV_{RIPPLE} - Output voltage ripple

F_S - Working frequency

ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX9811A, the schematic is figure 1.

$V_{IN} = 12V$

$V_{OUT}=3.3V$

$F_S=600kHz$

$I_{OUT}=10A$

$\Delta V_{RIPPLE}<=33mV$

$\Delta V_{DROOP}<=150mV$ @ 3A step

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT}=\frac{V_{IN}-V_{OUT}}{\Delta I_{RIPPLE}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S} \qquad ...(1)$$

$$I_{RIPPLE}=k\times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.3, then

$$L_{OUT}=\frac{12V-3.3V}{0.3\times 10A}\times\frac{3.3V}{12V}\times\frac{1}{600kHz}$$

$$L_{OUT}=1.33uH$$

Choose inductor from COILCRAFT DO3316P-152HC with L=1.5uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE}=\frac{V_{IN}-V_{OUT}}{L_{OUT}}\times\frac{V_{OUT}}{V_{IN}}\times\frac{1}{F_S}$$

$$=\frac{12V-3.3V}{1.5uH}\times\frac{3.3v}{12V}\times\frac{1}{600kHz}=2.66A \qquad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE}=ESR\times\Delta I_{RIPPLE}+\frac{\Delta I_{RIPPLE}}{8\times F_S\times C_{OUT}} \qquad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance, C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

In this example ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors. Two 22uF, X5R ceramic capacitor with 2mΩ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE}=2m\Omega\times 2.66A+\frac{2.66A}{8\times 600kHz\times 44uF}$$

$$=17.9mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot, when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(4)$$

where t is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(5)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(6)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(7)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \dfrac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(8)$$

For example, assume voltage droop during transient is 150mV for 3A load step.

Two 22uF, X5R ceramic capacitor with $2m\Omega$ ESR is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} = \frac{2m\Omega \times 22\mu F \times 3.3V}{3A} = 0.048\mu H$$

The selected inductor is 1.5uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E = \frac{1.5\mu H \times 3A}{3.3V} - 2m\Omega \times 22\mu F = 1.32us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 = \frac{2m\Omega \times 3A}{150mV} + \frac{3.3V}{2 \times 1.5\mu H \times 22\mu F \times 150mV} \times (1.32us)^2 = 1.03$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=2.

It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response,compensator is employed to provide highest possible bandwidth and enough phase margin.Ideally,the Bode plot of the closed loop system has crossover frequency between1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(9)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(10)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(11)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(12)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R_4>>2/gm. And it would be desirable if $R_1||R_2||R_3$>>1/gm can be met at the same time.

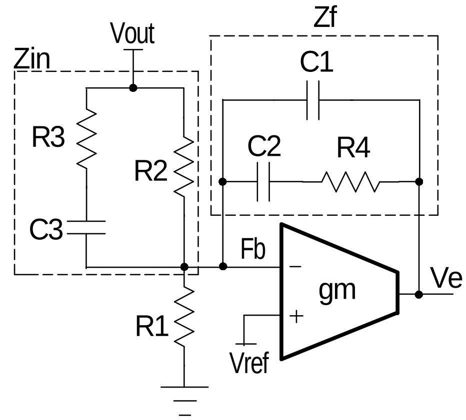


Figure 12 - Type III compensator using transconductance amplifier

Case 1: $F_{LC}<F_O<F_{ESR}$**(ceramic)**

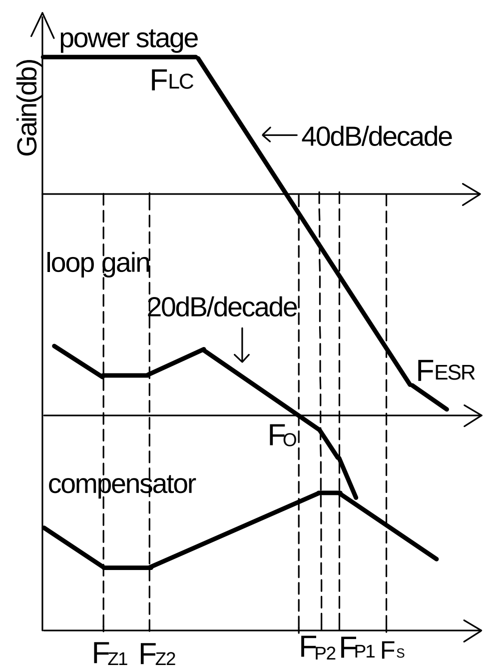


Figure 13 - Bode plot of Type III compensator

Design example for type III compensator are in order. The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and F_O<=1/10~1/5$F_{s.}$

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{1.5uH\times 44uF}}=19.6kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times 2m\Omega\times 44uF}=3.6MHz$$

2. Set R_2 equal to 40kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{40k\Omega\times 0.8V}{3.3V-0.8V}=12.8k\Omega$$

Choose R_1=12.7kΩ.

3. Set zero $F_{Z2}=0.5F_{LC}$ and $F_{p1}=3/4F_S$.

4. Calculate R_4 and C_3 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=100kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times 40k\Omega}\times\left(\frac{1}{9.8kHz}-\frac{1}{450kHz}\right)=397pF$$

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}=\frac{1.5V}{12V}\times\frac{2\times\pi\times 100kHz\times 1.5uH}{390pF}\times 44uF=13.3k\Omega$$

Choose C_3=390pF, R_4=13kΩ.

5. Calculate C_2 with zero F_{z1} at 20% of the LC double pole by equation (9).

$$C_2=\frac{1}{2\times\pi\times F_{z1}\times R_4}=\frac{1}{2\times\pi\times 0.2\times 19.6kHz\times 13k\Omega}=3.1nF$$

Choose C_2=3.3nF.

6. Calculate C_1 by equation (12) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times 13k\Omega\times 300kHz}=40pF$$

Choose C_1=33pF

7. Calculate R_3 by equation (11).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times 450kHz\times 390pF}=906\Omega$$

Choose R_3=1kΩ.

Case 2: $F_{LC}<F_O<F_{ESR}$(low ESR POSCAP, OSCON)

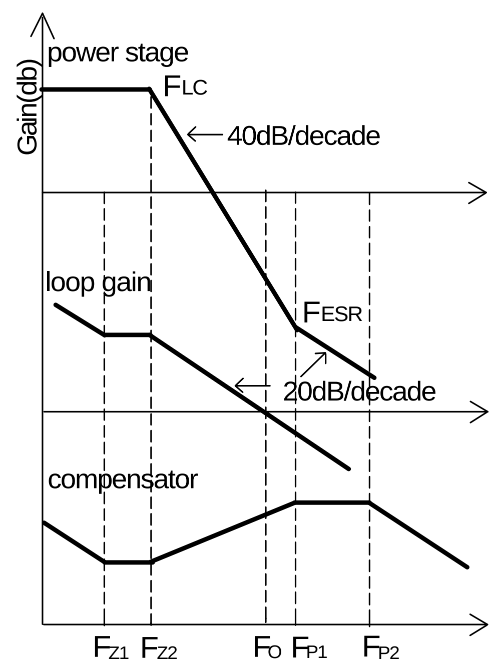


Figure 14 - Bode plot of Type III compensator ($F_{LC}<F_O<F_{ESR}$)

Typical design example of type III compensator in which one oscon capacitor (560uF, 7mohm) is chosen as output capacitor is shown as the following steps.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}} = \frac{1}{2\times\pi\times\sqrt{1.5uH\times 560uF}} = 5.5kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}} = \frac{1}{2\times\pi\times 7m\Omega\times 560uF} = 40.6kHz$$

2. Set R_2 equal to 10kΩ.

$$R_1 = \frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}} = \frac{10k\Omega\times 0.8V}{1.8V-0.8V} = 8k\Omega$$

Choose R_1=8.06kΩ.

3. Set zero $F_{z2} = F_{LC}$ and $F_{p1} = F_{ESR}$, calculate C_3.

$$C_3 = \frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right) = \frac{1}{2\times\pi\times 10k\Omega}\times\left(\frac{1}{5.5kHz}-\frac{1}{40.6kHz}\right) = 2.5nF$$

Choose C_3=2.7nF.

4. Calculate R_4 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=60kHz.

$$R_4 = \frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out} = \frac{1.1V}{12V}\times\frac{2\times\pi\times 60kHz\times 1.5uH}{2.7nF}\times 560uF = 10.7k\Omega$$

Choose R_4=10.7kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (9).

$$C_2 = \frac{1}{2\times\pi\times F_{Z1}\times R_4} = \frac{1}{2\times\pi\times 0.75\times 5.5kHz\times 10.7k\Omega} = 3.6nF$$

Choose C_2=3.3nF.

6. Calculate C_1 by equation (12) with pole F_{p2} at half the switching frequency.

$$C_1 = \frac{1}{2\times\pi\times R_4\times F_{P2}} = \frac{1}{2\times\pi\times 10.7k\Omega\times 300kHz} = 49pF$$

Choose C_1=47pF.

7. Calculate R_3 by equation (11) with $F_{p1} = F_{ESR}$.

$$R_3 = \frac{1}{2\times\pi\times F_{P1}\times C_3} = \frac{1}{2\times\pi\times 40.6kHz\times 2.7nF} = 1.45k\Omega$$

Choose R_3 =1.43kΩ.

Case 3: $F_{LC}<F_{ESR}<F_O$

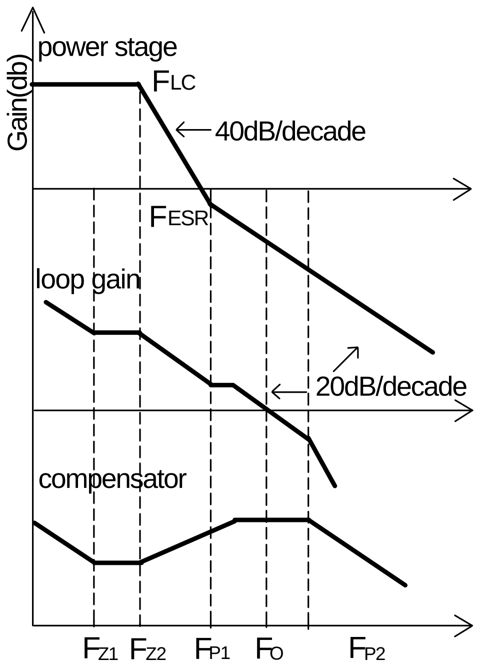


Figure 15 - Bode plot of Type III compensator ($F_{LC}<F_{ESR}<F_O$)

If electrolytic capacitors are used as output capacitors, typical design example of type III compensator in which the crossover frequency is selected as $F_{LC}<F_{ESR}<F_O$ and $F_O<=1/10\sim1/5F_s$ is shown as the following steps. Here two SANYO MV-WG1500 with 13 mΩ is chosen as output capacitor.

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{1uH\times3000uF}}=2.9kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times6.5m\Omega\times3000uF}=8.2kHz$$

2. Set R_2 equal to 10kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{10k\Omega\times0.8V}{1.8V-0.8V}=8k\Omega$$

Choose R_1=8kΩ.

3. Set zero $F_{Z2}=F_{LC}$ and $F_{p1}=F_{ESR}$.

4. Calculate C_3.

$$C_3=\frac{1}{2\times\pi\times R_2}\times(\frac{1}{F_{z2}}-\frac{1}{F_{p1}})=\frac{1}{2\times\pi\times10k\Omega}\times(\frac{1}{2.9kHz}-\frac{1}{8.2kHz})=3.5nF$$

Choose C_3=3.3nF.

5. Calculate R_3.

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times8.2kHz\times3.3nF}=5.9k\Omega$$

Choose R_3=5.9kΩ.

6. Calculate R_4 with F_O=60kHz.

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{ESR}\times\frac{R_2\times R_3}{R_2+R_3}=\frac{1.5V}{12V}\times\frac{2\times\pi\times60kHz\times1uH}{6.5m\Omega}\times\frac{10k\Omega\times5.9k\Omega}{10k\Omega+5.9k\Omega}=26.9k\Omega$$

Choose R_4=26.7kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (9).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times0.75\times2.9kHz\times26.7k\Omega}=2nF$$

Choose C_2=2.2nF.

6. Calculate C_1 by equation (12) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times26.7k\Omega\times300kHz}=20pF$$

Choose C_1=22pF.

B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 17. R_3 and C_1 introduce a zero to cancel the double pole effect. C_2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain=g_m \times \frac{R_1}{R_1+R_2} \times R_3 \quad \text{... (13)}$$

$$F_z=\frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (14)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (15)}$$

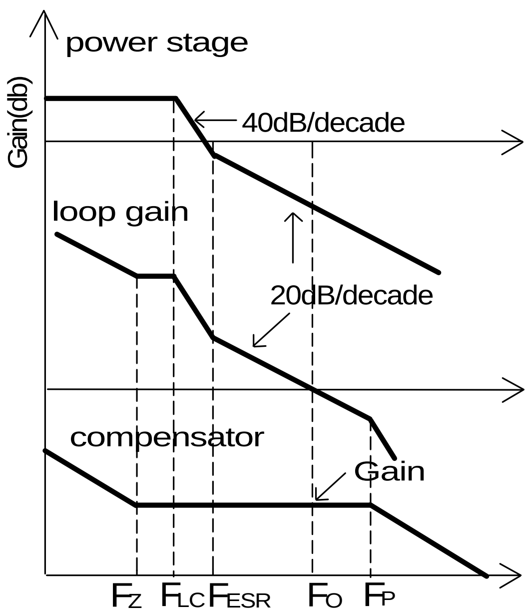


Figure 16 - Bode plot of Type II compensator

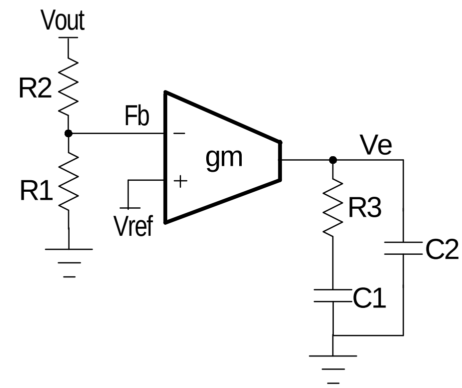


Figure 17 - Type II compensator with transconductance amplifier

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10\sim1/5F_s$.

The following is parameters for type II compensator design. Input voltage is 12V, output voltage is 1.8V, output inductor is 1uH, output capacitors are two 1500uF with 13mΩ electrolytic capacitors.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}$$
$$=\frac{1}{2\times\pi\times\sqrt{1uH\times 3000uF}}$$
$$=2.9kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}$$
$$=\frac{1}{2\times\pi\times 6.5m\Omega\times 3000uF}$$
$$=8.2kHz$$

2.Set R_2 equal to 1kΩ.

$$R_1=\frac{R_2\times V_{REF}}{V_{OUT}-V_{REF}}=\frac{1k\Omega\times 0.8V}{1.8V-0.8V}=800\Omega$$

Choose R_1=806Ω.

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=60kHz.

4.Calculate R_3 value by the following equation.

4.Calculate R_3 value by the following equation.

$$R_3 = \frac{V_{OSC}}{V_{in}} \times \frac{2\times\pi\times F_O \times L}{R_{ESR}} \times \frac{1}{g_m} \times \frac{V_{OUT}}{V_{REF}}$$
$$= \frac{1.5V}{12V} \times \frac{2\times\pi\times 60kHz \times 1uH}{6.5m\Omega} \times \frac{1}{2.0mA/V} \times \frac{1.8V}{0.8V}$$
$$= 8.15k\Omega$$

Choose R_3 =8.2kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1 = \frac{1}{2\times\pi\times R_3 \times F_z}$$
$$= \frac{1}{2\times\pi\times 8.2k\Omega \times 0.75 \times 2.9kHz}$$
$$= 8.9nF$$

Choose C_1=8.2nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{\pi \times R_3 \times F_s}$$
$$= \frac{1}{\pi \times 8.2k\Omega \times 300kHz}$$
$$= 129pF$$

Choose C_1=120pF.

Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT}, V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(16)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

See compensator design for R_1 and R_2 selection.

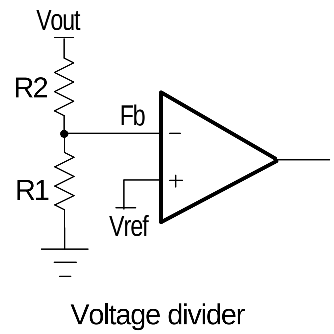


Figure 18 - Voltage divider

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply switching current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise.The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1-D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(17)$$

V_{IN} = 12V, V_{OUT}=1.8V, I_{OUT}=9A, the result of input RMS current is 3.2A.

For higher efficiency, low ESR capacitors are recommended. Two 10uF X5R ceramic capacitors are chosen as input bulk capacitors.

Soft Start and Enable

NX9811A has digital soft start for switching controller and has one enable pin for this start up. When the Power Ready (POR) signal is high and the voltage at enable pin is above 1.25V the internal digital counter starts to operate and the voltage at positive input of Error amplifier starts to increase, the feedback network will force the output voltage follows the reference and starts the output slowly. After 2048 cycles, the soft start is complete and the output voltage is regulated to the desired voltage decided by the feedback resistor divider.

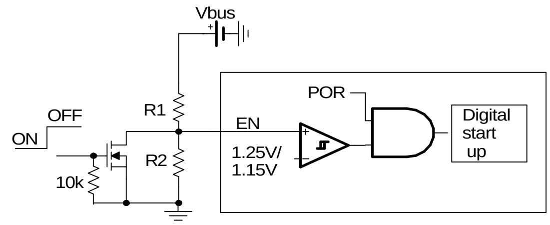


Figure 19 - Enable and Shut down the NX9811A with Enable pin.

The start up of NX9811A can be programmed through resistor divider at Enable pin. For example, if the input bus voltage is12V and we want NX9811A starts when Vbus is above 9V. We can select using the following equation.

$$R_1 = \frac{(9V - 1.25V) \times R_2}{1.25V}$$

The NX9811A can be turned off by pulling down the Enable pin by extra signal MOSFET as shown in the above Figure. When Enable pin is below 1.25V, the digital soft start is reset to zero. In addition, all the high side and low side driver is off and no negative spike will be generated during the turn off.

Over Current Protection

Over current protection is achieved by sensing current through the low side MOSFET. An internal current source of 40uA flows through an external resistor connected from OCP pin to SW node sets the over current protection threshold. When synchronous FET is on, the voltage at node SW is given as

V_{SW}=-$I_L \times R_{DSON}$

The voltage at pin OCP is given as

$I_{OCP} \times R_{OCP}$+V_{SW}

When the voltage is below zero, the over current occurss as shown in figure 20.

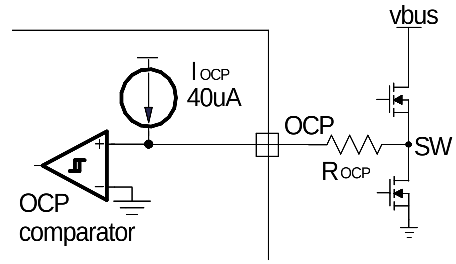


Figure 20 - Over current protection

The over current limit can be set by the following equation

$$I_{SET} = \frac{I_{OCP} \times R_{OCP}}{K \times R_{DSON}}$$

According to datasheet the lower MOSFET R_{DSON}=15mΩ, the worst case thermal consideration K=1.5 and the current limit is set at 15A, then

$$R_{OCP} = \frac{I_{SET} \times K \times R_{DSON}}{I_{OCP}} = \frac{15A \times 1.5 \times 15m\Omega}{40uA} = 8.43k\Omega$$

Choose R_{OCP}=8.25kΩ