Two Phases Synchronous Buck PWM Controller

General Description

The RT8807/A is a two phases synchronous Buck PWM controller with integrated drivers which is optimized for high-performance graphic microprocessor and computer applications. The IC integrates a voltage mode PWM controller, two 5V MOSFET drivers with internal bootstrap diodes, as well as output current monitoring and protection functions into the V/WQFN-24L 4x4 package.

The inductor currents are sensed by lossless DCR current sensing technique for current balance and over current protection. The RT8807/A also features a reference tracking mode operation in which the feedback voltage is regulated and tracks external input reference voltage. Other features include output current indication, adjustable operating frequency, adjustable soft-start, power good, external compensation, and enable/shutdown functions.

Ordering Information

RT8807 □ □

- Package Type
  QV : VQFN-24L 4x4 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

RT8807A □ □

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
- Operating Temperature Range
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

- **Two-Phase Power Conversion with Single 12V Power Supply**
- **Embedded 5V Upper Gate Driver and 12V Lower Gate Driver**
- **Internal Regulated 5V Output**
- **Precise Core Voltage Regulation**
- **Selectable Internal / External Reference**
- **Differential Inductor DCR Current Sense**
- **External Programmable Voltage Droop Control**
- **Enable Control for External Shutdown**
- **Adjustable Operating Frequency**
- **Adjustable Soft Start**
- **Power Good and Output Current Indication**
- **Adjustable Over Current Protection**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **Over Temperature Protection**
- **Proprietary BTR (Boost Transient Response) Feature Reducing Output Voltage Drop During Load Transition (For RT8807 Only)**
- **RoHS Compliant and 100% Lead(Pb)-Free**

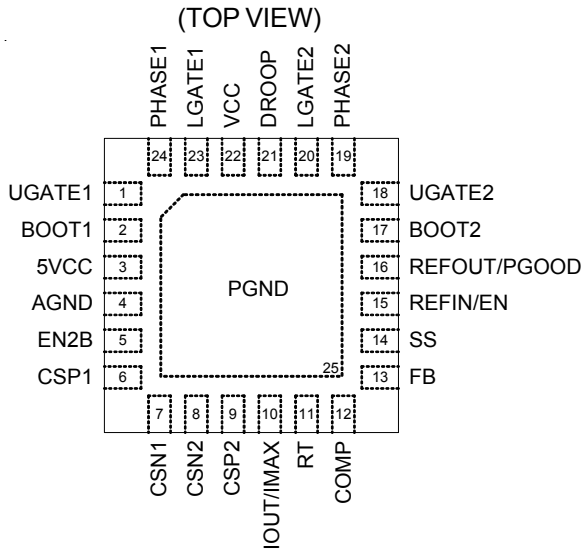
Applications

- Middle to High End GPU Core Power
- High End Desktop PC Memory Core Power
- Low Voltage, High Current DC / DC Converter
- Voltage Regulator Modules

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

Pin Configurations



V/WQFN-24L 4x4

Typical Application Circuit

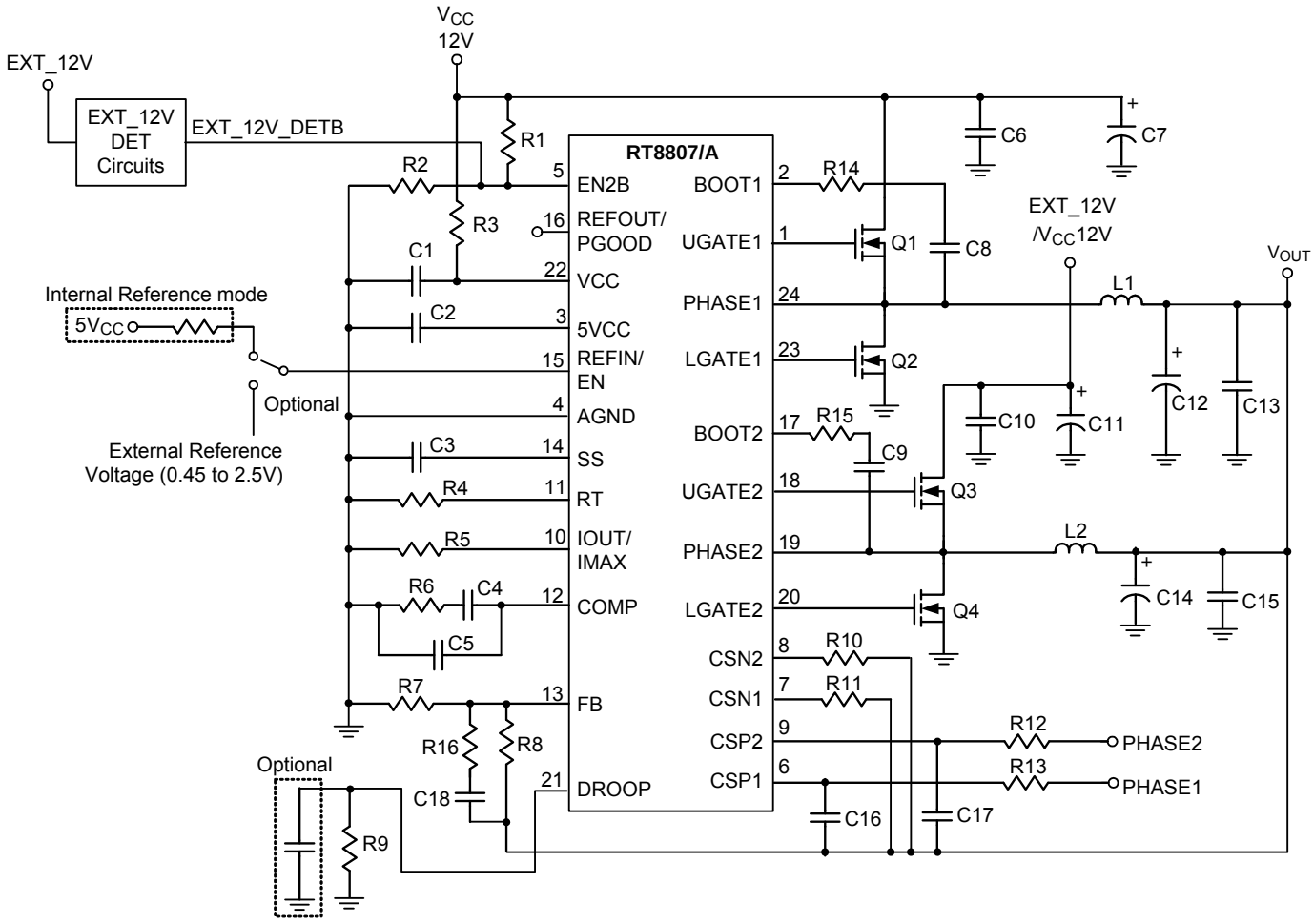
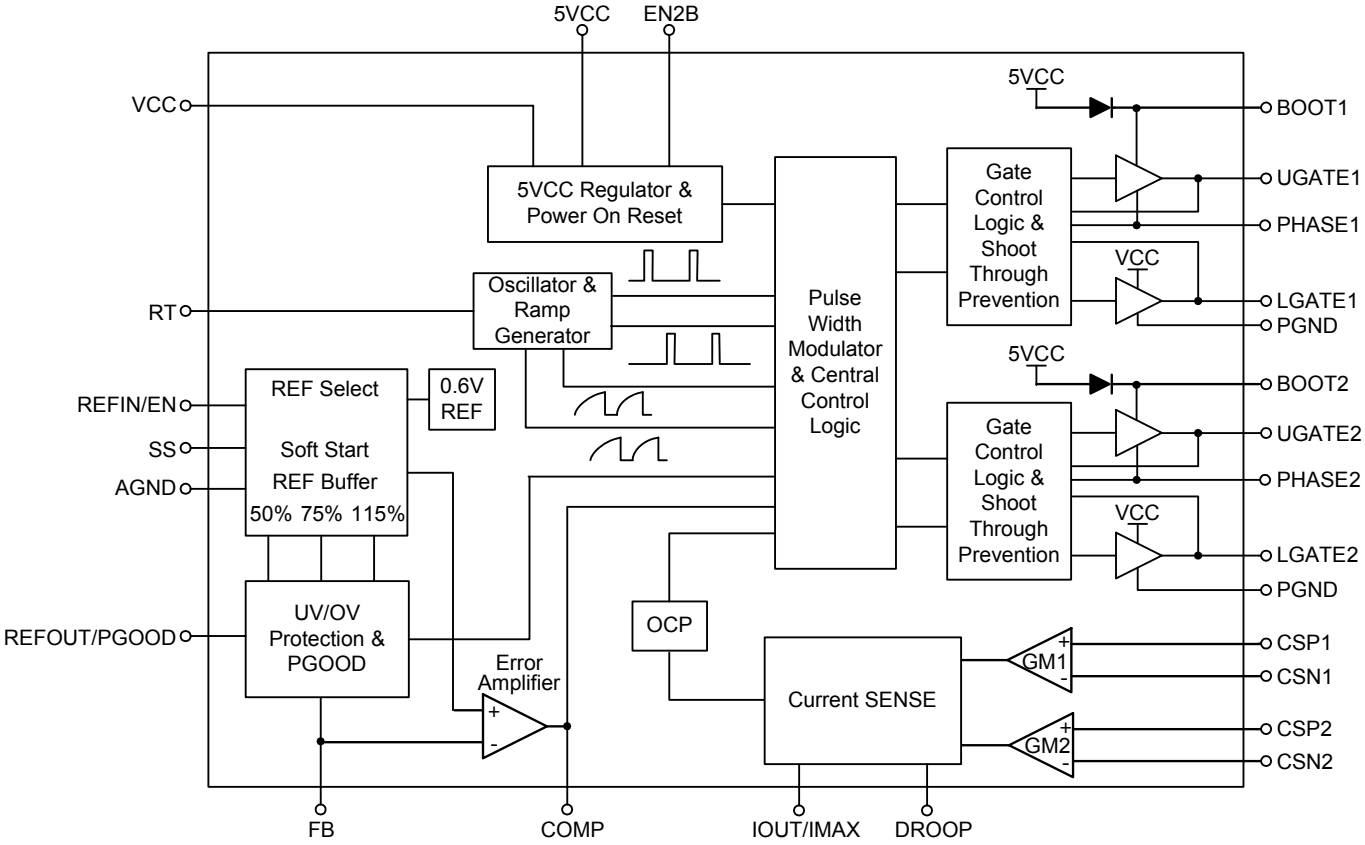


Figure 1. Typical Application Circuit with 12V Input

Function Block Diagram



Power up scheme to support dual power rails application

This feature is to support the following case in the application where one phase is powered by PCIEBUS_12V and the other phase is powered by EXT_12V.

- When the system is powered without EXT_12V Cable, RT8807/A will work with one phase and be able to boot system into Dos Warning screen.
- The Warning message tells user to power off the system first, plug in the EXT_12V Cable, and then reboot the system again.
- After system re-boot, RT8807/A could work with two phases.

Below is the power up sequence for dual V_{IN} (PCIEBUS_12V & EXT_12V) application. This application is classified into two cases :

<1> The external connector is not plugged while power on

The EXT_12V_DETB is pulled up to High. Soft-start will be released to ramp up after POR. After T1, RT8807/A latches EN2B signal and determines to operate in single phase. The time interval T1 is used to wait EN2B ready. Once single phase is confirmed, the external 12V power connector plugged or not will not affect the status.

<2> The external connector is plugged while power on

The EXT_12V_DETB is grounded by external cable detection circuits. RT8807/A latches EN2B at T1 and determines to operate in two phases. If the connector is removed later, RT8807/A will turn off phase 2 and enter single phase operation mode. Further plugged in/out will not affect the status anymore.

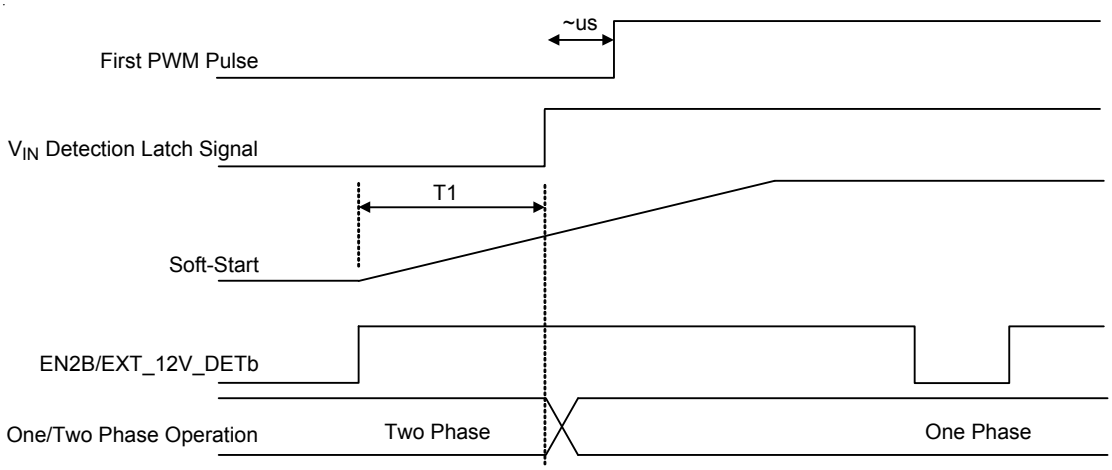


Figure 2. External Connector is not Plugged

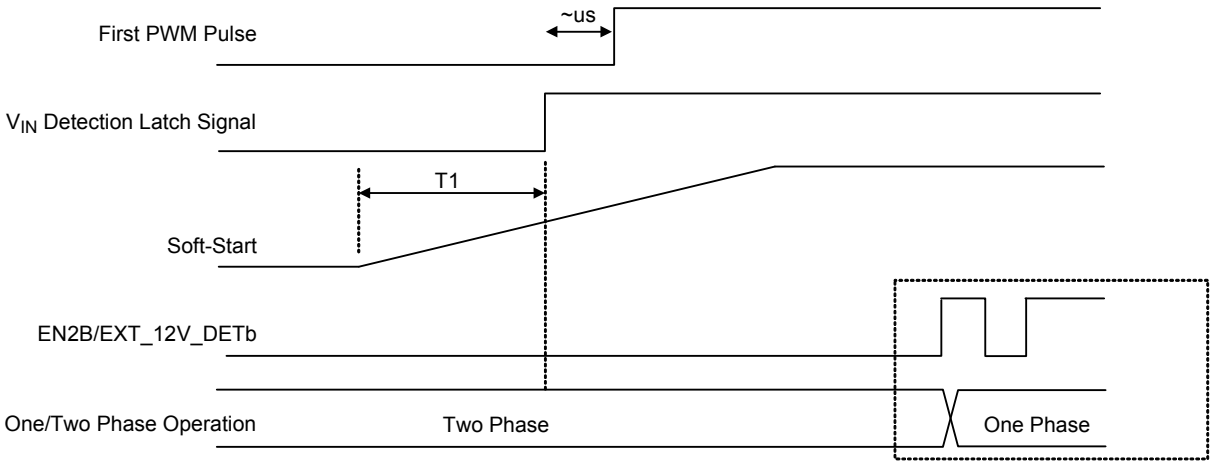


Figure 3. External Connector is Plugged

Functional Pin Description

UGATE1 (Pin 1), UGATE2 (Pin 18)

Upper Gate Drivers. Theses pins provide the gate drive for the converter's high-side MOSFET. Connect these pins to the high-side MOSFET gate.

BOOT1 (Pin 2), BOOT2 (Pin 17)

Bootstrap Power Pins. Theses pins power the high-side MOSFET drivers.

5VCC (Pin 3)

Internal Regulator Power Pin. The regulated voltage provides power supply for all low-voltage circuits. Bypass at least 1uF ceramic capacitor to sustain high PSRR.

AGND (Pin 4)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

EN2B (Pin 5)

EXT_12V Detection Pin. RT8807/A latches high/low status of this pin in soft start period. If the result is low, RT8807/A will enter two phase operation. If it's high, RT8807/A turns off phase2 and operate in single phase only.

CSP1 (Pin 6), CSP2 (Pin 9)

These pins are positive input of current sensing transconductance amplifiers 1 and 2.

CSN1 (Pin 7), CSN2 (Pin 8)

These pins are negative input of current sensing transconductance amplifiers 1 and 2.

IOUT/IMAX (Pin10)

Output Current Indication. This pin sends a current out (I_X) referred to the sum of two sensed inductor currents sense value. Connect this pin through a resistor to ground. (I_{OUT} = 4 x I_X). This pin also sets maximum current limit threshold.

RT (Pin11)

Frequency Timing Resistor. Connect a resistor from RT to AGND to set the clock frequency.

COMP (Pin 12)

Compensation Pin. This pin is the output of the error amplifier.

FB (Pin 13)

Feedback Pin. This pin is connected to the PWM converter output's voltage or a resistor divider. This pin also connects to the inverting input of error amplifier and the PGOOD/UV/OV detection circuits.

SS (Pin 14)

Soft-Start Pin. Connect a capacitor from this pin to ground to set the soft-start interval.

REFIN/EN (Pin 15)

External Reference Input.

- If pulled up to 5VCC, internal reference is used (0.6V)
- If driven by external voltage ranged from 0.45V to 2.5V, external reference is used
- If pulled below 0.4V, device is disabled.

REFOUT/PGOOD (Pin 16)

Reference Out and Power GOOD. This pin drives 1.15V out once FB exceeds ~72.5% of the reference voltage after soft- start ends. This pin keeps at this voltage regardless of internal or external reference is used.

PHASE1 (Pin 24) PHASE2 (Pin 19)

These pins are return nodes of the high-side driver. Connect these pins to high-side MOSFET sources together with the low-side MOSFET drain and the inductors.

LGATE1 (Pin 23), LGATE2 (Pin 20)

Lower Gate Drivers. Theses pins provide the gate drive for the converter's low-side MOSFET. Connect these pins to the low-side MOSFET gate.

DROOP (Pin 21)

Set the load line for droop control. Connect this pin with a resistor to ground.

VCC (Pin 22)

Provide a 12V supply voltage for the IC. Connect a 10Ω/1uF low pass filter to sustain high PSRR.

PGND [Exposed Pad (25)]

Power ground pin. Tie the synchronous PWM converter's low-side MOSFET source to this pin.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- –0.3V to 15V
- PHASE to GND
  - DC ---------- –2V to 15V
  - < 200ns ---------- –5V to 22V
- BOOT to PHASE ---------- –0.3V to 7V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC} + 7V
  - < 200ns ---------- –0.3V to 30V
- UGATE
  - DC ---------- V_{PHASE} –0.3V to V_{BOOT} + 0.3V
  - < 200ns ---------- V_{PHASE} –2V to V_{BOOT} + 0.3V
- LGATE
  - DC ---------- –0.3V to V_{CC} + 0.3V
  - < 200ns ---------- –2V to V_{CC} + 0.3V
- Other Input, Output or I/O Voltage ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - V/WQFN–24L 4x4 ---------- 1.923W
- Package Thermal Resistance (Note 4)
  - V/WQFN–24L 4x4, θ_{JA} ---------- 52°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –40°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage ---------- +12V ±10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, PGND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input						
VCC Supply Voltage	V_{CC}		10.8	12	13.2	V
VCC Supply Current	I_{CC}	REFIN/EN = 0V (static)	--	5	--	mA
5VCC Supply Output						
5VCC Supply Voltage	V_{5VCC}	V_{CC} = 12V	4.8	5.15	5.5	V
5VCC Output Sourcing	I_{5VCC}	V_{CC} = 12V	20	--	--	mA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power-On Reset						
VCC Rising Threshold	V_{VCCTH}	V_{CC} Rising	6.7	7.5	8.3	V
VCC Hysteresis	V_{VCCHY}		–	0.45	--	V
EN2B High Threshold	V_{EN2BTH}	EN2B Rising	1	1.15	1.3	V
REFIN/EN						
Enable Rising Threshold	V_{ENTH}	REFIN/EN Rising	0.35	0.4	0.45	V
Enable Hysteresis	V_{ENHYS}		–	50	--	mV
REFIN Tracking Range			0.45	--	2.5	V
Reference Voltage Accuracy (use Internal Reference)						
Reference Voltage	V_{REF}	REFIN Pull-High to 5VCC	0.591	0.6	0.609	V
Accuracy		FB Coupled to COMP	–1.5	--	+1.5	%
Reference Voltage Accuracy (use External Reference)						
Accuracy		V_{REFIN} = 0.45V to 0.6V	–6	--	+6	mV
		V_{REFIN} = 0.6V to 2.5V	–1	--	+1	%
REFOUT / PGOOD						
REFOUT/PGOOD Voltage	V_{REFOUT}	V_{FB} > 75% of Reference Voltage	1.127	1.15	1.173	V
Accuracy			–2	--	+2	%
REFOUT Output Sourcing	I_{REFOUT}		3	5	--	mA
Error Amplifier						
DC Gain	A_{DC}	No load	–	70	--	dB
Gain-Bandwidth	GBW	C_{LOAD} = 10pF	–	8	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF	5	--	--	V/us
Transconductance	GM		–	2400	--	uA/V
Current Sense Amplifier						
Max Current	$I_{GM(MAX)}$	V_{CSP} = 1V Sink Current from CSN	100	--	--	uA
Oscillator						
Running Frequency	f_{OSC}	R_{RT} = 20kΩ	450	500	550	kHz
Max Duty Cycle	D		70	75	80	%
Ramp Amplitude	ΔV_{RAMP}		–	2.6	--	V
Soft Start						
Soft Start Current	I_{SS}		14	20	30	uA
Protection						
Over Current Threshold	V_{OCP}	Sweep I_{OUT}/I_{MAX} Voltage	2.07	2.3	2.53	V
Over-Voltage Threshold	V_{OVP}	Sweep FB Voltage	115	125	135	%
Under-Voltage Threshold	V_{UVP}	Sweep FB Voltage	45	55	63	%
Over Temperature Threshold	T_{OTP}		–	160	--	°C
Power GOOD						
Active Threshold		V_{FB} Rising	65	72.5	80	%

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Gate Driver						
Upper Drive Source	$R_{USOURCE}$	BOOT – PHASE = 5V 250mA Source Current	--	1.5	3	Ω
Upper Drive Sink	R_{USINK}	BOOT – PHASE = 5V 250mA Sink Current	--	1.5	4	Ω
Lower Drive Source	$I_{LSOURCE}$	V_{CC} = 12V V_{LGATE} = 6V	1	–	--	A
Lower Drive Sink	R_{LSINK}	V_{CC} = 12V 250mA Sink Current	--	0.9	2	Ω

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

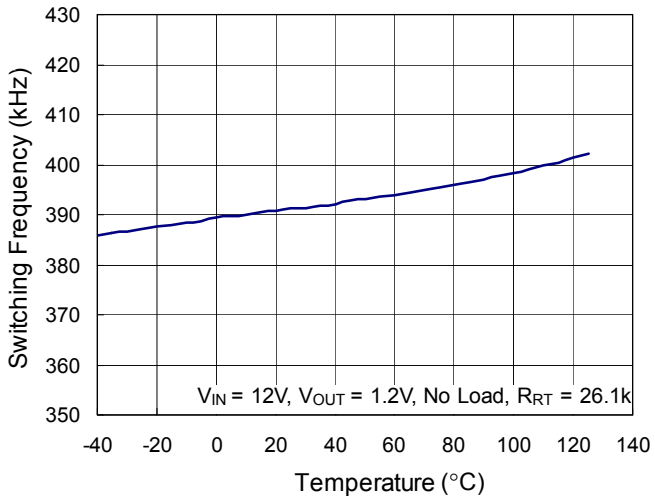
Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

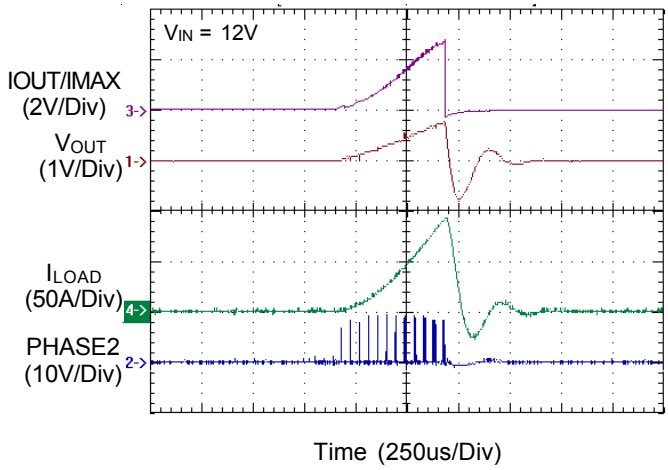
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

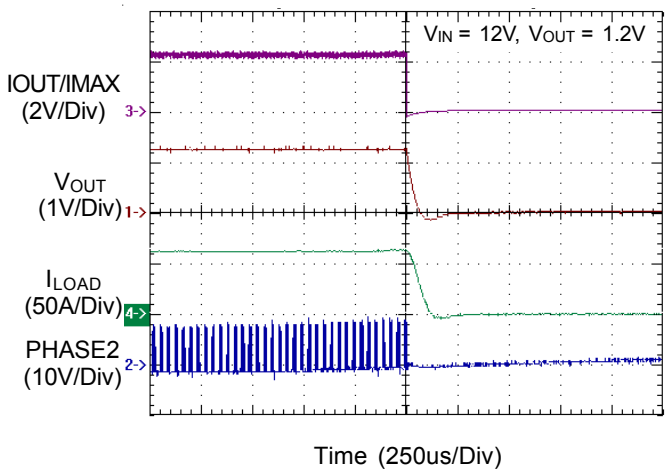
Switching Frequency vs. Temperature



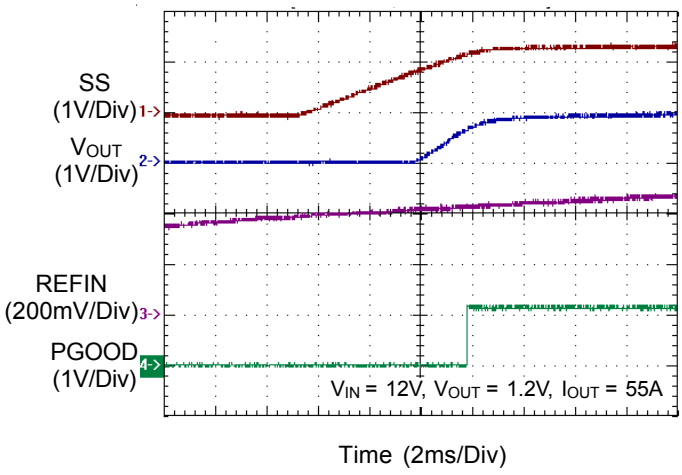
Start Up in Short Circuit



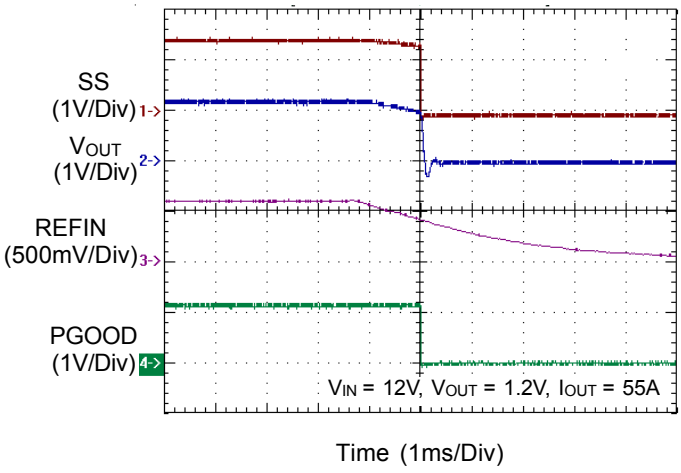
Over Current Protection



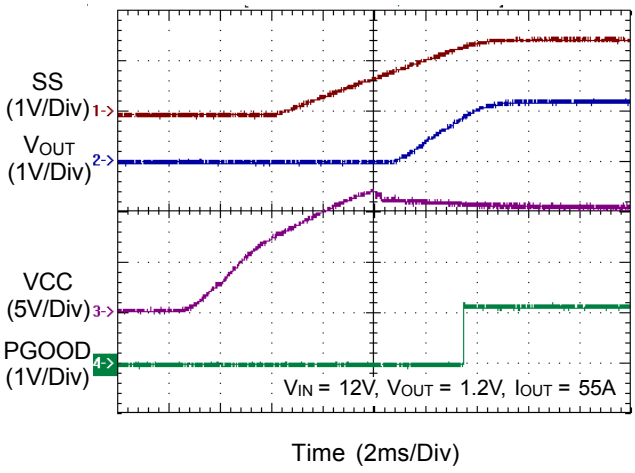
Power On from REFIN



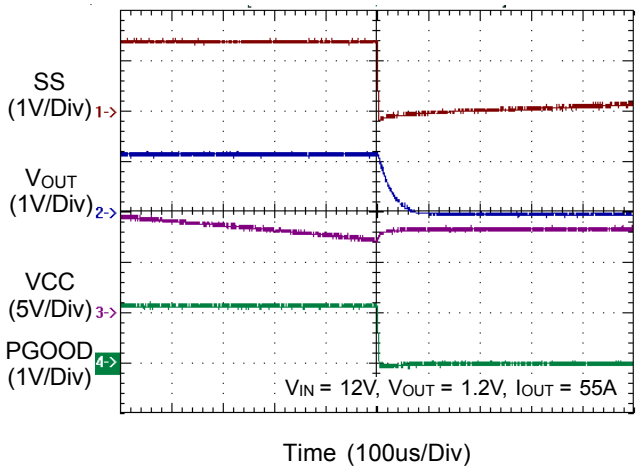
Power Off from REFIN



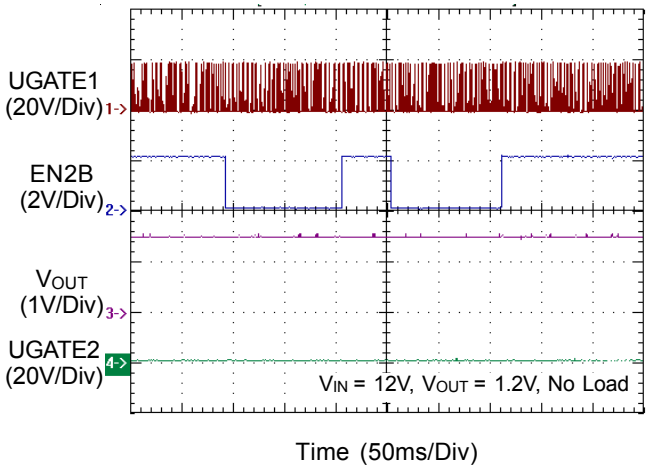
Power On from VCC



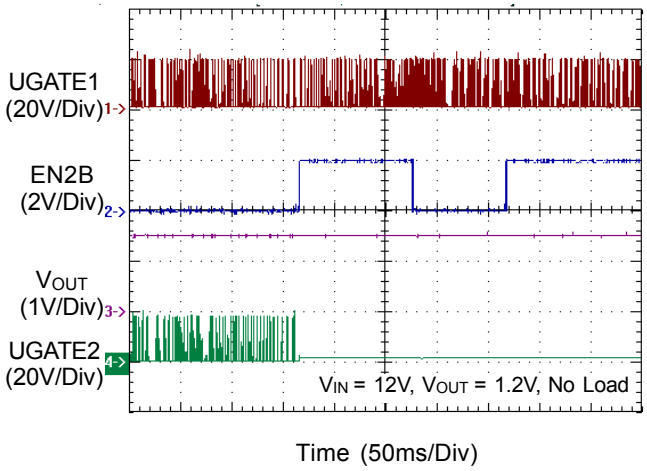
Power Off from VCC



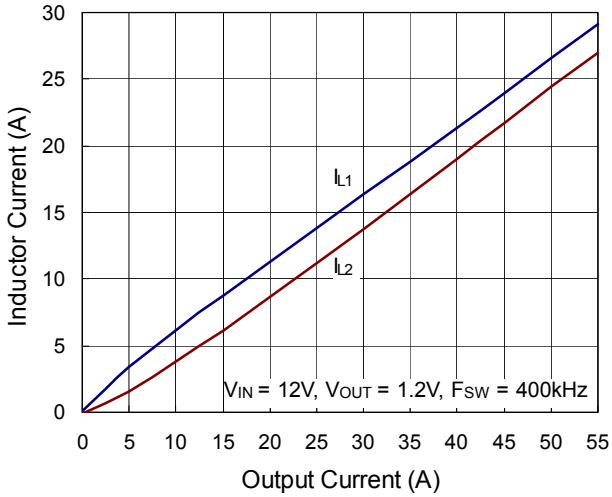
Single-phase Operation



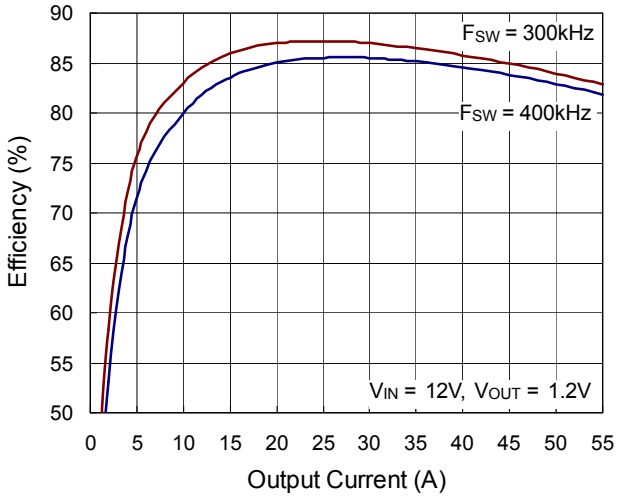
Two-phase to Single-phase



Inductor Current vs. Output Current



Efficiency vs. Output Current



Application Information

The RT8807/A is a dual-phase voltage-mode synchronous buck controller with embedded MOSFET drivers and protection functions for low-voltage high-current applications. The bootstrap diode is integrated into the IC to reduce the external component count. In addition, the number of operating phase (two-phase/single-phase) is selectable to provide user with more flexibility in circuit design. The inductor current is sensed by innovative DCR current sensing technique for current balance and over current protection.

Power On Reset

The RT8807/A initiates its soft start cycle only after the IC power supply, V_{CC}, and the internal regulated 5VCC are ready. The internally regulated 5VCC is used for all of the internal logic control circuit and the embedded high-side MOSFET driver. The bootstrap diode for the high-side MOSFET driver is integrated into the IC to reduce the external component count. In addition, V_{CC} is used for the low-side MOSFET driver to reduce the $R_{DS(ON)}$ of the low-side MOSFET for enhanced efficiency consideration.

The power on reset (POR) circuitry monitors the supply voltage to ensure that the supply voltage is high enough for controller's normal operation. Once V_{CC} and 5VCC exceed the POR rising threshold, the RT8807/A releases the reset state, and works according to the settings. Additionally, once any one of these two voltages is lower than its POR falling threshold value, the chip turns off. The hysteresis between the rising and falling thresholds ensures that once the chip is enabled, it will not be inadvertently turned off unless the bias voltage drops substantially.

Soft Start and Power Good

Once the POR state is released, the soft start cycle begins. A 20uA current source charges the capacitor, C_{SS}, which is connected between SS pin and GND to set the soft start time. Figure 1 shows the power on sequence.

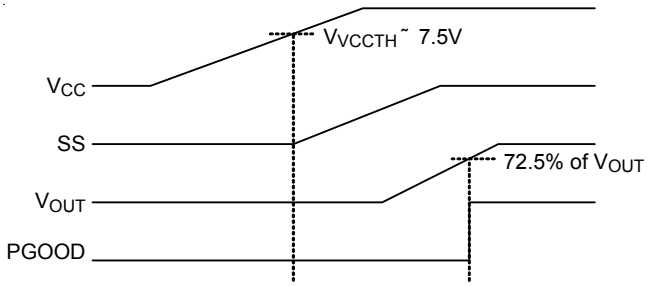


Figure 1. Power on Sequence

During the soft start, the voltage on SS pin gradually increases, and the output voltage of the error amplifier is clamped to prevent the inrush current from the input capacitors. Once the output voltage exceeds the power good threshold level (72.5% of output voltage), REFOUT/PGOOD pin will drive and maintain an reference voltage 1.15V unless V_{CC} falls below POR threshold or Under Voltage occurs.

Internal/External Reference

The RT8807/A supports the selectable internal/external reference voltage to provide more flexibility in practical applications. The selection of the internal/external reference is described in detail as follows.

a. Using Internal Reference

The internal reference voltage of the RT8807/A is set at 0.6V. When using the internal reference, REFIN/EN pin should be connected to 5VCC. REFIN/EN pin is also used for the enable function, the RT8807/A will not be enabled at start up if the voltage at the REFIN/EN pin is lower than V_{ENTH}.

b. Using External Reference

To use the external reference, the applied voltage on REFIN/EN pin should be within the tracking range (typically between 0.45V to 2.5V). This externally input voltage is used as the reference voltage for the error amplifier. Therefore, the RT8807/A operates in the tracking mode because the feedback voltage continuously tracks the external reference voltage.

Operating Frequency Setting

The converter switching frequency is programmed by simply connecting the resistor R_{RT} between RT pin and GND. Make sure the R_{RT} is firmly connected between RT pin and GND with a short trace length. If the R_{RT} is removed, there will not be any free running frequency. Figure 2 illustrates the switching frequency versus R_{RT}.

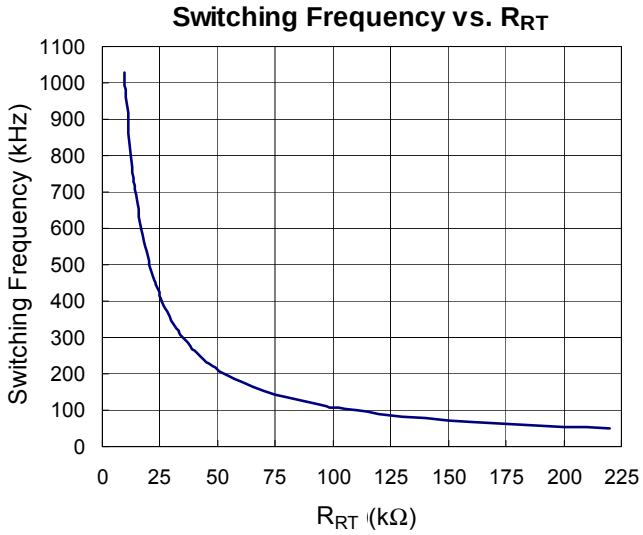


Figure 2. Switching Frequency vs. RT Resistance

Control Loop

The RT8807/A is a two-phase voltage-mode PWM controller. The control loop includes the power stage (MOSFETs, inductors and output capacitors), the error amplifier, the compensation network and the PWM modulator. The converter's output voltage is sensed as the feedback voltage through the divider resistors and then fed into the negative input of the high-gain error amplifier. The two-phase PWM signals are generated by the PWM modulator, which compares the output voltage of the error amplifier with two sawtooth waves, which are out of phase. Therefore, the output voltage of the converter is determined by the on-time duty ratio of the PWM signals. With proper compensation, the feedback voltage can be regulated to be equal to the reference voltage V_{REF} with required transient response.

Inductor Current Sense Setting

The DCR current sensing is a well-known lossless technique to obtain a voltage signal which is proportional to the inductor current. When the time constant of the R-C network is equal to the time constant of the inductor, the voltage drop across the DCR is equal to the voltage across the capacitor, namely $V_{DCR} = V_C$.

As shown in Figure 3, the differential GM amplifier converts the voltage signal to a current signal I_X for current balance and output voltage droop control. The following equations provide the calculation to determine the parameter values of the current sensing network and R_{CSN}.

$$\text{If } \frac{L}{DCR} = R \times C, \text{ than } V_C = V_{DCR} = DCR \times I_L$$

$$\text{The GM amplifier output current } I_X = \frac{V_C}{R_{CSN}}$$

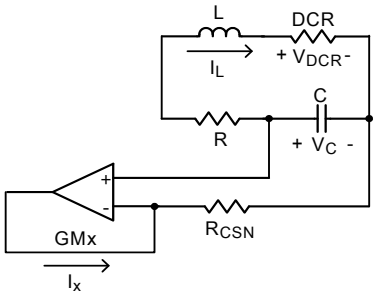


Figure 3. DCR Current Sense Circuit

Dead Zone Elimination

When the converter is in the light load condition, the voltage across the sensing capacitor, V_C, will be negative. However, the RT8807/A can not provide a negative I_X and consequently is not able to sense the negative inductor current. This results in a dead zone in the load line application. Therefore, a technique as shown in Figure 4 is utilized to eliminate the dead zone of the load line at light load condition. Referring to Figure 4, I_X can be expressed as follows when voltage V_C is negative.

$$I_X = \frac{(V_{OUT} + I_L \times DCR)}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN}}$$

To make sure that the RT8807/A can sense the inductor current, the right hand side of the above equation should always be positive :

$$\frac{V_{OUT}}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN2}} + \frac{I_L \times DCR}{R_{CSN}} \geq 0$$

Since R_{CSN2} >> DCR in practical application, the above equation can be simplified as :

$$\frac{V_{OUT}}{R_{CSN2}} \geq \left|\frac{I_L \times DCR}{R_{CSN}}\right|$$

$$\text{Therefore, } R_{CSN2} \leq \left|V_{OUT} \times \frac{R_{CSN}}{I_L \times DCR}\right|$$

For example, assuming the negative inductor current is equal to -5A at no load condition. For R_{CSN} = 390Ω, DCR = 1.7mΩ, V_{OUT} = 1.2V,

$$R_{CSN2} \leq \left|1.2 \times \frac{390}{-5 \times 1.7 \times 10^{-3}}\right|$$

$$R_{CSN2} \leq 55.06k\Omega$$

Choose R_{CSN2} = 54.9kΩ

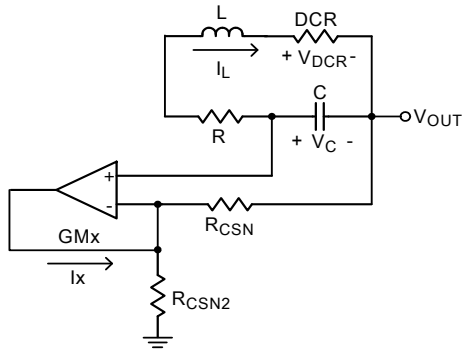


Figure 4. Application Circuit for Dead Zone Elimination

Over Current Protection Function

The over current threshold is determined by the resistor connected to IOUT/IMAX pin. The two GM amplifier's output currents are summed together and doubled, and then flows out into the resistor R_{IMAX}, which is connected between IOUT/IMAX pin and the ground. As shown in Figure 5, the RT8807/A uses an external resistor R_{IMAX} to set a programmable over current trip point. Once the voltage across the R_{IMAX} exceeds the threshold V_{OCP}, the OCP function will be triggered. The following equation provides the calculation of the R_{IMAX} value for a given maximum inductor current. If necessary, a small ceramic capacitor is recommended to be paralleled with the resistor for noise filtering to obtain accurate over current protection.

$$R_{IMAX} = \frac{V_{OCP} \times R_{CSN}}{2 \times I_{LOAD(MAX)} \times DCR}$$

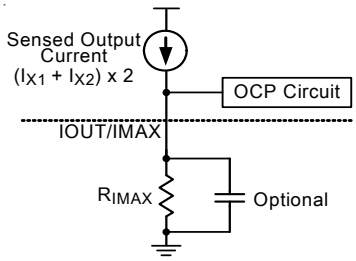


Figure 5. Over Current Protection Function

Output Voltage Droop Control and Load Line Setting

The RT8807/A supports the adaptive voltage droop control. The concept of the output voltage droop control is to set the output voltage level to be regulated slightly higher than the minimum value at light load, and somewhat lower than the maximum value at full load. As shown in Figure 6, a larger downward voltage drop during step load is allowed, which means the number of the required output capacitors can be reduced or allows the use of capacitor with higher ESR.

As a result, the full window of output voltage tolerance can be used during the transient period (see Figure 7), which reduces the overall cost. Another advantage of output voltage droop control is that the output power of the converter at full load is reduced, which greatly facilitates the thermal design.

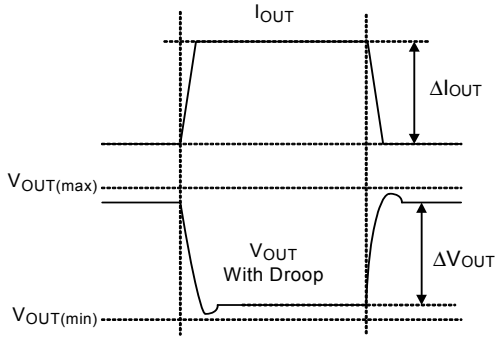


Figure 6. Output Voltage with Droop

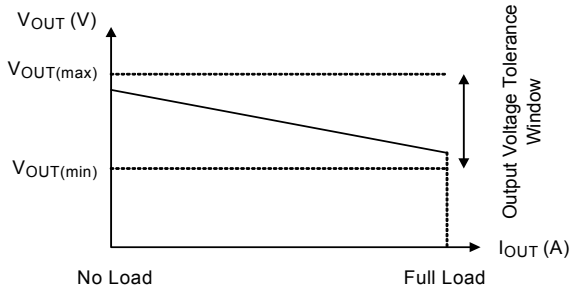


Figure 7. Load Line

The two GM amplifier output currents (I_{X1} & I_{X2}) are internally summed and doubled, and then sent to DROOP pin for droop setting. This current flows through the external resistor R_{DROOP}, which is connected between DROOP and GND.

Therefore, the voltage across R_{DROOP} becomes load-current-dependent. As shown in Figure 8, the voltage across R_{DROOP} is subtracted from the internal/external reference voltage and then sent to the positive input of the error amplifier. Therefore, the load line slope can be calculated using the following equation.

$$\text{Load line slope} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} + \frac{2 \times DCR \times R_{DROOP}}{R_{CSN}}$$

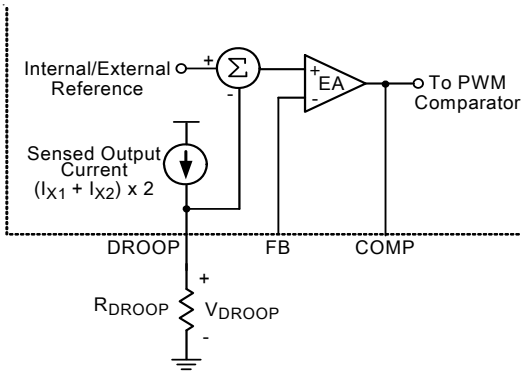


Figure 8. Output Voltage Droop Setting

Operating Phase Selection

The number of operating phase is designed to be selectable to have more flexibility in different applications. EN2B pin is used to select the number of operating phases.

After the initial turn-on of RT8807/A, an internal logic circuit checks the voltage at EN2B pin. The threshold voltage of dual-phase/single-phase operation is typically 1.15V. To set RT8807/A as the dual-phase PWM controller, the voltage at EN2B pin should be kept below 1.15V.

To set RT8807/A as a pure single-phase PWM controller, connecting EN2B pin to a voltage that is higher than 1.15V at power on. The RT8807/A then disables phase 2 (UGATE2 and LGATE2 are both held low) and operates as a single-phase PWM controller.

In addition to the selectable number of operating phase, the RT8807/A supports the operating phase transition. Notice that if the controller is set to be in dual-phase operation (voltage at EN2B pin is below the threshold), further changing the voltage at EN2B pin to be higher than the threshold will change the controller's operating state to single-phase operation. However, this operating phase transition can only be carried out one time and is NOT reversible. This means that once the controller changes its operating state from dual-phase to single-phase, it can not back to dual-phase operation no matter what the voltage change is made at EN2B pin.

Besides, also notice that if the RT8807/A is set to be in single-phase operation (voltage at EN2B pin is higher the threshold), it can not be changed to operate in dual-phase no matter what voltage change is made at EN2B pin. This dual-phase to single-phase operation transition is unidirectional.

Compensation Network Design

In order to have an accurate output voltage regulation with fast transient response, an adequate compensator design is necessary.

The RT8807/A uses a high-gain operational transconductance amplifier (OTA) as the error amplifier. As Figure 9 shows, the OTA works as the voltage controlled current source because it takes the difference of the two voltages as the input for current conversion.

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}, \text{ where } \Delta V_M = (V_{IN+}) - (V_{IN-})$$

$$\text{and } \Delta V_C = \Delta I_{OUT} \times Z_{OUT}$$

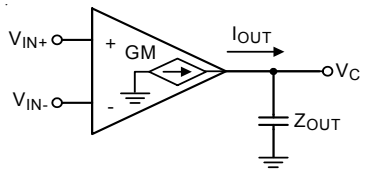


Figure 9. Operational Transconductance Amplifier, OTA

The OTA output current flows through an impedance to produce a voltage, which is referred to as the control voltage. This control voltage is then fed to the PWM modulator to compare with the sawtooth wave.

The first step of compensator design is to calculate the dc gain of the PWM modulator. Figure 10 shows the PWM modulator, which is composed of the PWM comparator, the drivers and both the high-side and low-side MOSFET. The dc gain of the modulator is calculated by the input voltage of the regulator, V_{IN}, divided by the peak-to-peak voltage of the oscillator, ΔV_{OSC}.

$$Gain_{modulator} = \frac{V_{IN}}{\Delta V_{RAMP}}$$

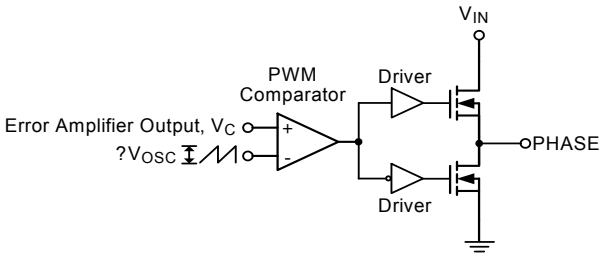


Figure 10. PWM Modulator

As shown in Figure 11, the inductor and the output capacitor together form a low-pass L-C output filter. The input to the L-C output filter is the PHASE node and the output is the regulator output. The ESR of the output capacitor plays an important role in the compensator design. The L-C filter introduces a double pole to the system transfer function with a slope of -40dB/dec above its corner frequency and a total phase lag of 180 degree. The ESR of the output capacitor introduces a zero to the system transfer function with a total phase shift of 90 degree.

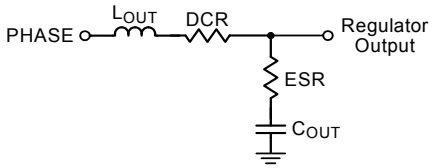


Figure 11. Inductor and Output Capacitor

The second step is therefore to calculate the frequencies of the pole and the zero. The frequency of the double pole is determined as follows.

$$F_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The frequency of the zero is determined as follows.

$$F_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

Note that the output capacitor(s) should have enough ESR to satisfy the stability requirement.

The third step is to design the compensation network. There are two kinds of compensation network: Type II and Type III, both consist of the error amplifier and the impedance network. Figure 12 shows the Type II compensator.

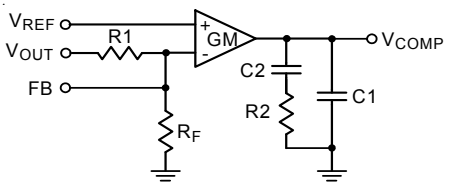


Figure 12. Type II Compensator

Figure 13 shows the Bode diagram of the Type II compensator. The frequencies of the single zero and the two poles are determined as follows.

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

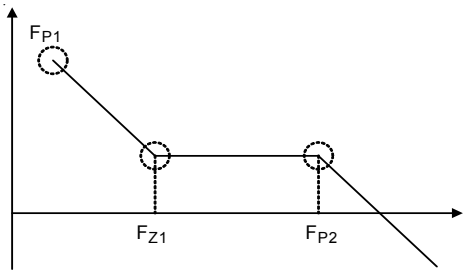


Figure 13. Gain Curve of Type II Compensator

Figure 14 shows the Bode plot of the converter's gain vs. frequency. The compensator helps to shape the profile of the gain curve with respect to frequency. The zero gives a 90° boost to the phase to counteract the phase decay of the double pole of the L-C filter. The first pole, F_{P1}, gives a shift to the gain curve in the low frequency range while the second pole, F_{P2}, provides further attenuation in the high frequency range.

In general, a converter system control loop with high bandwidth can achieve fast transient response but usually tends to lose stability. Therefore, it is always a trade-off between the control bandwidth and the system stability. Empirically, F_{Z1} is placed at about 10% lower than the double pole frequency of the L-C filter to have enough phase margin. In general, the control bandwidth should be higher than the frequency of the ESR zero but less than 1/5 of the switching frequency. In addition, the F_{P2} should be placed at half of the switching frequency.

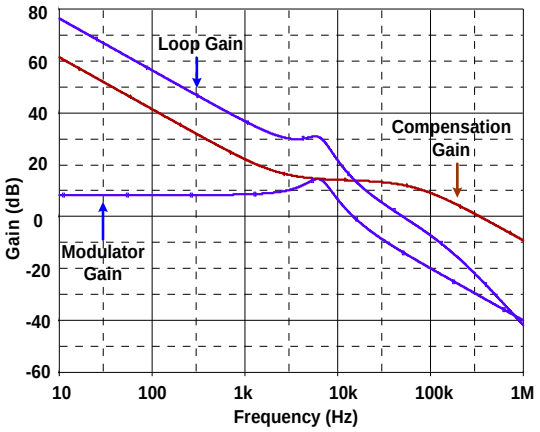


Figure 14. Converter System Bode Plot with Type II Compensator

For systems with low DCR and ESR parameters, the overall efficiency can be higher and the output voltage ripple can be lower. However, systems that have such L-C filters will experience a very sharp slope downward in the phase curve at the double pole and will be more difficult to compensate. Compared to the Type II compensator, the Type III compensator adds a pole-zero pair. The Type III compensator utilizes two zeros to give a 180° phase boost, and is usually used to compensate a converter with low ESR output capacitors (e.g. OSCON or pure MLCC) to provide the necessary phase margin for stability.

Figure 15 shows the Type III compensator, which introduces an extra pole-zero pair by inserting a series R-C circuit between the V_{OUT} node and the FB node.

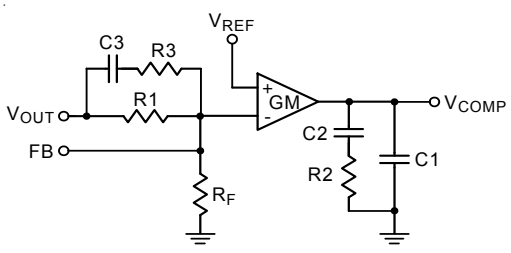


Figure 15. Type III Compensator

Figure 16 shows the Bode diagram of the Type III compensator. The frequencies of the three poles and two zeros are determined as follows.

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{P3} = \frac{1}{2\pi \times R3 \times C3}$$

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3}$$

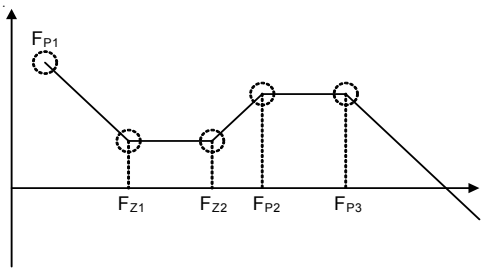


Figure 16. Gain Curve of Type III Compensator

Figure 17 shows the Bode diagram of the converter's gain vs. frequency with Type III compensator. It is recommended that F_{Z1} is placed at half of the L-C double pole, F_{Z2} is placed at the LC double pole, F_{P1} is placed at the ESR zero and F_{P2} is placed at half of the switching frequency.

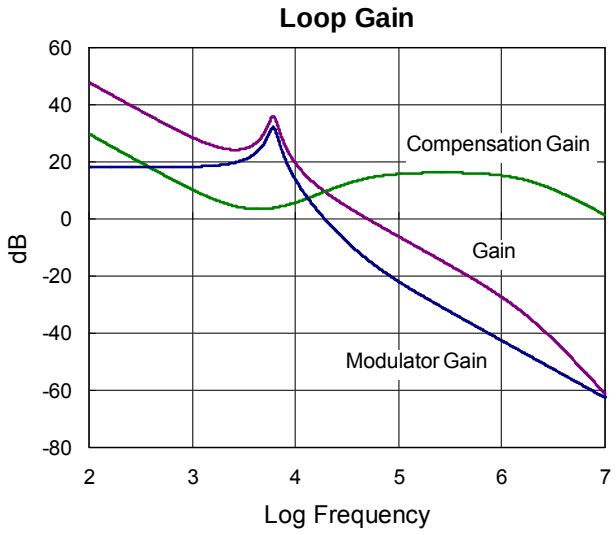


Figure 18. Converter System Bode Plot with Type III Compensator

Over Temperature Protection

The operating temperature within the chip is continuously monitored. The chip will be shut down when OTP occurs with a typical trip point of 160°C.

Power Stages

One of the most important concerns in designing a multi-phase converter is to determine the number of phases. Determining the number of phases highly depends on the overall cost, the system constraints, and usually differs case by case. The main concerns for the circuit designer include the total available board space, the type of component that can be used (through-hole/surface mount device), the maximum load current, and of the most importance, total cost. In general, the most economical solutions are those in which each phase handles a current ranging from 20A to 25A (using one high-side MOSFET and one low-side MOSFET). Design with all surface mount devices will tend toward to the lower end of this current range due to the power dissipation capability. If the power device in through-hole type is available, higher current per phase is possible. In cases where the board area is the design limitation, the current per phase can be pushed up to 40A. However, these designs require appropriate heat sinks and forced air cooling to remove the large amount of heat, which is generated by the power MOSFETs, the inductors and the PCB copper traces.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. In the low-voltage high-current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in choosing the high-side power devices.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Package Power dissipation

It is also important to consider the amount of power being dissipated in the two embedded MOSFET drivers when choosing power switches. Since there are two drives in the same package, the total power dissipation must not exceed the maximum allowable power dissipation for the VQFN package. Calculating the power dissipation in the drivers is crucial to ensure a safe operation of the controller. Exceeding the maximum allowable power dissipation will let the IC to be operated beyond the recommended maximum junction temperature of 125°C.

The maximum power dissipation for the 4x4 V/WQFN package is approximately equal to 1.923W at room temperature. The following equations provide the integrated drivers' power dissipation estimation.

$$P_D = (C_{UGATE} \times V_{BOOT-PHASE2} \times f_{SW}) + (C_{LGATE} \times V_{CC}^2 \times f_{SW})$$

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where the C_{UGATE} and the C_{LGATE} represent the C_{ISS} of the high-side MOSFET and the low-side MOSFET, respectively. From the above equations, it is clear that the junction temperature is directly proportional to the total C_{ISS} of all the external MOSFETs.

For instance, if C_{UGATE} = 1nF, C_{LGATE} = 5nF (two MOSFETs in parallel), $V_{BOOT-PHASE}$ = 5V, V_{CC} = 12V, switching frequency f_{sw} = 300kHz, the power dissipation in the driver per phase can be obtained :

$$P_D \approx 1n \times 5^2 \times 300k + 2 \times 5n \times 12^2 \times 300k = 439mW$$

Assuming the room temperature is equal to 30°C, the junction temperature for two-phase operation is :

$$T_J = 30°C + (52°C/W) \times (0.439W \times 2) = 75.6°C < 125°C,$$

which means the junction temperature is below the maximum recommended value for a safe operation.

Layout Considerations

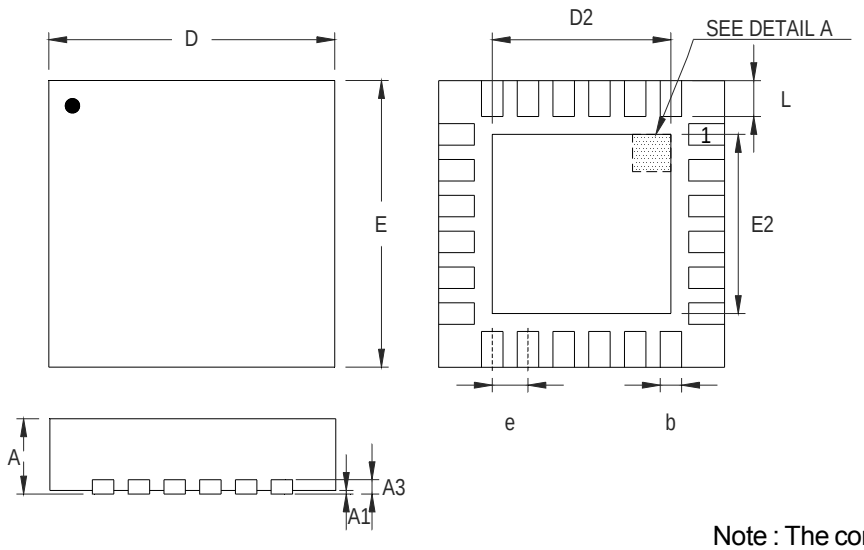
Layout plays a critical role in modern high-frequency switching converter design. Circuit board with careful layout can help the IC function properly and achieve low losses, low switching noise, and stable operation with improved performance. Without a carefully layout, the PCB could radiate excessive noise, causing noise-induced IC problems and then contribute to the converter instability. The following guidelines can be used to achieve optimal IC performance.

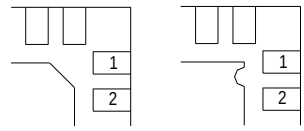
1. Power components should be placed first. Place the input capacitors close to the power MOSFETs, then locate the filter inductors and output capacitors between the power MOSFETs and the load.
2. Place both the ceramic and bulk input capacitor close to the drain pin of the high-side MOSFET. This can reduce the impedance presented by the input bulk capacitance at high switching frequency. If there is more than one high-side MOSFET in parallel, each should have its own individual ceramic capacitor.
3. Keep the power loops as short as possible. For low-voltage high-current applications, power components are the most critical part in the layout because they switch a large amount of current. The current transition from one device to another at high speed causes voltage spikes due to the parasitic components on the circuit board. Therefore, all of the high-current switching loops should be kept as short as possible with large and thick copper traces to minimize the radiation of electromagnetic interference.
4. Minimize the trace length between the power MOSFETs and its drivers.

Since the drivers use short, high-current pulses to drive the power MOSFETs, the driving traces should be sized as short and large as possible to reduce the trace inductance. This is especially true for the low-side MOSFET, since this can reduce the possibility of the shoot-through.

5. Provide enough copper area around the power MOSFETs and the inductors to aid in heat sinking. Use thick copper PCB to reduce the resistance and inductance for improved efficiency.
6. The bank of output capacitor should be placed physically close to the load. This can minimize the impedance seen by the load, and then improves the transient response.
7. Place all of the high-frequency decoupling ceramic capacitors close to their decoupling targets.
8. Small signal components should be located as close as possible to the IC. The small signal components include the feedback components, current sensing components, the compensation components, function setting components and any bypass capacitors. These components belong to the high-impedance circuit loop and are inherently sensitive to noise pick-up. Therefore, they must be located close to their respective controller pins and away from the noisy switching nodes.
9. A multi-layer PCB design is recommended. Make use of one single layer as the power ground and have a separate control signal ground as the reference of all signals.

Outline Dimension





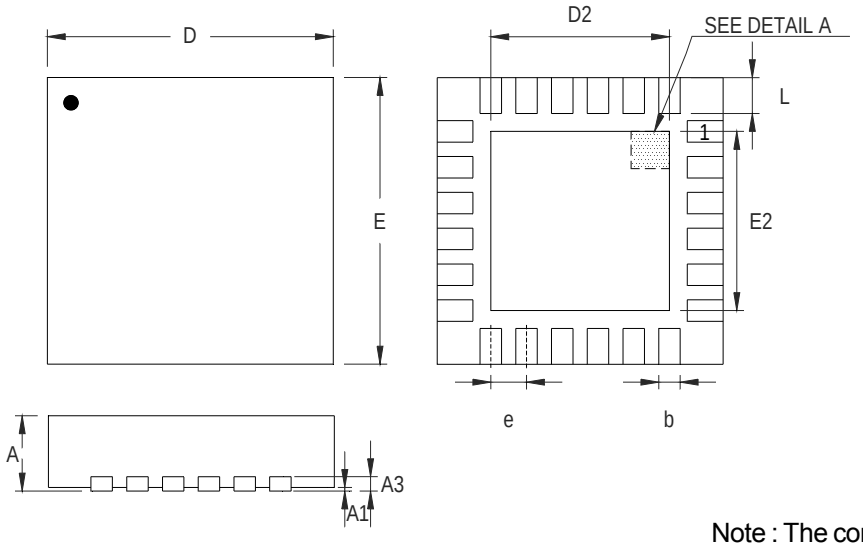
DETAIL A

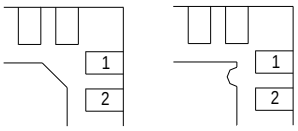
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 24L QFN 4x4 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	2.300	2.750	0.091	0.108
E	3.950	4.050	0.156	0.159
E2	2.300	2.750	0.091	0.108
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

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