VRM8.5 PWM and Triple Linear Power System Controller

General Description

The RT9238 is a 4-in-one power controller optimized for high-performance microprocessor and computer applications. The IC integrates a PWM controller, triple linear controller as well as monitoring and protection functions into a 28-pin SOP package. The PWM controller regulates the microprocessor core voltage with a synchronous buck converter. The first linear controller supplies the computer system's AGTL+ 1.2V bus power. The second linear controller provides power for the 1.5V AGP bus and the 3rd linear controller provides 1.8V power for the chipset core voltage and/or cache memory circuits.

The RT9238 features an Intel VRM8.5 compatible, TTL 5-bit programmable DAC that adjusts the core voltage from 1.090V to 1.865V in 25mV steps. The 5-bit DAC has a typical ±1% tolerance. The linear regulators provide fixed output voltages of 1.2V (V_{OUT2}), 1.5V (V_{OUT3}) and 1.8V (V_{OUT4}) or user-adjustable with an internal 1.265V reference. All the three linear regulators drive external N-MOSFET or NPNs bipolar for the pass transistor.

The RT9238 monitors all the output voltages. A power-good signal is issued when the core voltage is within ±10% of the DAC setting and the other levels are above their under-voltage levels. Additional build-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltage above 115% of the DAC setting. The PWM over-current function monitors the output current using the voltage drop across the MOSFET's $R_{DS(ON)}$, which eliminates the need for a current sensing resistor.

Applications

- Motherboard Power Regulation for Computers

Features

- **4-in-one Regulated Voltages for Microprocessor Core, AGTL+ Bus, AGP Bus Power, and North/South Bridge Core**
- **Compatible with ISL6524**
- **Power-good Output Voltage Monitor**

Switching section

- **VRM8.5 TTL-Compatible 5-bit DAC Programmable from 1.090V to 1.865V**
- **±1% DAC Accuracy**
- **Fast Transient Response**
- **VRM 8.5 Voltage Droop Tuning Uses MOSFET $R_{DS(ON)}$**
- **Fixed 200KHz Switching Frequency**
- **Adaptive Non-overlapping Gate Driver**
- **Over-current Monitor Uses MOSFET $R_{DS(ON)}$**
- **Over-voltage Protection Uses Lower MOSFET**

Linear Section

- **Fixed or User-adjustable Linear Regulator Output Voltage**
- **MOSFET and NPN Driving Capability**
- **Ultra Fast Response Speed**
- **Under-voltage Protection**
- **Internal Thermal Shutdown**

Pin Configurations

Part Number	Pin Configurations
RT9238CS (Plastic SOP-28)	TOP VIEW DRIVE2 [1] — [28] VCC FIX [2] — [27] UGATE1 VID3 [3] — [26] PHASE1 VID2 [4] — [25] LGATE1 VID1 [5] — [24] PGND VID0 [6] — [23] OCSET1 VID25 [7] — [22] FB1 PGOOD [8] — [21] VDAC VTTPG [9] — [20] ICOMP FAULT/VID4 [10] — [19] VSEN3 VSEN2 [11] — [18] DRIVE3 SS24 [12] — [17] GND SS13 [13] — [16] VAUX VSEN4 [14] — [15] DRIVE4

Ordering Information

RT9238☐ ☐
 └─Package type
   S : SOP-28

 └─Operating temperature range
   C: Commercial standard

Typical Application Circuit
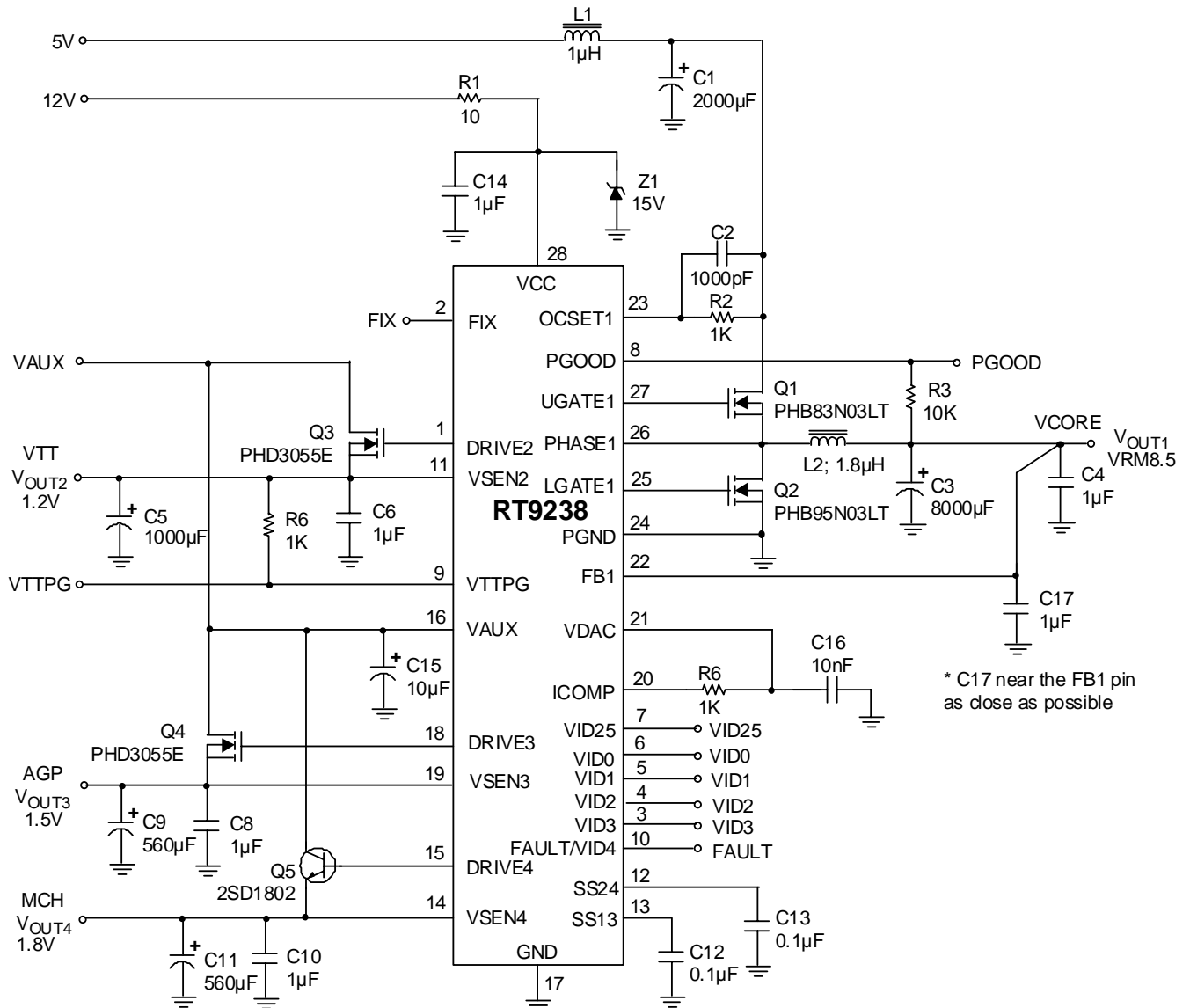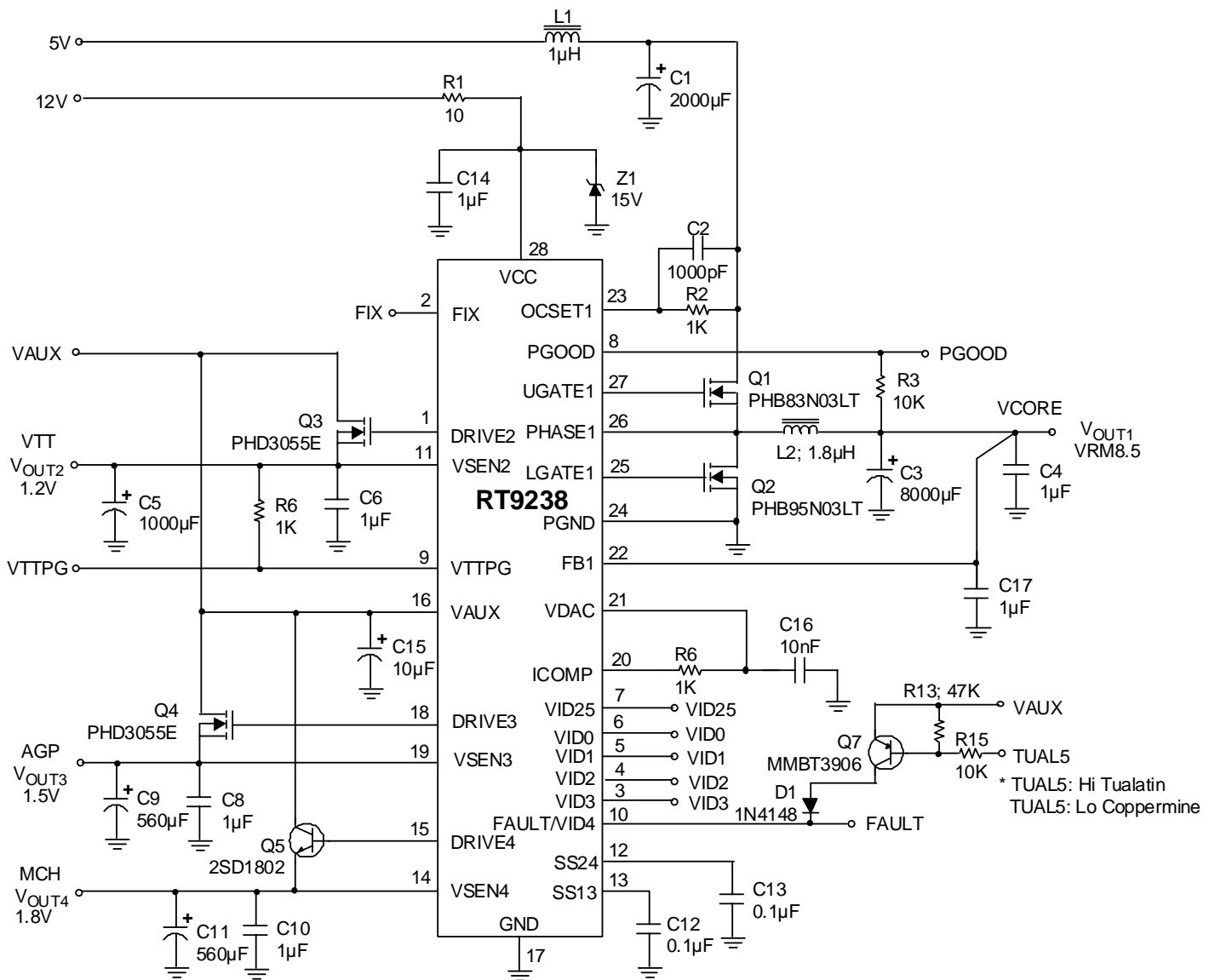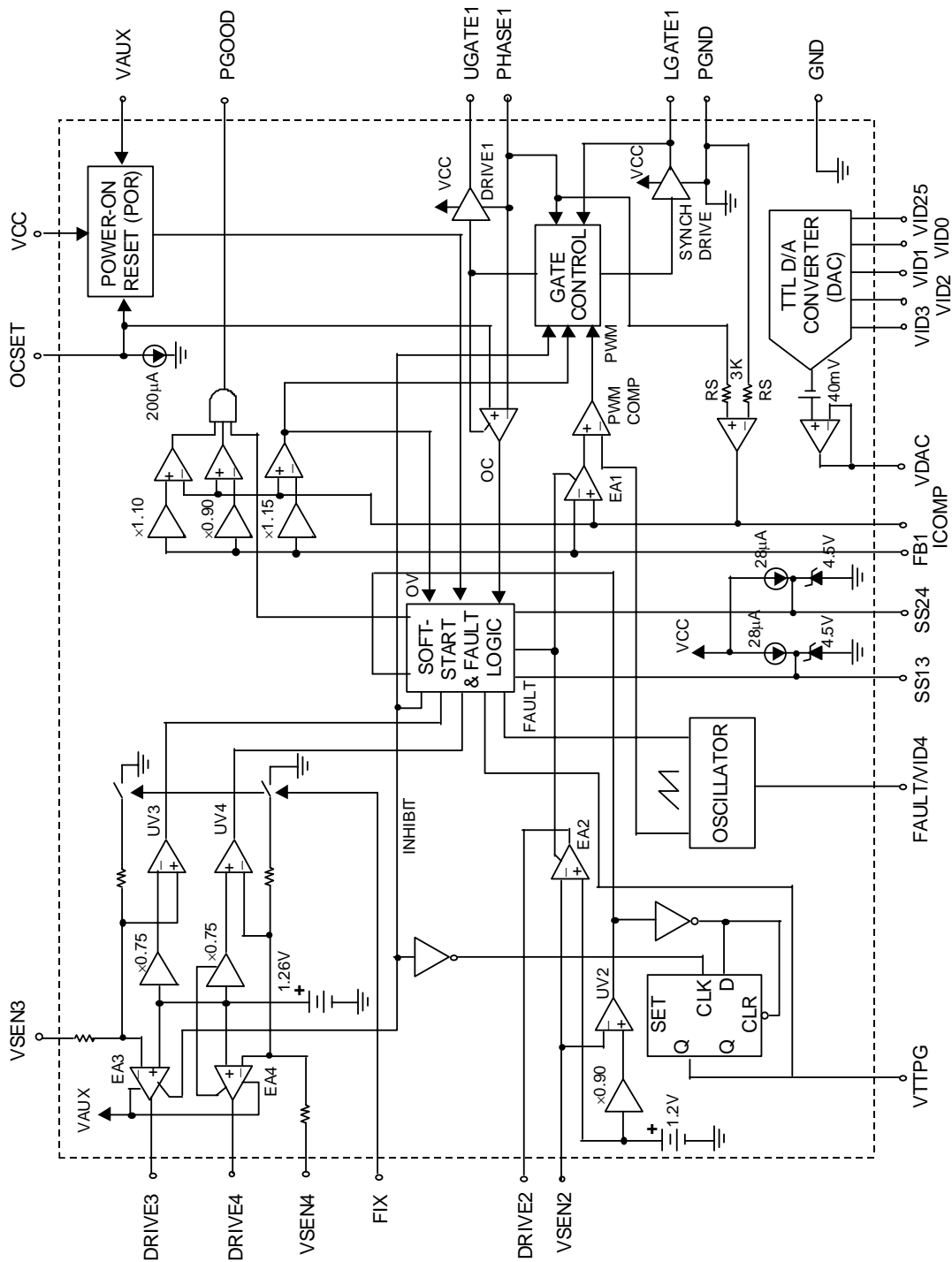

Fig.1 VRM 8.5 Power Solution

Fig.2 VRM 8.4 & 8.5 Power Solution

Function Block Diagram

Absolute Maximum Ratings

- Supply Voltage --- +15V
- FAULT/VID4 and GATE Voltage -- GND−0.3V ~ V_{CC}+0.3V
- Input, Output or I/O Voltage -- GND−0.3V ~ 7V
- Ambient Temperature Range --- 0°C ~ +70°C
- Operating Junction Temperature Range -------------------------------------- 0°C ~ +125°C
- Storage Temperature Range --- −65°C ~ +150°C
- Lead Temperature (Soldering, 10 sec.) ------------------------------------- 300°C
- Package Thermal Resistance
  SOP-28, θ_{JA} --- 60°C/W

Recommended Operating Conditions

- Supply Voltage --- +12V±10%
- Ambient Temperature Range --- 0°C to 70°C
- Junction Temperature Range -- 0°C to 125°C

CAUTION:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(V_{CC} = 12V, PGND = 0V, T_A = 25°C, Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Current						
Nominal Supply Current	I_{CC}	UGATE1, LGATE1, DRIVE2, DRIVE3, and DRIVE4 Open	--	10	--	mA
Power-On Reset						
VCC Rising Threshold		V_{OCSET1} = 4.5V	6.5	--	9.5	V
VCC Falling Threshold		V_{OCSET1} = 4.5V	6	--	9	V
Rising VAUX Threshold		V_{OCSET1} = 4.5V	--	1.5	--	V
VAUX Threshold Hysteresis		V_{OCSET1} = 4.5V	--	0.2	--	V
Rising V_{OCSET1} Threshold			--	1.25	--	V
DAC AND Band Gap Reference						
DAC (VID25-VID3) Input Low Voltage			--	--	0.8	V
DAC(VID25-VID3) Input High Voltage			2.0	--	--	V
DACOUT Voltage Accuracy		VDAC + 40mV	-10	--	+20	mV
Oscillator						
Free Running Frequency			180	200	225	KHz
Ramp Amplitude	ΔV_{OSC}		--	1.9	--	V_{P-P}

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Linear Regulators (V$_{OUT2}$, V$_{OUT3}$, and V$_{OUT4}$)						
VSEN3,4 Voltage Regulation	V$_{REG2,3,4}$	FIX = 0V	1.240	1.265	1.290	V
VSEN2 Regulation Voltage	V$_{REG2}$		1.180	1.200	1.240	V
VSEN3 Regulation Voltage	V$_{REG3}$	FIX = open	1.455	1.500	1.545	V
VSEN3 Bias Current	IB$_{VSEN3}$	FIX = open	--	260	--	μA
VSEN4 Regulation Voltage	V$_{REG4}$	FIX = open	1.746	1.800	1.854	V
VSEN4 Bias Current	IB$_{VSEN4}$	FIX = open	--	350	--	μA
Under-Voltage Level (All Linears) (VSEN/VREG)		VSEN3,4 Rising	--	75	--	%
Under-Voltage Hysteresis (All Linears) (VSEN/VREG)		VSEN3,4 Falling	--	100	--	mV
Output Drive Current (All Linears)		VAUX − V$_{DRIVER2,3,4}$ > 0.6V	20	40	--	mA
Synchronous PWM Controller Error Amplifier						
DC Gain			--	65	--	dB
PWM Controller Gate Driver						
UGATE Source	R$_{UGATE1}$	VCC = 12V VCC-V$_{UGATE1}$ = 1V	--	4	7	Ω
UGATE Sink	R$_{UGATE1}$	V$_{UGATE1}$ = 1V	--	3	7	Ω
LGATE Source	I$_{LGATE1}$	VCC = 12V, V$_{LGATE1}$ = 2V	--	1	--	A
LGATE Sink	R$_{LGATE1}$	V$_{LGATE1}$ = 1V	--	2	6	Ω
Protection						
V$_{OUT1}$ Over-Voltage Trip		FB1 Rising	112	118	125	%
FAULT Souring Current		V$_{FAULT}$ = 8V	5	10	--	mA
OCSET1 Current Source	I$_{OCSET}$	V$_{OCSET1}$ = 4.5V	170	200	230	μA
Soft-Start Current	I$_{SS13,24}$	V$_{SS13,SS24}$ = 2V	--	28	--	μA
Power Good						
V$_{OUT1}$ Upper Threshold		FB1 Rising	108	--	112	%
V$_{OUT1}$ Under Voltage		FB1 Rising	87	--	92	%
V$_{OUT1}$ Hysteresis (FB1/DACOUT)		Upper/Lower Threshold	--	2	--	%
VTTPG Upper Threshold		VSEN2 Rising	--	1.08	--	V
VTTPG Delay Threshold		SS13 Rising	--	1.25	--	V
VTTPG Voltage Low	V$_{VTTPG}$	I$_{VTTPG}$ = -4mA	--	--	0.5	V
PGOOD Voltage Low	V$_{PGOOD}$	I$_{PGOOD}$ = -4mA	--	--	0.5	V

Typical Operating Charateristics

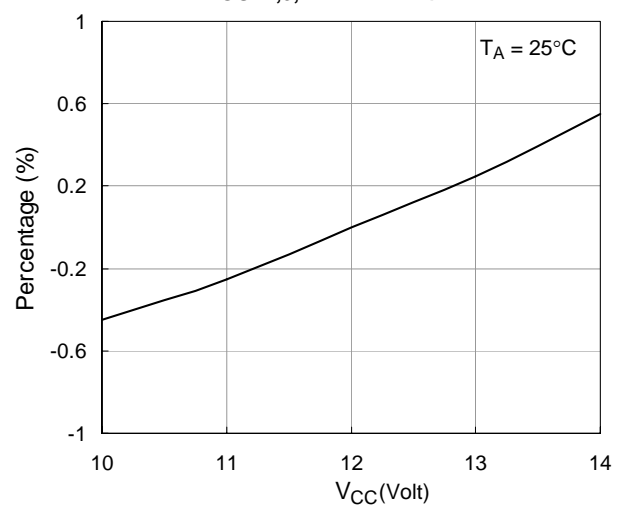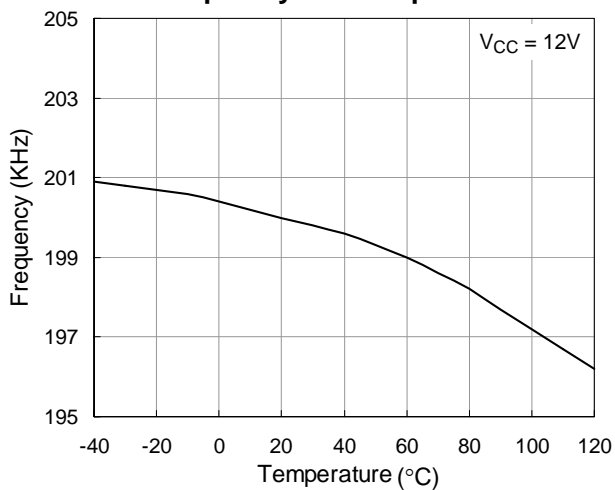### Frequency vs. V_CC
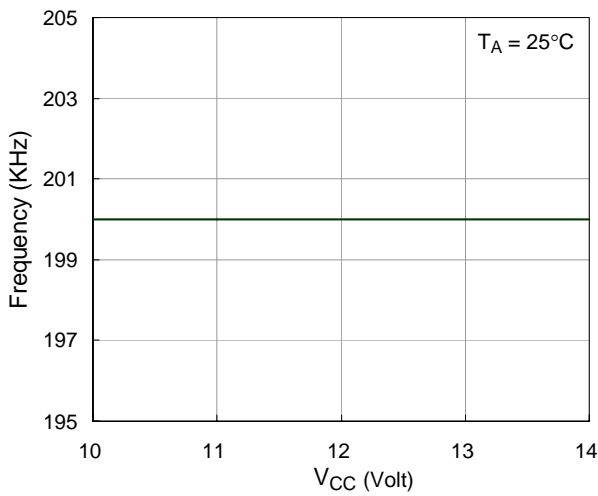
I_OCSET1 vs. V_CC
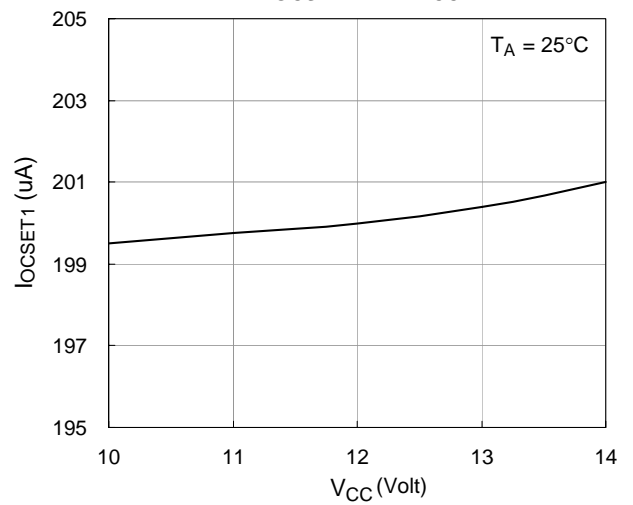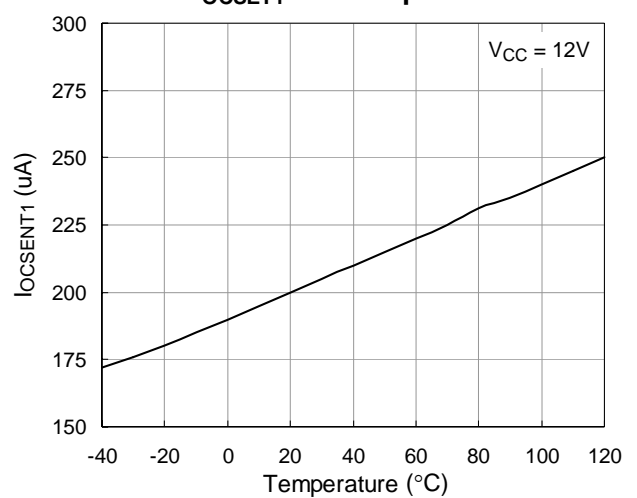

V_OUT1 Line Regulation
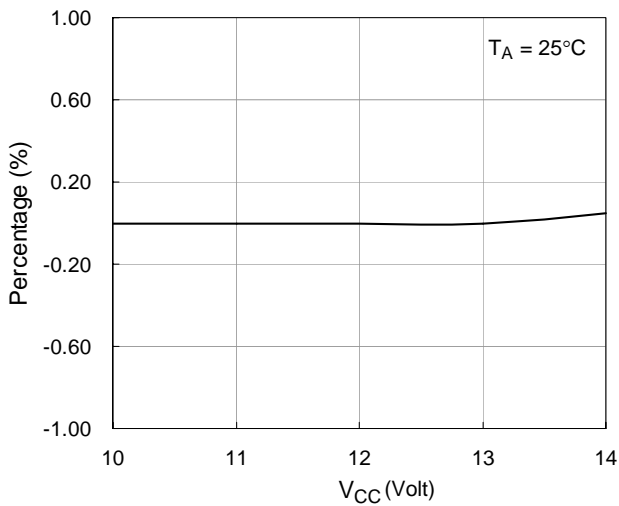
V_OUT2,3,4 Line Regulation

Frequency vs. Temperature

I_OCSET1 vs. Temperature

DS9238-01   July 2001

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V_{OUT1} vs. Temperature

$V_{CC} = 12V$

V_{OUT2,3,4} vs. Temperature

$V_{CC} = 12V$

Dead Time

UGATE1

LGATE1

1) Ch 1:   2 Volt 50 ns
2) Ch 2:   2 Volt 50 ns

Time

Dead Time

UGATE1

LGATE1

1) Ch 1:   2 Volt 50 ns
2) Ch 2:   2 Volt 50 ns

Time

V_{OUT2,3,4} Short

FAULT

SS13,24

1) Ch 1:   5 Volt 25 ms
2) Ch 2:   2 Volt 25 ms

Time

V_{OUT1} Short

UGATE1

LGATE1

SS13,24

1) Ch 1:   5 Volt 25 ms
2) Ch 2:   2 Volt 25 ms
3) Ref A: 5 Volt 25 ms
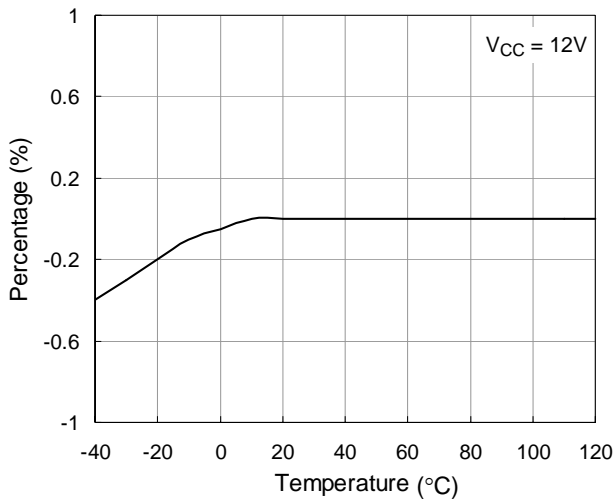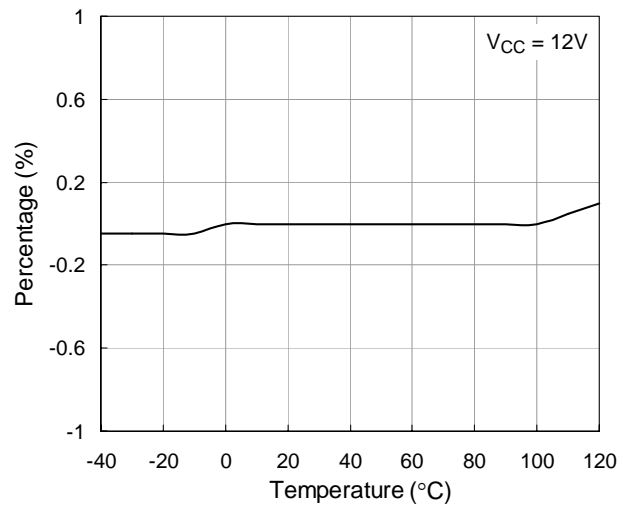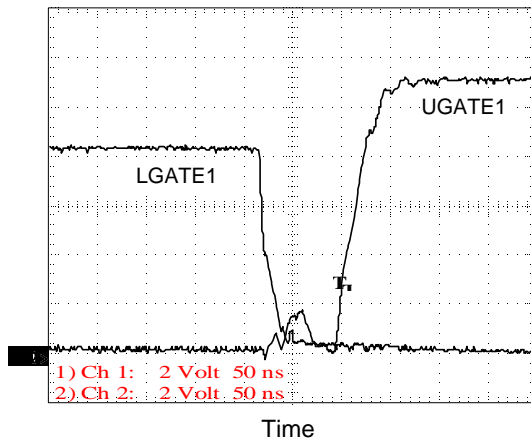
Time
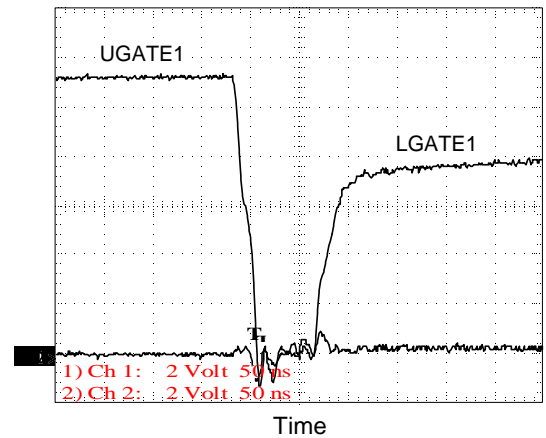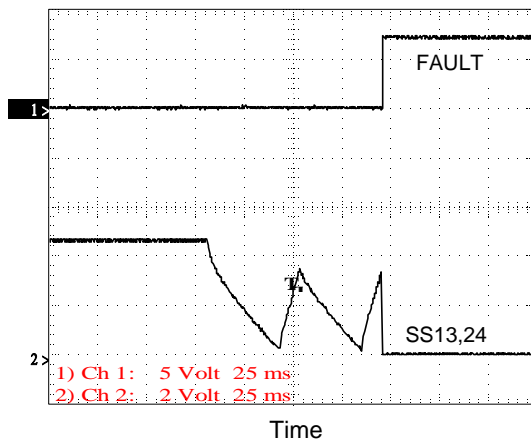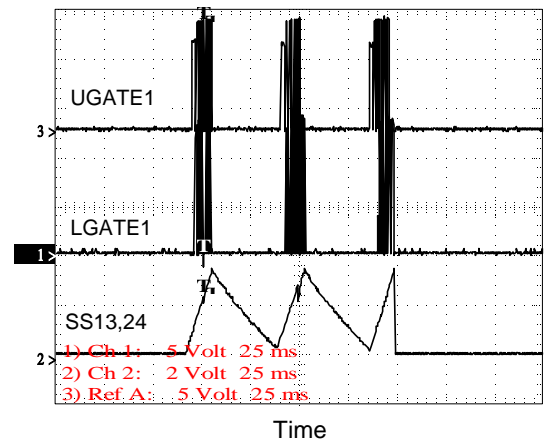
Functional Pin Description

DRIVE2 (Pin 1)

Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the VTT (V$_{OUT2}$) regulator's pass transistor.

FIX (Pin 2)

Grounding this pin bypasses the internal resistor dividers that set the voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.26V up to the input voltage (+3.3V or +5V) by way of an external resistor divider corrected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times (1 + \frac{R_{OUT}}{R_{GND}})$$

Where R$_{OUT}$ is the resistor connected from VSEN to the output of the regulator, and R$_{GND}$ is the resistor connected from VSEN to ground. Left open, this pin is pulled high enabling fixed output voltage operation.

VID25, VID0, VID1, VID2, VID3 (Pin 7, 6, 5, 4, and 3)

VID3-25 are TTL-compatible the input pins to the 5-bit DAC. The state logic of these five pins program the internal voltage reference, DACOUT. The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage of 32 combinations of VID levels.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the PWM converter output voltage. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage, or when any of the other outputs are below their under-voltage thresholds.

VTTPG (Pin 9)

VTTPG is an open collector output used to indicate the status of the VTT (V$_{OUT2)}$ regulator output voltage. This pin is pulled low when the output voltage is below 1.08V under-voltage threshold or

when SS13 pin is below 1.25V.

FAULT/VID4 (Pin 10)

This pin provides two combined functions. One is fault condition indicator, the other is VID4 for VRM8.4 DAC (see the Table I). Pull up this pin up to over 2V, it act like the VID4 of VRM8.4. When this pin is pulled high, the DACOUT provide 1.890V~2.090V output voltages.

Nominally, the voltage at this pin is pulled low by a internal 47kΩ, in the event of an over-voltage or over-current condition, this pin is internally pulled to about 8V (VCC = 12V).

VSEN2 (Pin 11)

Connect this pin to the output of the VTT (V$_{OUT2}$) linear regulator. This pin is also monitored for under-voltage events.

SS24 (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28μA (V$_{SS24}$>1V) current source, sets the soft-start interval of the V$_{OUT2}$ regulator. Pulling this pin below 0.8V induces a chip reset and shutdown.

SS13 (Pin 13)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28μA (V$_{SS13}$>1V) current source, sets the soft-start interval of the synchronous PWM converter (V$_{OUT1}$) and the AGP regulator (V$_{OUT3}$). A VTTPG high signal is also delayed by the time interval required by the charging of this capacitor from 0V to 1.25V.

VSEN4 (Pin 14)

Connect this pin to the output of the 1.8V regulator. This pin is monitored for under-voltage events.

DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.8V regulator's pass transistor.

VAUX (Pin 16)

This pin provides boost current for the three linear regulator output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for power-on reset (POR) purpose.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

DRIVE3 (Pin 18)

Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.5V regulator's pass transistor.

VSEN3 (Pin 19)

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for under-voltage events.

ICOMP (Pin 20)

This pin is non-inverting input of the PWM error amplifier. It determine the V_{OUT1} voltage. Connect a resistor (RF) to VDAC pin. A sense current of lower MOSFET is fed to this pin to pull low the DACOUT voltage. (see VDAC)

VDAC (Pin 21)

This pin is internal DAC buffer output. Connect a resistor(RF) from this pin to ICOMP pin. The resistor provide a voltage drop rated from lower MOSFET turn on voltage drop. A sample hold circuit sense the voltage drop of lower MOSFET(I_L x R_{DSON}) when LGATE1 turn on. The ratio is :

$$(I_L \times R_{DSON}) \times RF/3k$$

FB1 (Pin 22)

This pin is connected to the PWM converter's output voltage. This pin also connects to internal PWM error amplifier inverting input and power good monitor.

OCSET1 (Pin 23)

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200μA current source, and the upper MOSFET on-resistance set the converter over-current trip point.

An over-current trip cycles the soft-start function. The voltage at this pin is monitored for power-on reset (POR) purpose and pulling this pin low with an open drain device will shut down the IC.

PGND (Pin 24)

This is the power ground of UGATE1&LGATE1. Tie the synchronous PWM converter's lower MOSFET source to this pin.

LGATE1 (Pin 25)

Connect LGATE1 to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

PHASE1 (Pin 26)

This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection. This pin is also used to sense lower MOSFET voltage drop for V_{OUT1} voltage droop tuning.

UGATE1 (Pin 27)

Connect UGATE1 pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

VCC (Pin 28)

Provide a 12V supply voltage for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin monitored for power-on reset (POR) purpose.

Functional Description

Operation

The RT9238 monitors and precisely controls 4 output voltage levels (Refer to Figures 1, 2, and function block). It is designed for microprocessor computer applications with 3.3V, 5V, and 12V bias input from an ATX power supply. The IC has one PWM and three linear controllers. The PWM controller is designed to regulate the microprocessor core voltage (V_{OUT1}). The PWM controller drives 2 MOSFETs (Q1 and Q2) in a synchronous-rectified buck converter configuration and regulates the core voltage to a level programmed by the 5-bit digital-to-analog converter (DAC). The first linear controller (EA2) is designed to provide the AGTL+ bus voltage (V_{OUT2}) by driving a MOSFET (Q3) pass element to regulate the output voltage to a level of 1.2V. The remaining two linear controllers (EA3 and EA4) supply the 1.5V advanced graphics port (AGP) bus power (V_{OUT3}) and the 1.8V chipset core power (V_{OUT4}).

Initialization

The RT9238 automatically initializes in ATX-based systems upon receipt of input power. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage ($+12V_{IN}$) at the VCC pin, the 5V input voltage ($+5V_{IN}$) at the OCSET pin, and the 3.3V input voltage ($+3.3V_{IN}$) at the VAUX pin. The normal level on OCSET is equal to $+5V_{IN}$ less a fixed voltage drop (see over-current protection). The POR function initiates soft-start operation after all supply voltages exceed their POR thresholds.

Soft-Start

The 1.8V supply designed to power the chipset (OUT4), cannot lag the ATX 3.3V by more than 2V, at any time. To meet this special requirement, the linear block controlling this output operates independently of the chip's power-on reset. Thus, DRIVE4 is driven to raise the OUT4 voltage before the input supplies reach their POR levels. As seen in Fig.3, at time T0 the power is turned on and the

input supplies ramp up. Immediately following, OUT4 is also ramped up, lagging the ATX 3.3V by about 1.8V. At time T1, the POR function initiates the SS24 soft-start sequence. Initially, the voltage on the SS24 pin rapidly increases to approximately 1V (this minimizes the soft-start interval). Then, an internal 28μA current source charges an external capacitor (C_{SS24}) on the SS24 pin to about 4.5V. As the SS24 voltage increases, the EA2 error amplifier drives Q3 to provide a smooth transition to the final set voltage. The OUT4 reference (clamped to SS24) increasing past the intermediary level, established based on the ATX 3.3V presence at the VAUX pin, brings the output in regulation soon after T2.

As OUT2 increases past the 90% power-good level, the second soft-start (SS13) is released. Between T2 and T3, the SS13 pin voltage ramps from 0V to the valley of the oscillator's triangle wave (at 1.25V). Contingent upon OUT2 remaining above 1.08V, the first PWM pulse on PHASE1 triggers the VTTPG pin to go high. The oscillator's triangular wave form is compared to the clamped error amplifier output voltage. As the SS13 pin voltage increases, the pulse-width on the PHASE1 pin increases, bringing the OUT1 output within regulation limits. Similarly, the SS13 voltage clamps the reference voltage for OUT3, enabling a controlled output voltage ramp-up. At time T4, all output voltages are within power-good limits, situation reported by the PGOOD pin going high.

The T2 to T3 time interval is dependent upon the value of C_{SS13}. The same capacitor is also responsible for the ramp-up time of the OUT1 and OUT3 voltages. If selecting a different capacitor then recommended in the circuit application literature, consider the effects the different value will have on the ramp-up time and inrush currents of the OUT1 and OUT3 outputs.
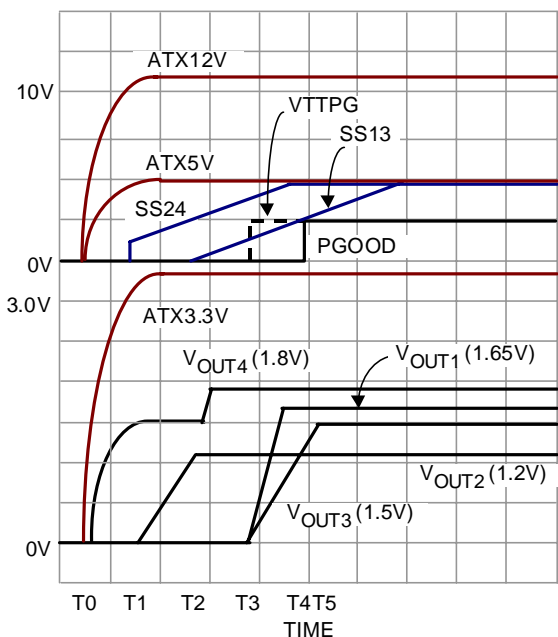
Fig.3 Soft-start Interval

Fault Protection

All four outputs are monitored and protected against extreme overload. The chip's response to an output overload is selective, depending on the faulting output.

An over-voltage on V_{OUT1} output (FB1) disables outputs 1, 2, and 3, and latches the IC off. An under-voltage on V_{OUT4} output latches the IC off. A single over-current event on output 1, or an under-voltage event on output 2 or 3, increments the respective fault counters and triggers a shutdown of outputs 1, 2, and 3, followed by a soft-start re-start. After three consecutive fault events on either counter, the chip is latched off. Removal of bias power resets both the fault latch and the counters. Both counters are also reset by a successful start-up of all the outputs.

Fig.3 shows a simplified schematic of the fault logic. The over-current latches are set dependent upon the states of the over-current (OC1), output 2 and 3 under-voltage (UV2, UV3) and the soft-start signals (SS13, SS24). Window comparators monitor the SS pins and indicate when the respective C_{SS} pins are fully charged to above 4.0V (UP signals). An under-voltage on either linear output (VSEN2, VSEN3, or

VSEN4) is ignored until the respective UP signal goes high. This allows V_{OUT3} and V_{OUT4} to increase without fault at start-up. Following an over-current event (OC1, UV2, or UV3 event), bringing the SS24 pin below 0.8V resets the over-current latch and generates a soft-started ramp-up of the outputs 1, 2, and 3.
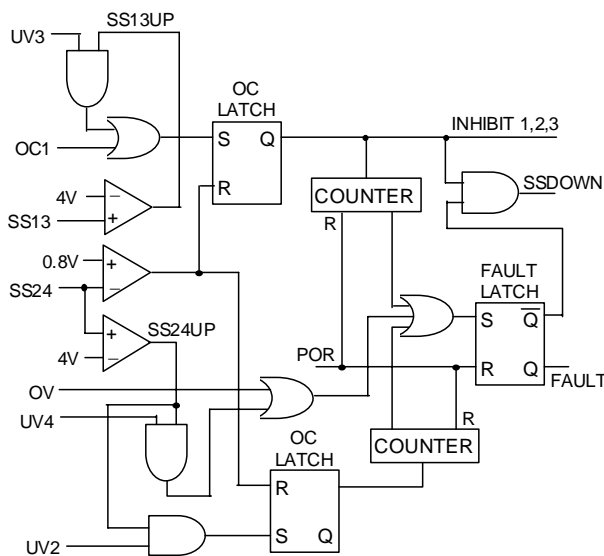

Fig.4 Fault Logic-simplified Schematic

OUT1 Over-Voltage Protection

During operation, a short across the synchronous PWM upper MOSFET (Q1) causes V_{OUT1} to increase. When the output exceeds the over-voltage threshold of 115% of DACOUT, the over-voltage comparator trips to set the fault latch and turns the lower MOSFET (Q2) on. This blows the input fuse and reduces V_{OUT1}.

A separate over-voltage circuit provides protection during the initial application of power. For voltages on the VCC pin below the power-on reset (and above ~4V), the output level is monitored for voltages above 1.3V. Should FB1 exceed this level, the lower MOSFET, Q2, is driven on.

Over-Current Protection

All outputs are protected against excessive over-currents. The PWM controller uses the upper

MOSFET's on-resistance, $R_{DS(ON)}$ to monitor the current for protection against a shorted output. All linear regulators monitor their respective VSEN pins for under-voltage to protect against excessive currents.

Fig.5 illustrates the over-current protection with an overload on OUT1. The overload is applied at T0 and the current increases through the inductor (L_{OUT1}). At time T1, the OC1 comparator trips when the voltage across Q1 ($i_D \bullet R_{DS(ON)}$) exceeds the level programmed by R_{OCSET} . This inhibits outputs 1, 2, and 3, discharges the soft-start capacitor C_{SS24} with 28μA current sink, and increments the counter. Soft-start capacitor C_{SS13} is quickly discharged. C_{SS13} starts ramping up at T2 and initiates a new soft-start cycle. With OUT2 still overloaded, the inductor current increases to trip the over-current comparator. Again, this inhibits the outputs, but the C_{SS24} soft-start voltage continues increasing to above 4.0V before discharging. Soft-start capacitor C_{SS13} is, again, quickly discharged. The counter increments to 2. The soft-start cycle repeats at T3 and trips the over-current comparator. The SS24 pin voltage increases to above 4.0V at T4 and the counter increments to 3. This sets the fault latch to disable the converter.
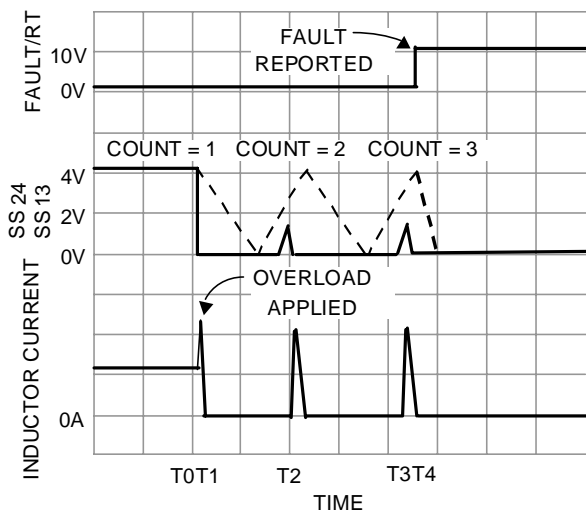

Fig.5 Over-current Operation

The three linear controllers monitor their respective VSEN pins for under-voltage. Should excessive currents cause VSEN3 or VSEN4 to fall below the linear under-voltage threshold, the respective UV signals set the OC latch or the FAULT latch, providing respective C_{SS} capacitors are fully charged. Blanking the UV signals during the C_{SS} charge interval allows the linear outputs to build above the under-voltage threshold during normal operation. Cycling the bias input power off then on resets the counter and the fault latch.

An external resistor (R_{OCSET}) programs the over-current trip level for the PWM converter. As shown in Fig.6, the internal 200μA current sink (I_{OCSET}) develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the over-current comparator (OC). When the voltage across the upper MOSFET ($V_{DS(ON)}$) exceeds V_{SET}, the over-current comparator trips to set the over-current latch. Both V_{SET} and V_{DS} are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

The OC trip point varies with MOSFET's $R_{DS(ON)}$ temperature variations. To avoid over-current tripping in the normal operating load range, determine the ROCSET resistor value from the equation above with:

1. The maximum $R_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{OCSET} from the specification table
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection'.
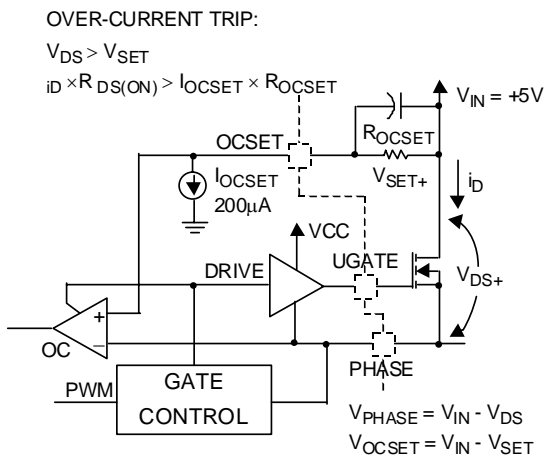
OVER-CURRENT TRIP:

$V_{DS} > V_{SET}$

$i_D \times R_{DS(ON)} > I_{OCSET} \times R_{OCSET}$

Fig.6 Current Limiting Setting

OUT1 Voltage Program

The output voltage of the PWM converter is programmed to discrete levels between 1.090V and

1.865V which are shifted high 40mV from 1.050V to 1.825V for voltage droop gap tuning. This output (OUT1) is designed to supply the core voltage of Intel's advanced microprocessors. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, since they are internally pulled to the VAUX pin through 5KΩ resistors. Changing the VID inputs during operation is not recommended and could toggle the PGOOD signal and exercise the over-voltage protection. The output voltage program is Intel VRM8.5 compatible.

Table 1. VOUT1 Voltage Program

Pin Name						Normal OUT1 Voltage
VID4	VID3	VID2	VID1	VID0	VID25	DACOUT
0	0	1	0	0	0	1.050+40mV=1.090
0	0	1	0	0	1	1.075+40mV=1.115
0	0	0	1	1	0	1.100+40mV=1.140
0	0	0	1	1	1	1.125+40mV=1.165
0	0	0	1	0	0	1.150+40mV=1.190
0	0	0	1	0	1	1.175+40mV=1.215
0	0	0	0	1	0	1.200+40mV=1.240
0	0	0	0	1	1	1.225+40mV=1.265
0	0	0	0	0	0	1.250+40mV=1.290
0	0	0	0	0	1	1.275+40mV=1.315
0	1	1	1	1	0	1.300+40mV=1.340
0	1	1	1	1	1	1.325+40mV=1.365
0	1	1	1	0	0	1.350+40mV=1.390
0	1	1	1	0	1	1.375+40mV=1.415
0	1	1	0	1	0	1.400+40mV=1.440
0	1	1	0	1	1	1.425+40mV=1.465
0	1	1	0	0	0	1.450+40mV=1.490
0	1	1	0	0	1	1.475+40mV=1.515
0	1	0	1	1	0	1.500+40mV=1.540

To be continued

Pin Name						Normal OUT1 Voltage
VID4	VID3	VID2	VID1	VID0	VID25	DACOUT
0	1	0	1	1	1	1.525+40mV=1.565
0	1	0	1	0	0	1.550+40mV=1.590
0	1	0	1	0	1	1.575+40mV=1.615
0	1	0	0	1	0	1.600+40mV=1.640
0	1	0	0	1	1	1.625+40mV=1.665
0	1	0	0	0	0	1.650+40mV=1.690
0	1	0	0	0	1	1.675+40mV=1.715
0	0	1	1	1	0	1.700+40mV=1.740
0	0	1	1	1	1	1.725+40mV=1.765
0	0	1	1	0	0	1.750+40mV=1.790
0	0	1	1	0	1	1.775+40mV=1.815
0	0	1	0	1	0	1.800+40mV=1.840
0	0	1	0	1	1	1.825+40mV=1.865
1	0	1	0	0	0	1.850+40mV=1.890
1	0	0	1	1	0	1.900+40mV=1.940
1	0	0	1	0	0	1.950+40mV=1.990
1	0	0	0	1	0	2.000+40mV=2.040
1	0	0	0	0	0	2.050+40mV=2.090

Notes: 0=connect to GND, 1=open or connect to 3.3V through pull up resistor

Application Guidelines

Soft-Start Interval

Initially, the soft-start function clamps the error amplifier's output of the PWM converter. This generates PHASE pulses of increasing width that charge the output capacitor(s). The resulting output voltages start-up as shown in Fig.3.

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. The soft-start interval and the surge current are programmed by the soft-start capacitor, C_{SS}. Programming a faster soft-start interval increases the peak surge current. Using the recommended $0.1\mu F$ soft start capacitors ensure all output voltages ramp up to their set values in a quick and controlled fashion, while meeting the system timing requirements.

Shutdown

The PWM output does not switch until the soft-start voltage (V_{SS13}) exceeds the oscillator's valley voltage. Additionally, the reference on each linear's amplifier is clamped to the soft-start voltage. Holding the SS24 pin low (with an open drain or open collector signal) turns off regulators 1, 2 and 3. Regulator 4 (MCH) will simply drop its output to the intermediate soft-start level. This output is not allowed to violate the 2V maximum potential gap to the ATX 3.3V output.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit

elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device over-voltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper MOSFET. Prior to turn-off, the upper MOSFET was carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using an RT9238 controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic de-coupling capacitors, close to the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the soft-start capacitor, C_{SS}. Locate these components close to their connecting pins on the control IC. Minimize any leakage current paths from any SS node, since the internal current source is only $28\mu A$.

A multi-layer printed circuit board is recommended. Fig.7 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical

component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but do not unnecessarily oversize this particular island. Since the PHASE node is subject to very high dV/dt voltages, the stray capacitor formed between these island and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.
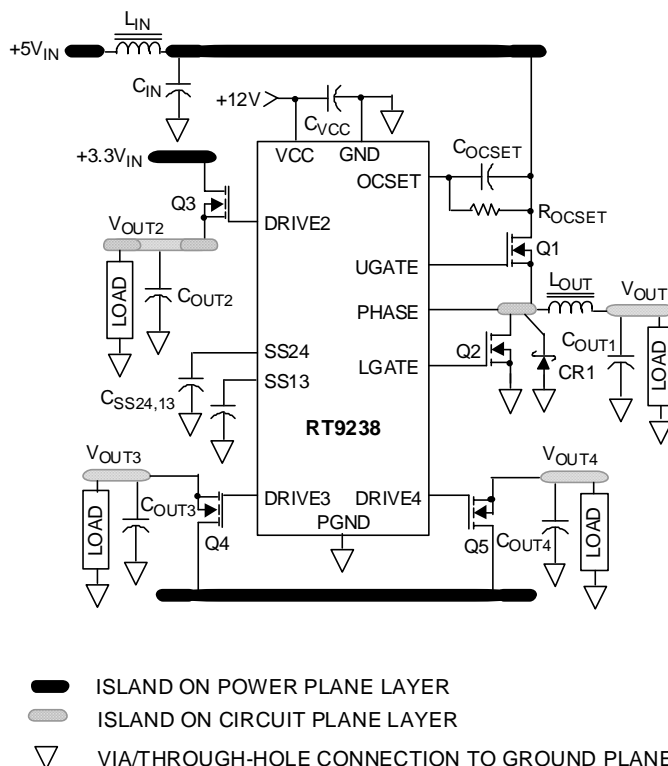

◼ ISLAND ON POWER PLANE LAYER
◼ ISLAND ON CIRCUIT PLANE LAYER
▽ VIA/THROUGH-HOLE CONNECTION TO GROUND PLANE

Fig.7 Layout Planning

PWM1 Controller Feedback Compensation
The PWM controller uses voltage-mode control for output regulation. An internal pole-zero compensation scheme is used with an active capacitor and a passive resistor shown in Fig.8. The zero FZ1 is fixed at about 1kHz to compensate the output 's LC pole FLC. The compensation is to

provide closed loop transfer function with 0 dB crossing frequency and adequate phase margin. For some suggestion LC combinations are L/C = 4μH/6000μF, 3uH/8000uF or 2μH/12000μF. Fig.9 shows an asymptotic plot of the DC-DC converter's gain vs. frequency.
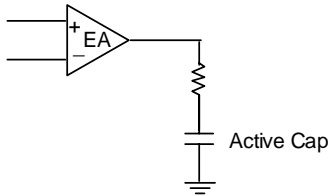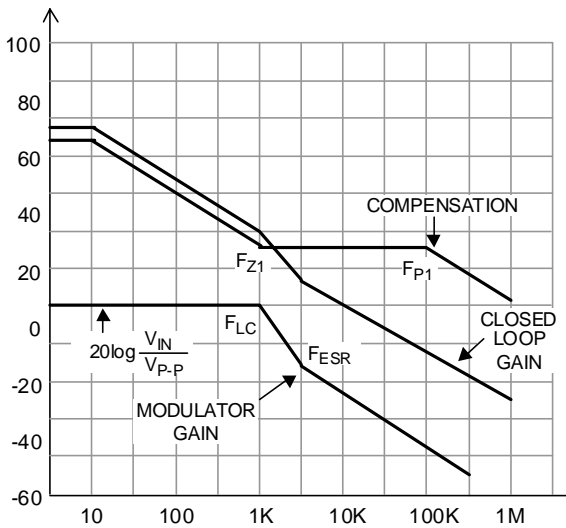

Fig.8 Error Amplifier Compensation

Fig.9 PWM Bode Plot

Transient Response

Modern micro-processsor's power supply request a voltage droop at load transient response and a loadlines at static state load changing as shown in Fig.10, and Fig.11.
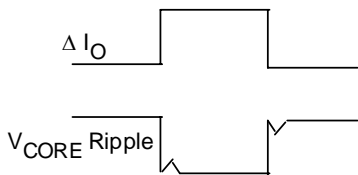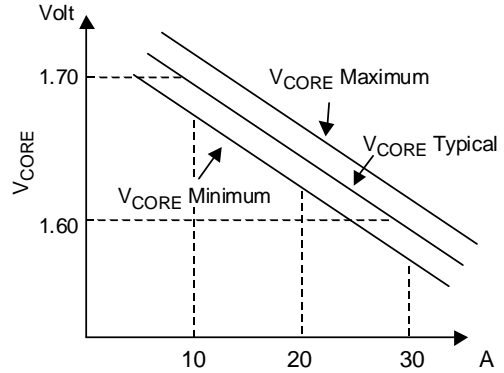

Fig.10 Transient Response

Fig.11 V_{CORE} Load Line

Two things have to be completed at load transient response, first is to sense the instantaneous load current, second is real time to drop the V_{CORE} voltage based on the loadlines. A RT9238 internal trans-conductance (Gm) amplifier sample the on-state drop across the lower MOSFET per clock cycle, the voltage drop is simply R_{DS-ON} x inductor current IL. In step-down DC-DC converter, the IL is relative to load current. The transferred rate of the Gm amplifier is 1/3k, this mean the current output of Gm amplifier is

$$I_{SENSE} = R_{DS(ON)} \times IL/3k.$$

Fig.12 shown the voltage droop tuning circuit, a DACOUT buffer amplifier connect a RF resistor to the non-inverting input of the PWM error amplifier, when load transient happened, the feedback I_{SENSE} current fitted to the non-inverting input of the PWM error amplifier to drop the VCORE voltage. The drop voltage is equal to
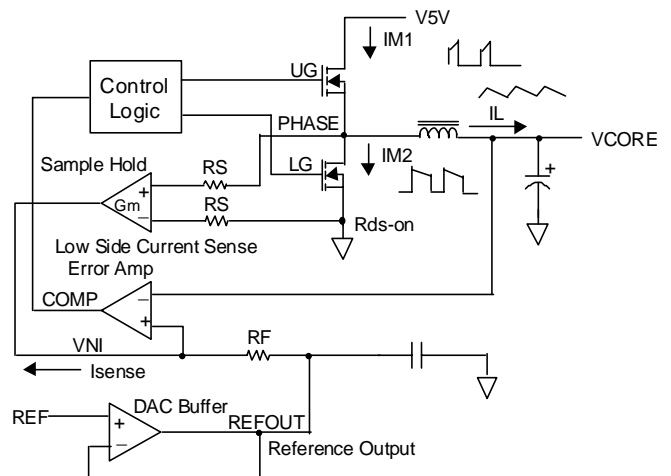
$$V_{DROOP} = I_{SENSE} \times RF$$

Fig.12 Voltage Droop Tuning
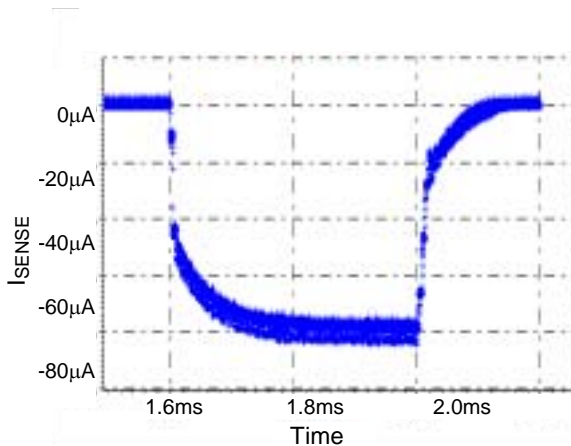
Fig.13, 14 shown the I_{SENSE} and VCORE wave forms.
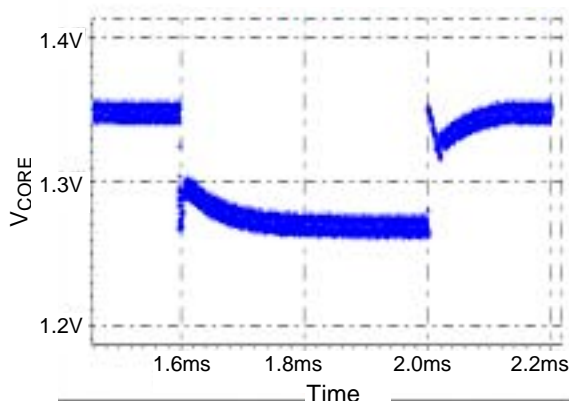

Fig.13 I_{SENSE} Current

Fig.14 V_{CORE} Wave Form at Load Transient

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general the output capacitors should be selected to meet the dynamic regulation requirements. Additionally, the PWM converter requires an output capacitor to filter the current ripple. The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output Capacitors

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Linear Output Capacitors

The output capacitors for the linear regulators provide dynamic load current. Thus capacitors C_{OUT2}, C_{OUT3}, and C_{OUT4} should be selected for transient load regulation.

PWM Output Inductor Selection

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's

response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, large inductance values increase the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the RT9238 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage. The maximum RMS current rating requirement for the input capacitors of a buck regulator is approximately 1/2 of the DC output load current. Worst-case RMS current draw in a circuit employing the RT9238 amounts to the largest RMS current draw of the switching regulator.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The RT9238 requires 5 external transistors. Two N-channel MOSFETs are employed by the PWM converter. The GTL, AGP, and memory linear controllers can each drive a MOSFET or a NPN bipolar as a pass transistor. All these transistors should be selected based upon $R_{DS(ON)}$, current gain, saturation voltages, gate supply requirements, and thermal management considerations.

PWM MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two main loss components: conduction losses and switching losses. These losses are distributed between the upper and lower MOSFET according to the duty factor. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

The equations presented assume linear voltage-current transitions and do not model power losses due to the lower MOSFET's body diode or the output capacitances associated with either MOSFET. The gate charge losses are dissipated by the controller IC (RT9238) and do not contribute to the MOSFETs' heat rise. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{Io^2 \times R_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{Io \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{Io^2 \times R_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The $R_{DS(ON)}$ is different for the two equations above even if the same device is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Fig.15 shows the gate drive where the upper MOSFET's gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the approximate gate-to-source voltage of Q1 is 7V. The lower gate drive voltage is about 8V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute

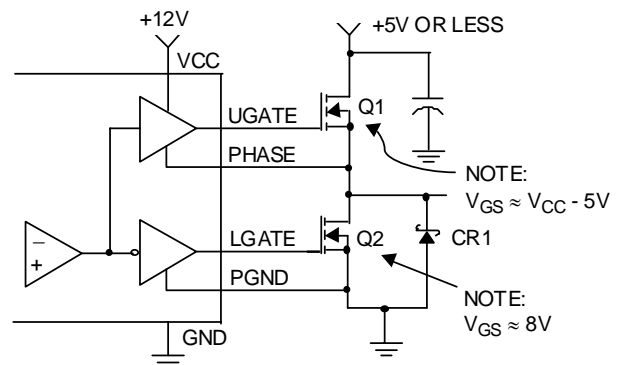gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

Fig.15 Upper Gate Drive-direct V_{CC} Drive

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. For best results, the diode must be a surface-mount Schottky type to prevent the parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but one must ensure the PHASE node negative voltage swing does not exceed -3V to -5V peak. The diode's rated reverse breakdown voltage must be equal or greater to 1.5 times the maximum input voltage.

Linear Controllers Transistor Selection

The RT9238 linear controllers are compatible with both NPN bipolar as well as N-channel MOSFET transistors. The main criteria for selection of pass transistors for the linear regulators is package selection for efficient removal of heat. The power dissipated in a linear regulator is

$$P_{LINEAR} = Io \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the maximum desired temperature with the maximum expected ambient temperature.

When selecting bipolar NPN transistors for use with the linear controllers, insure the current gain at the

given operating V_{CE} is sufficiently large to provide the desired output load current when the base is fed with the minimum driver output current.

In order to ensure the strict timing/level requirement of OUT4, a NPN transistor is recommended for use as a pass element on this output (Q5). An low gate threshold NMOS could be used, but meeting the requirements would then depend on the VCC bias being sufficiently high to allow control of the MOSFET.

Package Information
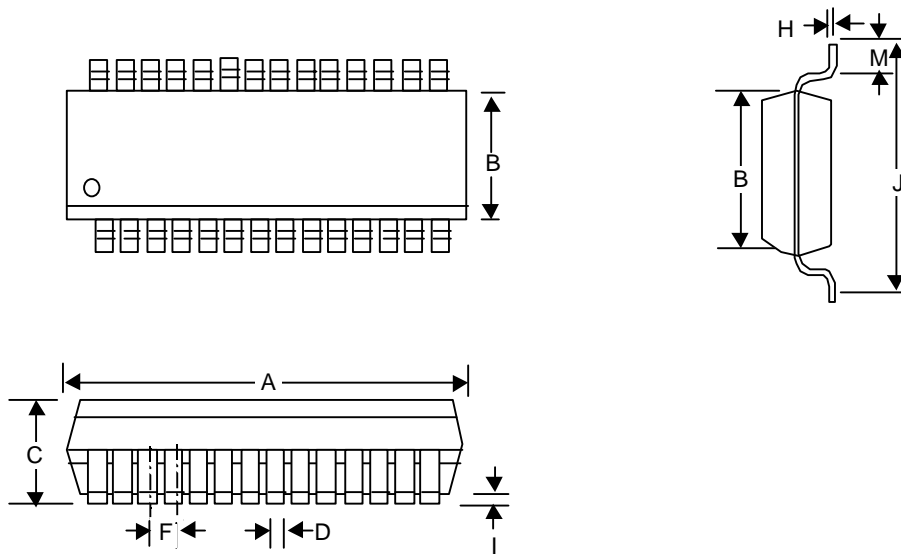
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	17.704	18.110	0.697	0.713
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

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