Dual Channel Synchronous-Rectified Buck MOSFET Driver

General Description

The RT9602 is a dual power channel MOSFET driver specifically designed to drive four power N-Channel MOSFETs in a synchronous-rectified buck converter topology. These drivers combined with RT9237/A and RT9241A/B series of Multi-Phase Buck PWM controllers provide a complete core voltage regulator solution for advanced microprocessors.

The RT9602 can provide flexible gate driving for both high side and low side drivers. This gives more flexibility of MOSFET selection.

The output drivers in the RT9602 have the capability to drive a 3000pF load with a 40nS propagation delay and 80nS transition time. This device implements bootstrapping on the upper gates with only a single external capacitor required for each power channel. This reduces implementation complexity and allows the use of higher performance, cost effective, N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The RT9602 can detect high side MOSFET drain-to-source electrical short at power on and pull the 12V power by low side MOS and cause power supply to go into over current shutdown to prevent damage of CPU.

Ordering Information

RT9602□ □

- Package Type
  S : SOP-14
- Operating Temperature Range
  C: Commercial Standard

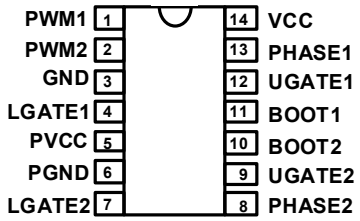
Features

- **Drives Four N-Channel MOSFETs**
- **Adaptive Shoot-Through Protection**
- **Internal Bootstrap Devices**
- **Small 14-Lead SOIC Package**
- **5V to 12V Gate-Drive Voltages for Optimal Efficiency**
- **Tri-State Input for Bridge Shutdown**
- **Supply Under-Voltage Protection**
- **Power ON Over-Voltage Protection**

Applications

- Core Voltage Supplies for Intel Pentium® 4 and AMD® Athlon™ Microprocessors
- High Frequency Low Profile DC-DC Converters
- High Current Low Voltage DC-DC Converters

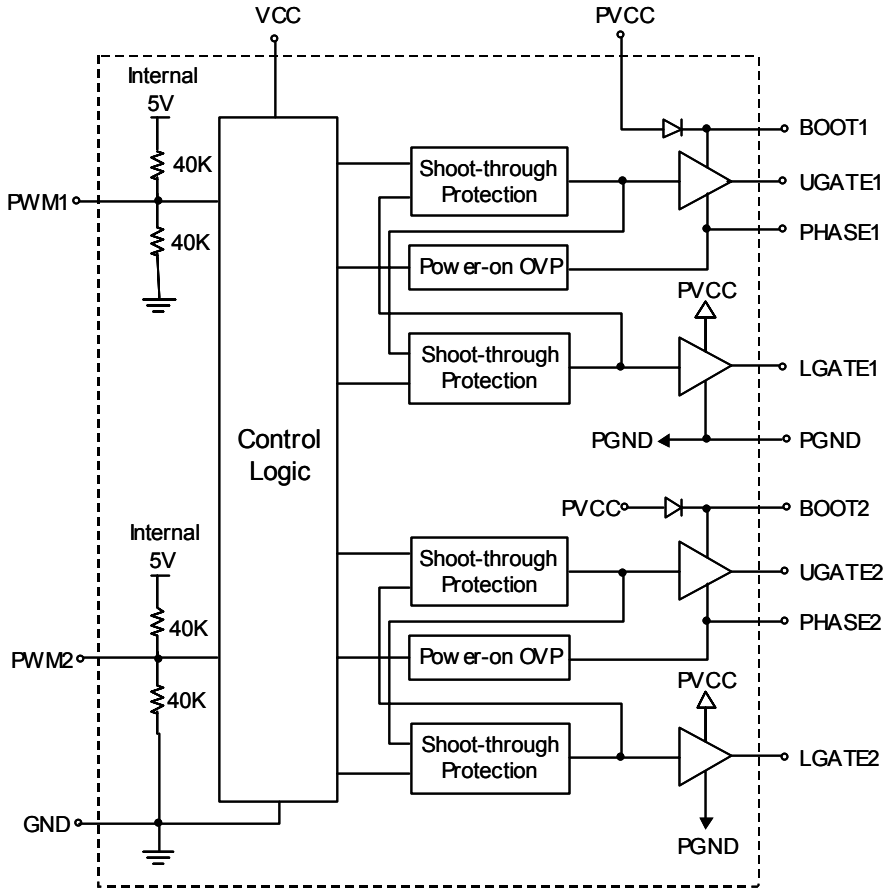
Pin Configurations

Part Number	Pin Configurations
RT9602CS (Plastic SOP-14)	TOP VIEW 

Pin Description

Pin No.	Pin Name	Pin Function
1	PWM1	Channel 1 PWM Input
2	PWM2	Channel 2 PWM Input
3	GND	Ground Pin
4	LGATE1	Lower Gate Drive of Channel 1
5	PVCC	Upper and Lower Gate Driver Power Rail
6	PGND	Lower Gate Driver Ground Pin
7	LGATE2	Lower Gate Drive of Channel 2
8	PHASE2	Connect this pin to phase point of channel 2. Phase point is the connection point of high side MOSFET source and low side MOSFET drain
9	UGATE2	Upper Gate Drive of Channel 2
10	BOOT2	Floating Bootstrap Supply Pin of Channel 2
11	BOOT1	Floating Bootstrap Supply Pin of Channel 1
12	UGATE1	Upper Gate Drive of Channel 1
13	PHASE1	Connect this pin to phase point of channel 1. Phase point is the connection point of high side MOSFET source and low side MOSFET drain
14	VCC	Control Logic Power Supply

Function Block Diagram



Absolute Maximum Ratings

- Supply Voltage (V_{CC}) ---------- 15V
- Supply Voltage (PV_{CC}) ---------- VCC + 0.3V
- BOOT Voltage (V_{BOOT}-V_{PHASE}) ---------- 15V
- Input Voltage (V_{PWM}) ---------- GND − 0.3V to 7V
- UGATE ---------- V_{PHASE} − 0.3V to V_{BOOT} + 0.3V
- LGATE ---------- GND − 0.3V to V_{PVCC} + 0.3V
- Package Thermal Resistance
  SOP-14, θ_{JA} ---------- 127.67°C /W
- Ambient Temperature ---------- 0°C to 70°C
- Junction Temperature ---------- 0°C to 125°C
- Storage Temperature Range ---------- –40°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Level (Note)
  HBM ---------- 2KV
  MM ---------- 200V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Current						
Bias Supply Current	I_{VCC}	f_{PWM} = 250kHz, V_{PVCC} = 12V, C_{BOOT} = 0.1μF, R_{PHASE} = 20Ω	--	5.5	8	mA
Power Supply Current	I_{PVCC}	f_{PWM} = 250kHz, V_{PVCC} = 12V, C_{BOOT} = 0.1μF, R_{PHASE} = 20Ω	--	5.5	10	mA
Power-On Reset						
V_{CC} Rising Threshold			8.6	9.9	10.7	V
Hysteresis			0.6	1.35	--	V
PWM Input						
Maximum Input Current		V_{PWM} = 0 or 5V	80	127	150	μA
PWM Floating Voltage		Vcc = 12V	1.1	2.1	3.7	V
PWM Rising Threshold			3.3	3.7	4.3	V
PWM Falling Threshold			1.0	1.26	1.5	V
UGATE Rise Time		V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
LGATE Rise Time		V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
UGATE Fall Time		V_{PVCC} = V_{VCC} = 12V, 3nF load	--	40	--	ns
LGATE Fall Time		V_{PVCC} = V_{VCC} = 12V, 3nF load	--	30	--	ns
UGATE Turn-Off Propagation Delay		V_{VCC} = V_{PVCC} = 12V, 3nF load	--	60	--	ns
LGATE Turn-Off Propagation Delay		V_{VCC} = V_{PVCC} = 12V, 3nF load	--	45	--	ns
Shutdown Window			1.26	--	3.7	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output						
Upper Drive Source	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 12V	--	1.75	3.0	Ω
Upper Drive Sink	R_{UGATE}	V_{VCC} = 12V, V_{PVCC} = 12V	--	2.8	5.0	Ω
Lower Drive Source	R_{LGATE}	V_{VCC} = 12V, V_{PVCC} = 12V	--	1.9	3.0	Ω
Lower Drive Sink	R_{LGATE}	V_{VCC} = V_{PVCC} = 12V	--	1.6	3.0	Ω

Note: Devices are ESD sensitive, especially for PHASE and LGATE pins. Handling precaution recommended. The human body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Operation Descriptions

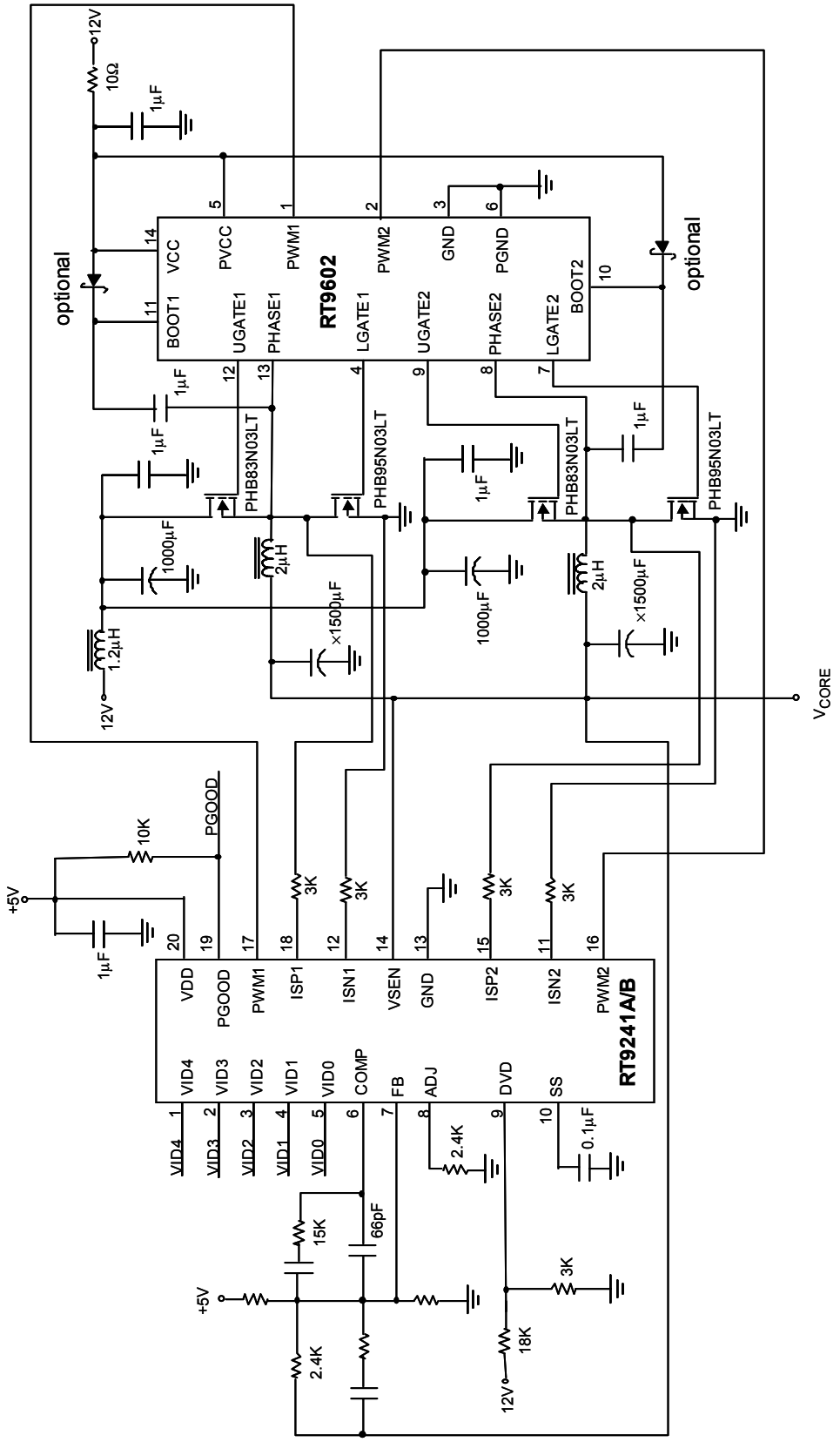
The RT9602 has power on protection function which held UGATE and LGATE low before VCC up cross the rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal turns low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot-through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high. The non-overlapping function is also presented between UGATE and LGATE signal transient.

The PWM signal is recognized as high if above rising threshold and as low if below falling threshold. Any signal level in this window is considered as tri-state, which causes turn-off of both high side and low-side MOSFET. When PWM input is floating (not connected), internal divider will pull the PWM to 1.9V to give the controller a recognizable level. The maximum sink/source capability of internal PWM reference is 60μA.

The PVCC pin provides flexibility of both high side and low side MOSFET gate drive voltages. If 8V, for example, is applied to PVCC, then high side MOSFET gate drive is 8V to 1.5V (approximately, internal diode plus series resistance voltage drop). The low side gate drive voltage is exactly 8V.

The RT9602 implements a power on over-voltage protection function. If the PHASE voltage exceeds 1.5V at power on, the LGATE would be turn on to pull the PHASE low until the PHASE voltage goes below 1.5V. Such function can protect the CPU from damage by some short condition happened before power on, which is sometimes encountered in the M/B manufacturing line.

Typical Application Circuit



Application Information

Driving power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When V_{gs} at 12V (or 5V), the gate draws the current only few nanoamperes. Thus once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

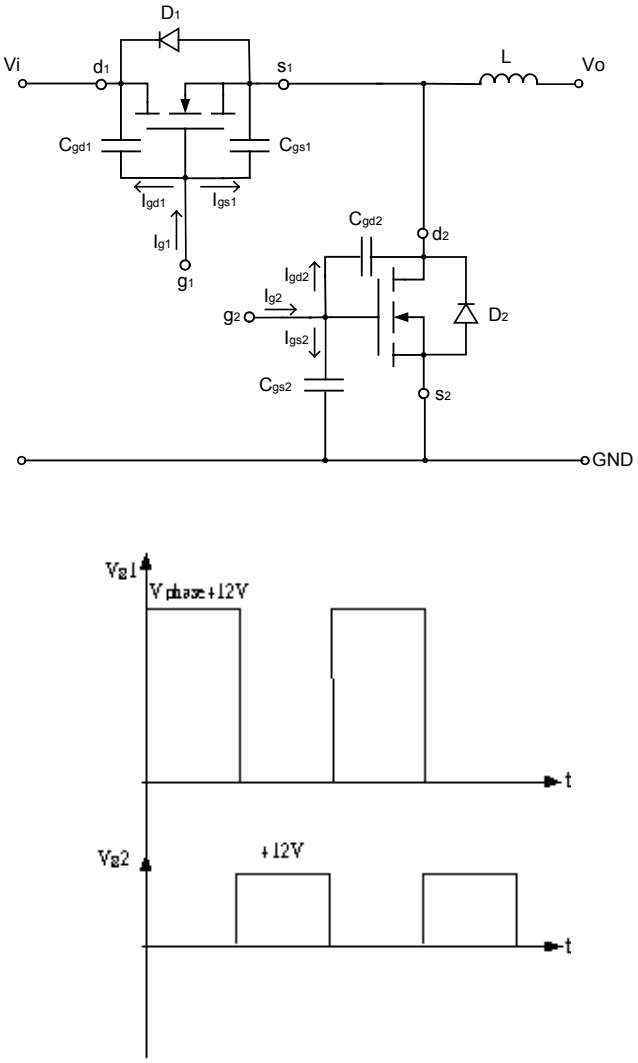


Figure 1. The gate driver must supply I_{gs} to C_{gs} and I_{gd} to C_{gd}

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 12V.The operation consists of charging C_{gd} and C_{gs}. C_{gs1} and C_{gs2} are the capacitances from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs} is referred as "C_{iss}" which is the input capacitance. C_{gd1} and C_{gd2} are the capacitances from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}," the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2}, are showed below

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1}\times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2}\frac{dV_{g2}}{dt} = \frac{C_{gs1}\times 12}{t_{r2}} \quad (2)$$

According to the design of RT9602, before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{12V}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to Vi. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{Vi+12V}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified BUCK converter, input voltage V_i = 12V, V_{g1} = V_{g2} = 12V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF,and t_r = 14nS. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF, and t_r = 30nS, from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428(A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88(A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326(A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4(A) \quad (8)$$

the total current required from the gate driving source is

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.745(A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28(A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Layout Consider

Figure 2. shows the schematic circuit of a two-phase synchronous-buck converter to implement the RT9602. The converter operates for the input rang from 5V to 12V.

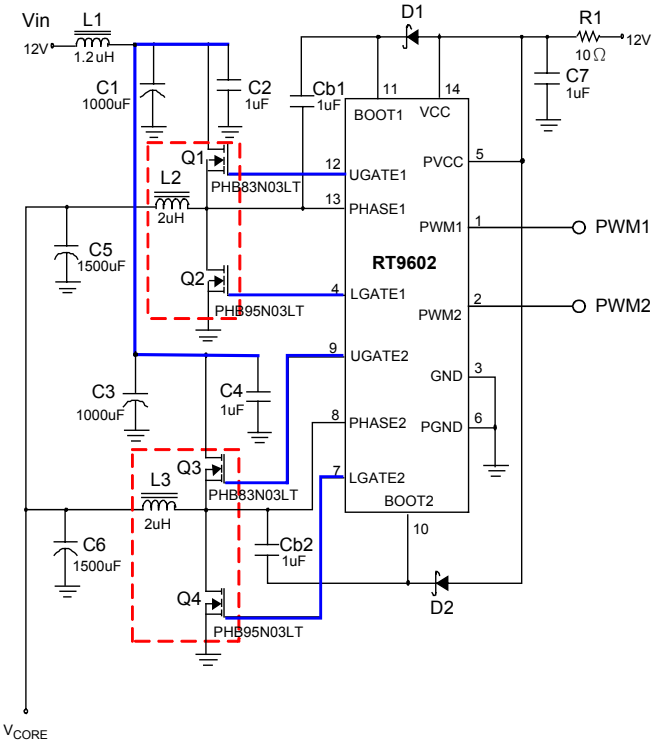


Figure 2. Two- Phase Synchronous-Buck Converter Circuit

When layout the PC board, it should be very careful. The power-circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 and Q3, Q4, L4 should be very close. The connection from Q1, and Q3 drain to positive sides of C1, C2, C3, and C4; the connection from Q2, and Q4 source to the negative sides of C1, C2, C3, and C4 should be as short as possible.

Next, the trace from Ugate1, Ugate2, Lgate1, and Lgate2 should also be short to decrease the noise of the driver output signals. Phase1 and phase2 signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C7 should be connected to PGND directly. Furthermore, the bootstrap capacitors (C_{b1}, C_{b2}) should always be placed as close to the pins of the IC as possible.

Select the Bootstrap Capacitor

Figure 3. shows part of the bootstrap circuit of RT9602. The V_{CB} (the voltage difference between BOOT1 and PHASE1 on RT9602) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by following constraints.

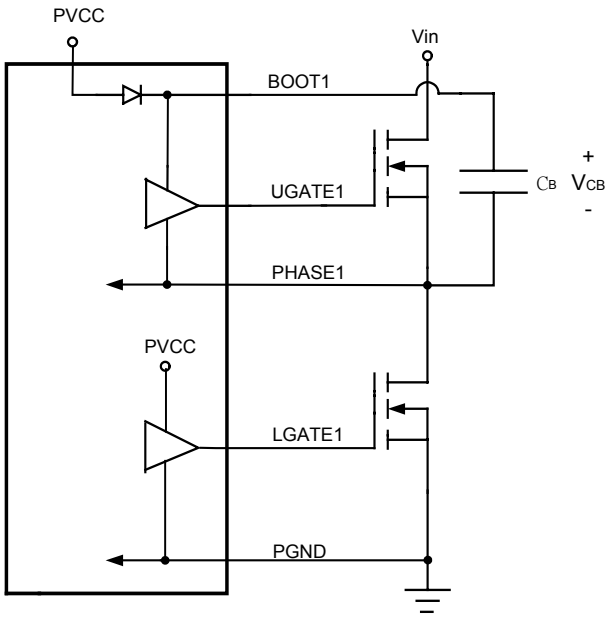


Figure 3. Part of Bootstrap Circuit of RT9602

In practice, a low value capacitor C_B will lead the overcharging that could damage the IC. Therefore to minimize the risk of overcharging and reducing the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1μF, and the larger the better. In general design, using 1μF can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. Here, to adopt either a ceramic or tantalum capacitor is suitable.

Power Dissipation

For not exceeding the maximum allowable power dissipation to drive the IC beyond the maximum recommended operating junction temperature of 125°C, it is necessary to calculate power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET. Figure 4. shows the power dissipation test circuit. C_L and C_U are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is 0.01μF.

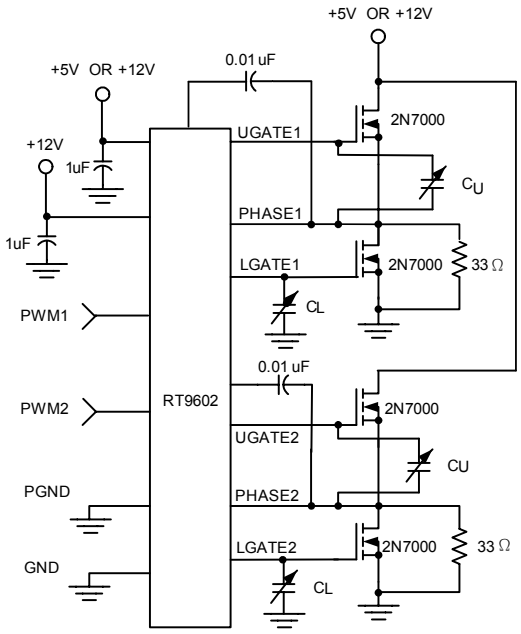


Figure 4. RT9602 Power Dissipation Test Circuit

Figure 5. shows the power dissipation of the RT9602 as a function of frequency and load capacitance. The value of the C_u and C_L are the same and the frequency is varied from 100kHz to 600kHz. PVCC and VCC is 12V and connected together. Figure 6. shows the same characterization for PVCC tied to 5V instead of 12V.

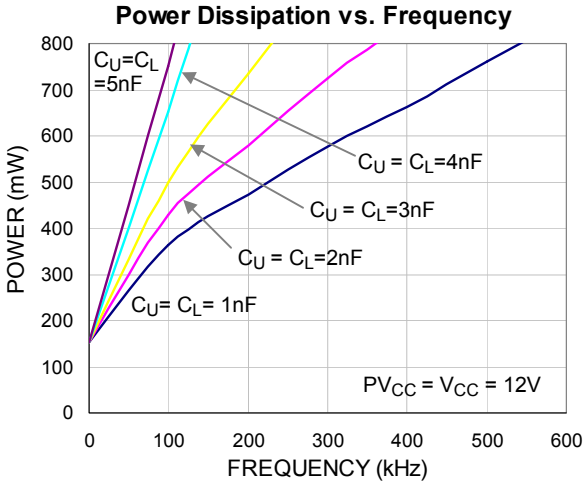


Figure 5. Power Dissipation vs. Frequency (RT9602)

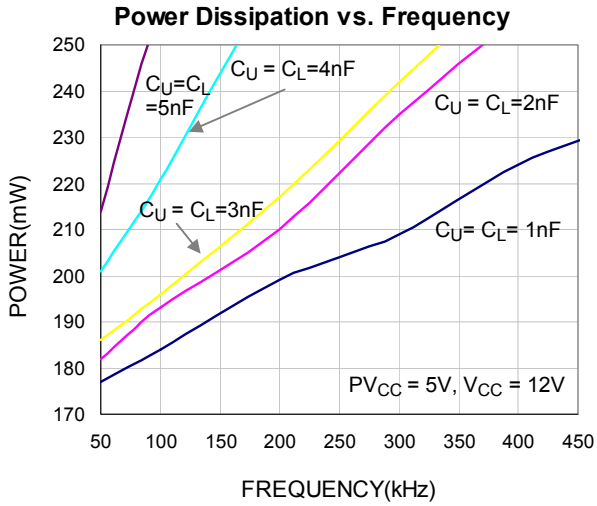


Figure 6. Power Dissipation vs. Frequency, PVCC = 5V

The operating junction temperature can be calculated from the power dissipation curves (Figure 5 and Figure 6). Assume the RT9602's PVCC = VCC=12V, operating frequency is 200kHz, and the C_U=C_L=1.5nF which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 5, the power dissipation is 500mW. In RT9602, the package thermal resistance θ_{JA} is 127.67°C/W, the operating junction temperature is calculated as:

$$T_J = 127.67°C/W \times 500mW + 25°C$$
$$= 88.84°C \quad (11)$$

where the 25°C is the ambient temperature.

The method to improve the thermal transfer is to increase the PC board copper area around the RT9602, first. Then, adding a ground pad under IC to transfer the heat to the peripheral of the board.

Power on Over-Voltage Protection Function

The RT9602 provides a protect function which can avoid some short condition happened before power on. The following discussion about the power on over-voltage protection function of RT9602 is based on the experiments of the high side MOSFET directly shorted to 12V. The test circuit as shown in the typical application circuit (with RT9241A/B dual-channel synchronous-rectified buck controller) the VCC and the phase signals are measured on the VCC pin and the phase pin of RT9602. The LGATE signal is measured on the gate terminal of MOSEFET.

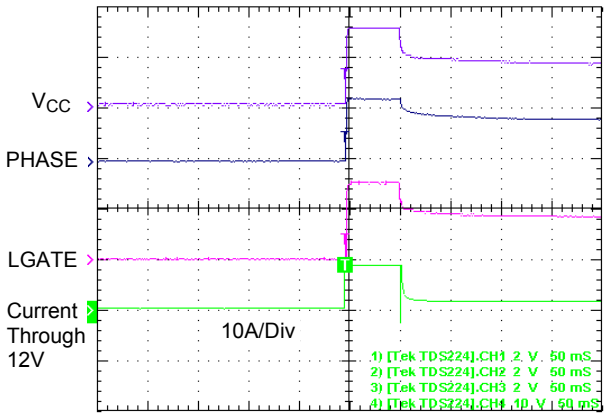


Figure 7.. High Side Direct Short

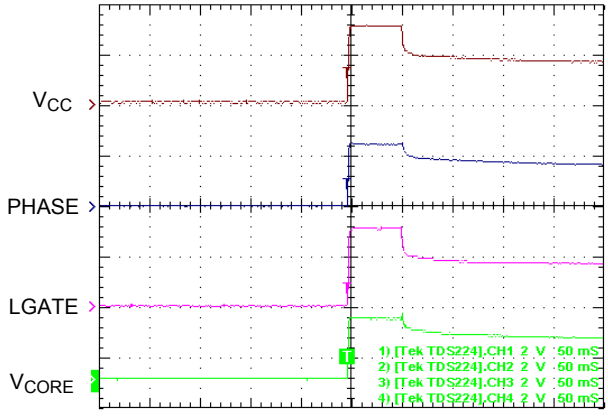


Figure 8. High Side Direct Short

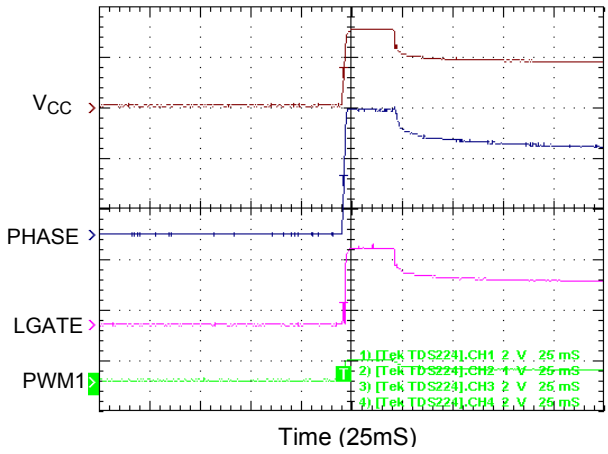
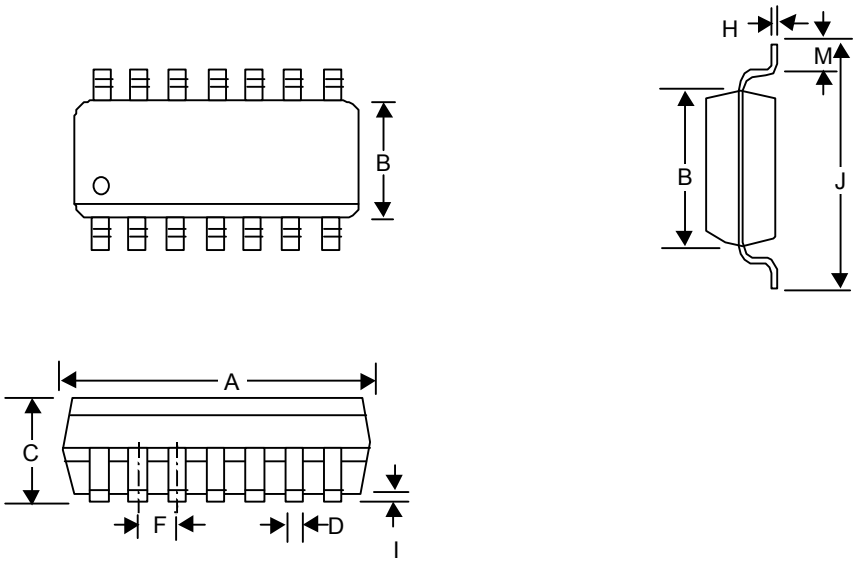


Figure 9. High Side Direct Short

Referring to Figure 7, when VCC exceeds 1.5V, RT9602 turns on the LGATE to clamp the Phase through the low side MOSFET. During the turn-on of the low side MOSFET, the current of ATX 12V is limited at 25A although the maximum current of ATX 12V listed on the case of ATX is 15A. After the ATX 12V shuts down, the VCC falls slowly. Please note that the trigger point of RT9602 is at 1.5V VCC, and the clamped value of phase is at about 2.4V. Next, reference to Figure 8, it is obvious that since the Phase voltage increases during the power-on, the V_{CORE} increases correspondingly, but is gradually decreased as LGATE and VCC decrease. In Figure 9, during the turn-on of the low side MOSFET, the VCC is much less than 12V, thus the RT9241A/B keeps the PWM signal at high impedance state.

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	8.534	8.738	0.336	0.344
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

14–Lead SOP Plastic Package

RICHTEK TECHNOLOGY CORP.
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

RICHTEK TECHNOLOGY CORP.
Taipei Office (Marketing)
8F-1, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com