Single 12V Input Supply Dual Regulator - Synchronous-Buck-PWM and Linear-Regulator Controller

General Description

The uP6161 integrates a high performance synchronous-rectified buck controller and a linear-regulator controller. This part works with a single +12V supply voltage and delivers two high quality output voltages for both processing unit and memory unit. An internal linear regulator provides optimum 9V drive voltage for efficiency and thermal management.

The buck controller features internal MOSFET drivers that supports bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count. It incorporates simple, single feedback loop, voltage-control with fast transient response.

The linear controller drives an external N-Channel MOSFET with under voltage protection during both soft start and normal operation.

Other features include adjustable operation frequency, internal soft start, under voltage protection, adjustable over current protection and shutdown function. With the above function, this part provides customers a compact, well protected and cost-effective solution. This part is available in SOP-14 and QFN3x3 -16L packages.

Applications

- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Cable Modems, Set Top Boxes, and DSL Modems**
- **Industrial Power Supplies; General Purpose Supplies**
- **12V Input DC-DC Regulators**
- **Low-Voltage Distributed Power Supplies**

Features

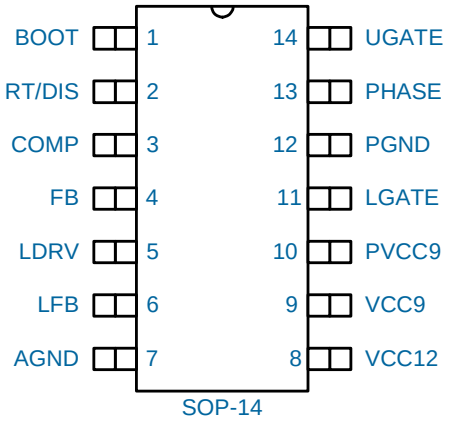
- **Operate with Single 12V Supply**
- **Self-Regulated 9V Drive Voltage**
- **Integrated Boot Diode**
- **Provide Two Regulated Voltages**
  - **One Synchronous-Rectified Buck Controller**
  - **One Linear Controller**
  - **Both Controllers Drive N-Channel MOSFETs**
  - **Smaller Converter Size**
- **Excellent Output Voltage Regulation**
  - **1.5% for Buck Controller**
  - **2% for Linear Controller**
- **Simple Single-Loop Control Design**
  - **Voltage-Mode PWM Control**
  - **Fast Transient Response**
  - **High-Bandwidth Error Amplifier**
- **Lossless, Programmable Overcurrent Protection**
  - **Uses Lower MOSFET $R_{DS(ON)}$**
- **Adjustable Frequency from 150kHz to 1MHz**
- **Internal Soft Start for Both Outputs**
- **Under Voltage Protection for Both Outputs including Soft Start Cycle**
- **SOP-14 and QFN3x3-16 packages**
- **RoHS Compliant and 100% Lead Free**

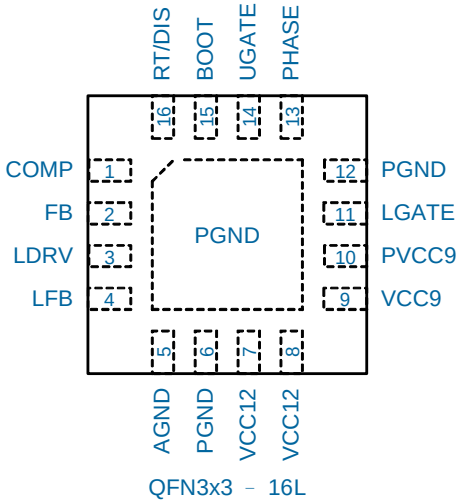
Ordering Information

Order Number	Package Type	Remark
uP6161S14	SOP - 14	
uP6161Q	QFN3x3 - 16	

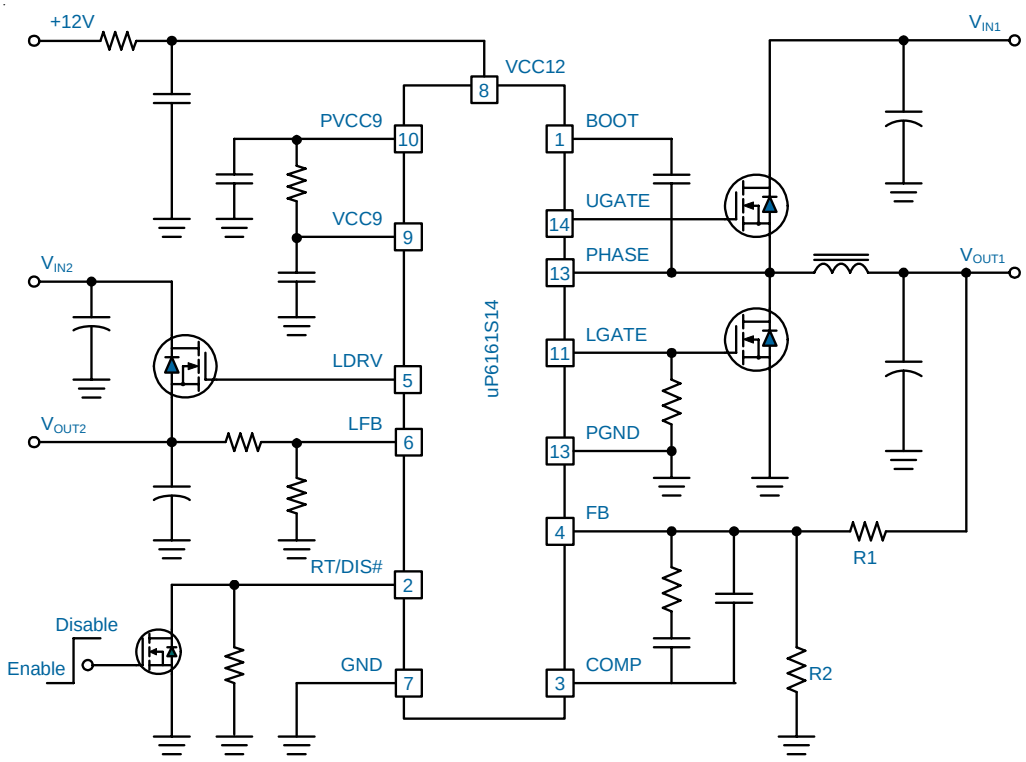
Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

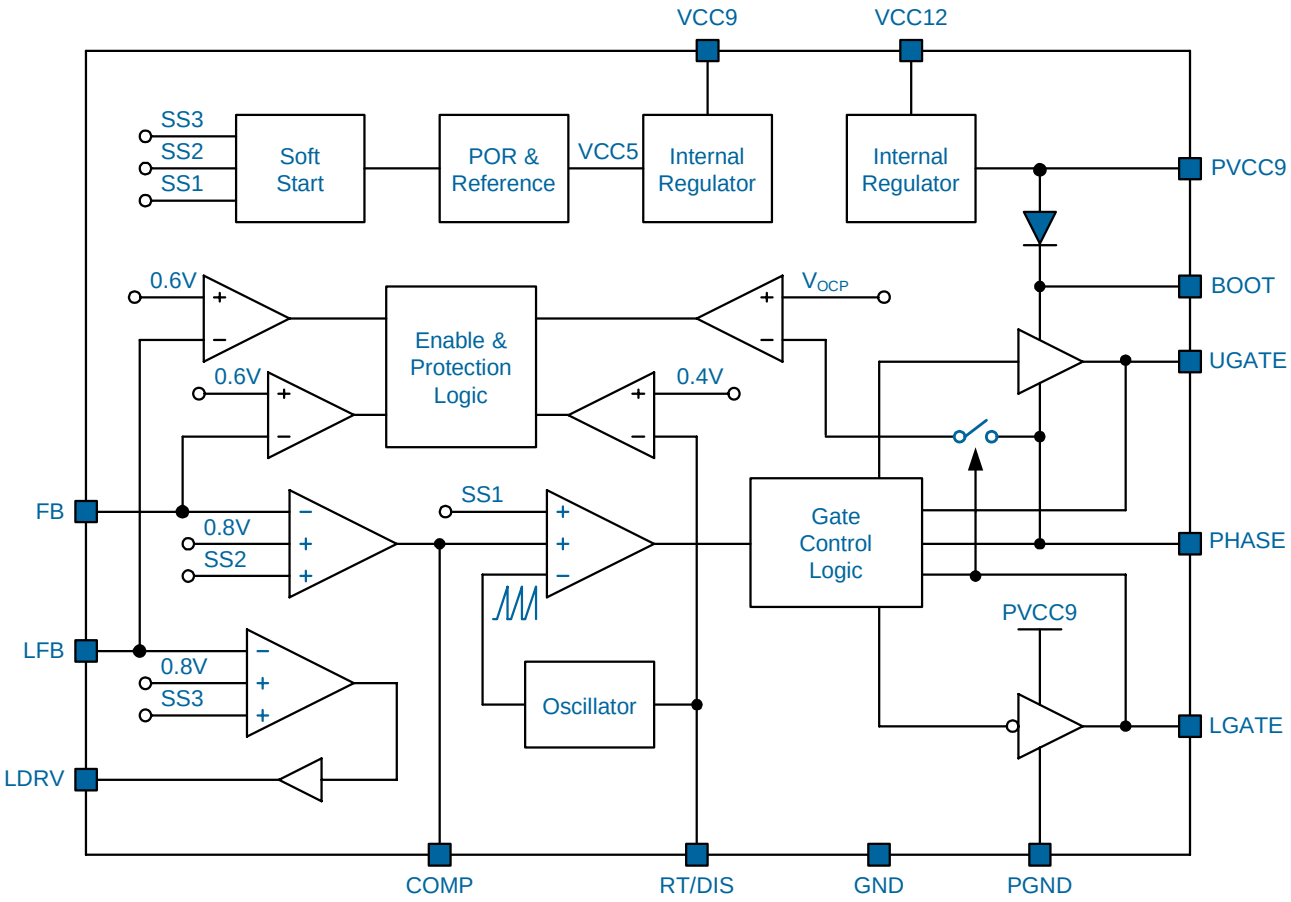




Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP	QFN		
1	15	BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
2	16	RT/DIS	**Frequency Setting and Chip Disable.** A resistor to GND sets the operation frequency of for the buck converter. Pulling this pin to GND disables both buck and linear regulators.
3	1	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the buck converter.
4	2	FB	**Feedback Voltage for Buck Converter.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
5	3	LDRV	**Driver Output for Linear Regulator.** This pin provides the gate voltage for the linear regulator pass transistor. Connect this pin to the gate of an external N-Channel MOSFET to form a linear regulator.
6	4	LFB	**Feedback Voltage for Linear Regulator.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage.
7	5	AGND	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
8	7, 8	VCC12	**Supply Voltage.** This is the power supply pin for the IC; it sources the internal 9V regulator used to the gate drivers. A minimum 1uF ceramic capacitor is required for locally bypassing the input voltage.
9	9	VCC9	**VCC9.** This pin supplies bias current for the IC. A minimum 1uF ceramic capacitor physically near the IC is required for locally bypassing the input voltage.
10	10	PVCC9	**Power PVCC9.** This is the output of the internal 9V linear regulator. It provides current required for driving N-Channel MOSFETs of buck converter. A minimum 1uF ceramic capacitor physically near the IC is required for locally bypassing the input voltage.
11	11	LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
12	6, 12	PGND	**Power Ground for the IC.**
13	13	PHASE	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
14	14	UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
Exposed Pad			**Power Ground for the IC.** For QFN package only. This exposed pad should be well soldered to PCB for effective heat conduction. Connect the exposed pad the ground.

Functional Description

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The buck controller features internal MOSFET drivers that supports 12V + 12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count. It incorporates simple, single feedback loop, voltage-control with fast transient response.

The linear controller drives an external N-Channel MOSFET with undervoltage protection during both softstart and normal operation.

Other features include adjustable operation frequency, internal softstart, undervoltage protection, adjustable overcurrent protection and shutdown function.

Supply Voltage

The uP6161 is designed to work with a single supply rail. It integrates two linear regulators providing optimal supply voltages for gate drivers and control circuitry respectively as shown in Figure 1. The 9V linear regulator generates 9V PVCC9 for gate drives achieving optimum balance between efficiency and thermal management. The 5V linear regulator works with VCC9 input generates VCC5 for internal control circuitry. If 12V driving voltage is preferred, simply connect +12V to the PVCC9 pin and let VCC12 open.

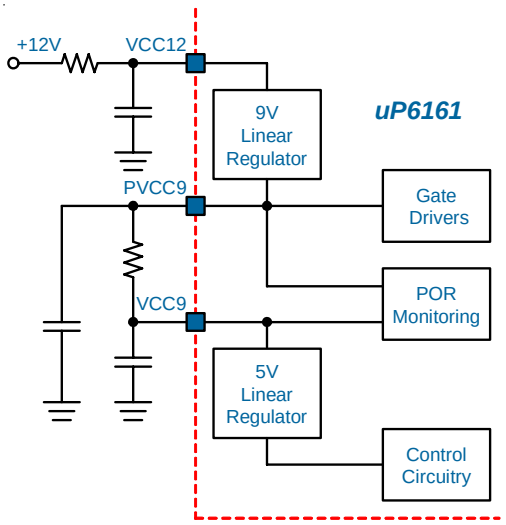


Figure 1. Supply Voltage Configuration

Both PVCC9 and VCC9 are continuously monitored for power on reset with typical rising threshold level as 7.5V. All the three supply inputs require minimum 1uF ceramic capacitors for local bypassing. Place the bypass capacitors physically near the IC. No external bypass capacitor is required for filtering the VCC5 voltage.

Bootstrap Circuitry

The uP6161 integrates MOSFET gate drives that are powered from the PVCC9 pin and support 12V+12V driving capability. A bootstrap diode is embedded to facilitates PCB design and reduce the total BOM cost. Connect a ceramic bootstrap diode between BOOT and PHASE pins to form a bootstrap circuit for providing charge to turn on/off the upper MOSFET. No external Schottky diode is required. Converters that consist of uP6161 feature high efficiency without special consideration on the selection of MOSFETs.

Chip Enable and Frequency Setting

The RT/DIS is a multifunctional pin: chip shutdown and frequency setting. Pulling low this pin to GND by an open drain/collector transistor shuts down the uP6161 and disables both buck and linear controllers.

The switching frequency is set by a resistor connecting to the RT/DIS pin as:

$$f_{OSC} = \frac{23500000}{R_{RT}} + 74000 \quad \text{(Hz)}$$

Figure 2 shows the dependence between the resistor chosen and the resulting switching frequency.

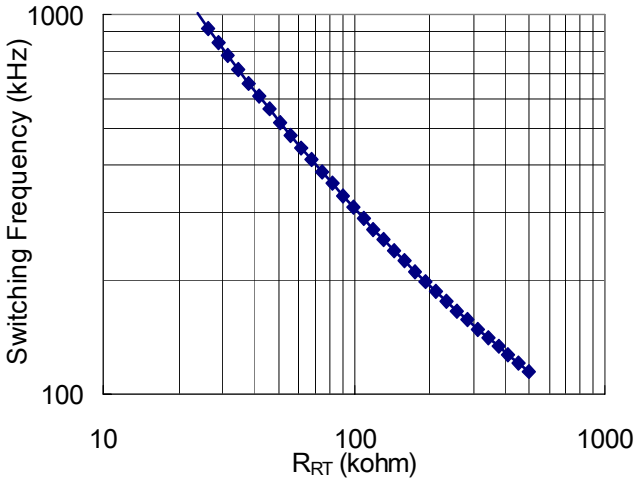


Figure 2. Switching Frequency vs. R_{RT}

Soft Start

Once POR is acknowledged and RT/DIS pin is released,

Functional Description

the uP6161 initiates its digital soft start cycle to prevent surge current from power supply input during turn on (referring to the Functional Block Diagram). The error amplifiers are three-input devices. Reference voltage V_{REF} or the internal soft start voltage SS2/SS3 whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifiers. SS2/SS3 internally ramps up to 0.8V in 4096 cycles of the internal oscillator frequency after the after the softstart cycle is initiated. Take 600kHz switching frequency for example (1.67us per cycle), the ramp-up time is about 6.8ms. Accordingly, the output voltages follow the soft start signals SS2/SS3 and linearly ramp up to their final level, resulting minimum inrush current from input voltage.

The SS2/SS3 signals keep ramping up after it exceeds the internal 0.8V reference voltages. However, the internal 0.8V reference voltages takes over the behavior of error amplifier after SS > V_{REF}. When the SS2/SS3 signal climb to its ceiling voltage (5V), the uP6161 claims the end of softstart cycle and enable the under voltage protection of the output voltages.

Figure 3 shows a typical start up interval for uP6161 where the RT/DIS pin has been released from a grounded (system shutdown) state. **Note the LDO output voltage (LVO) starts ramping up only after the PWM output voltage (SVO) is within regulation.**

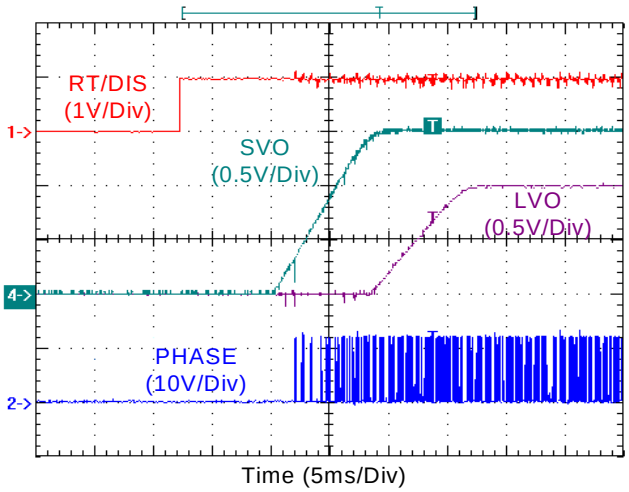


Figure 3. Softstart Behavior.

Power Input Detection

The uP6161 detects PHASE voltage for the present of power input when the UGATE turns on the first time. If the PHASE voltage does not exceed 2.0V when the UGATE turns on, the uP6161 asserts that power input in not ready and stops the softstart cycle. However, the internal SS continues ramping up to 5VDD. Another softstart is initiated after SS ramps up to 5VDD. The hiccup period is about 8ms. Figure 4 shows the start up interval where V_{IN} does not present initially.

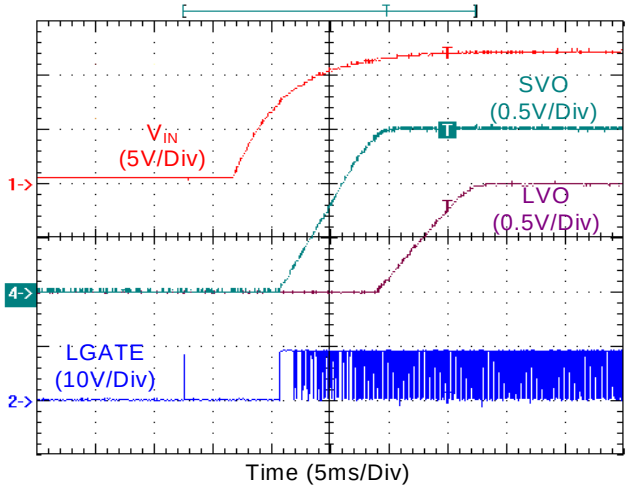


Figure 4. Softstart where V_{IN} does not Present Initially.

Output Voltage Selection

The output voltage can be programmed to any level between the 0.8V internal reference, up to the 80% of V_{IN} supply. The lower limitation of output voltage is caused by the internal reference. The upper limitation of the output voltage is caused by the maximum available duty cycle (80% typical). This is to leave enough time for overcurrent detection. Output voltage out of this range is not allowed.

A voltage divider sets the output voltage (refer to the Typical Application Circuit on page 1 for detail). In real applications, choose R2 in 100Ω ~ 10kΩ range and choose appropriate R1 according to the desired output voltage.

$$V_{OUT} = V_{REF} \times \frac{R1+R2}{R2} = 0.8V \times \frac{R1+R2}{R2}$$

Overcurrent Protection (OCP)

The uP6161 detects voltage drop across the lower MOSFET (V_{PHASE}) for overcurrent protection when it is turned on. If V_{PHASE} is lower than the user-programmable voltage V_{OCP}, the uP6161 asserts OCP and shuts down the converter. The OCP level can be calculated according the on-resistance of the lower MOSFET used.

$$I_{OCP} = -\frac{V_{OCP}}{R_{DS(ON)}} \qquad (A)$$

Connecting a resistance from LGATE to GND selects the

appropriate V_{OCP} as shown in Table 1. Also shown in Table 1 is OCP level if a lower MOSFET with 10mΩ $R_{DS(ON)}$ is used.

When programming the OCP level, take into consideration the conditions that affect $R_{DS(ON)}$ of the lower MOSFET, including operation junction temperature, gate driving voltage and distribution. Consider the $R_{DS(ON)}$ at maximum operation temperature and lowest gate driving voltage.

Table 1. OCP Level Selection

R_{OCP} (Ω)	open	42k	24k	10k
V_{OCP} (mV)	-375	-300	-225	-150
I_{OCP} (A)	37.5	25	22.5	15

Another factor should taken into consideration is the ripple of the inductor current. The current near the valley of the ripple current is used for OCP, resulting the averaged OCP level a little higher than the calculated value.

Output Under Voltage Protection of Linear Regulator

The LDRV and LFB voltages are monitored during both softstart and normal operation for output under voltage protection. The uP6161 asserts UVP if the error amplifier saturates, LDRV goes to ceiling high and LFB voltage is lower than 0.6V for 10us. This demands $V_{CC12} > (V_{OUT} + V_{TH} + 1V)$ where V_{TH} is the threshold voltage of the external N-Channel MOSFET. This is to ensure that the output voltage can follow the softstart signal and will not saturate the error amplifier. That means a low threshold voltage MOSFET is required for low V_{CC12} applications. This also demands that V_{IN2} should be ready before the soft start cycle is initiated.

The uP6161 disables the output voltages upon the triggering of UVP. The uP6161 repeats the softstart cycle if the output under voltage is not removed.

Absolute Maximum Rating

Supply Input Voltage, VCC12 (Note 1) ---------- -0.3V to +15V
PHASE to GND
DC ---------- -1V to 15V
< 200ns ---------- -3V to 30V
BOOT to PHASE ---------- -0.3V to +15V
UGATE to PHASE ---------- -0.3V to (BOOT - PHASE +0.3V)
PVCC9, VCC9, LDRV ---------- -0.3V to VCC12 + 0.3V
LGATE ---------- -0.3V to + (PVCC9 + 0.3V)
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
θ_{JA} SOP-14 ---------- 120°C/W
θ_{JC} QFN3x3-16 ---------- 5°C/W
θ_{JA} QFN3x3-16 ---------- 68°C/W
Power Dissipation, P_D @ T_A = 25°C
SOP-14 ---------- 0.83W
QFN3x3-16 ---------- 1.47W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC12} ---------- +10.8V to 13.2V

Electrical Characteristics

(V_{CC12} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC12}		10.8	--	13.2	V
Supply Current	I_{CC12}	UGATE and LGATE Open; V_{CC12} = 12V, Switching	--	4	--	mA
Quiescent Supply Current	I_{CC12_Q}	V_{FB} = V_{REF} + 0.1V, No Switching	--	3	--	mA
Power Input Voltage	V_{IN1}		3.0		13.2	V
Power On Reset						
VCC12 POR Threshold	$V_{CC12RTH}$		--	8.7	--	V
PVCC9 POR Threshold	$V_{VCC9RTH}$	PVCC9 = VCC9 rising	--	7.5	8	V
POR Hysteresis	V_{CC9HYS}	PVCC9 = VCC9 falling	--	0.8	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PVCC9 LDO						
PVCC9 Output Voltage	PVCC9	V_{CC12} = 12V	--	9.0	--	V
Oscillator and Soft Start						
Switching Frequency	f_{OSC}	R_{RT} = 45.3kΩ	540	620	700	kHz
Sawtooth Amplitude	ΔV_{OSC}		--	4	--	V
Soft Start Interval	T_{SS}	f_{OSC} = 620kHz	--	6.8	--	ms
Reference Voltage						
Reference Voltage for PWM	V_{REF}		0.788	0.8	0.812	V
Reference Voltage for LDO	V_{REF}		0.784	0.8	0.816	V
Error Amplifier for Buck Controller						
Open Loop DC Gain	A_O	Guaranteed by Design	55	70	--	dB
Gain-Bandwidth Product	GBWP	Guaranteed by Design	--	10	--	MHz
Slew Rate	SR	Guaranteed by Design	4	6	--	V/us
COMP High Output Voltage	V_{COMP_H}		--	4.7	--	V
COMP Low Output Voltage	V_{COMP_L}		--	0.6	--	V
COMP High Source Current	I_{COMP_H}		--	-2.8	--	mA
Undervoltage Level (V_{FB}/V_{REF})	V_{UVP}		70	75	80	%
Buck Controller Gate Drivers						
UGATE Source Current	I_{UG_SRC}	PV_{CC} = 9V, V_{BOOT} - V_{UG} = 8V	--	-1.5	--	A
UGATE Sink Output Impedance	R_{UG_SNK}	PV_{CC} = 9V, I_{UG} = 100mA	--	2	4	Ω
LGATE Source Current	I_{LG_SRC}	PV_{CC} = 9V, V_{LG} = 1V	--	-1.5	--	A
LGATE Sink Output Impedance	R_{LG_SNK}	PV_{CC} = 9V, I_{LG} = 100mA	--	2	4	Ω
Maximum Duty Cycle			70	75	80	%
Linear-Regulator Controller						
Open Loop DC Gain	A_O	Guaranteed by Design	55	70	--	dB
Gain-Bandwidth Product	GBWP	Guaranteed by Design	--	2	--	MHz
Slew Rate	SR	Guaranteed by Design	2	4	--	V/us
FB Bias Current	I_{FB}	V_{FB} = 0.8V	--	0.01	1	uA
LDRV High Output Voltage	V_{LDRV_H}	PVCC = 9V	--	8.5	9.0	V
LDRV Low Output Voltage	V_{LDRV_L}	PVCC = 9V	--	0.0	0.5	V
LDRV High Source Current	I_{LDRV_H}		5	--	--	mA
LDRV Low Sink Current	I_{LDRV_L}		5	--	--	mA
Undervoltage Level (V_{LFB}/V_{REF})	V_{UVP}	Percent of Nominal	70	75	80	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
Over Current Threshold	V_{PHASE}	R_{LGATE} = open	--	-375	--	mV
Enable Threshold	$V_{RT/DIS}$		0.3	0.4	0.5	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

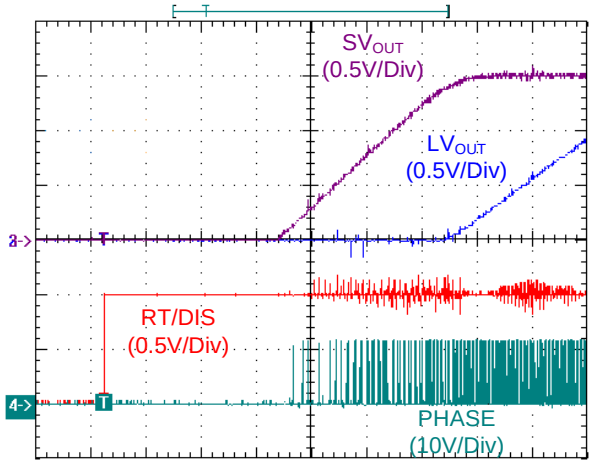
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

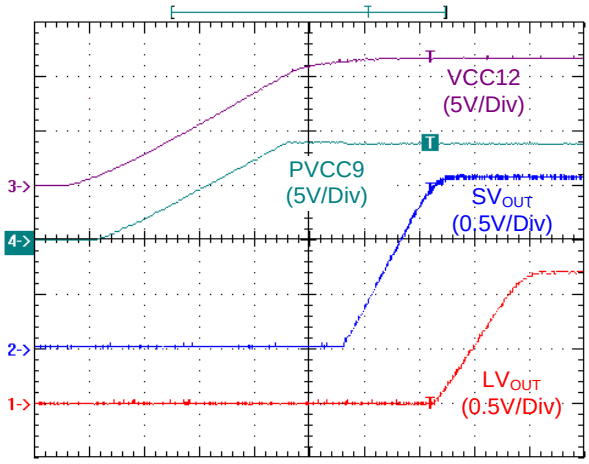
Typical Operation Characteristics

Turn On Waveforms



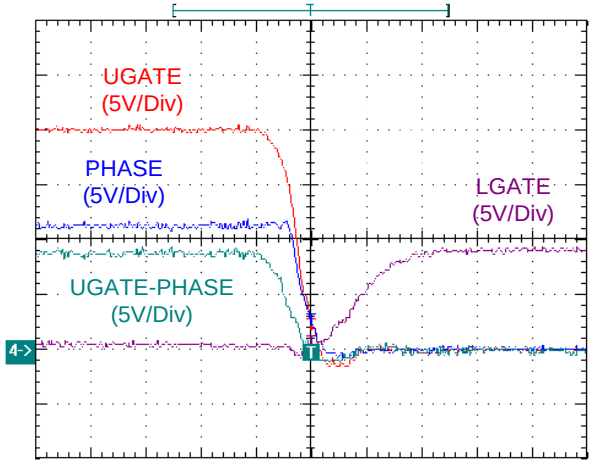
2.5ms/Div

Power On Waveforms



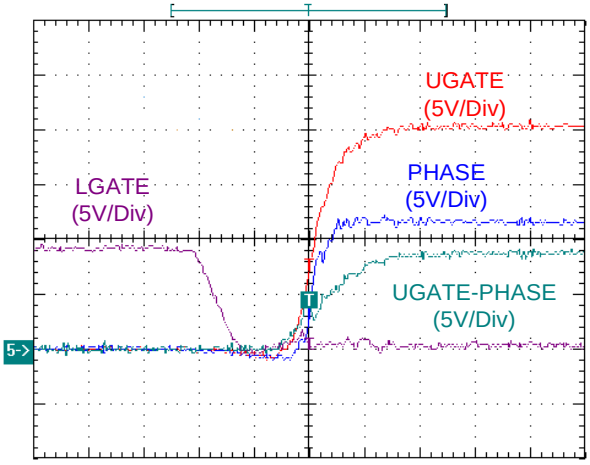
5ms/Div

Gate Waveforms



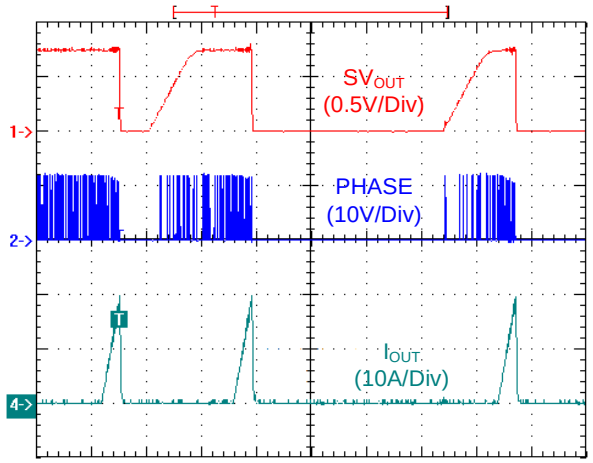
25ns/Div

Gate Waveforms



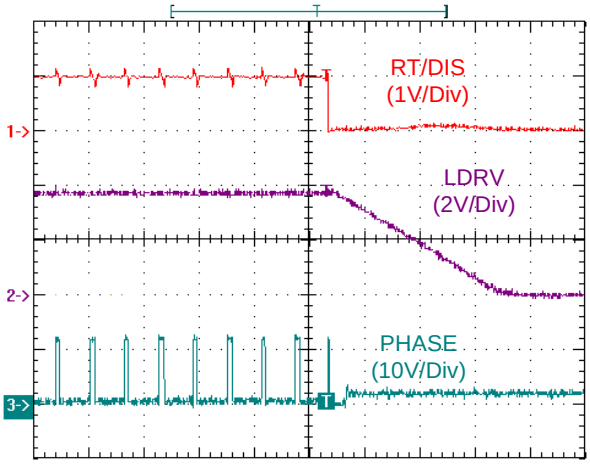
25ns/Div

Over Current Protection



10ms/Div

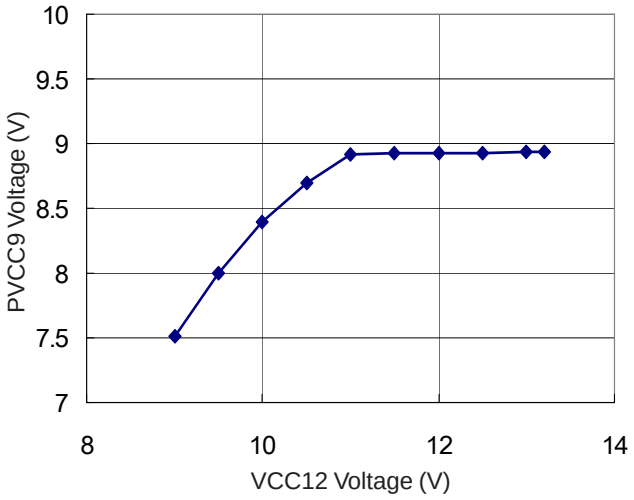
Trun Off Waveforms



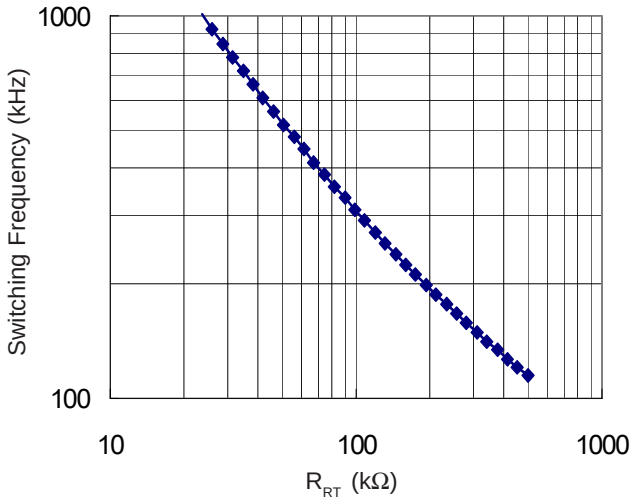
5us/Div

Typical Operation Characteristics

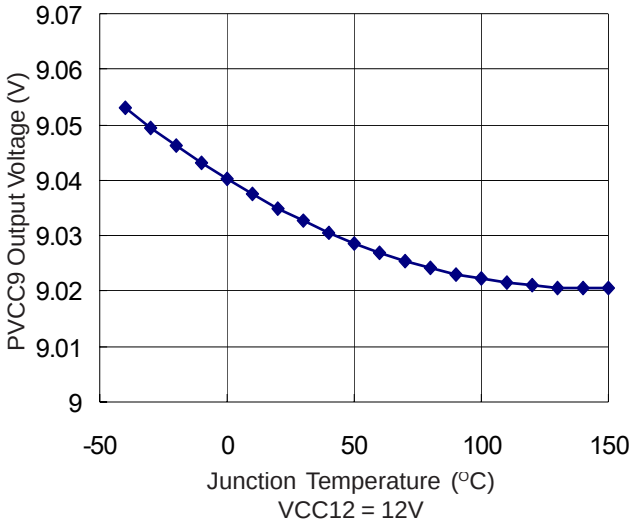
PVCC9 Voltage vs. VCC12 Voltage



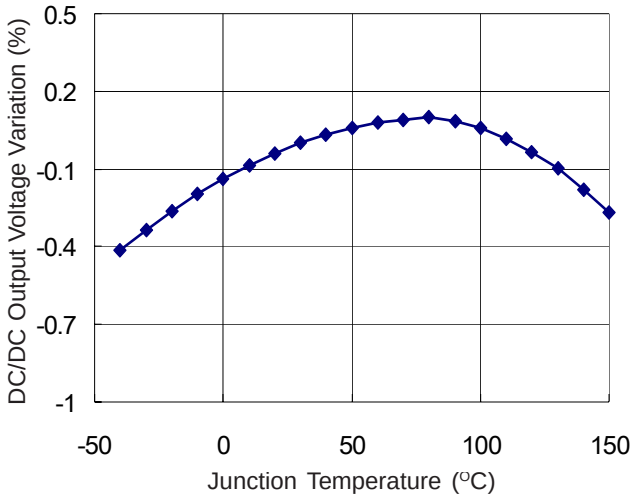
Switching Frequency vs. R_{RT}



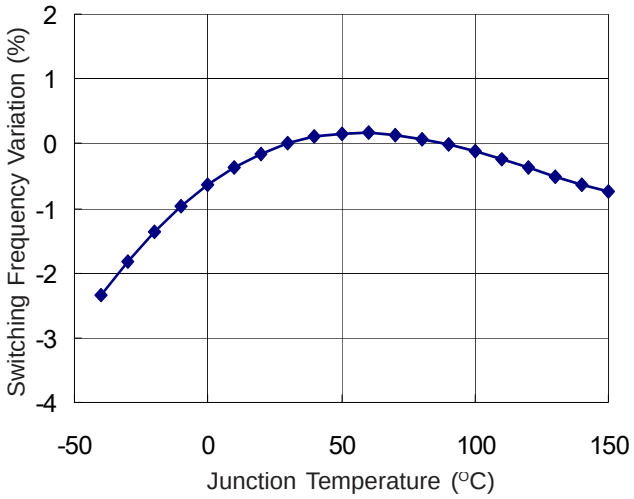
PVCC9 Voltage vs. Temperature



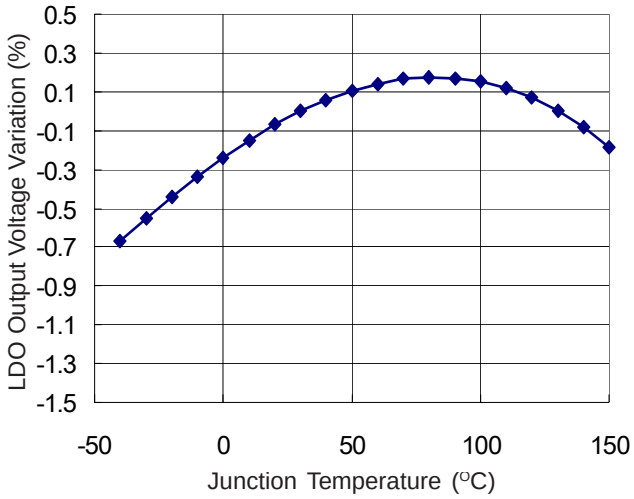
DC/DC Output Voltage vs. Temperature



Switching Frequency vs. Temperature



LDO Output Voltage vs. Temperature



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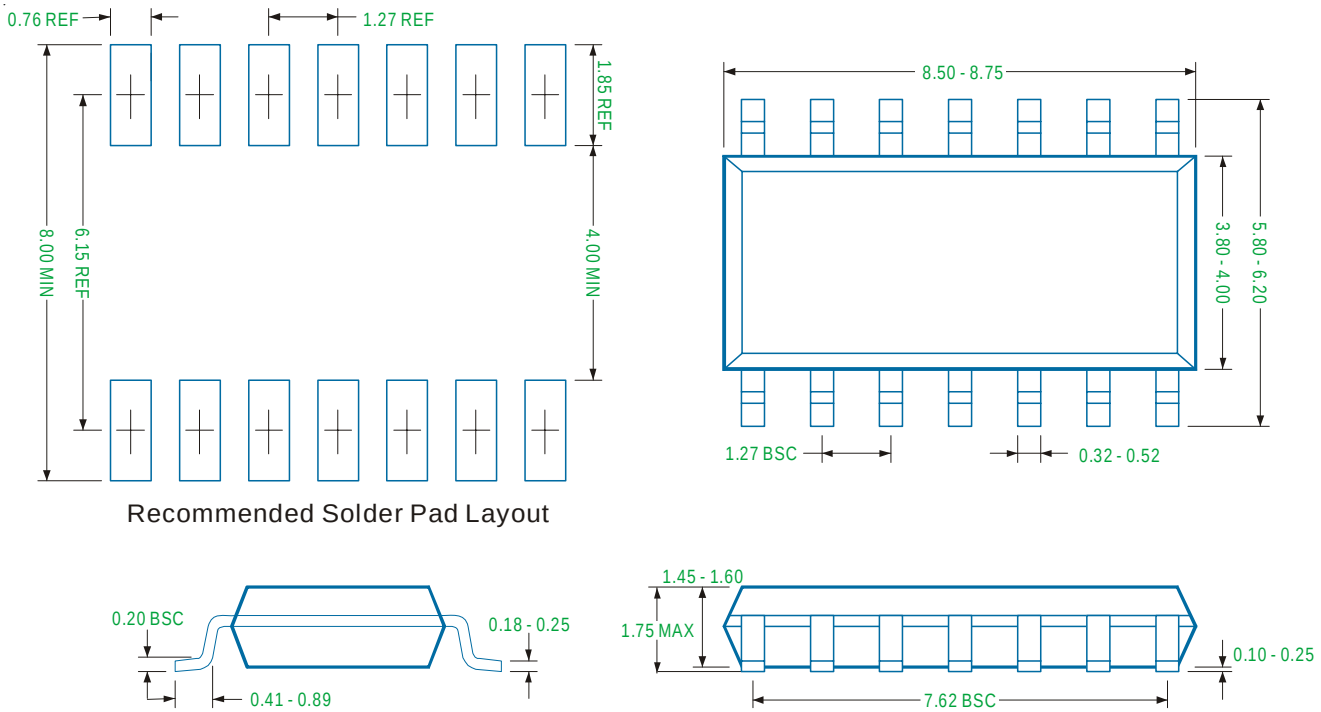
Package Information

SOP-14 Package

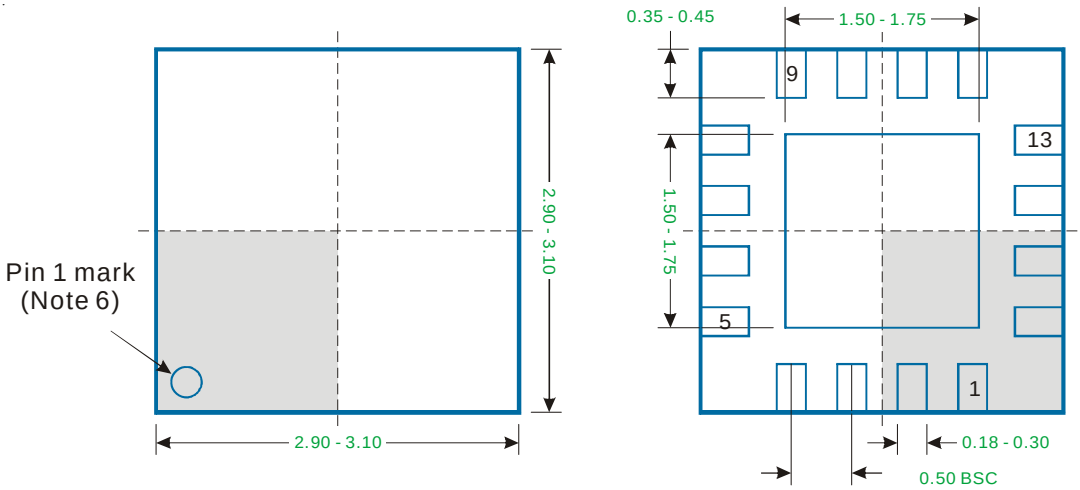


Note

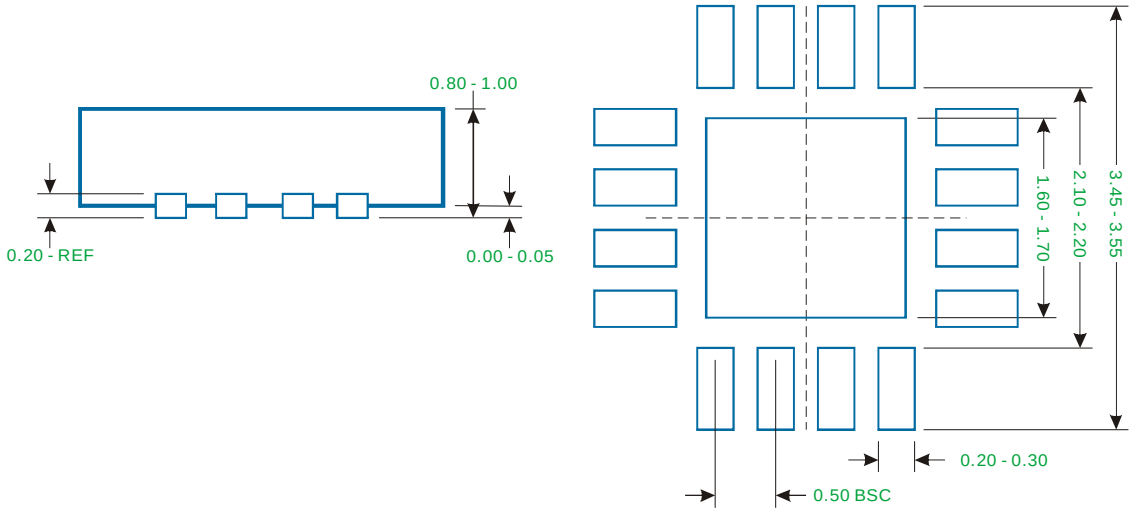
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

QFN3x3 - 16L Package



Bottom View - Exposed Pad



Recommended Solder Pitch and Dimensions

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