design ideas

Edited by Bill Travis

DDS circuit generates precise PWM waveforms

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Pulse-width modulation is a simple way to modulate, or change, a square wave. In its basic form, the duty cycle of the square wave changes according to some input. The duty cycle is the ratio of high and low times in the square wave. A waveform with a 50% duty cycle would be high for 50% of the time and low for 50% of the time, and a waveform with a 10% duty cycle would be high for 10% and low for 90%. Many applications exist for PWM, including motor control, servo control, light dimming, switching power supplies, and even some audio amplifiers. In applications such as MEMS (micro-electromechanical-system) mirror-actuator control, a feedback system needs to regulate the PWM. A circuit monitors and controls the PWM output and varies the duty cycle according to the requirements of the application. The output frequency tunes the actuator, and the duty cycle sets the actuator's speed. The feedback loop controls the threshold level. This Design Idea describes a high-frequency, high-resolution PWM with feedback control. First, it might be useful to discuss some PWM theory.

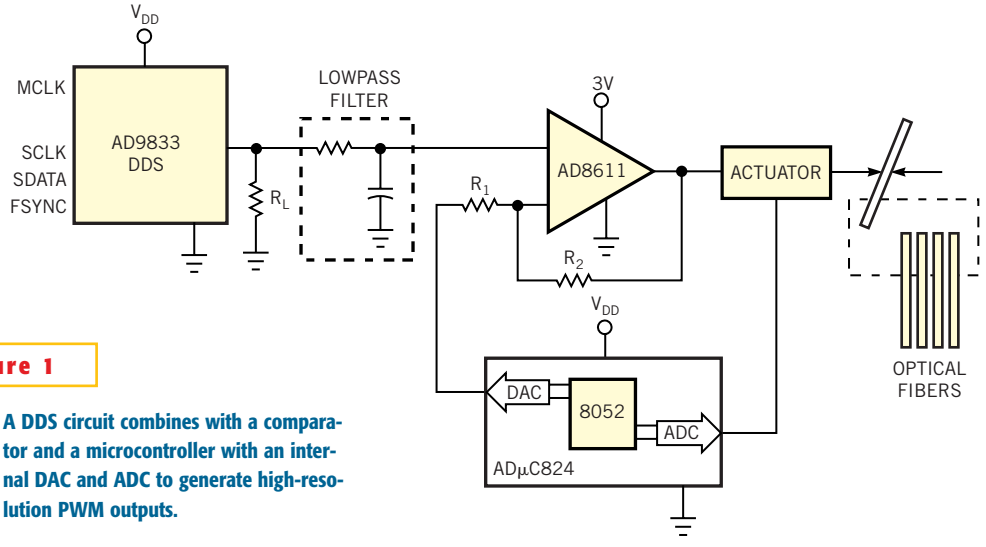

Figure 1

A DDS circuit combines with a comparator and a microcontroller with an internal DAC and ADC to generate high-resolution PWM outputs.

ALTERNATIVE ARCHITECTURES

Traditional PWMs use two op amps to generate a sawtooth waveform, a potentiometer to generate a dc reference, and a comparator to generate the PWM output. The advantage of this type of design is that the circuit is practical and inexpensive. Unfortunately, you cannot easily program the frequency without changing component values, and fine-frequency tuning is difficult. Another problem with this method is that accurate control of the duty cycle is difficult. You could use a digital potentiometer in place of the mechanical one, but this replacement results in a more costly design. A second method for generating PWM waveforms uses an ADμC824 MicroConverter. In addition to providing two PWM outputs, it also integrates ADCs, DACs, an 8052-compatible microcontroller, and flash memory. You can configure the PWM with resolution as high as 16 bits. However, the programmed frequency affects the resolution of the PWM. The frequency and resolution of the PWM are as follows: $F_{PWM} = 16.777$ MHz/N, where N is the resolution in bits.

An internal PLL derives the 16.77-MHz reference clock from a 32-kHz crystal. This reference clock samples the output of the PWM. As stated, N, the number of bits, is the resolution of the PWM. For 16-bit resolution the maximum frequency is 266 Hz. The resolution at 200 kHz drops to approximately 6 bits. Thus, the ADμC832 is the ideal low-cost approach for low-frequency, high-resolution applications but not for a high-frequency, high-resolution application.

DDS IMPLEMENTATION

Applications requiring high-resolution frequency tuning and pulse-width-modulation tuning in real time can use a DDS (direct digital synthesizer) to provide a high-accuracy sawtooth waveform with fine-frequency resolution across a large bandwidth. You can then use this signal as the input to a comparator in either

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open- or closed-loop applications. **Figure 1** shows an easy method of generating programmable square waves with programmable duty cycles. The AD9833 DDS drives a programmable triangular wave into one input of the AD8611 comparator and controls the frequency of the output waveform. The feedback loop from the actuator controls the threshold level of the comparator. The AD8611 is a single 4-nsec comparator with a latch function and complementary output. The input signal from the DDS connects directly to the inverting input of the comparator. The output feeds back to the noninverting input through R_1 and R_2. The ratio of R_1 to R_1+R_2 establishes the width of the hysteresis window with V_{DAC} setting the center of the window or the average switching voltage. The output switches low when the input voltage is greater than V_{HI} and does not switch high again until the input voltage is lower than V_{LO}, as the following expressions show: $V_{HI}=(V^+-1.5\ V-V_{DAC})(R_1/(R_1+R_2))+V_{DAC}$, and $V_{LO}=V_{DAC}(R_2/(R_1+R_2))$, where V^+ is the positive supply voltage to the comparator and V_{DAC} is the level that the DAC sets. The AD8611 can accept a 100-MHz signal with 400-mV p-p levels and can also accept input signals in the tens of millivolts. The AD9833 can provide sinusoidal- and triangular-wave outputs using the DDS architecture. It includes a numerical-controlled oscillator employing a 28-bit phase accumulator, a sine ROM, and a 10-bit D/A converter on a single chip (**Figure 2**).

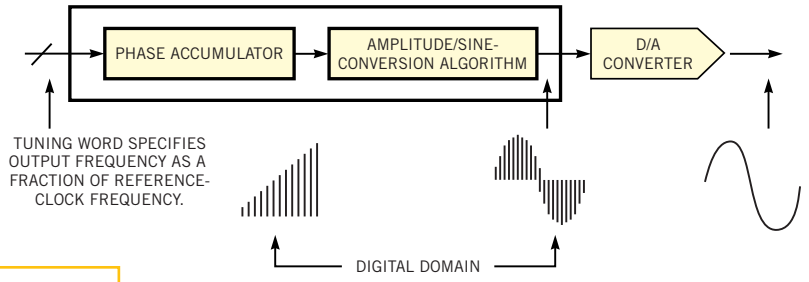

Figure 2

A DDS circuit includes a numerical-controlled oscillator employing a 28-bit phase accumulator, a sine ROM, and a 10-bit D/A converter on a single chip.

You typically think of sine waves in terms of their magnitude expression: $a(t)=\sin(vt)$. However, these waveforms are nonlinear and are difficult to generate. On the other hand, the angular information is linear in nature. That is, the phase angle rotates through a fixed angle for each unit in time. Knowing that the phase of a sine wave is linear and given a reference interval (clock period), you can determine the phase rotation for that period:

$\text{Phases}=\omega dt;$

$\omega=\Delta\text{Phase}/dt;$

$f=(\Delta\text{Phase}\times f_{MCLK})/2\pi,$

where dt is the reciprocal of f_{MCLK}, the master clock. You can generate output frequencies using this formula, knowing the phase and master-clock frequency. The phase accumulator provides the 28-bit linear phase. The sine ROM stores the amplitude coefficients of the output sine wave in digital format. The DAC converts the sine wave to its analog domain. If you bypass the sine ROM, the part delivers triangular waveforms instead of sinusoidal waveforms. You program the device by writing to the frequency registers. The analog output from the part is then $f_{OUT}=(f_{MCLK}/228)\times(\text{frequency-register word})$.

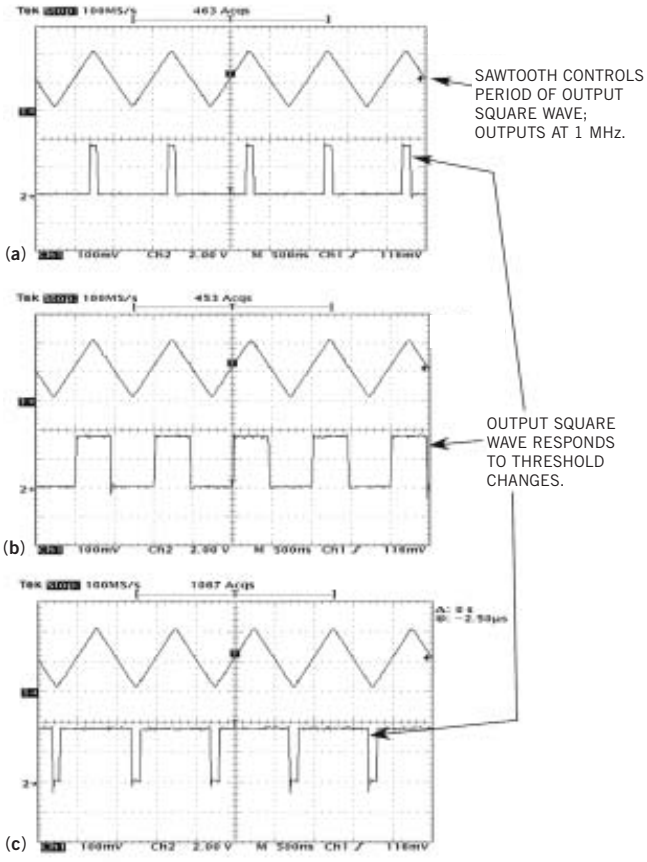

Figure 3

Applying different thresholds to the comparator in the circuit of Figure 1 has these effects.

The DDS outputs have 28-bit resolution, so effective frequency steps on the order of 0.1 Hz are possible to a maximum of approximately 10 MHz. Two phase registers provide 12-bit phase resolution. These registers phase-shift the signal by $P_{SHIFT}=(2\pi/4096)\times(\text{phase-register word})$. A 25-MHz crystal oscillator provides the master reference clock for the DDS. The output stage of the DDS is a voltage-output DAC with a typical swing of 0.7V p-p into an internal 200Ω resistor. Adding load resistor R_L reduces the peak-to-peak output voltage, thus allowing you to tune the peak-to-peak output of the DDS to the input range of the comparator. A filter stage generally appears on the output

of the DDS. The purpose of this stage is to filter feedthrough from the reference clock, images, and higher frequencies and to bandlimit the signals under consideration.

Figure 3 shows typical output plots from the AD8611 comparator in **Figure 1**. The input signal from the DDS is a triangle wave set to 1 MHz. Each plot shows the PWM output for various threshold voltages. In the closed-loop circuit of **Figure 1**, you can tune the output of the PWM to 12-bit accuracy. You have access to many possible ways of providing pulse-width modulation; the approach depends on the application. For low-resolution applications, traditional methods using op amps and potentiometers are acceptable and inexpensive. For low-frequency, high-resolution applications, the ADμC832 provides a one-chip approach with added features for free. For high-resolution, high-frequency applications requiring fine-frequency tuning, you can combine a DDS and a comparator to generate precise, high-frequency PWM waveforms.□

High-CMRR instrumentation amp works with low supply voltages

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Modern battery-cell voltages of 3 to 3.6V require circuits that offer efficient low-voltage operation. This Design Idea proposes an ac-coupled instrumentation-amplifier design that features high CMRR (common-mode-rejection ratio), wide dc input-voltage tolerance, and a first-order highpass characteristic. Most of these features stem from a high-gain first-stage design. The circuit uses popular-value and -tolerance components. **Figure 1a** shows the simplified amplifier circuit. The general principle is that the capacitor, C, and the R_3 resistors buffer and ac-couple the input signal. The second stage comprises two differential amplifiers, A_D. Each of them amplifies half the differential input signal. A summing operation yields the following expression for V_{OUT}:

$$V_{OUT} = A_D(V_A - V_B + V_C - V_D) = A_D\left(\frac{2sR_3C}{1+2sR_3C}\right).$$

In **Figure 1a**, V_A, V_B, V_C, and V_D are the two differential amplifiers' inputs, and A_D is the gain. The time constant $2R_3C$ defines the highpass cutoff frequency. **Figure 1b** shows the detailed circuit. The input stage comprises op amps A_1, A_2, A_3, and A_4. A_1 and A_2 are the main gain stages. Because their inverting and noninverting inputs are at the same potential, the input voltages supply the R_3 resistors. The buffers A_3 and A_4, along with the R_2 resistors, produce an amplification factor, $1+R_3/R_2$, for the current in R_3, because R_2 and R_3 connect to equal potentials. This circuit structure is the heart of the design. The voltage on capacitor C has no ac component, and A_1 and A_2 each amplifies one-half of the differential-input ac signal. C filters the input dc component, which appears at the A_3 and A_4 outputs. The second stage is a unity-gain, four-input adder-subtracter stage. It implements the above equation, where A_D is $1+R_1/(R_2||R_1)$. Assuming $R_3>>R_2$, $A_D=1+R_1/R_2$.

Another possible implementation for the second stage could use two differential-channel ADCs, producing a

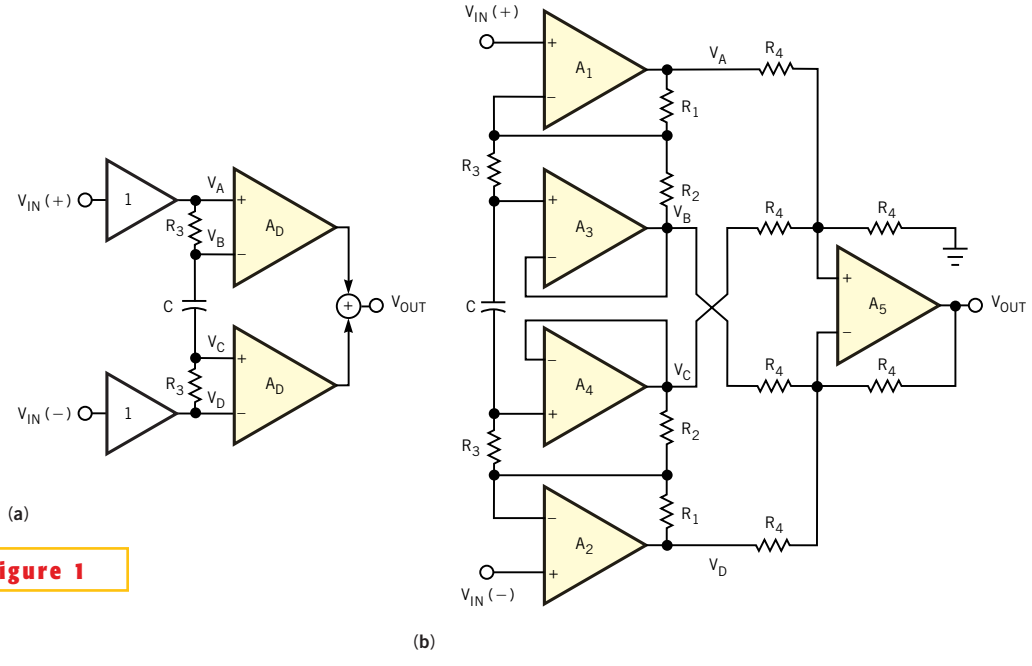

Figure 1

Capacitor C ac-decouples the simplified amplifier circuit (a); the detailed circuit (b) uses gain stages and an adder-subtracter stage.

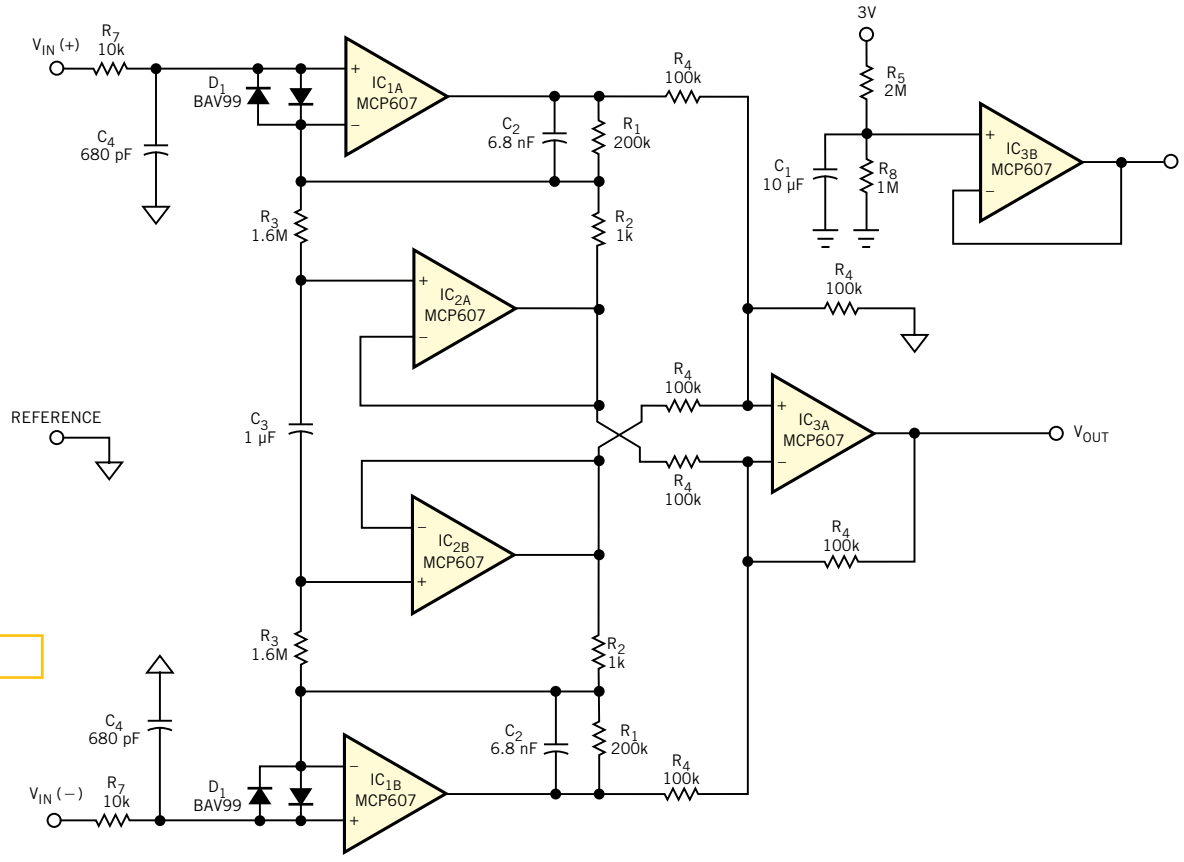

Figure 2

This high-CMRR instrumentation amplifier operates from extremely low supply voltages.

digitized V_{OUT}, ready for microcomputer processing. If a ±5V supply is available, it is possible to obtain V_{OUT} by using two difference amplifiers on one chip, such as the INA2134. You can calculate the minimum CMRR as:

$$\text{CMRR} = \frac{A_{D(1-4)}}{A_{CM(1-4)}} \times \frac{A_{D5}}{A_{CM5}} = \frac{A_D}{4\Delta/(1+R_4/2R_4)} = \frac{1.5A_D}{4\Delta},$$

where $A_{D(1-4)}$ is the differential gain of amplifiers A_1 through A_4, $A_{CM(1-4)}$ is the common-mode gain of these amplifiers, A_{D5} is the differential gain of amplifier A_5, and A_{CM5} is the common-mode gain of A_5. Δ is the tolerance of the R_4 resistors in the circuit. A very important parameter is the op amps' input offset voltage, especially for A_3 and A_4. The A_1 and A_2 offsets do not contribute to error, because they add to the input signal's dc component, which capacitor C cancels. The maximum output-voltage error attributable to op-amp offset voltage is:

$$V_{MAX} = \left(V_{IOA3MAX} + V_{IOA4MAX}\right)\left(1+\frac{R_1}{R_2}\right) + 3V_{IOA5MAX} \approx 2A_D V_{IOA34MAX},$$

where V_{IOMAX} are the maximum offset voltages of the corresponding op amps. In selecting op amps, you should note the following: A_3, A_4, and A_5 should be low-offset and high-CMRR types, and A_1 and A_2 should have high open-loop gain, CMRR, and gain-bandwidth products. **Figure 2** shows a practical amplifier circuit. The power supply is one 3V lithium battery. You can use several op-amp types, such as MCP607s or OPA2336s. Because of the input common-mode voltage range, you set the signal ground to one-third of the supply voltage. The D_1 diodes prevent the circuit from latching up. The R_7-C_4 networks provide RF-noise filtering at the inputs. You derive the network's values from the following consideration: With $R_7C_4 = (R_1||R_2||R_3)C_2 \sim R_2C_2$, the high-frequency zero in the amplifier's transfer function cancels:

$$A_D(s) = \frac{V_{OUT}}{V_{IN}(+) - V_{IN}-} = \frac{2sC_3R_3}{(1+sC_4R_4)(1+2sC_3R_3} \times \left(1+\frac{R_1}{R_2 \,||\, R_3}\right) \times \left(\frac{1+sC_2(R_1 \,||\, R_2 \,||\, R}{1+sC_2R_1}\right).$$

The circuit has the following advantages:

- The first stage ensures the overall gain, thus providing high CMRR without the use of high-precision resistors in the second stage.
- By connecting the low-frequency-determining RC network to the inverting inputs of the op-amp pair that amplifies the input signal, the circuit needs no additional input buffers.
- The circuit delivers a standard, first-order highpass characteristic, using passive components with popular values and tolerances.
- The differential-input range is as high as 2V, using a 3V supply.
- The circuit consumes low supply current and power: approximately 120 µA, 0.4 mW.□

Use a DAC to vary LVDT excitation

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LVDTs (linear variable differential transformers) are electromechanical measuring devices that convert the position of a magnetic core into electrical signals. You generate these signals via excitation on the primary side. The results on the secondary side—typically, two secondary windings—depend on the position of the core (**Figure 1**). The excitation typically ranges in amplitude from 1 to 10V and in frequency from 1 to 10 kHz, depending on the type of LVDT you employ. Traditionally, for one circuit to provide such variability in frequency and amplitude, you can use either an LC tank with adjustable components or a sine-wave generator under microcontroller control. It can be difficult to achieve precision over time and temperature with the LC-tank circuit because of variations in passive components. You also must manually perform calibration. You can more easily obtain precision over time and temperature through the use of a microcontroller-controlled sine-wave-generator chip, and calibration can be automatic, but the method incurs a greater expense than the LC-tank circuit. The circuit in **Figure 2** presents an alternative.

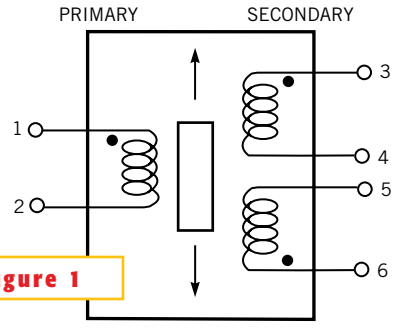

Figure 1

An LVDT is an electromechanical measuring device that converts the position of a magnetic core into electrical signals.

Rather than using a sinusoidal signal to excite the LVDT, a triangular wave comes from the integration of a square-wave output provided by a microcontroller timer. With the use of a current-output DAC, such as the AD7564 from Analog Devices (www.analog.com), you can create a circuit that provides an alternative at a lower cost than that of a sine-wave-generator chip and with greater ease of modification than with an LC-tank circuit. Beginning with the microcontroller, the frequency of the excitation wave depends on the configuration of the microcontroller's timer. You can configure a free-running timer, for example, to toggle the output based on the comparison match of a preset count. You base the count on the desired frequency output and the timer's internal clock rate. You then adjust the output of the microcontroller's timer to remove offset. You need to eliminate as much offset in the signal as possible because such offset adversely affects the transformation process. You can use an op amp to remove the offset because the offset is constant—in this case, half the voltage that powers the microcontroller. In general, you should choose an op amp with low offset and low bias, not only for the difference stage, but also later.

Once you center it about common, the signal becomes a triangular wave. The integrator you use is basically a single-pole, lowpass filter with a configurable (via the DAC) corner frequency. The corner frequency you choose guarantees that integration of the excitation signal occurs. To accommodate variability in frequency and amplitude, the DAC provides an easy interface. With two channels of the AD7564, the circuit can emulate variable resistors for the feed-forward and the feedback of the integrating op amp. (The other two channels could serve for the demodulation gain of each LVDT secondary.) You can use these "resistors" to form the corner frequency for the "lossy" integrator and to establish the gain through the circuit, ensuring that the signal is integrated and that the amplitude of the excitation signal is appropriate for the LVDT.

You need to make several calculations in advance to determine the configura-

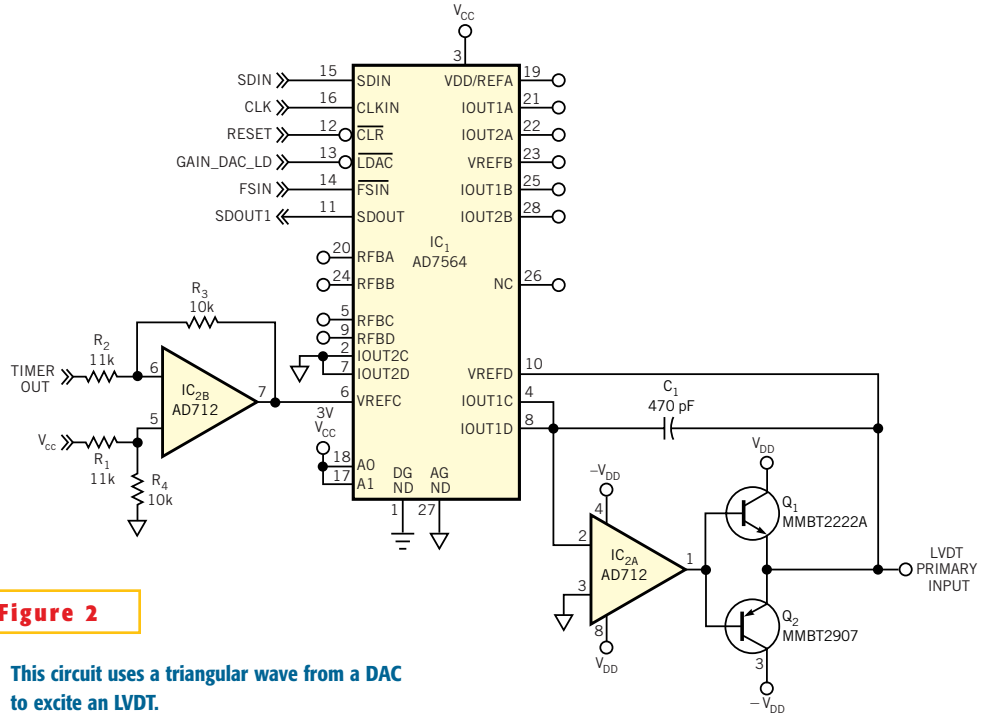

Figure 2

This circuit uses a triangular wave from a DAC to excite an LVDT.

tion of the DAC and the establishment of the resistances. According to the data sheet, the resistance of the R-2R ladder in the Analog Devices AD7564 DAC is typically 9.5 kΩ. You can calculate the feedback resistance using the following formula: $R_{FB}=1/(2\pi f_D C)$, where f_D is the desired corner frequency of the integrator and C is the value of the capacitor you use. You can then assemble the data word for that effective resistance accordingly: $N_{FB}=(4096\times 9500)/R_{FB}$, where N_{FB} is the digital word loaded into the DAC. The feed-forward resistance of the integrator circuit is then $R_I=R_{FB}/(\text{gain factor})$, where the gain factor depends on the desired output amplitude. The data word for that effective resistance becomes $N_I=(R_{FB}/R_I)N_{FB}$ or $N_I=(\text{gain factor})\times N_{FB}$. In most cases, you may need to use additional drive current from the output of the "lossy" integrator to drive the primary coil of the LVDT. This approach may entail the addition of transistors and other components.

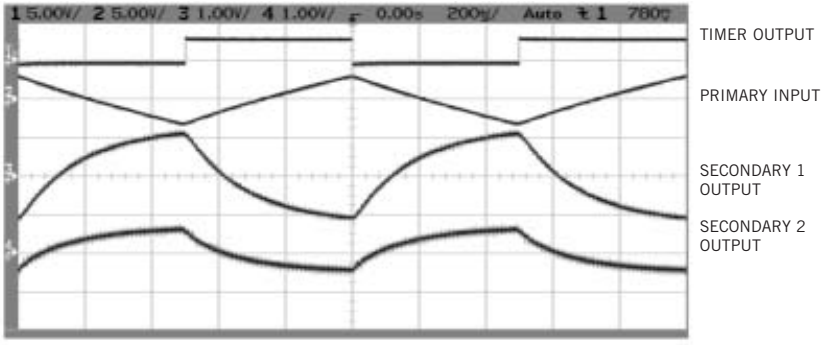

Figure 3 Although what appears on the secondary side differs from the excitation signal, it is sufficient because of the inherent filtering properties of the LVDT.

You have some flexibility in the type of excitation signal the circuit uses because it is common practice to calibrate an LVDT. **Figure 3** illustrates the output of the excitation circuit and the results on the secondary side of the LVDT. Although what appears on the secondary side differs from the excitation signal, it is sufficient because of the inherent filtering properties of the LVDT. The output of each secondary side generally transforms into a constant root-mean-square or mean-absolute-deviation value. In the situation of two secondary coils, a comparison between those values occurs. As long as you excite both coils in the same manner—which is guaranteed because only one primary coil exists—and the output signal is of sufficient resolution, then a triangular wave can excite such an LVDT.□