Edited by Bill Travis

DPPs make nonvolatile microvolt DAC

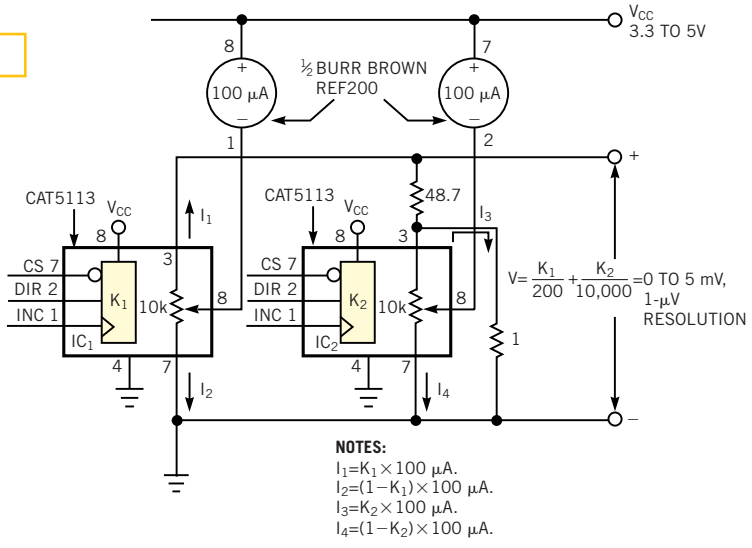
Stephen Woodward, University of North Carolina, Chapel Hill, NC

The availability of a seemingly limitless variety of monolithic DAC chips makes it easy to implement most digital-to-analog-conversion applications with a single off-the-shelf device. Sometimes, an unusual set of requirements necessitates a multichip approach, however. One example of such a requirement is the need for nonvolatility of the DAC's setting in power-up and -down cycles. Another example is the need for output resolution and stability at less than 1 µV. The circuit in **Figure 1** combines inexpensive DPPs (digitally programmed potentiometers) from Catalyst Semiconductor (www.catsemi.com) with precision current references from Burr-Brown (www.ti.com) to achieve both nonvolatility and less-than-1-µV performance. Accurate simulation of the signals from high-temperature platinum-rhodium-based thermocouples requires less-than-1-µV performance. These temperature sensors have Seebeck coefficients of only 6 µV/°C. Therefore, only voltage sources with 1-µV-level stability and precision can simulate such sensors.

To achieve such low output drift would normally require the use of active circuit elements, such as chopper-stabilized amplifiers, with offset temperature coefficients not much higher than 1 nV/°C. The circuit in **Figure 1** takes a different approach by using current division and a passive and, therefore, inherently drift-free output that needs no amplifiers. Each half of the REF200 sources a 100-µA reference current. The twin currents each connect to the wiper of DPPS, IC_1 and IC_2. There, they split into two currents (for example, I_1 and I_2) in a wiper-to-total ratio, K_1, which the programmed setting of the DPP determines. $I_1=K_1\times100$ µA, and $I_2=(1-K_1)\times100$ µA. I_1 passes through the series combination of the 48.7Ω resistor and the 1Ω output resistor and thereby generates the output voltage: $V=K_1(50\Omega\times100\ \mu A)=0$ to 5 mV as K_1 varies from 0 to 1. The operation is straightforward and drift-free. Unfortunately, the resolution with a single potentiometer is inadequate for many precision applications.

IC_1, a CAT5113, like other DPPs, offers the versatility of an uncommitted resistance element and nonvolatility of the setting. Its resolution, however, is only 100 steps, which is slightly worse than 7 bits and equivalent to 50 µV in this circuit. You therefore incorporate a second DPP, IC_2, in the converter. IC_2's output current acts into the 1Ω load for a 50-to-1 resolution enhancement over IC_1 alone. IC_2 thus adds a 0- to 100-µV contribution to V. Hence, the composite output is $V=K_1/200+K_2/10{,}000$ with a 5-mV span and 1-µV resolution. The circuit is an ideal approach for such applications as the simulation of thermocouple signals in precision temperature-measurement and -control systems.

Figure 1



Digitally programmed potentiometers combine to form a novel, microvolt-level DAC.

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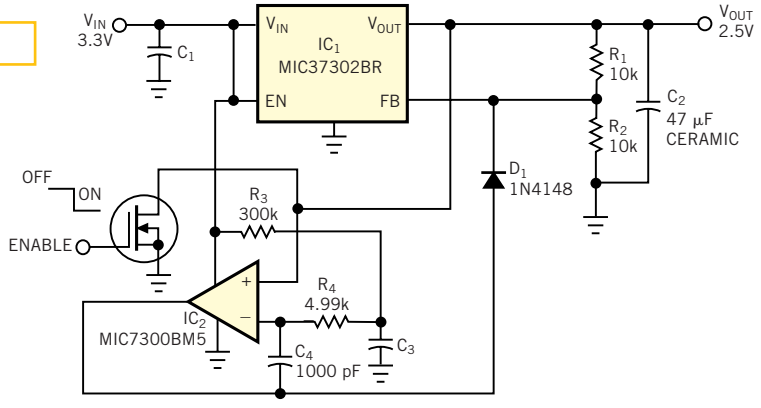
Circuit manages power-up sequencing

Martin Galinski, Micrel Semiconductor, San Jose, CA

Power sequencing poses a unique problem in power management. Because improper sequencing may cause damage to many types of processors, power-up sequencing of these devices is critical. Devices that may require power-up sequencing control include FPGAs, ASICs, and DSP chips. These devices can require tracking I/O and core voltages. Requirements for power-up sequencing may change according to device type and manufacturer, so it's important that you review sequencing requirements for each device. This design use Xilinx's (www.xilinx.com) power-up requirements for the Spartan-II and Spartan-IIE families. The I/O voltage must reach full supply voltage in 2 to 50 msec. Also, the slew rate of the supply voltage must not exceed 900 mV/msec but must exceed 50 mV/msec. The circuit in **Figure 1** addresses these issues, allowing for consistent and reliable power-up sequencing.

The power-up sequencing circuit uses an RC (R_3 and C_3) timing network to control the slew rate of the output during turn-on. IC_2 compares the output of the low-dropout regulator with the voltage at the RC network. It then adjusts the output of the regulator, via the feedback voltage, to match the RC charge voltage. When the voltage between R_3 and C_3 reaches the low-dropout regulator's regulation voltage, the output of IC_2 pulls low, reverse-biasing D_1, thereby removing the power-up sequencing circuit from the control loop. R_4 and C_4 provide compensation to maintain a smooth voltage during the turn-on cycle. R_1 and R_2 provide the output regulation voltage. You can calculate R_1 and R_2 from the following expression: $R_1 = R_2 (V_{OUT}/1.240 - 1)$. **Figure 2** shows slewing characteristics of the output with various values of C_3.

Figure 1



This circuit controls the power-up sequencing for Xilinx's Spartan ICs.

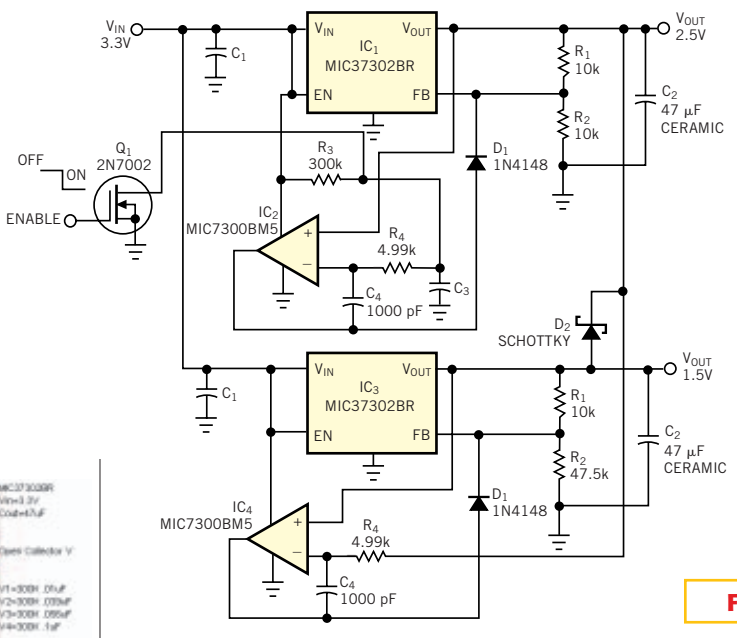


Figure 3

This circuit controls the I/O and core-voltage power-on and power-off sequencing.

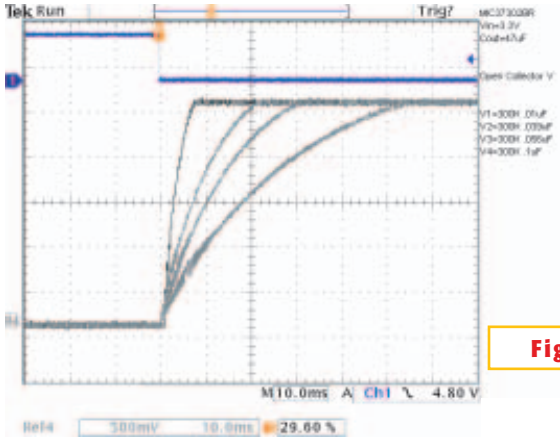


Figure 2

C_3 controls the rise time of the output of Figure 1's circuit.

Figure 3 is an I/O and core-voltage-sequencing circuit. Instead of using an RC charge voltage to control the turn-on, IC_3 of the core regulator compares the output of the I/O during turn-on and matches the core voltage until it reaches the regulation voltage. **Figure 4** shows the I/O and core voltages during the power-on cycle. Equally important is the power-down cycle. The I/O voltage must never reach 0.6V below the core voltage. This condition can forward-bias the substrate diode, damaging the processor. D_2, a Schottky diode with a forward voltage drop of 0.4V, keeps the I/O voltage from dropping 0.6V below the core voltage during the power-down cycle (**Figure 5**).

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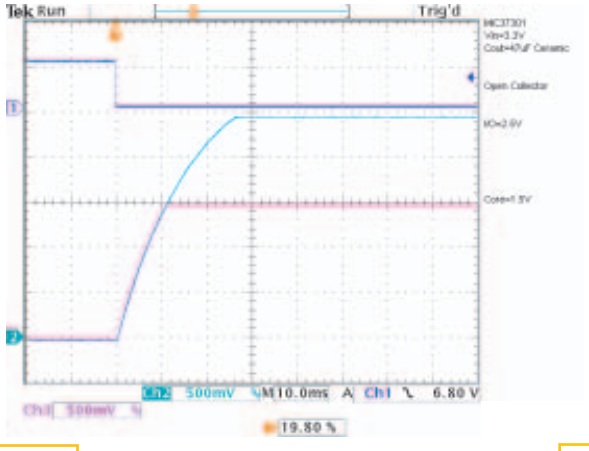


Figure 4

The I/O and core voltages have controlled rise times during the power-on phase.

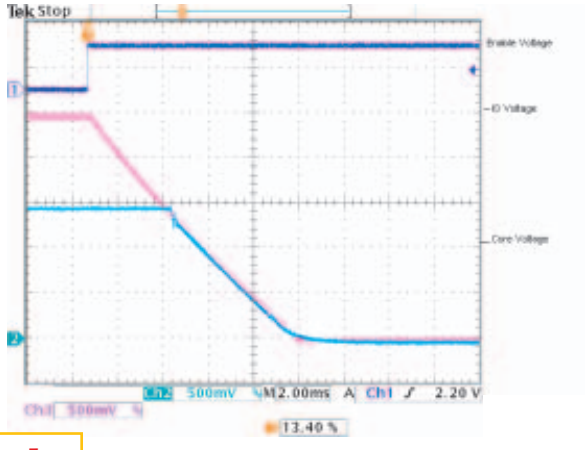


Figure 5

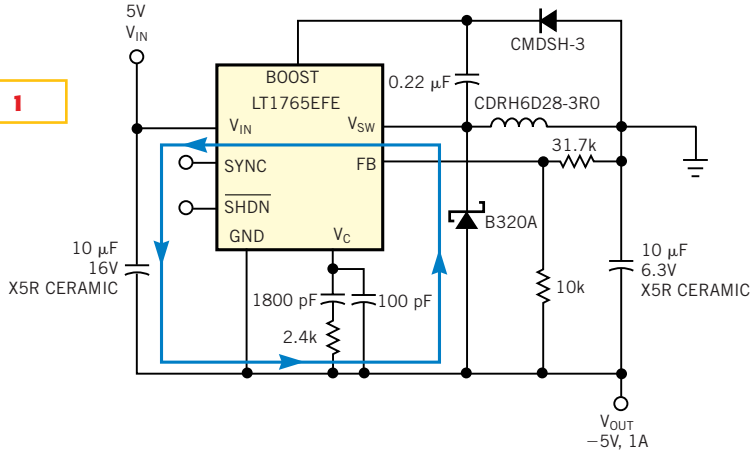
A Schottky diode keeps the I/O voltage from dropping 0.6V below the core voltage.

Lower dc/dc-converter ripple by using optimum capacitor hookup

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Low-ripple-voltage positive-to-negative dc/dc converters find use in many of today's high- frequency and noise-sensitive disk drives, battery-powered devices, portable computers, and automotive applications. Like a positive buck converter, a positive-to-negative converter can have low output-ripple voltage if you place the bulk input capacitor between V_{IN} and V_{OUT} rather than between V_{IN} and ground. A common misconception is that positive-to-negative converters in the first configuration have noisy outputs. This configuration actually solves noise problems rather than introducing them. In either configuration, the V_{IN} and ground pins of the IC connect to V_{IN} and V_{OUT}, respectively (**figures 1** and **2**). Therefore,

Figure 1



This +5-to-−5V converter with the bulk input capacitor between V_{IN} and V_{OUT} has low output ripple. The high-di/dt path, indicated here with blue lines, does not include the output capacitor.

placing the input capacitor between V_{IN} and V_{OUT} is equivalent to placing it between the IC's V_{IN} and ground pins (**Figure 1**). The other, commonly accepted method of placing the bulk input capacitor between V_{IN} and ground (**Figure 2**) significantly increases the output-voltage ripple (**figures 3** and **4**). To make matters worse, this configuration requires an additional high-frequency bypass capacitor between the V_{IN} and ground pins of the IC.

In simple positive-to-negative converters, such as those in **figures 1** and **2**, the output-voltage ripple is

$$\Delta V_{OUT(P-P)} = ESR_{COUT} \times \Delta I_{COUT(P-P)}.$$

Low-ESR output capacitors, such as ceramics, help to minimize the output-voltage ripple in dc/dc converters. For a given output-capacitor ESR, you can further reduce the output-voltage ripple by minimizing the current ripple that the output capacitor is forced to absorb. In **Figure 2**, the output capacitor is part of the high-di/dt switching-current path, making the output voltage ripple proportionately larger. With the bulk input capacitor placed as shown in **Figure 1**, the peak-to-peak ripple current in the output capacitor is equal to the peak-to-peak ripple current in the inductor: $\Delta I_{COUT(P-P)} = \Delta I_{L(P-P)} = (V_{IN} \times$ duty cycle$)/(f_{SW} \times L)$, where $\Delta I_{COUT(P-P)}$ = output ripple current, $\Delta I_{L(P-P)}$ = inductor ripple current, and f_{SW} = switching frequency.

When the bulk input capacitor is placed as shown in **Figure 2**, the peak-to-peak ripple current in the output capacitor is much higher than the inductor's ripple current alone; it is almost equal to the inductor's ripple current plus the input capacitor's ripple current: $\Delta I_{CIN(P-P)} = I_{L(P)} = I_{OUT} + I_{IN} + \Delta I_{L(P-P)}/2$, and $\Delta I_{COUT\ (P-P)} \sim \Delta I_{L(P-P)} + \Delta I_{CIN(P-P)}$. With much lower output-capacitor ripple current, the output capacitor in the circuit in **Figure 1** can be much smaller than that of the circuit in **Figure 2**. Also, it needs to handle much less rms ripple current (approximately equal to peak-to-peak ripple current divided by the square root of 12). Another advantage of removing the output capacitor from the high-di/dt switching loop (by judicious placement of the input capacitor) is a greatly simplified layout. You must place the high-di/dt components in **Figure 1** in the smallest loop possible to minimize trace inductance and the resulting voltage (noise) spikes. With one fewer component to worry about in the layout, you can more easily create a noise-free circuit using the layout in **Figure 1** than it is using the one in **Figure 2**.

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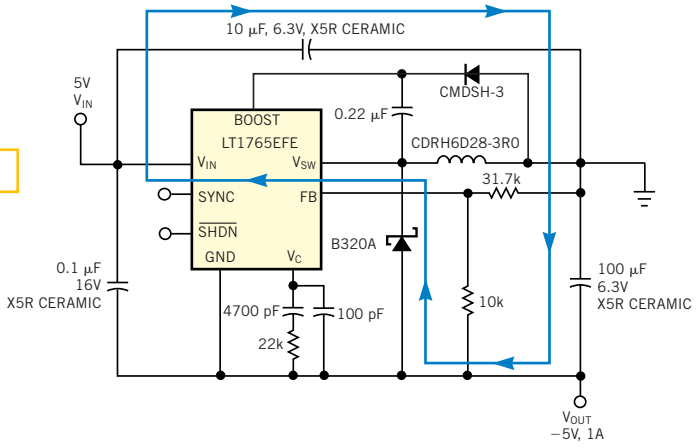


Figure 2 This +5-to–5V converter with the bulk capacitor between V_{IN} and ground has much higher output ripple than the circuit in Figure 1. The high-di/dt path, indicated here with blue lines, includes the output capacitor, thus increasing output ripple.

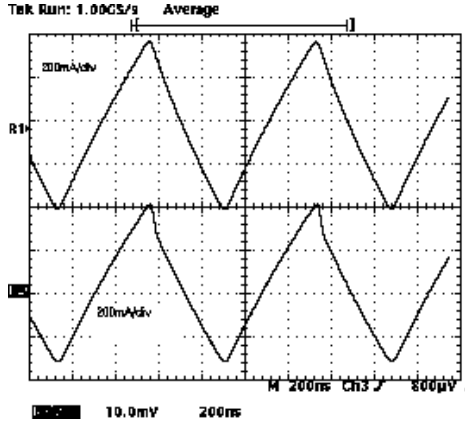


Figure 3 In the circuit in Figure 1, the output capacitor's peak-to-peak current ripple is equal to the inductor's peak-to-peak ripple with 1A output.

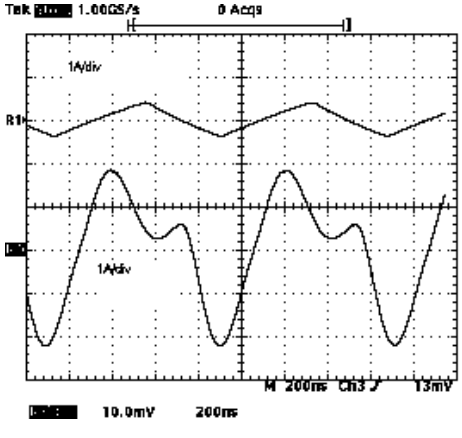


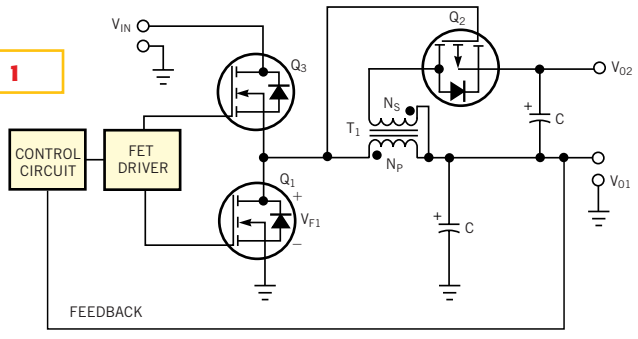
Figure 4 In the circuit in Figure 2, the output capacitor's peak-to-peak current ripple is five times as high as the inductor's peak-to-peak ripple and, therefore, five times as high as the current ripple shown in Figure 3 with 1A output.

Add an auxiliary voltage to a buck regulator

John Betten, Texas Instruments, Dallas, TX

You often need more than one regulated output voltage in a system. A frequently used and reasonably simple way to create this auxiliary output voltage is to add a second winding to the output inductor, creating a coupled inductor or a transformer, followed by a diode to rectify (peak-detect) this output voltage. The biggest drawback of this approach is that the diode's voltage drop varies with temperature and load current and can have a 2-to-1 variation, resulting in poor output-voltage regulation. This problem becomes more critical as output voltages decrease and may require the addition of a linear regulator. The circuit shown in **Figure 1** is an alternative approach that replaces this diode with Q_2, a p-channel FET. The circuit works as follows:

Figure 1



This synchronous buck converter has an auxiliary-output winding.

During the conduction time of FET Q_1, the voltage across the primary winding of transformer T_1 clamps to the voltage, $V_{OUT}+V_{F1}$, where V_{F1} is the voltage drop across FET Q_1. Through transformer action, the voltage on the secondary winding of inductor L_1 is equal to the turns ratio between the windings times the voltage across the primary winding. The output capacitor on the auxiliary output, V_{02}, then charges to the peak of the secondary-winding voltage. FET Q_2 turns off when Q_3 turns back on to prevent the output capacitor from discharging. The secondary voltage floats; you can add it to the main output voltage by tying one end of the secondary winding to the main output. You can also tie it to ground for an output voltage lower than V_{01}, if desired. The equation that defines the auxiliary-output voltage for the circuit in **Figure 1** is:

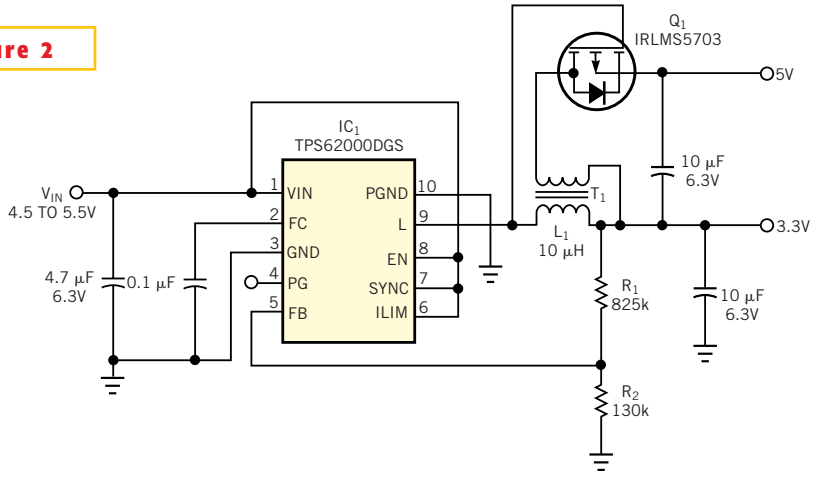
$$V_{02}=V_{01}\left(1+\frac{N_S}{N_P}\right)+\left(V_{F1}\times\frac{N_S}{N_P}-V_{F2}\right).$$

The second half of this equation represents a voltage-error term between FETs Q_1 and Q_2. To cancel out the error attributable to the FET voltage drops, you need to make the voltage drop of FET Q_2 equal to $V_{F2}=V_{F1}\times(N_S/N_P)$, where N_S/N_P is the transformer's turns ratio. Because these FET voltages are a function of the output currents and the on-resistance of the FETs, you can select the on-resistance of FET Q_2 by using the following equation:

$$R_{Q2}=R_{Q1}\times\frac{N_S}{N_P}\times\left[(1-d)\left(1+\frac{I_{01}}{I_{02}}\right)-d\times\frac{N_S}{N_P}\right],\ \text{where}\ d=\frac{V_{01}}{V_{IN}}.$$

In **Figure 2**, the main output voltage is 3.3V, yielding an inductor primary voltage when Q_1 is conducting equal to only 3.44V, because of the low voltage drop across FET Q_1. Thus, if you wanted a 5V output, the secondary winding would need to develop an additional 1.7V, necessitating a 2-to-1 step-down turns ratio. The desired on-resistance of the FET internal to IC_1 from the above equation should be 0.16Ω to cancel the voltage drop across Q_1 at maximum loads and while operating from a 5V input voltage. This example uses a 0.20Ω FET with a voltage drop equal to only 88 mV. This choice allows for good voltage matching between FETs Q_1 and the FET internal to IC_1, resulting in excellent error cancellation, less power loss, and better overall output-voltage regulation than diode rectification provide. An added benefit of this approach is that you can use it with controllers that have integrated switching FETs, because you don't need access to Q_1 and Q_3 gate drives. Measured results, although varying both outputs' loads over their full operational range, showed less than a ±3% variation in the

Figure 2



This circuit is similar to the one in Figure 1, but uses an integrated buck-converter IC.

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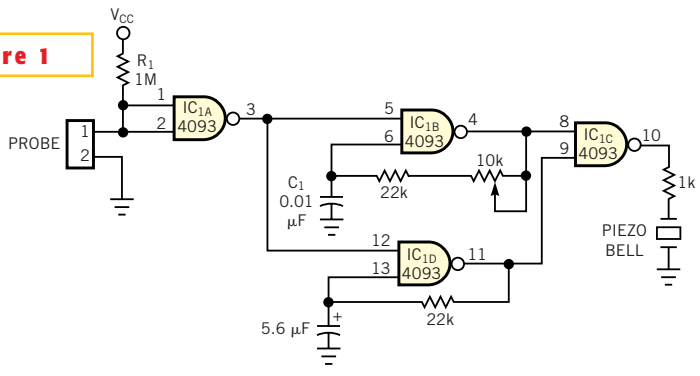
Circuit checks "swamp-cooler" water level

Daniel Krones, Precision Design Services, Sky Forest, CA

A "swamp cooler" is an easy way to obtain effective air conditioning, especially in hot and dry climates, if a water source is readily available. Although most units are very reliable, the storage-reservoir control usually uses a single level-detector component. Failure of this component can lead to serious water damage. The circuit of **Figure 1** provides a simple, inexpensive backup alarm signal if the water level exceeds the preset height. The circuit uses a single Schmitt-trigger IC to detect the water level, using the conductivity of the water to drop the input level of IC_{1A}. A 1- to 10-MΩ resistor is suitable for R_1. You might have to experiment to determine a suitable value, depending on the conductivity of the water supply.

Figure 1



Detect water level in a swamp-cooler reservoir with this simple circuit.

The highest practical vale of R_1 provides the widest range. The NAND gates IC_{1B} and IC_{1D} implement gated oscillators to create a pulsed tone to drive the piezoelectric-bell audible alarm. Current consumption in the off state is lower than 10 µA, thus allowing the use of a simple battery to drive the circuit. A button-cell lithium watch battery is sufficient. The small physical size and wiring simplicity of the circuit allow you to simply glue the unit to the side of the cooler. Use a short piece of twin-lead, 300Ω transmission line for the electrodes.

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