design ideas

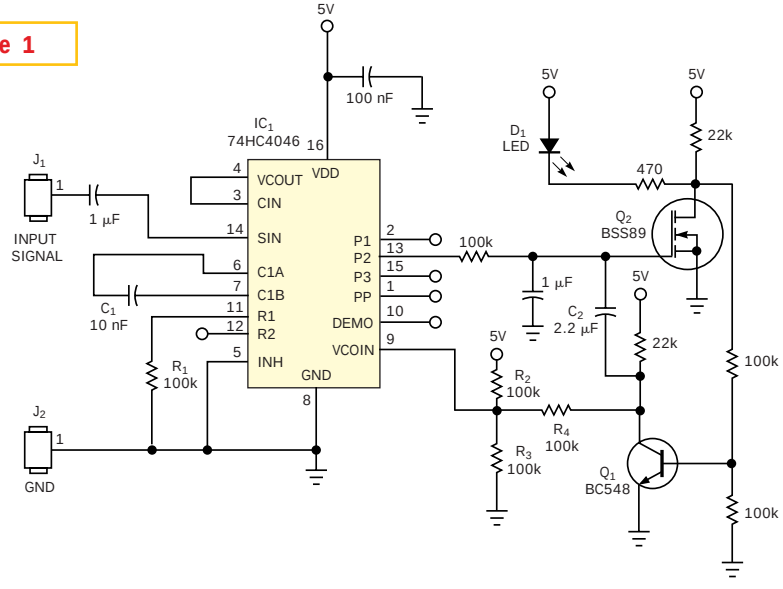
Edited by Bill Travis

Frequency comparator has status output

Susanne Nell, Breitenfurt, Austria

The original application for the circuit in **Figure 1** was to check the number of revolutions of an engine with only one LED as an indicator. The measurement of the number of revolutions usually involves sensors with a frequency output proportional to the number of revolutions. The circuit compares the frequency output of such a sensor with a lower and upper limit and gives a visual result, using one LED. If the frequency is below the lower limit, the LED remains unlit. If the frequency is between the limits, the LED blinks at a constant rate, and if the speed is higher than the upper limit, the LED stays permanently lit. Although a microcontroller can do this job, it is sometimes better to use an analog circuit—for example, if the frequency you want to check is too high for a simple controller. The circuit in **Figure 1** uses one standard, inexpensive IC, and you need not write any software. It is also less costly than a comparable microcontroller-based circuit.

Figure 1



This analog frequency comparator uses an LED to indicate upper and lower frequency limits.

The main part is IC_1, a 74HC4046 PLL chip. With a 12V supply, you can also use the CD4046 without an additional voltage regulator. The chip contains an oscillator, a phase comparator, and one amplifier for the input signal. The input signal connects to the input of the phase comparator with its integrated ac amplifier. The circuit compares this amplified signal with the VCO frequency. This frequency is adjustable, using C_1, R_1, and the voltage on Pin 9. If the frequency of the input signal is lower than that of the VCO, the output of the phase comparator (Pin 13) is low. In this case, Q_2 is off, Q_1 is on, and the LED is off, indicating "low frequency." Resistors R_2, R_3, and R_4 determine the voltage on Pin 9 and the lower frequency limit switching point. If the frequency of the input signal increases and reaches the value of the VCO's frequency, the phase comparator's output switches high.

This high-level output turns Q_2 on and Q_1 off. With Q_1 off, the voltage of the VCO increases to a second higher value determined by R_2 and R_3, and the VCO generates the frequency for the high-limit switching point. If the frequency of the input signal is between these two limits, the phase comparator generates a rectangular waveform. The feedback capacitor, C_2 determines the frequency of this waveform. With a value of 2.2 µF for C_2, you can achieve a frequency of approximately 1 Hz. This frequency is the blinking rate for the LED. If the frequency of the input signal increases to a point higher than the upper VCO frequency value, the phase comparator output stays high, and the LED turns on permanently. With the values shown in **Figure 1**, the lower and upper frequency limits are 3.81 and 7.35 kHz, respectively.

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Envelope follower combines fast response, low ripple

Harry Bissell, Royal Oak, MI

Envelope followers extract amplitude information from complex audio waveforms. The resulting dc voltage often drives nonlinear stages, such as voltage-controlled amplifiers or filters. You must make a careful trade-off between the speed of response to a rapidly changing input signal and the amount of ripple in the dc output that you can tolerate. If the system is too slow, the output has low ripple but badly distorts the envelope shape. If it's too fast, ripple can modulate the nonlinear stages, causing audible distortion products. Audio sources, such as a guitar, pose special problems. The instrument has an attack of a few milliseconds and a long decay time. The musician may "mute" the strings at any time, causing the normal exponential decay to terminate abruptly. The waveform is sometimes unsymmetrical and may have multiple zero crossings. The fundamental frequency range is typically from approximately 80 Hz to 1.5 kHz. Previous circuits have used a full-wave bridge and a large averaging filter. A filter time constant sufficient to reduce ripple makes the circuit unable to follow rapid changes in amplitude. Peak-detecting circuits can follow the rapid attack and provide low ripple during the exponential decay but cannot follow the rapid decay of a muted string. The design in **Figure 1** features fast attack and low ripple with minimal filtering, and it can follow a rapid decrease in signal (mute).

The circuit uses three identical peak-hold circuits in parallel that reset in a round-robin fashion. The circuit applies the input signal to all three stages simultaneously. As each stage resets in turn, the two remaining stages still hold the last peak voltage. Diodes select the highest held voltage at the output of each peak-hold stage. A small RC filter smoothes the step response as the peak-hold circuits reset, so a lower output voltage results. To ensure that one of the detectors holds the highest peak value for the entire input period, the reset clock period is slightly longer than one-half the period of the lowest input frequency. **Figure 2** illustrates typical circuit operation and

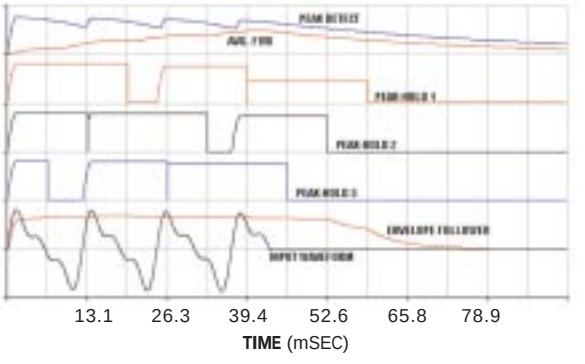
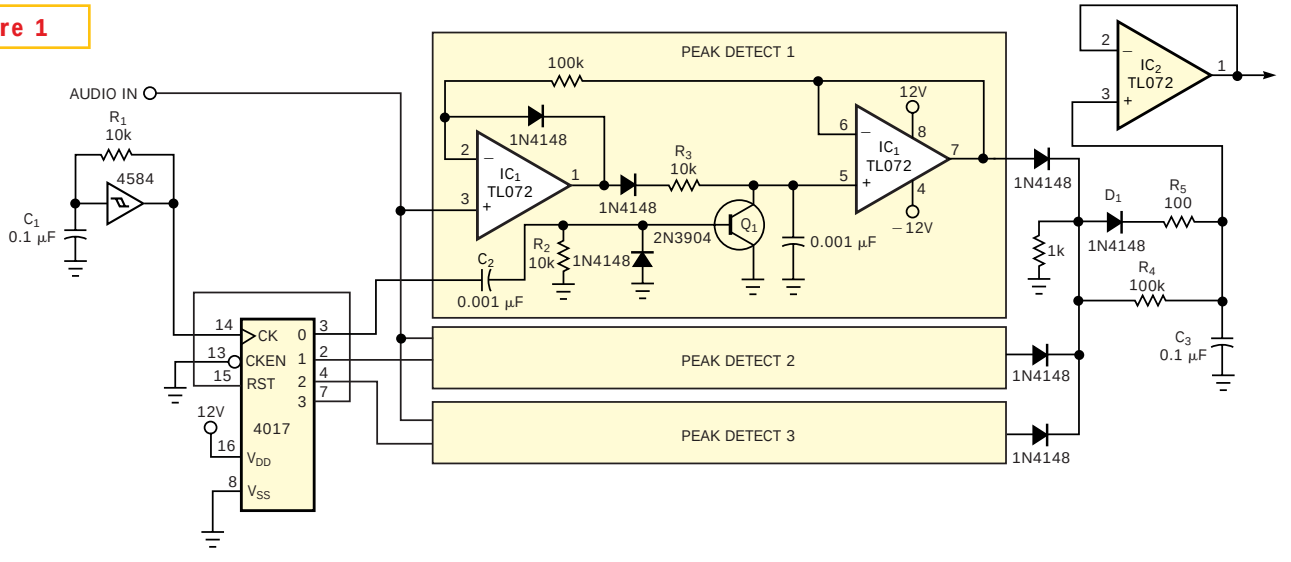


Figure 2 Waveforms of typical circuit operation show the improvement over full-wave average and peak-detecting circuits with similar time constants.

Figure 1



This envelope detector provides the seemingly contradictory features of fast response and low ripple.

shows the improvement over full-wave average and peak-detecting circuits with similar time constants. CMOS Schmitt inverter IC_1 forms the master reset clock, and C_1 and R_1 produce the desired period. CMOS counter IC_2 is a ring counter that provides the sequential reset pulses. The peak-hold circuit is a classic configuration with the addition of the reset circuit. R_2 and C_2 differentiate the rising edge of the reset pulse; this edge drives the base of Q_1. Series resistor R_3 prevents excessive op-amp current while Q_1 is conducting. The filter network comprising R_4, R_5, C_3, and D_1 provides minimal filtering to reduce the step changes in the output during unusually fast decay times.

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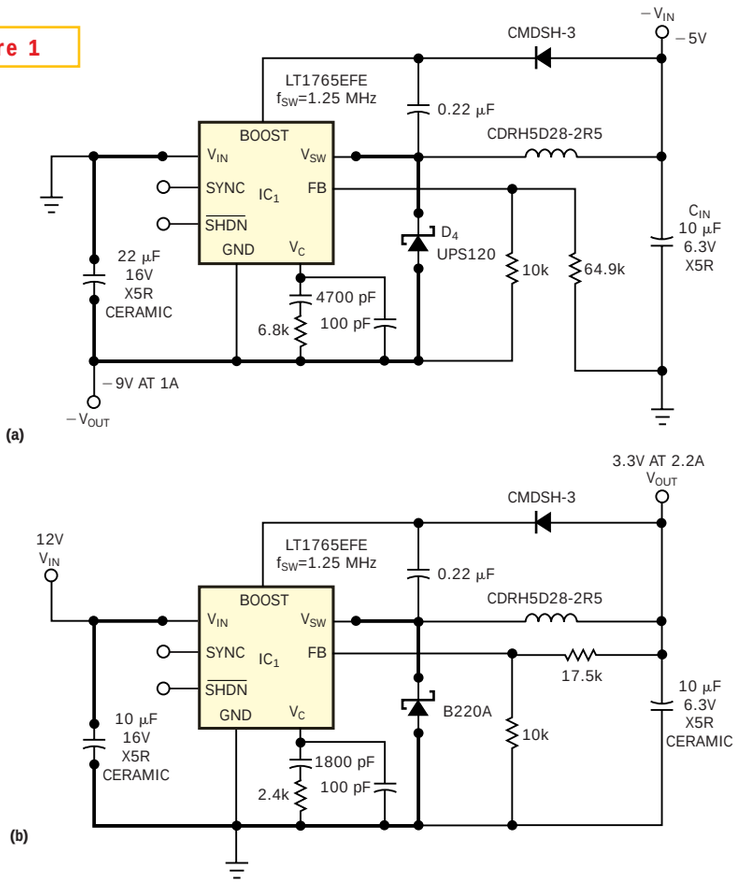
Positive regulator makes negative dc/dc converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Power-supply designers can choose from a plethora of available positive buck regulators that can also serve as negative boost dc/dc converters. Some buck regulators have a negative-feedback reference voltage expressly for this purpose, but ICs that have positive-reference feedback voltages far outnumber these negative-feedback regulators. You can take advantage of this greater variety of devices by using a positive buck switch-mode regulator to create an excellent negative boost converter. All you need are a few small modifications to the typical buck-converter configuration. **Figure 1a** shows a −5V-input to −9-output, 1.4A negative boost converter using the LT1765EFE positive-buck-converter, switch-mode regulator. This IC accepts 3 to 25V input, uses a 1.2V feedback voltage, and has an internal 3A power switch. The 1.25-MHz switching frequency of the LT1765EFE helps reduce the size of the inductor and input and output capacitors**. Figure 1b** shows a typical positive-buck-converter application for the LT1765EFE: a 12V-input to 3.3V-output, 2.2A dc/dc converter. **Figure 2** shows an efficiency plot for the regulator in **Figure 1a**.

Figure 1



The LT1765EFE positive buck converter can make a negative boost converter (a) or a positive buck converter (b).

In **Figure 1a,** the ground pin of the IC connects to the negative voltage V_{OUT}. This connection makes the negative-boost-converter configuration provide a positive voltage at the FB pin with respect to the ground pin of the IC. In this topology, the maximum input voltage rating of the IC has to be greater than the magnitude of output voltage for the negative boost converter. The IC must also have a minimum input-voltage rating that is less than the magnitude of the input voltage, to ensure that the circuit turns on upon power-up, because the output voltage can have an initial state of 0V.

Note that the maximum output current for the negative boost converter in **Figure 1a** is much lower than the maxi-

mum output current of the positive buck converter in **Figure 1b**, even though they use the same switch-mode-regulator IC. The buck-converter IC in both circuits has an internal power switch with a switch current rating of 3A. You choose the inductor based on maximum output current, peak switch current, and desired ripple current. First calculate the duty cycle (DC) and then calculate either the ripple current, I_{PP}, based on the chosen inductor, L, or the inductor value based on the desired ripple current. It is generally good practice to choose the inductor value so that the peak-to-peak ripple current is approximately 40% of the input current. These calculations are approximate and ignore the effect of switch, inductor, and Schottky-diode power losses. You calculate as follows:

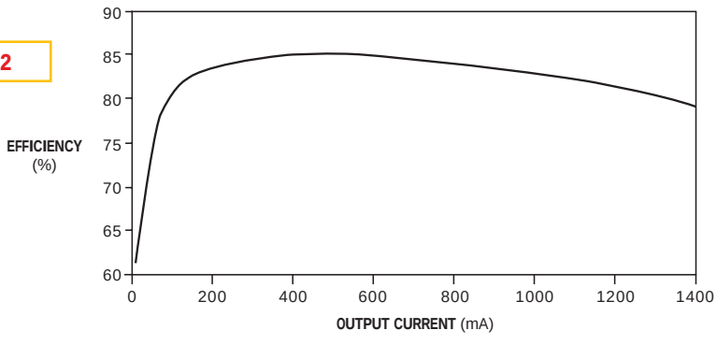
$DC=(V_{OUT}-V_{IN})V_{OUT}$; $I_{IN}\sim(V_{OUT}\times I_{OUT})/(V_{IN}\times\eta)$, where η is the overall efficiency. $I_{PP}=I_{IN}\times 40\%$; $I_{PP}=(DC\times V_{IN})/(f\times L)$, where f is the switching frequency; and $L=(DC\times V_{IN})/(f\times I_{PP})$.

Maximum inductor current, I_{LMAX}, is equal to the peak switch current in this configuration. The IC has a maximum switch current, I_{SWMAX}, of 3A, so the maximum inductor current must remain below 3A. To keep switch current below the maximum, you might need more inductance to keep the ripple current low enough. ($I_{LMAX}=I_{SWMAX}=I_{IN}+I_{PP}/2$.) Maximum output current, I_{OUTMAX}, is an approximation derived from the maximum allowable input current given the ripple current: $I_{OUTMAX}=(I_{SWMAX}-I_{PP}/2)\times(V_{IN}\times\eta)/V_{OUT}$. As in a typical boost converter, the input capacitor in the negative boost topology has low ripple current, and the output capacitor has high discontinuous ripple current. The size of the output capacitor is typically larger than that of the input capacitor to handle the greater rms ripple current:

$I_{CINRMS}=I_{PP}/\sqrt{12}$, and $I_{COUTRMS}=\sqrt{(1-DC)}\times(I_{IN}^2+I_{PP}^2/12)$.

The output capacitor's ESR has a direct effect on the output-voltage ripple of the dc/dc converter. Choosing higher frequency switch-mode regulators reduces the need for excessive rms ripple-current rating. Regardless, a low-ESR output capacitor, such as a ceramic, can minimize the output-voltage ripple of the negative boost converter: $\Delta V_{OUTPP}=I_{SWMAX}\times ESR_{COUT}$. **Figures 1a** and **1b** show the high-di/dt switching paths of the negative boost and positive buck dc/dc converters. You must keep this loop as small as possible by minimizing trace lengths to minimize trace inductance. The discontinuous currents in this path create high di/dt values. Any trace inductance in this loop results in voltage spikes that can render a circuit noisy or uncontrollable. For this reason, circuit layout can be just as important as component selection. Note that the layout of a negative boost regulator differs from that of a positive buck regulator, even though they use the same IC.

Figure 2



Efficiency of the negative boost converter in Figure 1a is as high as 85% and typically greater than 80%.

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Multiplexer amplifiers form large, multiplane-multiplexer structures

Bill Stutz, Maxim Integrated Products, Sunnyvale, CA

The variety of video sources available to a home-video-switching system has grown from a few composite inputs to many multisignal sources. These sources include cable, HDTV, satellite dishes, VCR, DVD, video games in broadcast, and multi-PC or graphic KVM (keyboard-video-mouse) applications. Each requires an N×M-to-1 multiplexer, in which M is the number of sources and N is the number of channels that make up the signal. As an example, 16 RGB or Y, Pb, and Pr sources require a 3×16-to-1 multiplexer. Constructing such a multiplexer is difficult, and programming the source selection requires that you combine the individual 16-to-1 multiplexer control with the three channels (**Table 1**). You can configure a group of analog multiplexers as a large, multiplane video multiplexer that easily selects

multichannel video sources, such as YC, RGB, and Y Pb Pr. The cited 3×16-to-1 multiplexer comprises six 8-to-1 multiplexers (**Figure 1**) controlled by a 4-bit binary code for source selection. (MAX4315 ICs include a 2V/V fixed-gain output buffer.)

The only external circuitry required is an SN7404 hex inverter for inverting the shutdown signals and 75Ω source and load resistors for implementing unity gain when driving a back-terminated load. Substituting a MAX4312 eight-channel video multiplexer with variable-gain output buffer allows variable gain and rejects input common-mode voltages. The high bandwidth and slew rate of these ICs make them ideal for selecting standard video and high-definition broadcast video, as well as graphics sources with UXGA and higher resolutions for KVM applications. The design requires no additional buffering, because the ICs can directly drive 150Ω back-terminated coaxial cable to within less than 0.75V of the supply rails, using single or dual supplies. Their 40-nsec switching speed and 10-mV p-p glitch voltage allow, in addition to source selection, insertion of on-screen display, closed captioning, and teletext in broadcast and graphics video.

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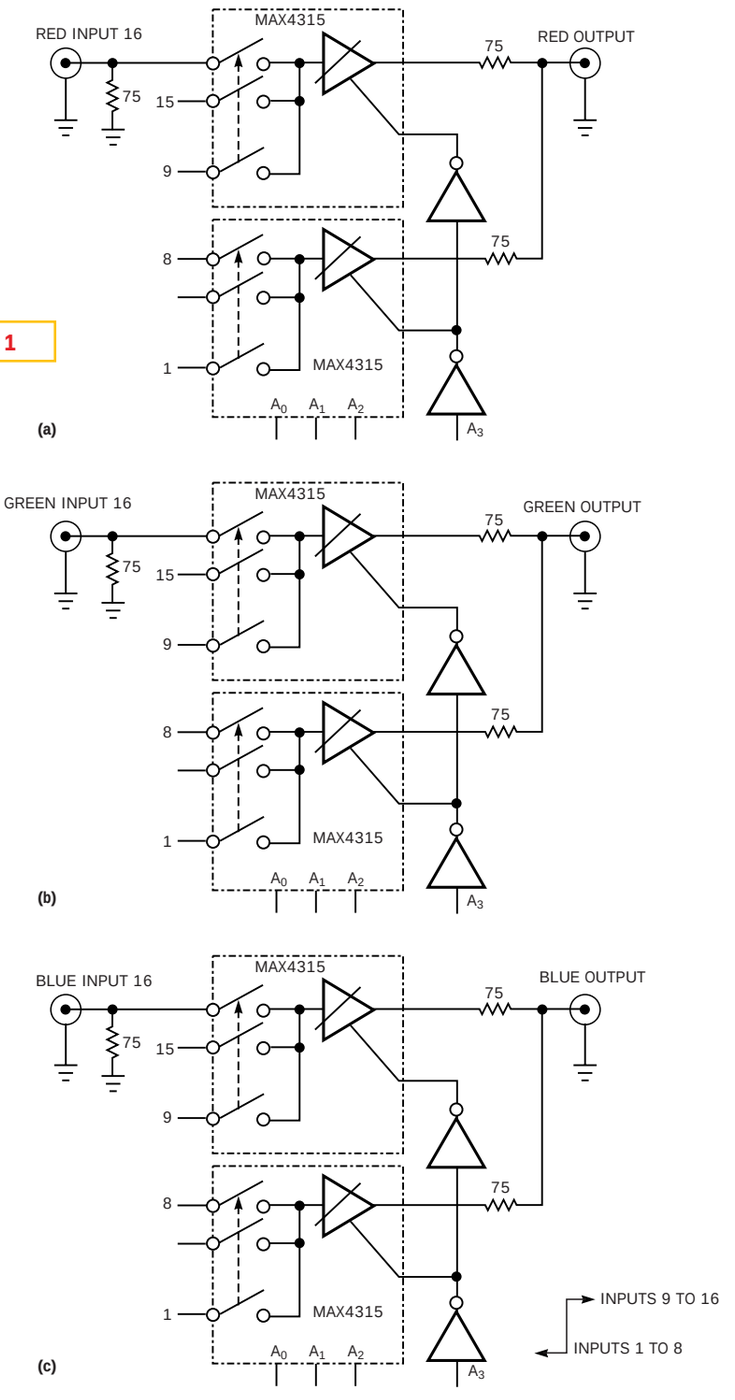
TABLE 1—SOURCE-SELECTION PROGRAMMING

RGB	A0	A1	A2	A3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

Figure 1



This multiplane multiplexer selects any one of 16 input signals, each of which comprises red (a), green (b), and blue (c) channels.

Circuit provides watchdog for microcontrollers

VM Holla, Bangalore, India

The watchdog circuit in **Figure 1** uses a single NAND Schmitt-trigger IC. The circuit is more cost-effective than dedicated, commercially available watchdog ICs. The circuit generates an active-high reset signal upon power-up and remains in a low state as long as the control input receives pulses. Whenever the pulsing at the control input stops, whether the circuit is in a high or a low state, the circuit emits a reset signal. Upon power-up, both inputs of gate IC_{1C} are low, forcing the Reset output to switch high and the $\overline{\text{Reset}}$ to go low. Thus, the outputs of both IC_{1B} and IC_{1D} are high. The high outputs charge the capacitors in the circuit, and, when both inputs of IC_{1D} reach a high level, the Reset output goes low, and $\overline{\text{Reset}}$ goes high. As long as the control input receives pulses, the outputs of IC_{1B} and IC_{1D} deliver pulses. The pulses hold the input of gate IC_{1C} high and the Reset output low.

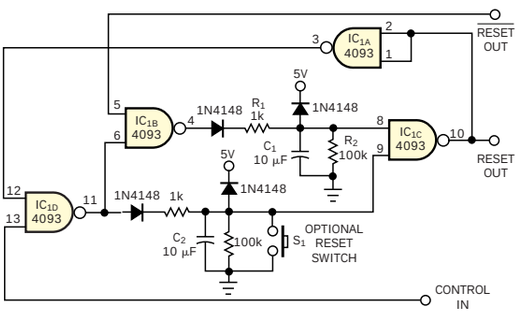


Figure 1 This watchdog-timer circuit is a cost-effective alternative to dedicated watchdog ICs.

When the control signal remains in a high state, C_2 begins discharging. When the control signal switches low, the Reset output goes high. The same scenario prevails with C_1 when the control signal remains low. You can choose the values of R_1, C_1, R_2, and C_2 as a function of the watchdog-time duration and the reset pulse width required. With the values shown, the circuit is appropriate for MCS51-family microcontrollers. The duration of the watchdog time is approximately 300 msec, and the reset pulse width is approximately 10 msec.

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Circuit translates I²C voltages

Peter Liu, Optron X, Allentown, PA

This Design Idea explores level-shifting an I²C bus from 5V/ground (positive domain) to ground/−5V (negative domain). In multisupply systems, you sometimes face a situation in which digital information stored in logic circuits running from 5V to ground needs conversion to analog signals referenced to a negative supply. Converting from digital to analog in the positive domain and then level-shifting to reference the negative rail introduces errors and results in a large component count. A better approach is to level-shift the digital data lines and convert with negative-referenced A/D converters. I²C is a bidirectional system employing a two-wire bus: one clock line and one data line. Pullup resistors and open-collector outputs establish dominant-low signaling. **Figure 1** shows a typical setup, in which the microcontroller is the master, and all the peripherals are slaves. Each device has a unique I²C address. The master always generates the clock, but, depending on

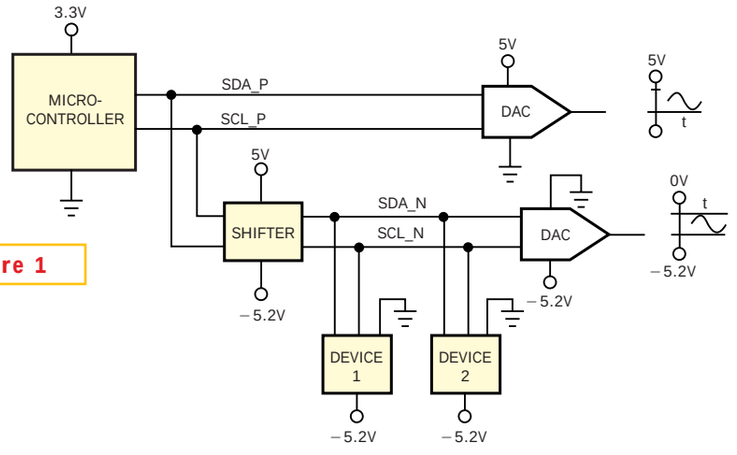
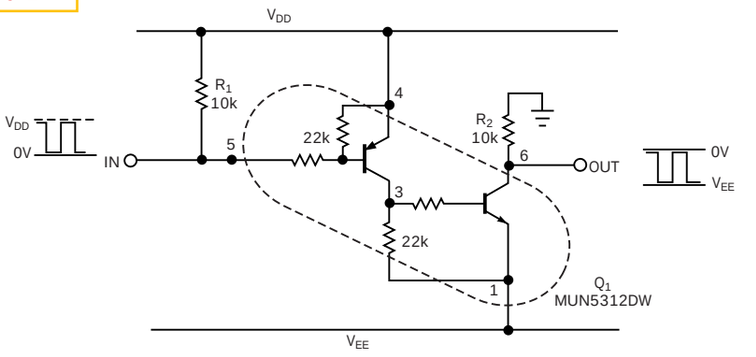


Figure 1 In this typical I²C configuration, the microcontroller is the master, and all the peripheral devices are slaves.

the desired direction of data flow, either the master or the slave could be the transmitter on the data line.

To understand the level-shifting procedure, consider the simple circuit in **Figure 2**. The circuit level-shifts the clock line unidirectionally. Q_1 comes with a pnp, an npn, and four bias resistors, all in one small SOT-363 package. R_1 provides the necessary pullup function in the positive domain, and R_2 does the same in the negative domain. The operation of the circuit is straightforward. When V_{IN} is set to V_{DD}, Q_1 remains off, so $V_{OUT}=0V$ (logic high). When V_{IN} is set to 0V, Q_1 is on, so $V_{OUT}=V_{EE}$ (logic low). This unidirectional circuit does not allow the master to detect when the slave holds the clock low. Therefore, if you desire I²C clock-extension (wait-stating), you would need a bidirectional level-shifting circuit.

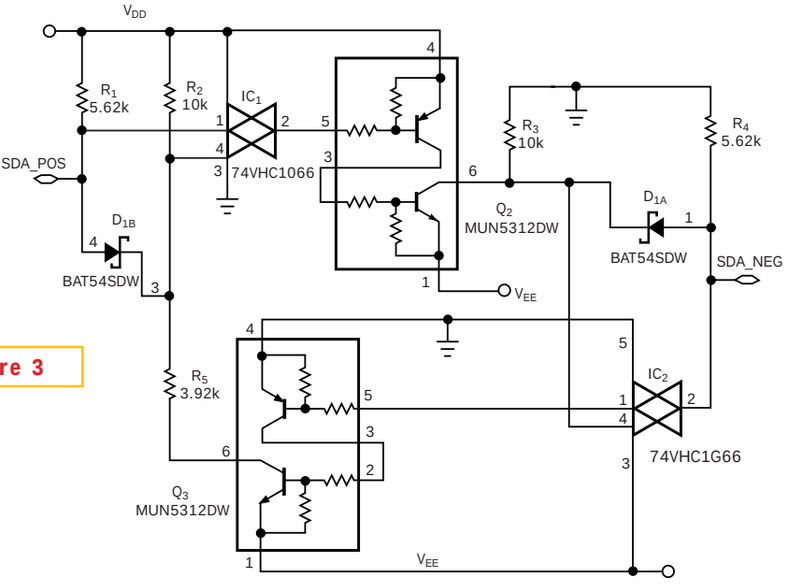
Figure 2



This transistor arrangement level-shifts the data or clock signals from positive to negative levels.

The data line needs a bidirectional circuit. Even when the master is transmitting, the master needs to detect when the negative-domain slave pulls the data line low on every ninth bit to acknowledge the transmitted byte. Also, when instructed, the slave may need to transmit data back to the master. In the slave-transmitter mode, the slave would have to detect when the master pulls the data line low on every ninth bit to acknowledge the transmitted byte. Despite this added complexity, you can still accomplish the task with just five SOT-363-size packages and five discrete resistors (**Figure 3**). To see that the circuit in **Figure 3** is topologically the same as the one in **Figure 2**, assume transmission gates IC_1 and IC_2 are on and ignore the lower half of the circuit for the moment. With SDA_POS set to V_{DD}, Q_2 is off, R_3 and R_4 pull up to 0V, resulting in SDA_NEG=0V (logic high). With SDA_POS set to 0V, Q_2 is on, so SDA_NEG~VEE (logic low).

Figure 3



A bidirectional level shifter translates data and clock signals from positive levels to negative levels, and vice versa.

Now, trace the return path from slave to master. With SDA_NEG set to 0V (logic high), Q_3 is off, and R_1 pulls SDA_POS up to V_{DD}. With SDA_NEG set to V_{EE} (logic low), Q_3 is on, and $R_1||R_2$ forms a voltage divider with R_5 to yield SDA_POS~0V. You select R_1, R_2, and R_5 to yield $V_{DD}=5V$ and $V_{EE}=-5.2V$. If desired, you could use additional transistors to construct the return path so that it doesn't depend on resistors to set logic levels. Transmission gates IC_1 and IC_2 and Schottky diodes D_{1A} and D_{1B} break the positive feedback path that would otherwise result when either master or slave pulls SDA to a logic low. Note that, without these components, Q_2 and Q_3 would form a latch. The circuit in **Figure 3** easily meets I²C timing requirements at a 50-kHz clock rate. For 100-kHz operation, it is best to use an MUN5311, which has 10-kΩ internal resistors instead of 22 kΩ. You can use the same bidirectional circuit in **Figure 3** for the clock signal, to cover all the I²C modes of operation.

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