Edited by Bill Travis

Autoreferencing circuit nulls out sensor errors

Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA

The autoreferencing circuit in **Figure 1** nulls out the error of a sensor, such as a pressure transducer, at its reference level—for example, at ambient pressure. The circuit is an analog-digital-feedback control system that uses a digitally programmable potentiometer to provide the variability. The circuit in **Figure 1** is designed to accommodate a pressure transducer with a nominal 1V±50-mV output at ambient pressure and provide a voltage of 1V±1 mV. Amplifier IC_{1A} is a summing/difference circuit whose inputs are the sensor's output voltage, V_{SENSE}; a voltage shift, V_{SHIFT}, of 100 mV; and a correction voltage, V_{CORR}. IC_{1B} functions as a comparator, comparing the output voltage of the summing amplifier with the ideal output voltage of the sensor, 1V. The logic output of the comparator sets the direction for incrementing or decrementing the potentiometer's wiper, whose buffered wiper voltage provides the correction voltage, V_{CORR}.

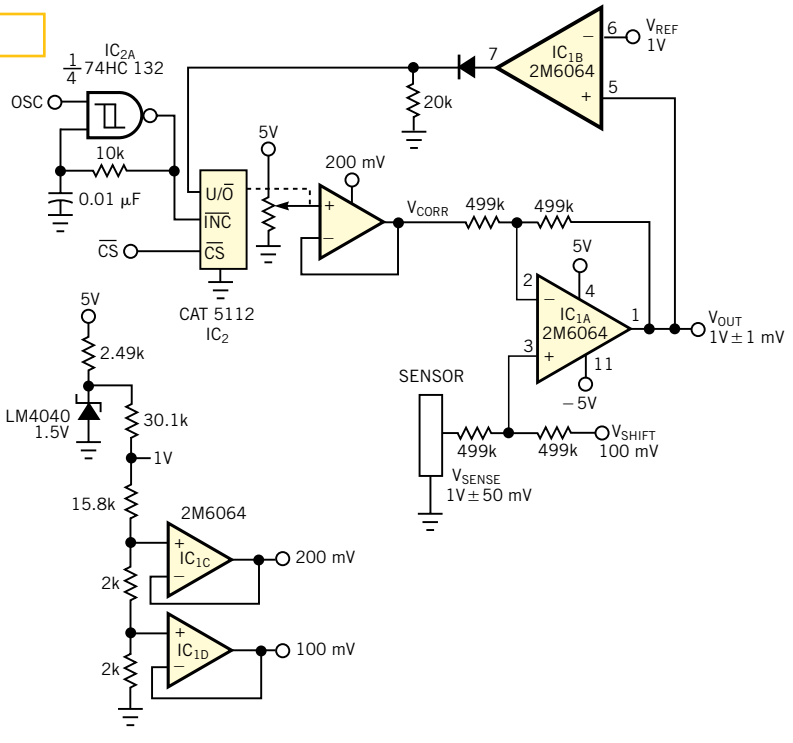
The potentiometer is a Catalyst 30-tap digitally programmable potentiometer with an increment/decrement interface. The correction voltage varies from 0 to 200 mV and subtracts from the shifted sensor voltage. Mathematically, $V_{OUT}=(V_{SENSE}+V_{SHIFT})-V_{CORR}$, where $0\le V_{CORR}\le 200$ mV, $V_{SHIFT}=100$ mV, and $0.95V\le V_{SENSE}\le 1.05V$. The 100-mV, 200-mV, and 1V references for the circuit come from a 2.5V reference, stepped down by a resistive divider and buffered by voltage followers. IC_{2A} implements a square-wave oscillator whose frequency is approximately equal to 1/RC—in this case, 10 kHz. You program the autoreferencing circuit using the logic-input signals OSC and $\overline{CS}$. The circuit becomes disabled when OSC is low and $\overline{CS}$ is high. When the circuit is disabled, V_{OUT} is at its last corrected value.

The circuit becomes enabled and corrects the output voltage for a new sensor or different set of conditions when OSC is high and $\overline{CS}$ is low. To store the current wiper setting of the digitally programmable potentiometer in nonvolatile memory, first make OSC low and then bring $\overline{CS}$ from low to high. If power disappears and is later restored, the potentiometer goes to the corrected value stored in nonvolatile memory. The measured error in the system is less than 1 mV, but better performing amplifiers, a higher resolution potentiometer, and more accurate resistors can reduce the error to the low-microvolt region. This circuit uses three ICs and a handful of discrete parts and is an alternative, low-cost approach to more complex autoreferencing circuits using DACs, ADCs, and microprocessors.

Is this the best Design Idea in this issue? Vote at www.ednmag.com.

Publish your Design Idea in *EDN*. See the What's Up section at www.ednmag.com.

Figure 1



This autoreferencing circuit nulls out output errors at a sensor's reference (ambient) condition.

Low-power keypad consumes only 100 nA

Mike Mitchell, Texas Instruments, Dallas, TX

Often in the use of products with keypads, one or more keys become "stuck" or are being pressed. For example, a cell phone in the bottom of a purse or in a hip pocket could have one or more of its keys inadvertently pressed and held down for a considerable period. Depending on the circuit design and implementation of the keypad interface, this condition could cause excess current to flow, thereby draining the batteries in portable equipment. The circuit in **Figure 1** is a keypad interface that solves this problem by using an ultralow-power microcontroller. The circuit typically consumes 100 nA while awaiting a key press and consumes a maximum of only 2 µA if all keys are stuck or held down. An added bonus of the circuit is that it requires no crystal.

The circuit uses the MSP430, IC_1, because it offers low power consumption, individually configurable I/O pins with interrupt on rising or falling edges, and wake-up time of less than 6 µsec. In normal mode, port pins P3.0 to P3.3 drive the rows high. The columns connect to port pins P1.0 to P1.2, configured as inputs with interrupts enabled and set to interrupt on a rising edge. The pulldown resistors hold the inputs low in the inactive state. The MSP430 then goes into low-power Mode 4, in which the microcontroller draws 100 nA. This state continues indefinitely until you depress a key. The circuit is completely interrupt-driven with no need for polling. When you depress a key, the column associated with that key receives a rising edge, thereby waking the MSP430. The timer for the delay uses the internal digitally controlled oscillator of the MSP430, an RC-type oscillator. The digitally controlled oscillator is subject to tolerances, so you use a debounce delay to yield a worst-case minimum delay of 25 msec. That figure translates to a worst-case maximum delay of approximately 86 msec and a typical delay of approximately 40 msec. This range is eminently usable for keypad-debouncing purposes. After the debounce delay, the circuit scans the keypad to determine which key you depressed.

After you depress a key, the MSP430 goes into a "wait-for-release" mode, in which it drives only the necessary row for the key you depressed. (Other rows switch low.) The microcontroller reconfigures the P1.x I/O to interrupt on a falling edge, and it again goes into low-power Mode 4 and waits for the release of the key. Again, the circuit needs no polling at this point. The detection of the key release is completely interrupt-driven, allowing the MSP430 to stay asleep while the key is held, thereby reducing current consumption. Once you release the key, the circuit again executes the debounce-delay routine. After the debounce delay, the circuit again scans the keypad to determine whether any other keys are being held. If so, the wait-for-release mode continues. When all the keys are released, the MSP430 reverts to "wait-for-press" mode. During the wait-for release mode, only one row of the keypad goes high, thereby limiting the maximum current consumption to the condition in which all three keys on a single row are pressed. For a 3V system, this condition equates to approximately 2 µA. Any other key press does not result in increased current consumption, because the corresponding row is not in a high state. You can download the software for the microcontroller from the Web version of this article at www.ednmag.com.

Is this the best Design Idea in this issue? Vote at www.ednmag.com.

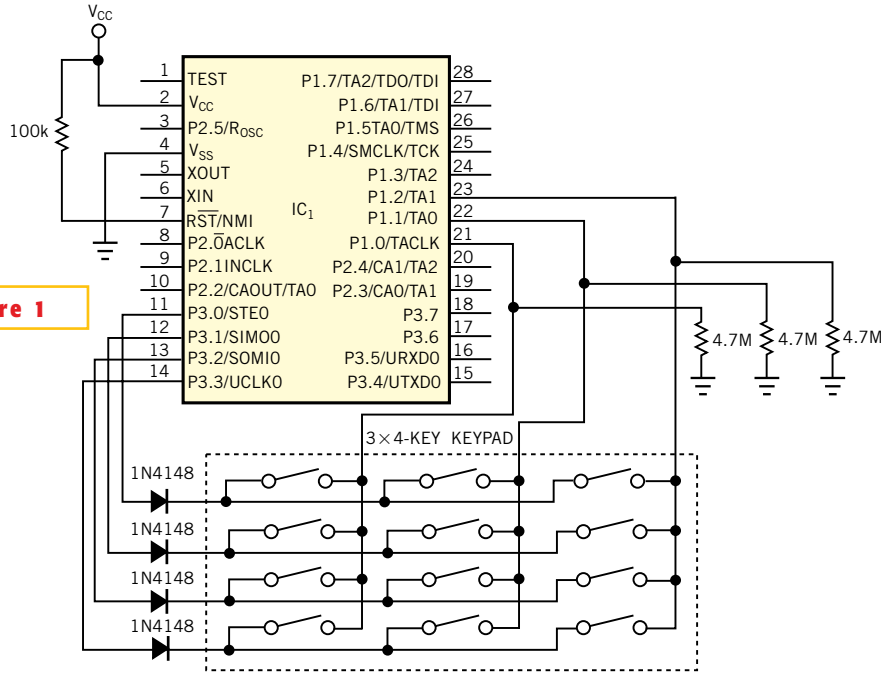


Figure 1

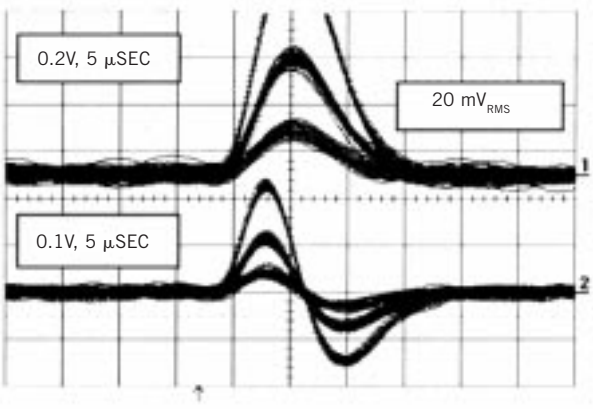
This keypad interface draws only 100 nA in standby mode and avoids "stuck-key" problems.

Time-tag impulses with zero-crossing circuit

Elio Rossi, Itesre-CNR, Bologna, Italy

A "constant-fraction discriminator" usually performs the time-tagging of impulsive events, which have a peaking time of the signal amplitude. The implementation of this technique requires a delay in the input signal of approximately the same amount as the signal's rise time. You can attain this delay by using a coaxial cable of an appropriate length. For many applications, in which the rise time for impulsive events is 1 to 10 µsec, you must consider alternative solutions, because of the length of the cable you'd require. **Figure 1** shows the typical output from a spectroscopic amplifier, where the presence of a large amount of detector noise with Gaussian distribution is a limiting factor for system performance in amplitude and timing resolution. The time-tagging of such pulses is subject to two well-known types of errors: the jitter related to the noise and the "walking time" arising from the amplitude variation of the signals. You can eliminate the walking time by differentiating the signal and detecting the zero crossings. The jitter is related to the noise around the zero-crossing line.

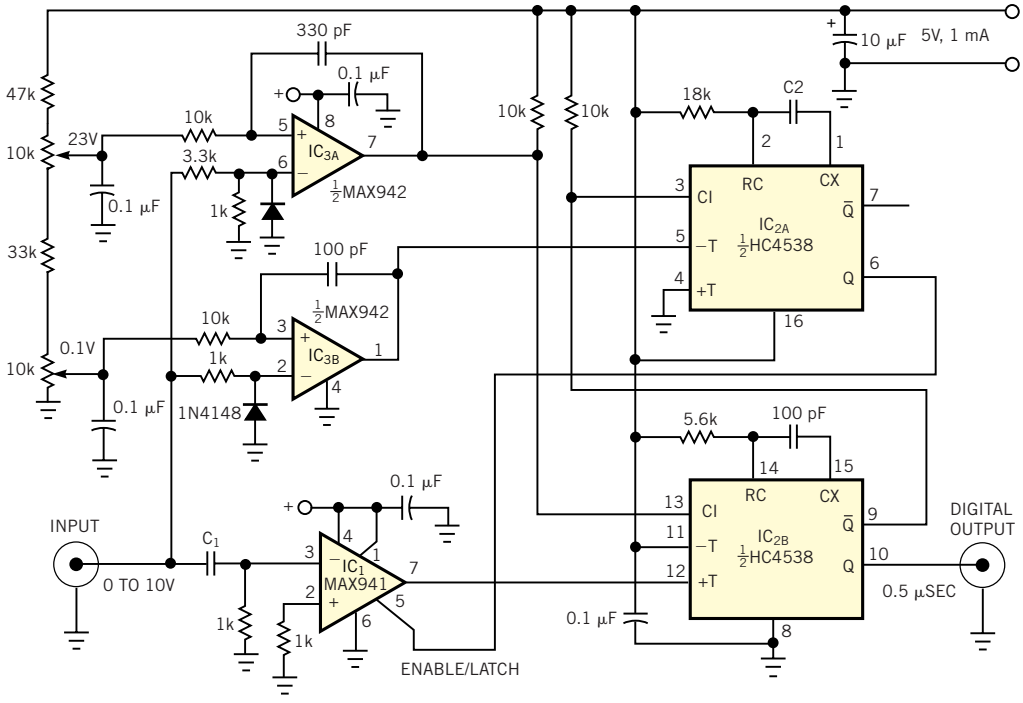
Figure 1



A spectroscopic amplifier produces differentiated signals (lower traces) in response to input impulses (upper traces).

In **Figure 2**, an arming discriminator with a fixed threshold of 100 mV ($5\times V_{RMS(NOISE)}$) enables the IC_1, a MAX-941 zero-crossing discriminator, via the

Figure 2

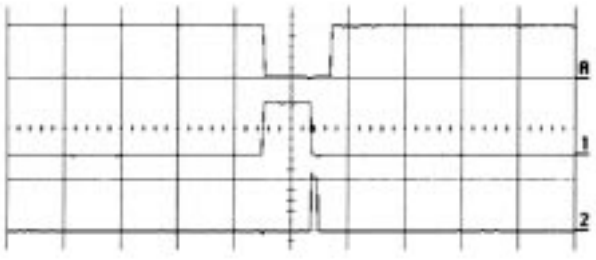


A discriminator and a zero-crossing detector eliminates "walking-time" error for impulsive events.

first half of IC_2, an HC4538 resettable monostable multivibrator. The propagation delay in these ICs allows enabling the zero-crossing discriminator when the differentiated signal is well over the baseline noise for the full range of the input signal. The positive-going output pulse from IC_3, a MAX941, corresponding to the zero-crossing time, reaches the output with a fixed length of 0.5 µsec, set by the second monostable multivibrator. This second multivibrator resets the first and latches the MAX941 at the high output level until a new trigger arrives from the arming discriminator. In this way, you avoid spurious triggers at the beginnings and ends of input pulses. The upper-threshold discriminator output, with a minimum output length of 5 µsec, serves to "veto" the 0.5-µsec output and works even for highly saturated input signals. Because of the input configuration of the MAX942, it is necessary to reduce the upper threshold level to less than 2.8V. **Figures 3** and **4** show the timing sequences for 0.2V and 10V input signals, respectively.

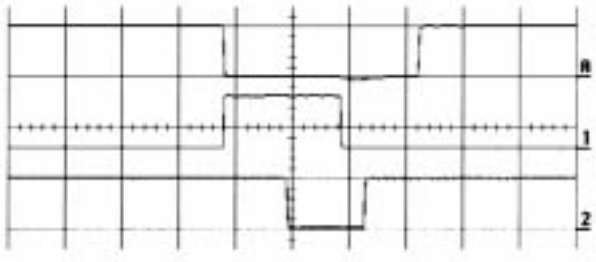
You can obtain the same results using many different implementations of the circuit, depending on the ICs available off the shelf. For example, you can substitute the MAX941 with a common discriminator and a CMOS analog switch to commutate the threshold from a positive voltage to ground. A single flip-flop then completes the circuit. This design uses an amplification stage with back-to-back limiting diodes in front of the zero-crossing discriminator. **Table 1** shows the results, with comparisons to the shaping-time value of 3 µsec. You measure the walking time and jitter using a pulse generator, preamplifier, shaping amplifier, time-to-amplitude converter, and multichannel analyzer. **Figure 5** shows just three of the many histograms used to calculate the walking time and jitter results.

Figure 3



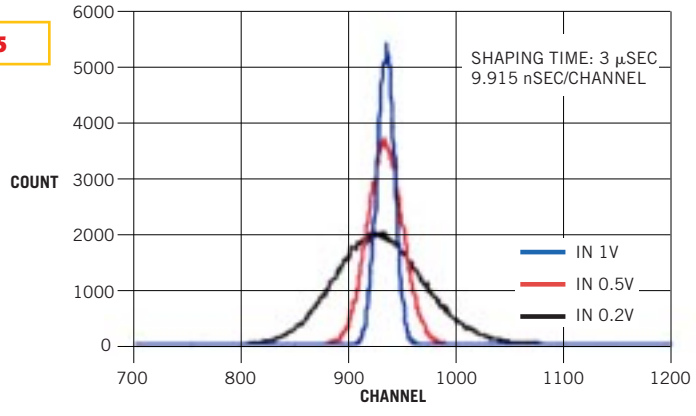
For 200-mV input, Trace A is the output from the arming discriminator, Trace 1 is the Enable signal for the MAX941, and Trace 2 is the signal output.

Figure 4



For a 10V input, Trace A is the output from the lower level discriminator, Trace 1 is the Enable signal for the MAX941, and Trace 2 is the output from the upper level discriminator.

Figure 5



These jitter histograms are for input signals of 0.2, 0.5, and 1V.

Is this the best Design Idea in this issue? Vote at www.ednmag.com.

TABLE 1–MEASUREMENT RESULTS AT 1 kHz AND WITH 20 mV RMS OF NOISE

Shaping time (µsec)	Peak time (µsec)	C_1 (nF)	C_2 (nF)	Jitter	$0.1V_{IN}$[1]	$0.2V_{IN}$	$0.5V_{IN}$	$1V_{IN}$	$2V_{IN}$	$5V_{IN}$	$10V_{IN}$	Walk
1	2	0.47	0.33	σ (µsec)	0.249	0.145	0.06	0.029	0.015	0.009	0.006	0.06 µsec
3	6	1	1	σ (µsec)	0.594	0.395	0.156	0.081	0.042	0.017	0.009	0.2 µsec[2]
6	12	2.2	2.2	σ (µsec)	1.608	0.939	0.372	0.195	0.096	0.04	0.021	1.1 µsec[2]
3	6	1	1	Amplifier	0.664	0.417	0.161	0.081	0.042	0.017	0.009	0.47 µsec[3]

Circuit provides reference for multiple ADCs

Ron Gatzke and Tanja Hofner, Maxim Integrated Products, Sunnyvale, CA

The achievable accuracy for systems with multiple ADCs depends directly on the reference voltages applied to the ADCs. Medical-ultrasound-imaging systems, for example, commonly include a large number of ADCs in the system's beam-former electronics, with the ADCs usually organized in groups of 16, 24, 32, and so on. To obtain maximum beam accuracy, you must minimize errors in the ADC path. Poor accuracy of the reference voltages of the individual ADCs degrades the overall system accuracy. Another source of degradation is the distributed load, which comprises many individual resistive and capacitive loads. Several approaches are available to provide the reference voltage for such ADC arrays:

- Individual on-chip references. Though this approach offers a convenient local connection to each ADC, it can result in relatively poor matching among the converters.
- A single external reference voltage applied to all ADC reference inputs. Such a configuration allows you to engineer an external reference voltage of arbitrary accuracy but incurs errors from the small variations among the internal ladders of the ADCs.
- An external reference directly driving the ADCs' reference-ladder taps. This option delivers maximum gain accuracy by directly controlling the reference voltage applied to each ADC ladder. However, it requires driving the relatively low resistance of the ladders. Moreover, some ADCs do not allow access to that internal bias point.

ADC ACCURACY

In many applications, gain and noise level have a major effect on ADC accuracy. The gain of an ADC is in effect the slope of its transfer function, which relates analog inputs to the allowable range of digital-output codes. One way to quantify gain is to measure the full-scale input range, which is a direct function of the reference-voltage level. For medical-ultrasound-imaging systems, variations in the full-scale ranges of the ADCs can cause errors in beam formation. The variations also affect the ADCs' clipping point—an effect that may be important is certain signal-demodulation schemes. An ADC's noise level determines its usable dynamic range. This dynamic range should be as great as possible. The reference-noise component of ADC noise can be additive or multiplicative. Local bypass capacitors on the individual ADCs can easily filter additive noise. Multiplicative noise, on the other hand, is more insidious. For ultrasound applications, reference noise in the audio-frequency

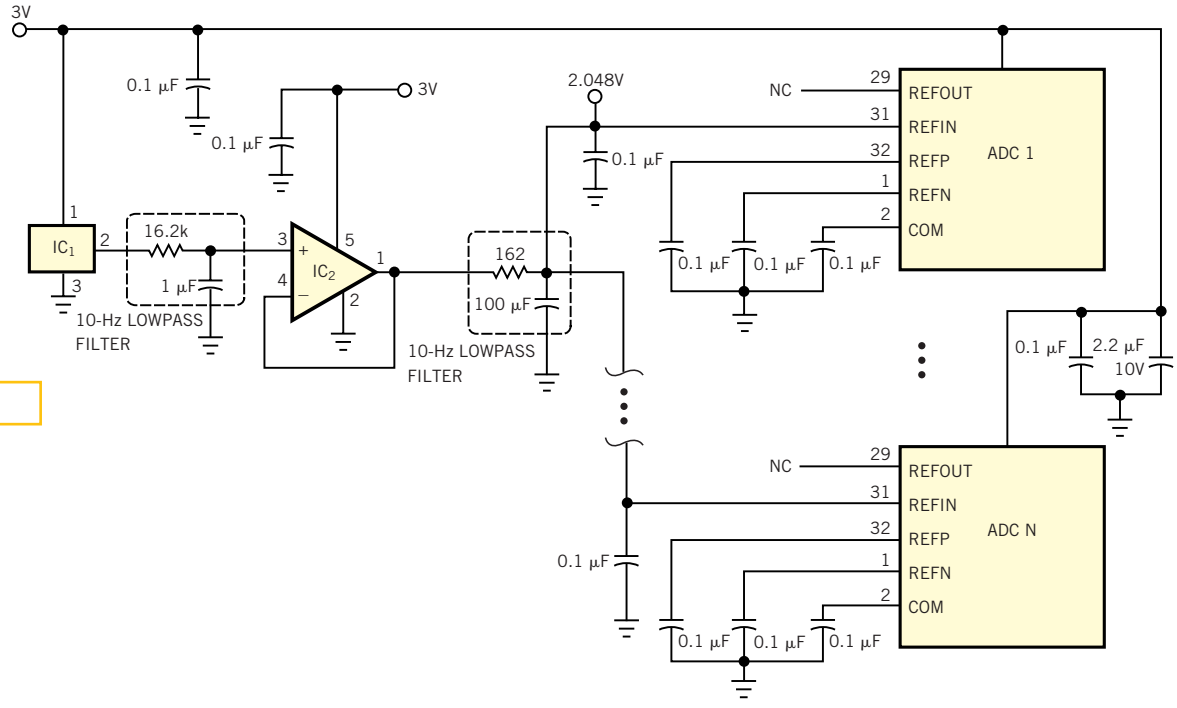


Figure 1

For ultrasound applications, a single, low-noise reference circuit can drive as many as 1000 ADCs.

spectrum can modulate large "stationary" signals in the RF spectrum. Such signals arise from stationary tissue in the ultrasound target.

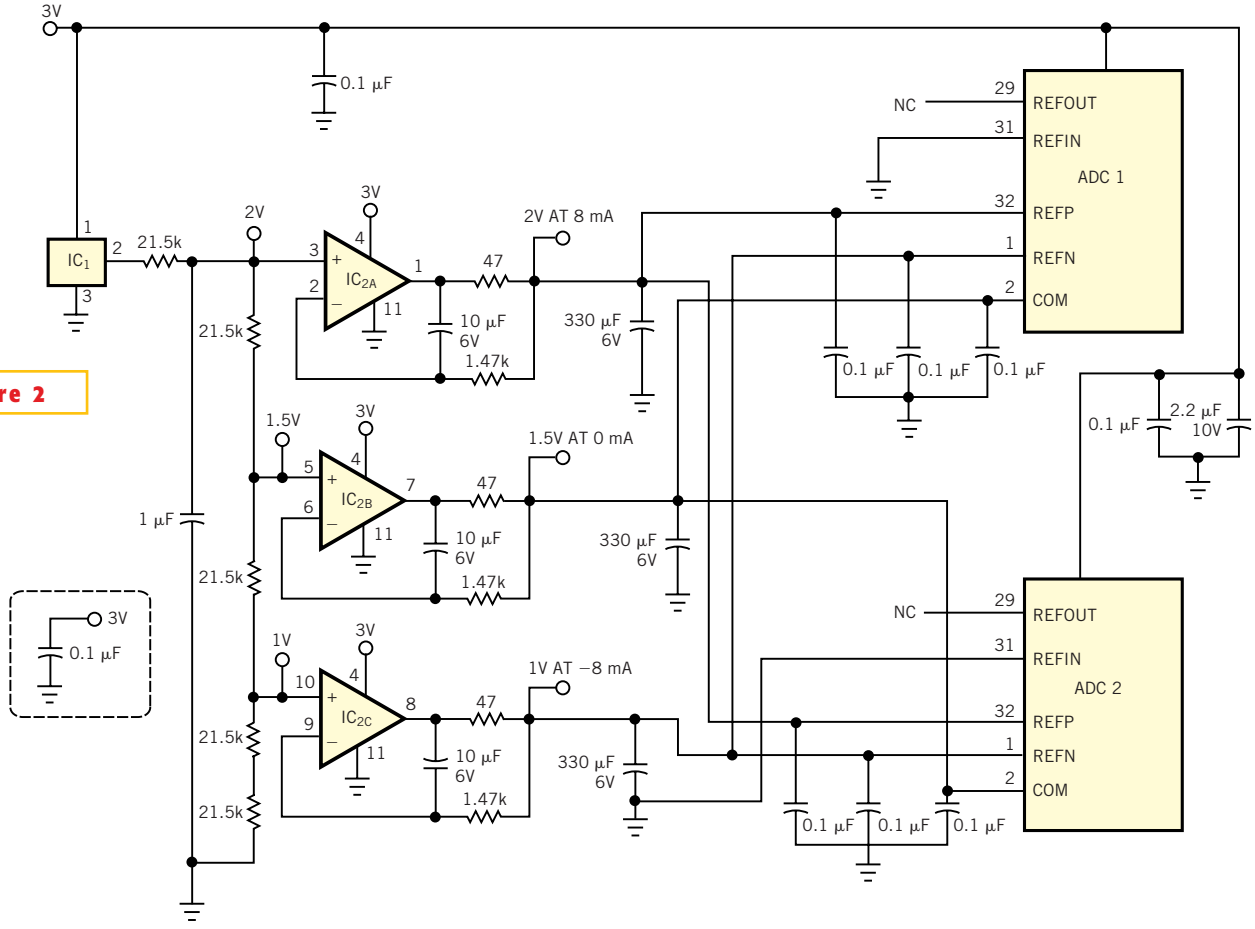
Audio modulation produces sidebands in the RF signal that a Doppler detector can demodulate, producing audio tones. To estimate the amount of audio noise tolerable in an ultrasound application, assume a nearly full-scale RF signal applied to a 10-bit ADC such as the MAX1448. The device's dynamic range of almost 60 dB equates to a noise floor of −60 dBFS (relative to full scale). You can normalize that noise level to a 1-Hz bandwidth. The Nyquist bandwidth for an 80-MHz sampling rate is 40 MHz. The correction factor is $\sqrt{40\ \text{MHz}}$=76 dB, which places the ADC's noise floor at −60 dBFS−76 dBFS=−136 dBFS. Because a conservative design requires the reference-voltage noise to be at least 20 dB lower (−156 dBFS), a 2V reference requires an extremely low noise level of 33 nV p-p (approximately 8 nV/$\sqrt{\text{Hz}}$).

A multiple-ADC array may require a more accurate reference voltage than the one internal to each converter. The reference voltage internal to MAX144x converters, for example, has an accuracy of ±1%. The following two circuits are reference designs for such arrays. They feature a single, common low-frequency noise filter, and they offer high-frequency noise suppression via local decoupling capacitors connected to individual ADCs.

SINGLE EXTERNAL REFERENCE

Multiple-converter systems based on the MAX144x family are well-suited for use with a common reference voltage. You can the REFIN pin of these converters to an external reference source and thus eliminate the need for any circuit modification. Moreover, the high input impedance of REFIN (even of multiple REFIN terminals connected in parallel) results in only a small load-current drain. **Figure 1** shows a precision source, such as the MAX6062, that generates an external dc level of 2.048V and exhibits a noise-voltage density of 150 nV/$\sqrt{\text{Hz}}$. The output of the IC passes through a one-pole lowpass filter with 10-Hz cutoff frequency to op amp IC_2, which buffers the reference. The buffered reference voltage then passes through a second 10-Hz lowpass filter. IC_2 exhibits a low offset voltage for high gain accuracy and a low noise level. The passive 10-Hz filter following the buffer attenuates noise produced in the voltage-reference IC and buffer stage. The filtered noise density, which decreases with frequency, meets the noise levels re-

Figure 2



For ultrasound applications, a precision, low-noise reference circuit can drive as many as 32 ADCs.

quired for precision-ADC operation.

Converters of the MAX144x family specify a typical gain error of ±4.4% (better than ±0.5 dB). This performance is better than the gain tolerance of all other building blocks in the signal path of an ultrasound receiver. Note that the circuit in **Figure 1** ensures proper power-up/power-down sequencing, because all active parts receive their power from the same supply-voltage rail. This approach yields excellent gain matching and an extremely low noise level with minimal circuitry. The circuit should prove adequate in many applications that require multiple gain-matched ADCs.

PRECISION EXTERNAL REFERENCE

For applications requiring more stringent gain matching, the MAX144x family fills the bill. In **Figure 2**, connecting each REFIN to analog ground disables the internal reference of each device. You can thus directly drive the internal reference ladders from a set of external reference sources. These voltages can have an arbitrarily tight tolerance; the ADCs typically track them within 0.1%. ADCs of this family have 4-kΩ resistance across the ladder's reference connection, so it's easy for the reference source to drive the load, even with many ADCs connected in parallel. IC_1 generates a dc level of 2.500V, followed by a 10-Hz lowpass filter and a precision voltage divider. The buffered outputs of this divider provide 2, 1.5, and 1V, with an accuracy that depends on the tolerances of the divider resistors. The quad op amp IC_2, selected for its low noise and dc offset, buffers the three voltages.

The individual voltage followers connect to 10-Hz lowpass filters, which filter both the reference-voltage and buffer-amplifier noise to a level of 3 $nV/\sqrt{Hz}$. The 2 and 1V reference voltages set the differential full-scale range of the associated ADCs at 2V p-p. The 2 and 1V buffers drive the ADCs' internal ladder resistances between them. The load is 4 kΩ divided by the number of ADCs in the circuit. As an example, 32 ADCs draw 8 mA from the supplies, a load current that is well within the capability of IC_2. The gain accuracy of the configuration in **Figure 2** can be almost arbitrarily tight, depending on the accuracy grade of IC_1 and the tolerances of the resistors in the voltage divider. The gain matching of the ADCs in such a configuration is typically 0.1%. With a noise level below 3 $nV/\sqrt{Hz}$ at 100 Hz, this circuit provides exemplary performance. As in **Figure 1**, the common power supply for all active components removes any concern about power-supply sequencing.

Is this the best Design Idea in this issue? Vote at www.ednmag.com.