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Edited by Bill Travis

Double DAC rate by using mixers as switches

Randall Carver, Analog Devices, Greensboro, NC

You can effectively double the sample rate of a DAC by interleaving two DACs into a single unit. Updating each DAC on an alternating basis and switching to the appropriate output double the effective throughput of the overall system. It is essential to overall performance that you use a high-quality, high-speed switch in the multiplexing of the DACs' outputs. The current-mode DACs in this Design Idea allow for current-steering implementation of the output switch. Current steering uses two differential-transistor pairs cross-coupled in the form of a four-quadrant multiplier (**Figure 1**). In this topology, the saturation voltages of the transistors are minimal, voltage swings are small, and switching speeds are high.

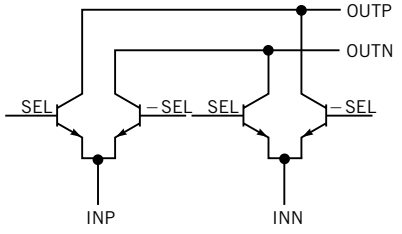

Figure 1 You can use cross-coupled differential transistor pairs as current-mode switches.

The 2.5-GHz AD8343 mixer contains a complete four-quadrant-multiplier structure that you can use as a high-speed, current-mode switch. The bias circuitry internal to the AD8343 sets the dc voltage at the emitters to approximately 1.2V, which in turn sets the compliance voltage necessary at the DAC

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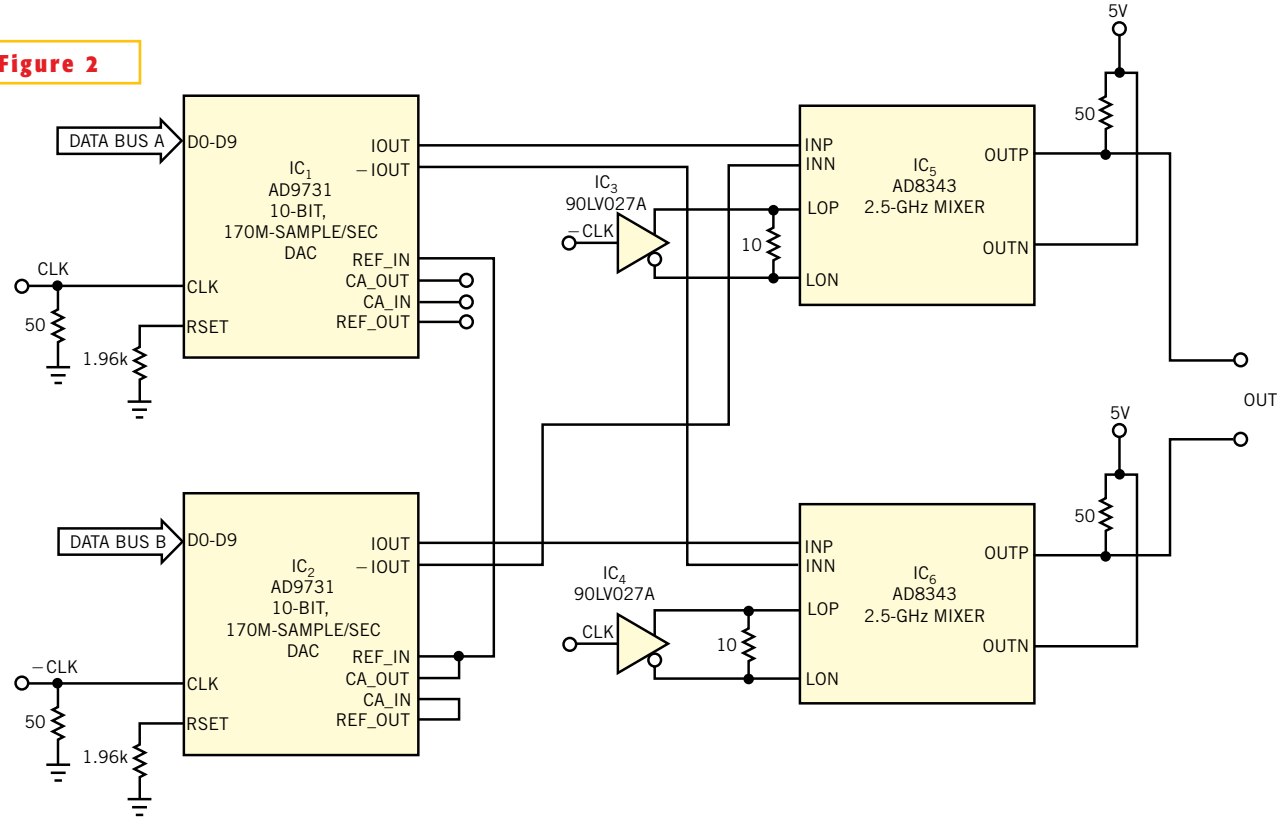
Figure 2



"Ping-ponging" the outputs of two DACs effectively doubles the throughput rate.

outputs. With only a minimal drive signal at the base connections, the emitters appear as a virtual ac ground. The reduced voltage swing at these nodes minimizes the effect of any parasitic capacitances. This Design Idea uses two AD8343 mixers as high-speed switches to multiplex the differential output currents derived from two AD9731 DACs (**Figure 2**). On the output side of the mixers, the termination resistors allow for a dc path to the supply, provide for the current-to-voltage conversion, and present a single-ended back-termination impedance of 50Ω. This configuration allows the circuit to drive a remotely located, 100Ω, differential load via two 50Ω coaxial cables. The low-level clock signals at the LO inputs come from high-speed LVDS buffers terminated in resistances of 10Ω. The approximate ±3.5-mA p-p drivers produce roughly 70-mV p-p drive at the LO inputs. **Figure 3** shows that the circuit provides output rise and fall times faster than 200 psec.□

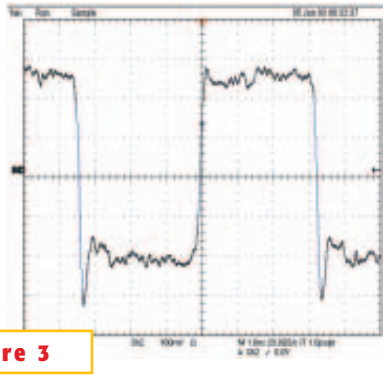


Figure 3

The circuit in Figure 2 produces outputs with less-than-200-psec rise and fall times.

DDS IC plus frequency-to-voltage converter make low-cost DAC

Noel McNamara, Analog Devices, Limerick, Ireland

Precision DACs are essential in many consumer, industrial, and military applications, but high-resolution DACs can be costly. Frequency-to-voltage converters have good nonlinearity specifications—typically, 0.002% for the AD650—and are inherently monotonic. This Design Idea shows how you can use a frequency-to-voltage converter and a DDS (direct-digital-synthesizer) chip for precise digital-to-analog conversion. The DDS chip generates a precision frequency proportional to its digital input. This frequency serves as the input to a voltage-to-frequency converter, thereby generating an 18-bit analog voltage proportional to the original digital input. **Figure 1** shows how the AD650 is configured for frequency-to-voltage conversion. With $R_1+R_3=20$ kΩ and $C_{OS}=620$ pF, a full-scale input frequency of 100 kHz produces a full-scale output voltage of 10V. (See Analog Devices (www.analog.com) application note AN-279 for more details on using the AD650 as a frequency-to-voltage converter.)

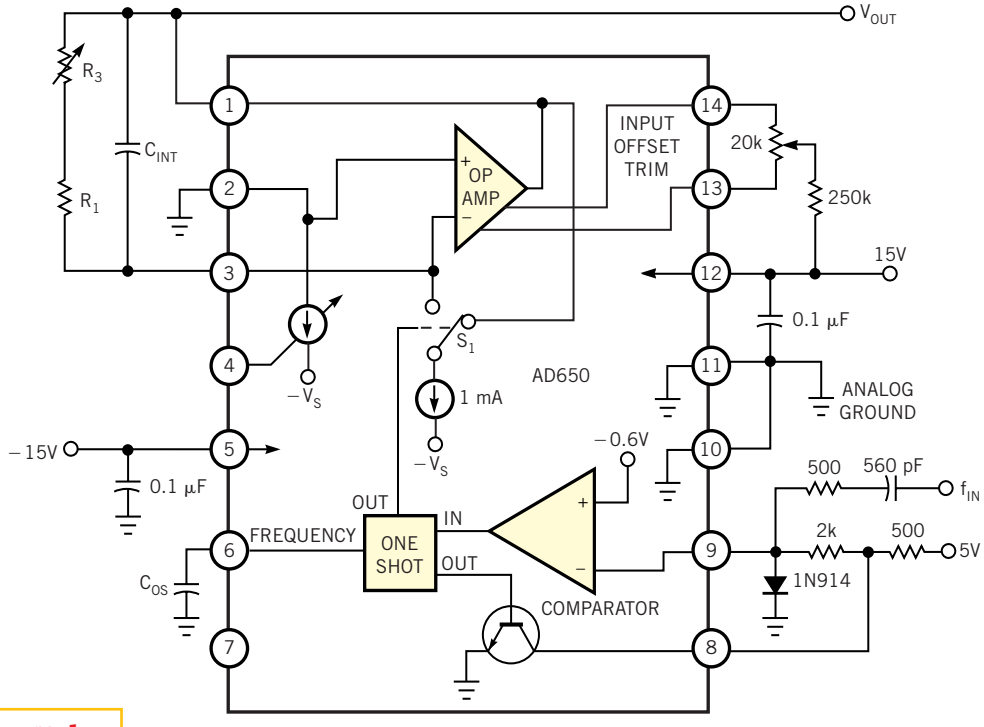


Figure 1

This circuit shows the AD650 in a frequency-to-voltage configuration.

Resolution of 18 bits requires a programmable clock source with a frequency resolution of 0.38 Hz (100 kHz/262,144). The AD9833 low-power DDS IC with on-chip 10-bit DAC is ideal for this task, because setting the clock frequency requires no external components. The device contains a 28-bit accumulator, which allows it to generate signals with 0.1-Hz resolution when you operate it with a 25-MHz master clock. **Figure 2** shows a block diagram of the AD9833 DDS chip. **Figure 3** shows the complete system. The most significant bit of the on-chip DAC switches to the V_{OUT} pin of the AD9833, thus generating the 0V-to-

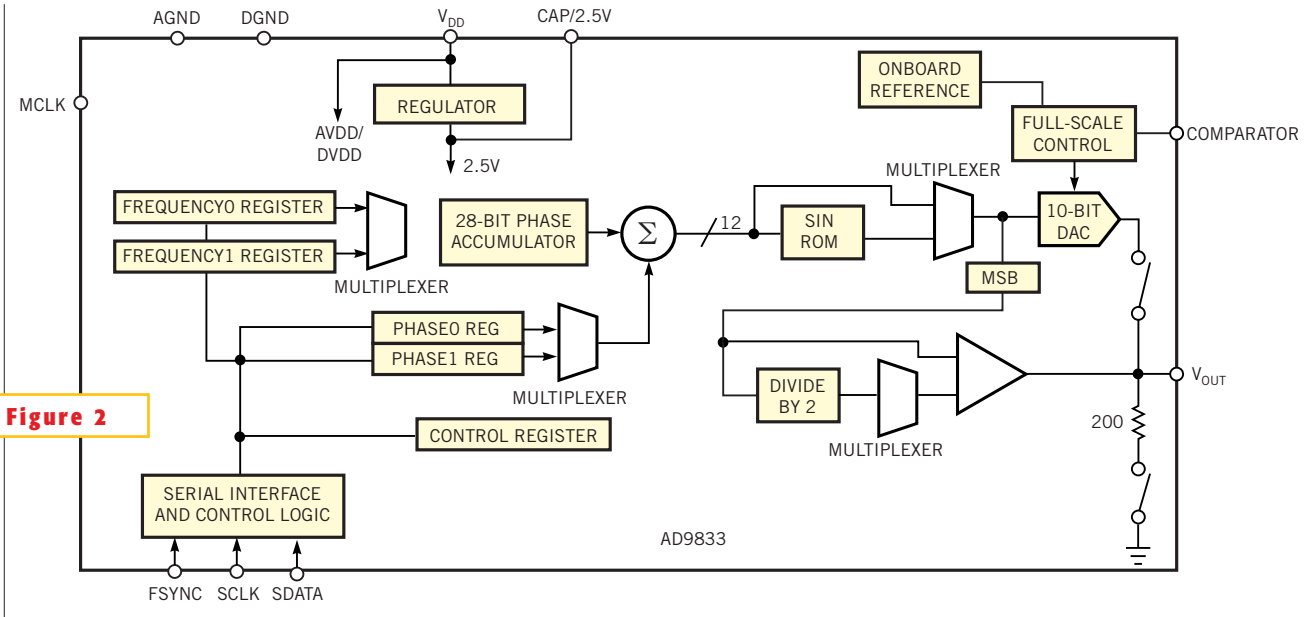


Figure 2

This DDS chip generates signals with 0.1-Hz resolution from a 25-MHz clock.

V_{DD} square wave that serves as the clock input to the AD650 voltage-to-frequency converter. Writing to frequency-control registers via a simple three-wire interface sets the clock frequency, thus programming the voltage output.□

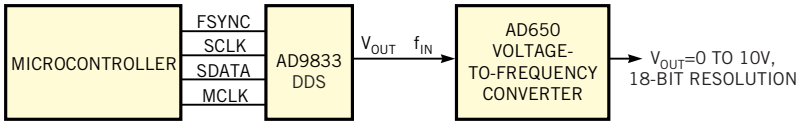


Figure 3

This DAC system delivers 0 to 10V output with 18-bit resolution.

Low-noise ac amplifier has digital control of gain and bandwidth

Philip Karantzalis, Linear Technology, Milpitas, CA

In low-noise analog circuits, a high-gain amplifier serves at the input to increase the SNR. The input signal level determines the input-stage gain; low-level signals require the highest gain. It is also standard practice in low-noise analog-signal processing to make the circuit's bandwidth as narrow as possible to pass only the useful input-signal spectrum. The optimum combination of an amplifier's gain and bandwidth is the goal of a low-noise design. In a data-acquisition system, digital control of gain and bandwidth provides dynamic adjustment to variations in input-signal level and spectrum. **Figure 1** shows a simplified circuit for an ac

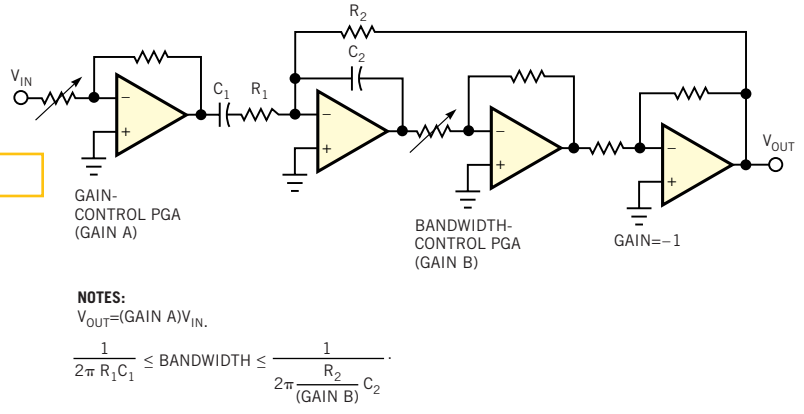
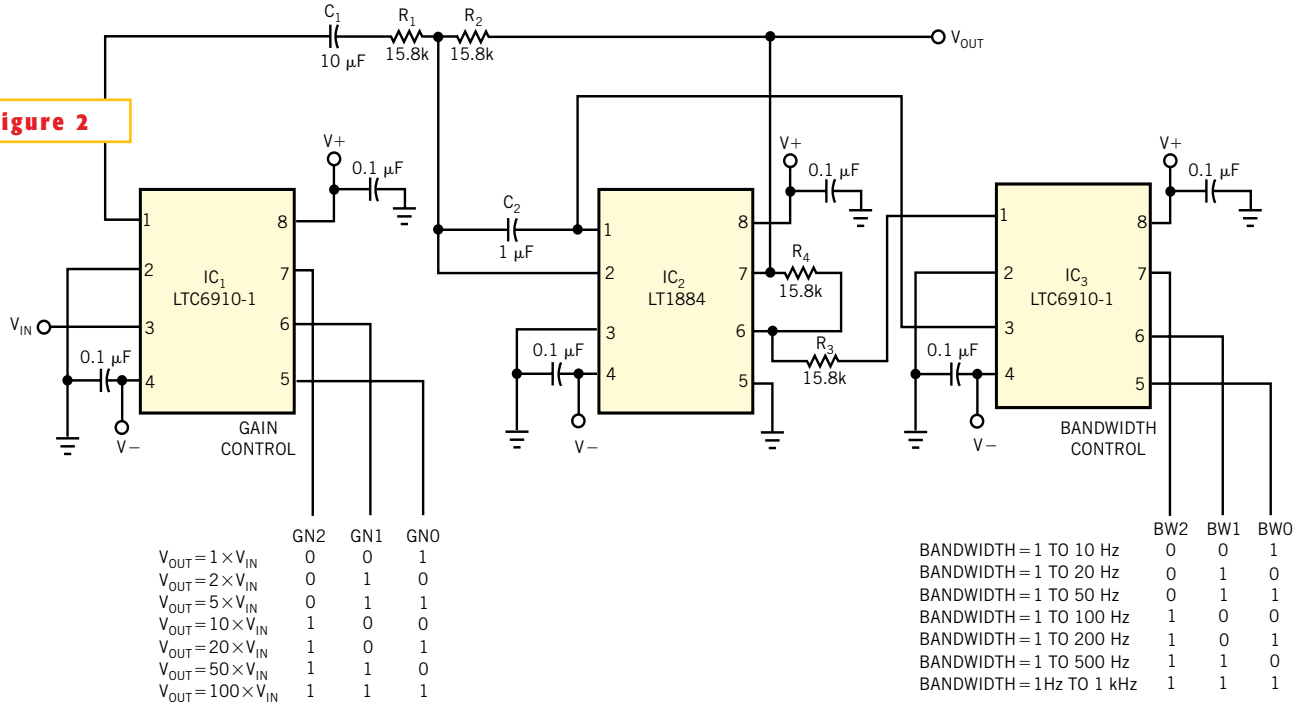


Figure 1

This ac-amplifier configuration offers both gain and bandwidth control.

Figure 2



	GN2	GN1	GN0
$V_{OUT}=1\times V_{IN}$	0	0	1
$V_{OUT}=2\times V_{IN}$	0	1	0
$V_{OUT}=5\times V_{IN}$	0	1	1
$V_{OUT}=10\times V_{IN}$	1	0	0
$V_{OUT}=20\times V_{IN}$	1	0	1
$V_{OUT}=50\times V_{IN}$	1	1	0
$V_{OUT}=100\times V_{IN}$	1	1	1

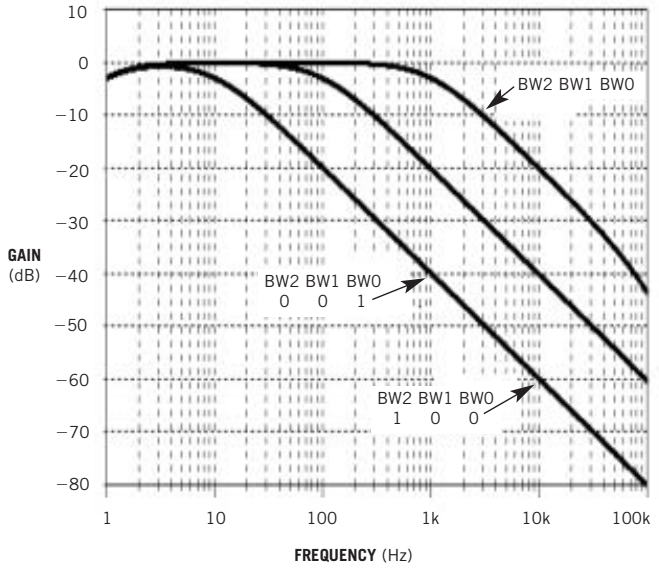
	BW2	BW1	BW0
BANDWIDTH = 1 TO 10 Hz	0	0	1
BANDWIDTH = 1 TO 20 Hz	0	1	0
BANDWIDTH = 1 TO 50 Hz	0	1	1
BANDWIDTH = 1 TO 100 Hz	1	0	0
BANDWIDTH = 1 TO 200 Hz	1	0	1
BANDWIDTH = 1 TO 500 Hz	1	1	0
BANDWIDTH = 1Hz TO 1 kHz	1	1	1

This detailed implementation of the circuit in Figure 1 operates with dual power supplies.

amplifier with control of both gain and bandwidth. The amplifier's input is a PGA (programmable-gain amplifier) providing gain control (Gain A). Following the input PGA is a first-order highpass filter formed with capacitor C_1 and input resistor R_1 of an integrator circuit. Inside the integrator's feedback path, the gain of a second PGA (Gain B) multiplies the integrator's −3-dB frequency, thus providing bandwidth control.

Figure 2 shows a complete circuit implementation using two LTC6910-1 digitally controlled PGAs and an LT1884 dual op amp. The input LTC6910-1, IC_1, provides digital gain control from 1 to 100 using a 3-bit digital input to select gains of 1, 2, 5, 10, 20, 50, and 100. The circuit's lower −3-dB frequency is fixed and set to 1 Hz. A second LTC6910-1, IC_3, is inside an LT1884-based (IC_2) integrator loop.

Figure 3



The frequency response of Figure 2's circuit shows unity gain and three digital bandwidth-control inputs.

The integrator's digital gain control becomes digital bandwidth control, which provides an upper −3-dB frequency control of 10 Hz to 1 kHz. The circuit's low-noise LT1884 op amp and LTC6910-1 (9 nV/$\sqrt{\text{Hz}}$ for each device) combine to provide high SNR. For example, the SNR is 76 dB for a 10-mV peak-to-peak signal with a gain of 100 and 100-Hz bandwidth or 64 dB for a 100-mV peak-to-peak signal with a gain of 10 and 1-kHz bandwidth. With an LT1884 dual op amp (gain-bandwidth product of 1 MHz), the circuit's upper frequency response can increase to 10 kHz by reducing the value of C_2. (The lower −3-dB frequency increases by reducing the value of C_1.) The circuit in **Figure 2** operates with ±5.5V dual power supplies. You can convert it to a single-supply 2.7 to 10V circuit by grounding Pin 4 of IC_1, IC_2, and IC_3; connecting a 1-µF capacitor from Pin 2 of IC_1 to ground; and connecting Pin 2 of IC_1 to pins 3 and 5 of IC_2 and Pin 2 of IC_3. **Figure 3** shows the frequency response of the circuit in **Figure 2** with unity gain and three digital bandwidth-control inputs.□

1-kV power supply produces a continuous arc

Robert Sheehan, Linear Technology, Milpitas, CA

Designing a high-voltage switching power supply that can produce a sustained arc can be challenging. This compact and efficient design delivers 1 kV at 20W and can withstand a continuous arcing, or short-circuit, condition (**Figure 1**). It uses standard, commercially available components. R_1 sets the LTC1871 switching-regulator controller for a nominal operating frequency of 120 kHz. The circuit operates as a discontinuous flyback structure, producing 333V across C_1. The diode/capacitor charge-pump multiplier triples this voltage to create 1000V at the output. **Figure 2** shows the switching waveforms. When the primary switch, Q_1, is on, the output rectifiers are reverse-biased, and energy is stored in the transformer, T_1. When Q_1 turns off, energy transfers to the secondary winding, and C_2 and C_3 pump up the output voltage through the rectifiers. The primary voltage goes high and is clamped through the transformer and rectifier, D_1, by the voltage across C_1. The transformer is well-coupled, so the leakage inductance creates little voltage spike. A small RC snubber across the primary winding damps the ringing and reduces EMI (electromagnetic interference).

For current-limit protection, the circuit in **Figure 1** contains two active circuits and one passive element. The voltage across the current-sense resistor, R_2, limits peak primary current to 7.5A. Q_2 provides secondary-side current limit. Notice the bump on the leading edge of the current ramp of Trace 2 in **Figure 2**. This bump coincides with the positive excursion of the voltage across R_3 in Trace 4, which is the refresh

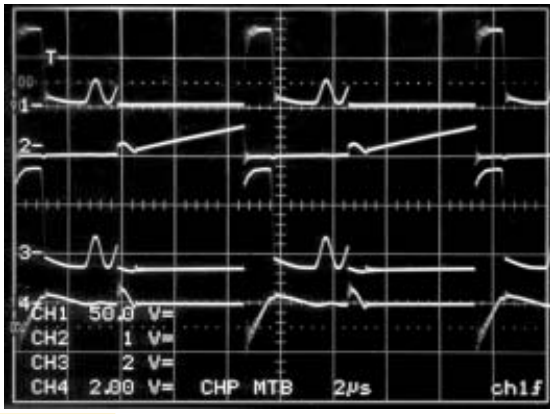
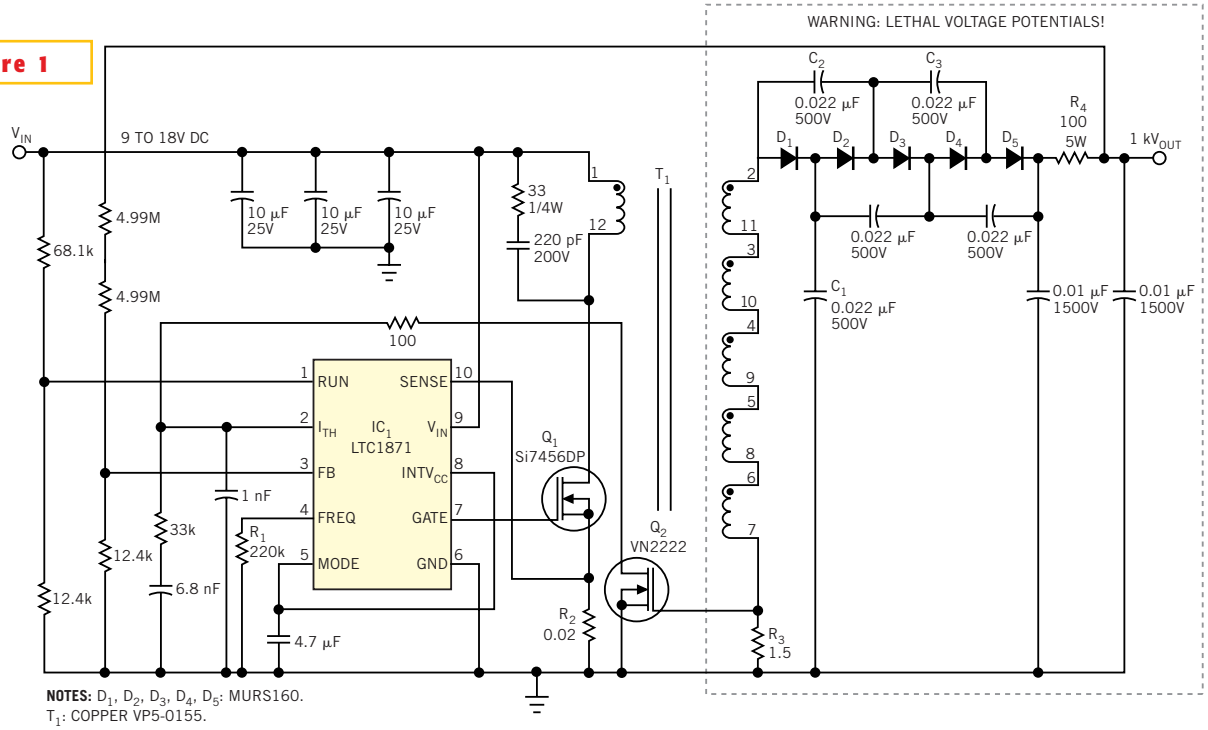


Figure 2 These are the switching waveforms for the circuit in Figure 1. Channel 1is the primary-switch voltage at T_1, Pin 12; Channel 2 is the primary-switch current into Q_1 drain (10A/division); Channel 3 is the secondary-switch voltage at T_1, Pin 2 (200V/division); Channel 4 is the voltage across R_3. (Secondary-switch current=2V/1.5Ω=1.33A/division.)

Figure 1



This circuit delivers 1 kV from a low-voltage input and can produce continuous arcing.

current for C_2 and C_3. When the circuit is overloaded, this slug of current becomes high enough to enhance Q_2, folding back the load current (**Figure 3**). A hard short circuit results in relatively low power dissipation. Omitting Q_2 for the secondary-side current limit results in substantially increased short-circuit current and internal power dissipation, resulting in failure of the primary switch Q_1. R_4 provides a load impedance for the power supply.

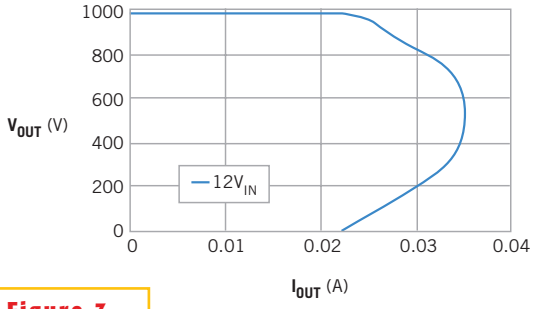


Figure 3 The circuit in Figure 1 has a foldback current-limiting characteristic.

This load helps to limit the peak-current stress in the multiplier capacitors and diodes. Don't skimp on the power rating for R_4, because dissipation during a continuous arc can be substantial. Should R_4 fail open, the feedback circuit forces a full duty cycle with catastrophic results. Too low a value for R_4 can result in charred circuits and hours of debugging. (Yes, a hearty explosion elicits a round of applause from the lab crew.) Arcing is the most stressful condition, and the output capacitor constantly charges and discharges (**Figure 4**). As a final figure of merit, the circuit is efficient (**Figure 5**). The efficiency reaches 87.3% at 12V input and a full load of 20W and increases to 87.7% with an overload of 24W.

So what is this circuit good for? A battery-operated bug zapper, perhaps. And, like raking a live wire across a grounded file, this is a great tool for befuddling the AM-radio listeners on the production floor. The circuit probably doesn't deliver enough energy for use as an ion generator for a plasma cutter, though one engineer I knew was willing to give it a try. A previous version of the circuit used a monolithic switcher, and with the right materials for banana jack and plug, created a bright orange glow and enough heat to raise thoughts about the fire extinguisher (plenty of ozone, too). I'd stay away from using this circuit as a cat trainer or an electric fence. The circuit does generate a lethal voltage potential, and lawsuits can be quite costly. Prototype this circuit at your own risk.□

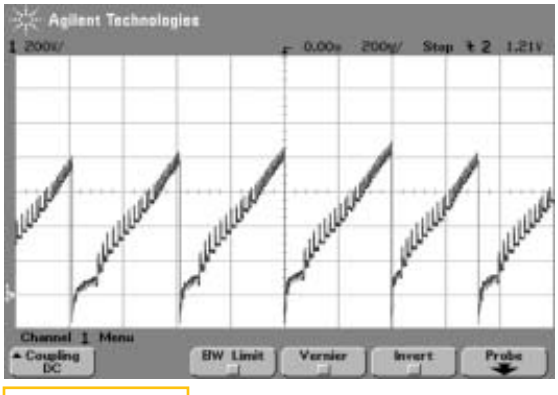


Figure 4 These waveforms represent the output voltage of the circuit in Figure 1 when arcing occurs.

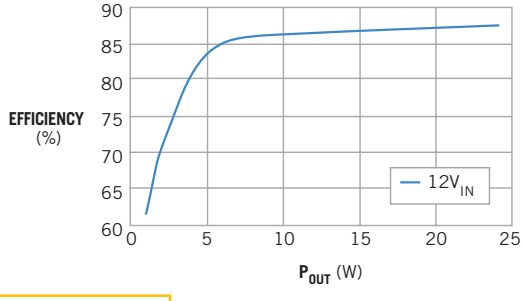


Figure 5 The conversion efficiency of the circuit in Figure 1 is well over 85%.