design ideas

Edited by Bill Travis

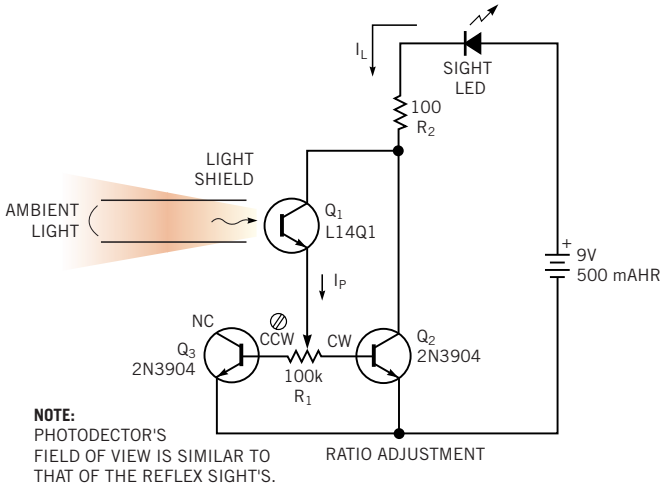
Circuit controls intensity of reflex optical sights

Stephen Woodward, University of North Carolina, Chapel Hill, NC

A POPULAR CATEGORY of aiming/pointing aids is the reflex, or "red-dot," sight. This system finds use in such diverse applications as astronomy, archery, and shooting. In the reflex sight, light from an internal source—typically a high-intensity red LED—reflects from a curved, transparent optical (reflex) element through which you view the target. The result of this geometry is that the image of the LED (the red dot) appears superimposed on the target image, thus indicating the point of aim. When you correctly adjust the aiming point of the telescope, bow, or gun, the target and LED images coincide. The reflex sight offers several advantages over competing pointing technologies, such as telescopic and open sights. These benefits include rapid and intuitive target acquisition, noncritical eye positioning, and a wide field of view.

For best sight performance, the intensity of the red-dot light source must at least roughly match the illumination level of the target. Otherwise, if the source is too dim, the aim-point dot loses itself in the brightness of the target. If too bright, the dot flares, and its apparent size increases, obscuring the point of aim and making precise pointing difficult or impossible. For this reason, most reflex sights require manual adjustment of the source intensity. Although this adjustment is effective enough, the time and attention needed to optimize intensity with a manual control detracts from the fast and intuitive target-acquisition capabilities of the red dot. The circuit in **Figure 1** uses phototransistor Q_1 to sense target brightness and automatically adjust the LED output. The circuit maintains near-constant dot size over a wide range of ambient-light levels.

Figure 1



This simple circuit automatically adjusts red-dot intensity in reflex optical sights.

Potentiometer R_1 divides Q_1's photocurrent, I_P, between the LED driver, Q_2, and the bias transistor, Q_3 (connected as a diode). The adjustment of R_1 therefore determines the ratio between drive current, I_L, and ambient (target) intensity over the range of 1 to B, where B is the beta of Q_2 (greater than 100). The prototype of the intensity-control circuit was packaged in a small plastic enclosure attached to the side of a Compasseco Inc (www.compasseco.com) Tech Force model 90 30-mm objective reflex sight. The light shield mimics the field of view of the sight, so the light that Q_1 samples represents the target intensity visible through the sight. Proper adjustment of R_1 results in good compensation of dot intensity for a wide range of both incandescent and natural light. The circuit effectively maintains a constant angular dot diameter of 4 minutes of arc under outdoor ambient lighting ranging from dark overcast to full sunlight. The circuit also delivers similar performance under indoor incandescent-lighting conditions. Compensation with fluorescent lamps, however, is less satisfactory because of the absence of an adequate near-infrared component in the spectrum of these light sources. You could probably fix this shortcoming by using a suitable visible-light filter in front of Q_1.

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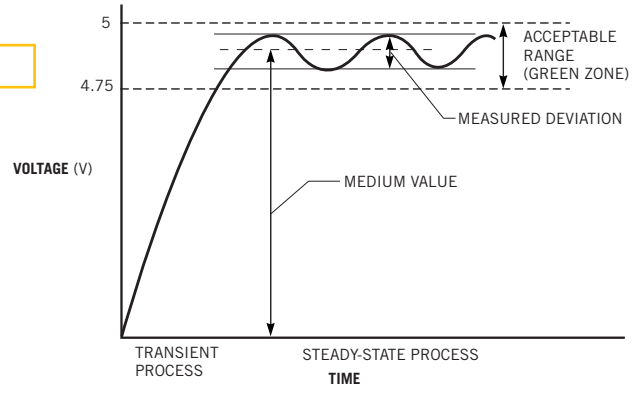
Indicator features expanded scale

Abel Raynus, Armatron International, Melrose, MA

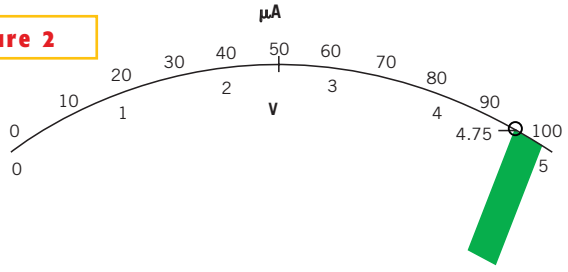
Test equipment for a production line should be user-friendly (read "idiot-proof") and should offer minimal test time. In many cases, the test fixture must give an operator only one answer: pass or fail. Usually, two indicators assume this role: green for pass and red for fail. In most applications, a sensor transforms the tested parameter to a voltage; the test fixture must measure this voltage and display the result. Sometimes, an operator needs to observe the dynamics of the tested parameter to verify that the results are inside the permitted "green zone." For example, when evaluating a regulated system's behavior, the operator is often interested in measuring the parameter's deviation and estimating its average value after the process reaches steady state (**Figure 1**). In this situation, using an analog meter with marked red and green zones is preferable to using a digital or bar-graph LED display.

Figure 1



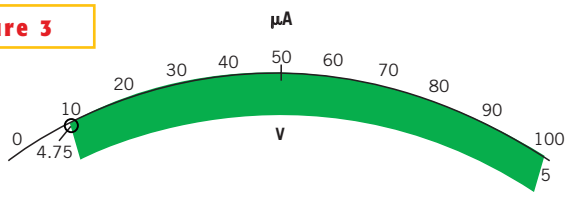
It's desirable to observe deviations in values inside the acceptable "green zone."

Figure 2



It's difficult to discern deviations from the norm when the green zone represents only 10% of full-scale.

Figure 3

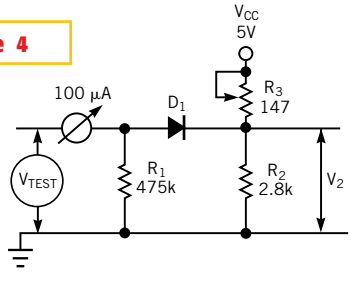


Expanding the green zone to 90% of full-scale makes readings much easier.

Assume that the range of the tested voltage is 4.75 to 5V. To make a voltmeter with maximum 5V reading by using a 100-µA dc meter, you would use a series resistor of 50 kΩ. The meter scale is linear, and the tested voltage zone represents only 5% of full-scale (**Figure 2**). It is difficult for an operator to observe the meter reading inside such a narrow zone. It would be desirable to expand the test zone to, say, 90% of full-scale (**Figure 3**). The circuit in **Figure 4** does just that. When the tested voltage, V_{TEST}, is lower than the threshold voltage, V_2, the diode, D_1 does not conduct, and the voltmeter comprises the microammeter and resistor, R_1. When the tested voltage surpasses the threshold V_2, the diode conducts, and resistor R_2 connects in parallel with R_1. The voltmeter's impedance decreases, thereby expanding the measurement scale. You can calculate the values of resistors R_1, R_2, and R_3 as follows:

- The voltage at the beginning of the tested zone, 4.75V, should consume 10% of the scale, with a corresponding current of 10 µA. Hence, neglecting the internal meter impedance, R_1 equates to 4.75V/10 µA, or 475 kΩ.
- After the measured voltage exceeds the threshold level, 4.75V, the voltmeter impedance equates to $R_{1,2}=(5-4.75)V/(100-10)$ µA, or 2.8 kΩ.
- Hence, $(R_1R_{1,2})/(R_1-R_{1,2})=(475\times 2.8)/(475-2.8)=2.8$ kΩ, and $R_3=R_2(V_{CC}/V_2-1)=2.8\ (5/4.75-1)=147\Omega$.

Figure 4



This simple circuit expands the acceptable test results to 90% of full-scale.

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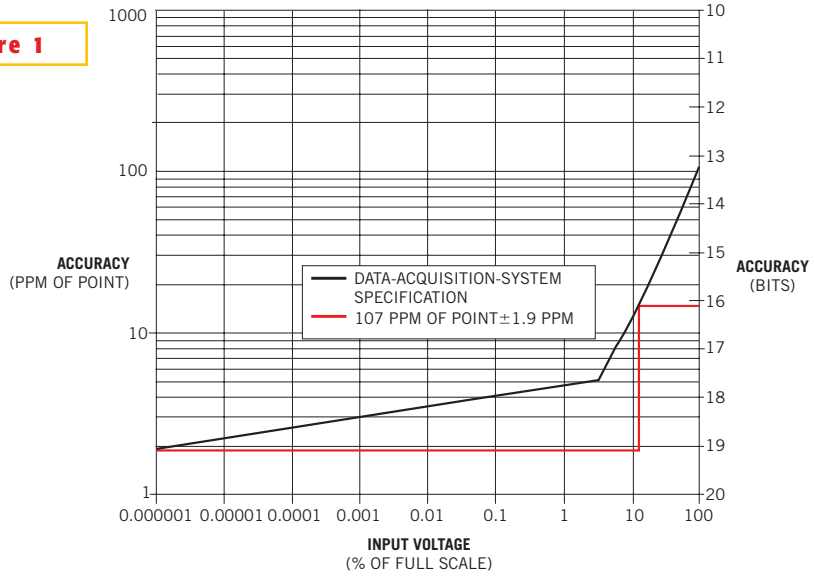
16-bit ADC provides 19-bit resolution

Alain Guery and Charles Kitchin, Analog Devices, Wilmington, MA

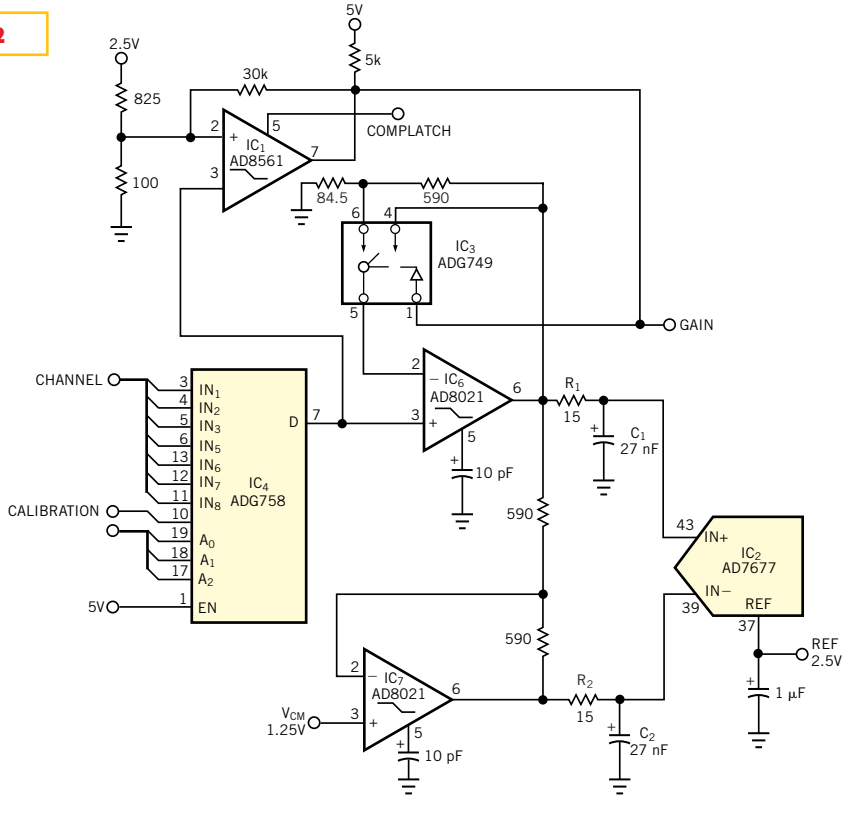
Many data-acquisition systems require both high accuracy and a fast acquisition rate. These attributes allow the system to detect small data signals and to group more sensor channels into the same system. With more channels, the system can be smaller, less expensive, and less power-consuming. Long-distance optical communications and medical equipment, such as CT scanners, can benefit from a fast and accurate data-acquisition system. Optical power systems, such as laser pumps, need to constantly monitor their power levels. In such systems, the incoming laser-power range and the laser control-loop response time are such that the system needs a dynamic range of 90 dB or more and a sampling rate of 1M sample/sec. In CT scanners, 16- to 22-bit resolution is necessary for the data-acquisition system to process the large dynamic range of the X-rays through various body tissues. A large number of photodetectors (more data-acquisition channels) and high data accuracy improve the image resolution.

Figure 1



Using a programmable-gain amplifier ahead of an ADC increases the accuracy of a 16-bit ADC to 19 bits.

Figure 2



This system provides 19-bit accuracy by combining a programmable-gain amplifier with a 16-bit ADC.

These two examples show the need for relative accuracy, as opposed to absolute accuracy. Although it's important to be able to detect a 10-nW change in an optical power of 1 µW, it is almost irrelevant to see the same 10-nW difference between 1 mW and 1.00001 mW. However the ADC's accuracy appears under the integral-nonlinearity specification as an absolute error. For the best relative accuracy, a classic solution is to use a programmable-gain amplifier in front of an accurate ADC. The AD7677 ADC specifies ±15-ppm of full-scale nonlinearity (±1 LSB at the 16-bit level). A programmable-gain amplifier ahead of this converter must be able to settle

quickly enough with the same resolution and speed as the ADC. It also must have the lowest noise possible, because the amplifier sets the SNR of the data-acquisition system. To meet these challenges, the amplifier in this design uses an AD8021, an op amp combing speed, accuracy, and fast settling time. The noise density of the AD8021 is only 2 nV/$\sqrt{\text{Hz}}$. **Figure 1** shows how the gain settings of the programmable-gain amplifier divide the specified accuracy of the ADC. The system reaches 19-bit accuracy when the input level is low.

Relative accuracy is normally specified as parts per million of reading plus or minus the absolute minimum error. The circuit in **Figure 2** can achieve a relative accuracy of 107 ppm±1.9-ppm maximum error. Analog multiplexer IC_4 combines many lower bandwidth channels to take advantage of the 1M-sample/sec sampling rate of the ADC. Because the programmable-gain amplifier presents a high input impedance to the multiplexer, you can cascade the multiplexer, thus increasing the number of channels. The multiplexer also provides a simple way to calibrate the offset and gain errors at each gain setting by applying a calibration-reference voltage to one of the multiplexer's input ports. You need to calibrate only at power-up or when operating conditions, such as temperature, change. The amplification chain comprises the multiplexer, the comparator, and the amplifier on one side and the ADC on the other side. The successive-approximation structure of the AD7677 ADC allows the individual sections in the amplification chain to work simultaneously. While the ADC converts one sample, the comparator/amplifier can settle the following channel. Therefore, the data-acquisition system can operate at the ADC's maximum sampling rate.

Shortly after the analog multiplexer settles, the fast comparator, IC_1, applies the appropriate gain setting. The comparator's thresholds are such that the amplifier does not saturate or clip the signal after amplification by IC_6 and IC_7. The AD8561 comparator has a response time of 7 nsec. It integrates a latch signal that holds the gain constant during the time the amplifier settles and the ADC acquires the signal. The usual programmable-gain-amplifier configuration requires the user to predict the amplifier's gain setting before applying the signal at the input. The programmable-gain amplifier in **Figure 2** has an "autorange" feature that selects the most appropriate programmable-gain amplifier gain to maximize accuracy without incurring saturation or clipping. The comparator incorporates hysteresis to reduce gain-setting change when signals are close to the limits of an individual gain range. The circuit automatically boosts the ADC accuracy to 19 bits while maintaining a full-speed sampling rate of 1M sample/sec.

IC_6 amplifies the multiplexer signal using one of two possible gain settings: 1 or 8. You can modify the feedback network to provide different gains to a maximum of 25. The analog switch, IC_3, controls the gain setting. The high gain-bandwidth product of the AD8021 op amp provides more than enough bandwidth, so its compensation capacitor remains the same for all gains. Amplifier IC_7 generates the differential signal for the ADC. The settling times of the comparator and the amplifier and the acquisition time of the ADC are all significantly less than the ADC's full conversion period of 1 µsec. The RC noise filters at the two ADC inputs, R_1/C_1 and R_2/C_2, use this extra time. These filters limit the noise bandwidth of the programmable-gain amplifier, which is the main noise source of the data-acquisition system when IC_7 operates at a gain of −1.

Figure 3 shows the circuit's nonlinearity. The photo shows a maximum nonlinearity of 0.44 LSB and a minimum of −0.37 LSB for the highest gain setting, which poses the most difficult challenge. This nonlinearity corresponds to a typical error of ±0.9 ppm. At a gain of 8, output noise is 85 µV rms. If desired, you can further reduce the noise by using software averaging. **Figure 4** shows the complete data-acquisition system assembled using the AD7677 evaluation board. The pc-board area measures 15×30 mm.

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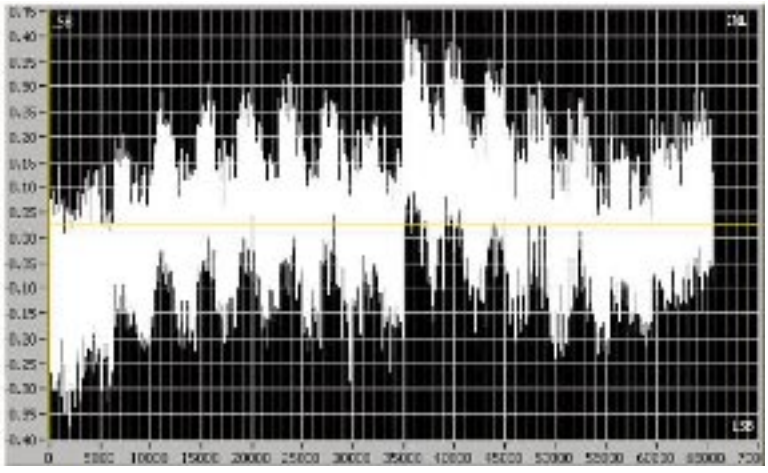
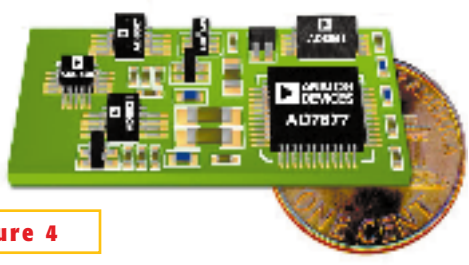
Figure 3



This plot shows the differential nonlinearity of a data-acquisition system for all possible ADC codes.

Figure 4



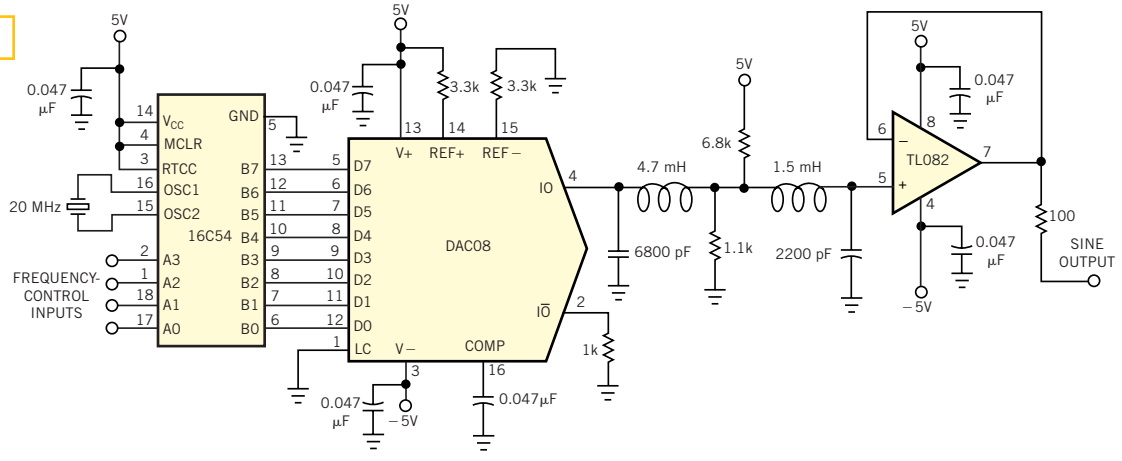
The dime shows the relative size of the complete data-acquisition system.

Microcontroller emulates numerically controlled oscillator

Tom Napier, North Wales, PA

Microcontrollers commonly add intelligence or digital functions to products, but they can also provide a variety of analog signals. An 18-pin PIC 16C54 microcontroller, combined with an inexpensive, 8-bit DAC and a simple lowpass filter, can generate sine waves from dc to approximately 50 kHz with a tuning resolution of 24 bits. The accuracy and stability of the output is as good as that of the crystal driving the microcontroller. You can connect a binary data signal to one or more PIC ports to apply FSK (frequency-shift-keying), BPSK (binary-phase-shift-keying), or QPSK

Figure 1



An inexpensive microcontroller and DAC emulate a numerically controlled oscillator.

LISTING 1—16C54 NUMERICALLY CONTROLLED OSCILLATOR-EMULATION ROUTINE

```
START   MOVLW   0
        TRIS    PORTB           ;Set port B to output
        MOVWF   PHASL           ;Initialize phase
        MOVWF   PHASM
        MOVWF   PHASH
        MOVWF   ZER             ;Constant = 256
        MOVLW   64
        MOVWF   MAX             ;Constant = 64

; Set up default frequency, here 1000 Hz

        MOVLW   64
        MOVWF   FREQL
        MOVLW   150
        MOVWF   FREQM
        MOVLW   1
        MOVWF   FREQH

        GOTO    DONE

; Set up fixed return address in stack

RETX    CALL    RETY
        GOTO    LOOP            ;Start generating output

RETY    RETLW   0               ;Dummy to fix return address

DONE    CALL    RETX            ;Set up fixed return address

; Look-up return reenters at this point with sine sample in W

LOOP    BTFSC   TEMP,INV        ;Test if inversion needed
; Replace previous instruction by BTFSC PHASH,INV
; if BPSK modulation not needed.
        SUBWF   ZER,0           ;Invert output
        MOVWF   PORTB           ;Output sample

; Check if user wants to load a new frequency
        BTFSC   PORTA,DAT       ;Test for change flag
        GOTO    NEW             ;Get new user frequency
```

```
; Three-byte addition of control to phase accumulator
        MOVF    FREQL,0         ;Get frequency low byte
        ADDWF   PHASL,1         ;Increment phase low byte
        MOVF    STATUS,0
        ANDLW   1               ;W = carry
        ADDWF   PHASM,1         ;Add carry
        BTFSC   STATUS,CY       ;Skip if no carry
        INCF    PHASH,1         ;Propagate carry
        MOVF    FREQM,0         ;Get frequency mid byte
        ADDWF   PHASM,1         ;Increment phase mid byte
        BTFSC   STATUS,CY       ;Skip if no carry
        INCF    PHASH,1         ;Propagate carry
        MOVF    FREQH,0         ;Get frequency high byte
        ADDWF   PHASH,1         ;Increment phase high byte

        SWAPF   PORTA,MOD       ;Modulation input to bit 7
        XORWF   PHASH,0         ;XOR inversion bit
        MOVWF   TEMP            ;Save inversion bit
; Remove above three instructions if modulation not needed.

        MOVF    PHASH,0
        ANDLW   63              ;Get table index
        BTFSC   PHASH,REV       ;Test if reversal needed
; Replace above instruction by BTFSC TEMP,REV for QPSK

        SUBWF   MAX,0           ;Reverse index direction
        ADDWF   PC,1            ;Jump to table

; Partial sine look-up table
; 65 entries - sines of first quadrant

        RETLW   128
        RETLW   131
        RETLW   134
        :
        :
        RETLW   255
```

(quadrature-phase-shift-keying) modulation to the output. **Figure 1** shows the emulation scheme, and **Listing 1** controls the operation of the microcontroller. The 16C54's firmware emulates a 24-bit numerically controlled oscillator. A fixed-length loop continuously adds the contents of one set of registers (the frequency control) to another set (the phase accumulator). The phase accumulator increments at a rate proportional to the desired output frequency and wraps around once per output cycle.

With a 24-bit accumulator, the output frequency is $f \times N/[67108864(L+2)]$, where f is the clock frequency, N is the tuning control number, and L is the number of instructions in the loop. (The loop period is two instruction times longer than the instruction count, L.) For example, if the PIC's clock crystal's frequency is 16.777 MHz, and the loop has 30 instructions, you can set any frequency to approximately 40 kHz in steps of 1/128 Hz. Once per loop, the highest byte of the phase accumulator selects an output sample from a 65-element look-up table, which contains one quadrant of a sine wave. To create the other three quadrants, bit 6 determines whether to read the table forward or backward, and bit 7 specifies the output sign. An exclusive-OR operation on bit 7 with a port bit generates BPSK operation. An exclusive-OR operation on both bits 6 and 7 with port bits generates QPSK modulation. The result goes to the DAC via the PIC's 8-bit output port. A 50-kHz lowpass filter then converts the DAC's output into a smooth sine wave.

You can preset the output frequency or load it serially via two pins of the PIC's 4-bit port. You obtain FSK by using an input bit to select which of two frequency-control registers to use. If the two frequencies have a large common multiple, as in minimum-shift keying, the accumulator can be shorter, leading to a higher output frequency for a given clock input. Without modulation, the firmware loop can be as short as 26 instruction times (**Listing 1**). You can insert nonoperation instructions to make the loop-repetition rate a convenient submultiple of the crystal frequency. For example, a 31-instruction loop and a 20-MHz crystal yield a scale factor close to 104 steps/Hz.

The code takes advantage of a quirk in the 16C54's operation: If two addresses exist on the return stack, the first copies endlessly into the second every time the routine pops the second. The initialization code puts two copies of the loop-start address into the return stack, causing all subsequent RETLW instructions to jump to the start of the loop. Indexing into the look-up table with a calculated GOTO instruction both supplies an output sample and executes a jump to restart the loop. This procedure is much faster than executing a CALL, a GOTO, a RETLW, and a further GOTO. You can download **Listing 1** from the Web version of this article at www.ednmag.com.

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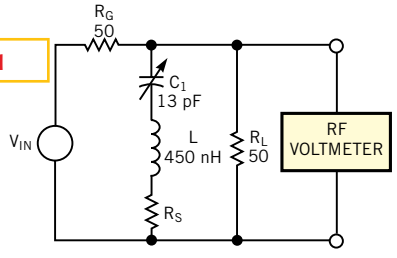
Method simplifies testing high-Q devices

Alan Victor, IBM Microelectronics, Research Triangle Park, NC

THE DESIGN of low-phase-noise oscillators requires careful attention to resonator unloaded Q. In the construction of a low-phase-noise, high-frequency oscillator, the goal is to achieve an unloaded-Q figure greater than 400 in a reasonable package. Also, you need to monitor the effect of the package and pc-board arrangement. Shielding, inappropriate grounding, and some construction techniques can degrade unloaded Q. Q meters; various bridges, such as Maxwell and Hayes; and both vector and scalar impedance analyzers are useful but inconvenient-to-use test instruments. You must carefully set up test fixturing and calibration that duplicates the final environment to obtain reasonable agreement with the final measured results. A simple test set uses nothing more than the voltage-divider relation with the device under test embedded as a series trap network (**Figure 1**). You can measure the inductor's value, or calculate it from known equations based on the inductor's form factor, such as solenoid, toroid, helical, or flat spiral. You use the inductor's value to select C_1, a variable, air-dielectric high-Q capacitor. At resonance, the impedance of the inductor-capacitor combination goes to zero, so the effective load is the series resistance R_S in parallel with the 50Ω termination resistance.

Figure 1



A simple test set allows you to determine the unloaded Q of an inductor.

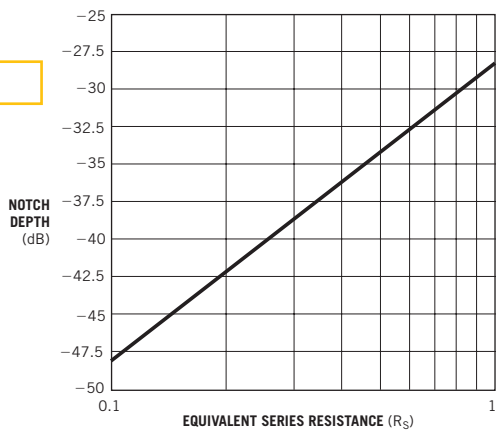
TABLE 1–NOTCH DEPTH VERSUS SERIES RESISTANCE

R_S (Ω)	Notch depth (dB)
0.1	−47.993
0.2	−42.007
0.3	−-38.52
0.4	−36.055
0.5	−34.151
0.6	−32.602
0.7	−31.297
0.8	−30.171
0.9	−29.181
1	−28.299

You use an RF generator and voltmeter to read the depth of the notch the trap creates. This attenuation depth is a function of the remaining finite-series resist-

ance of the resonator. **Table 1** shows the notch attenuation for R_S ranging from 0.1 to 1Ω. These values assume 50Ω source and termination impedance and the component values shown in **Figure 1**. Unloaded Q equates to X_L/R_S, where X_L is the reactance of the inductor, and R_S is the equivalent series resistance. **Figure 2** shows the notch attenuation as a function of the equivalent series resistance. In addition, a crosscheck is available: You can the 3-dB bandwidth of the notch and calculate unloaded Q from f_0 divided by the bandwidth. Finally, as a "sanity check," you can readily reduce the unloaded Q to a known value by inserting a series resistance in the trap circuit. The reduction in unloaded Q should correlate with added resistance value. Any variations you notice in these simple experiments are usually the result of subtle factors. One factor in particular is a component operating near its self-resonant frequency. In the test case of **Figure 1**, six-gauge wire on a 0.75-in. Delron rod with careful construction lets you achieve unloaded Q near 500 at 70 MHz. The measurement technique unveils issues with shielding, namely the reduction in Q from the effect of the shield on the solenoid coil. The details of the measurement are as follows:

Figure 2



The notch depth of the circuit in Figure 1 at resonance is inversely related to the equivalent series resistance of the inductor.

Assume an inductor with known L and X_L at a frequency of interest f_0. The inductor shall resonate in a series-tuned (trap) configuration, driven from a 50Ω generator and terminated in a 50Ω shunt. An RF voltmeter placed across the shunt reads notch depth in decibels. From **Figure 2**, you can determine the unloaded Q from the expression $Q=X_L/R_S$. For example, a solenoid inductor measuring 0.75 in. in diameter and wound with five turns of six-gauge wire has a measured inductance of 460 nH at 65 MHz. The inductor series-resonates at 65 MHz with a 13-pF capacitor. You set the signal generator at 65 MHz and use a variable, air-dielectric capacitor to fine-tune the notch at 65 MHz. The measured notch depth is 36 dB. R_S is 0.4Ω, and the unloaded Q is 469. You can readily notice changes in the depth of the notch with fine variations in coil position relative to conducting surfaces.

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