design ideas

Edited by Bill Travis

Gate-drive method extends supply's input range

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Industrial and telecom applications often require a nonisolated, low-voltage supply from a high-voltage input. IC manufacturers have responded to that need with the application of high-voltage processes and offer control ICs that work to 50V and higher. That voltage is sometimes insufficient, and you need further design techniques to extend the input voltage. The buck converter in **Figure 1** represents one such technique. In addition to allowing circuit operation over a wide input-voltage range, the technique reduces power dissipation, because the control circuit does not operate directly from V_{IN}. The circuit uses a linear regulator and a source-switched driver to buffer a control IC from a line whose voltage is as high as 110V. When you apply the input voltage, current flows through resistor R_2 and zener diode D_2, clamping the gate voltage of FET Q_1 to 9.1V. C_2 reaches a voltage of approximately 6V, which is equal to Q_1's gate voltage minus its typical turn-on threshold of 3V. FET Q_1 now acts as a crude linear regulator and allows the control circuit to become active.

The source-switched driver of Q_2, Q_4, and Q_5 then comes into play to allow the supply to come into regulation. The TL5001's open-collector output switches to a low state to turn on the main power switch, Q_3. With the gate of FET Q_5 also held at 9.1V and the output pin of the TL5001 low, current flows through Q_5's

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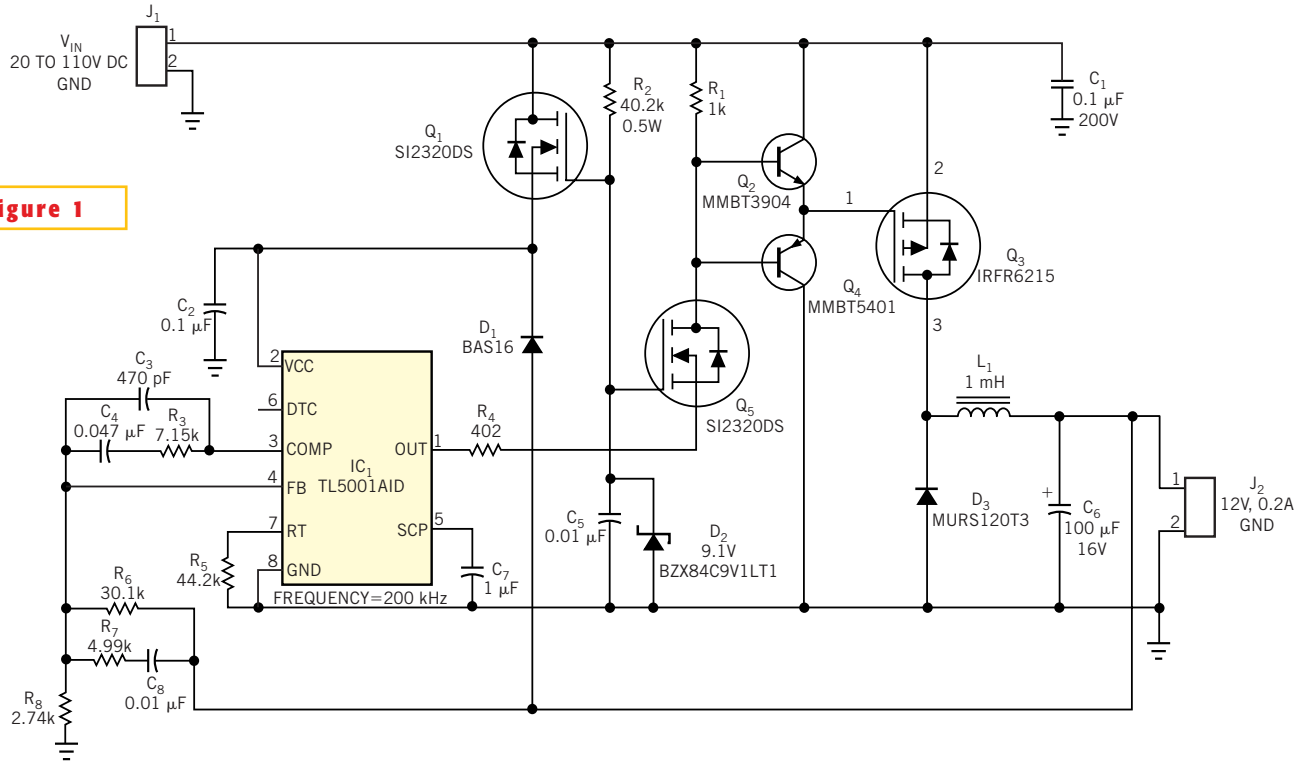
Figure 1



A buck converter uses switched-source gate drive to generate high output voltages.

drain-to-source pins. The amount of drain current that flows is equal to: (9.1V−Q_5's turn-on threshold−IC_1's Pin 1 saturation voltage)/R_4. In this example, this current is nominally approximately 12 mA. Because most of this current flows through R_1, the value of R_1 sets the voltage amplitude used for the gate drive of Q_3. With a value of 1 kΩ for R_1, the voltage across it is 12V. Transistors Q_2 and Q_4 form an npn/pnp pair to quickly switch gate-drive current into and out of Q_3. The base-emitter junction of Q_4 conducts when a voltage drop exists across R_1. This conduction quickly pulls down the gate of Q_3 from V_{IN} to approximately 11.2V (12V−V_{BE}). Because Q_3 is a p-channel FET, pulling the gate to 11.2V lower than the source turns it on. When current is not flowing in R_1, the base of Q_2 pulls up to V_{IN}, a voltage that forward-biases its base-emitter junction.

The gate of Q_3 quickly charges to near-V_{IN} potential, thereby turning off Q_3. This drive circuit is fast, because none of the transistors operates in a saturated mode; therefore, Q_3 can attain 0.5-µsec turn-on time. This speed means that the circuit can achieve reasonably high operating frequencies with the low duty cycles you encounter in a high-voltage input. You can scale this gate-drive circuit for higher or lower input voltages by the proper selection of the drain-source (or collector-emitter) ratings of Q_1, Q_3, Q_4, and Q_5. All must have voltage ratings greater than the input voltage, and all, except for Q_1, should also be able to switch at high speeds. The addition of diode D_1 offers two advantages. It allows the control circuit to operate after start-up from the output voltage, rather than the input voltage. This method is more efficient, inasmuch as the input voltage is relatively high. A bias-power savings of approximately sevenfold is the result. Also, adding D_1 pulls the source pin of Q_1 to approximately 11.2V, thus Q_1 turns off. All bias power to the controller now comes from the output voltage, and Q_1 no longer dissipates power.□

Active-clamp/reset-PWM IC becomes more versatile

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The UCC3580 (www.ti.com), IC_1 in **Figure 1**, is an active-clamp/reset-PWM IC that has all the requisites of a power-supply IC except for current limit. You can use the shutdown pin (16) for this purpose (see the UCC3580 data sheet). But when the shutdown pin activates, the soft-start capacitor normally connected to Pin 15 discharges, and the converter starts again, resulting in hiccup mode. Poor dynamic response ensues because of this circuit behavior. The problem becomes especially serious when you hot-plug a load card, with typically 100-µF decoupling across the converter's output, into the motherboard. You can avoid this problem by not using the shutdown pin for current limiting. Instead, use the

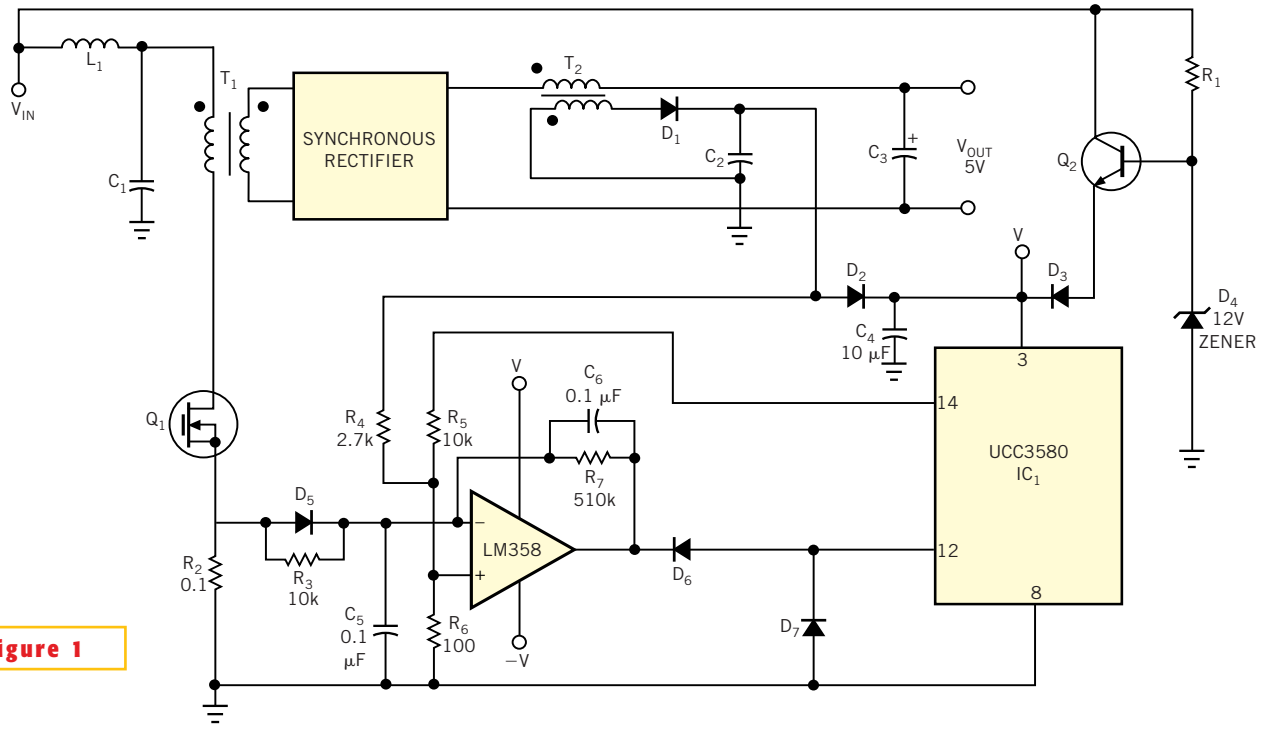

Figure 1

This circuit does not use the shutdown pin of the PWM IC; instead, it relies on the error amplifier's output to provide current limit.

error amplifier's output pin, Pin 12. Q_1 is the main switch, T_1 is the main transformer, and C_1 is the bulk capacitor. Q_2, D_3, and D_4 provide power (+V) for IC_1 during start-up and current limit. D_1 and C_2 rectify and filter the voltage from the auxiliary winding of T_2 to power the control circuit during normal operation. R_2 senses the current in the main switch, Q_1.

The LM358 op amp provides current limit. Diode D_6 isolates the op amp and Pin 12 of IC_1 during normal operation. According to the data sheet of UCC3580, the error amplifier's output should pull down to 0.3V or lower for 0% duty cycle. This condition forces you to use a negative supply (−V) for the op amp to obtain rated performance. As **Figure 1** shows, the same supply voltage (+V) serves for the PWM IC and the op amp. You can obtain the negative supply voltage (−V) for the op amp from another winding on T_2. Even though the voltages that T_2 generates decrease in foldback condition, the op amp continues to obtain +V from Q_2. A negative voltage (−V) from T_2 is adequate for proper operation of the op amp. The Schottky diode, D_7, from Pin 12 to ground protects the error amplifier's output from large negative voltages.

The inverting input of the op amp senses the peak pulse voltage across R_2. Diode D_5 helps C_5 to charge to peak voltage (peak detection), and R_3 helps to discharge C_5 when the peak voltage across R_2 decreases. Use a slow diode for D_5. The reference voltage at the noninverting input has two components—first, from the fixed 5V reference (Pin 14) of IC_1; second, from the voltage generated by the T_2 winding. This voltage decreases with output voltage, and voltage foldback occurs at the noninverting input. The 50-mV component from the fixed 5V reference is necessary for start-up. As the current limit starts, the output voltage starts to decrease, and the noninverting-input voltage also decreases, causing foldback. With this circuit, if the current limit starts at an output current of 10A, the output short-circuit current is 2A. The output recovers even with minimal current hysteresis. The positive voltage that the T_2 winding generates decreases from 13V just before current limit to 3V at short circuit. This circuit does not influence the transient response of the converter.□

Circuit provides hiccup-current limiting

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Current-limit protection is an essential feature for power-supply systems. The three major types of current-limit-protection mechanisms are constant, foldback, and hiccup. Hiccup current limit performs the best of the three types; however, the implementation is rather complex. In this scheme, upon detection of an overcurrent event, the whole power supply shuts down for an interval before it tries to power itself up again. The cycle repeats until the overcurrent fault disappears. With such operation, the dissipation in the power supply itself is minimal. You can incorporate the circuit in **Figure 1a** into the PWM circuit of a switch-mode power supply to implement the hiccup feature. **Figure 1b** represents a typical shunt-voltage regulator to regulate the V_{CC} that powers the PWM controller.

Most PWM controllers have an undervoltage-protection feature, in which the internal circuitry shuts down whenever its V_{CC} drops below a certain threshold. For example, assume that the circuit in **Figure 1a** works with a UCC3570 PWM controller. In this chip, an excessive current that causes the Count pin to exceed 4V or the ILIM pin to exceed 0.6V sets the shutdown latch. This action then forces the PWM controller's output to go low and discharge the soft-start capaci-

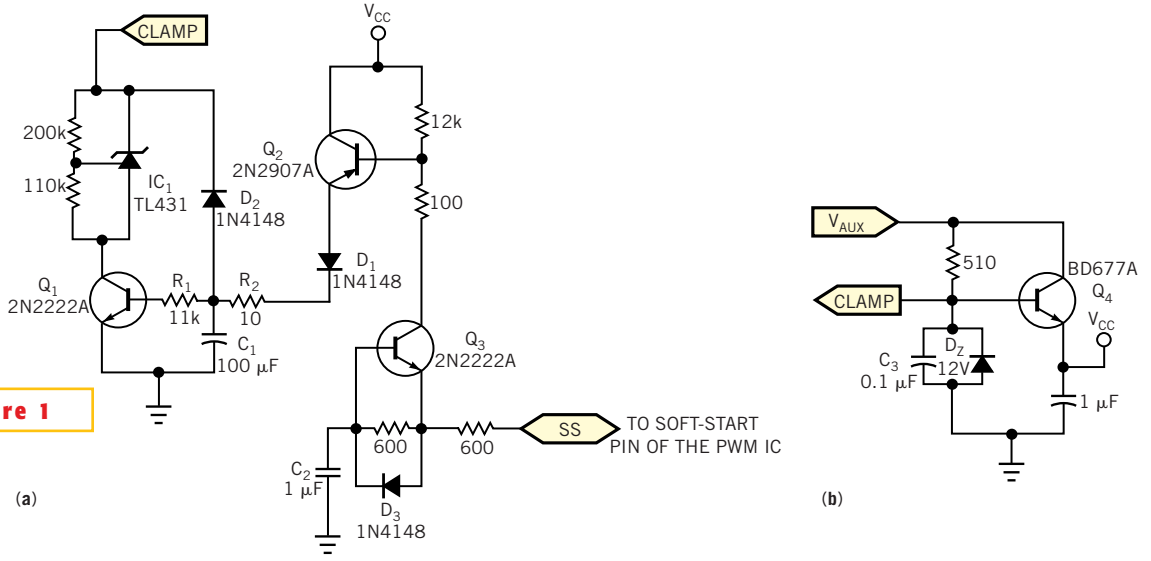

Figure 1

You can incorporate hiccup circuitry (a) into your PWM-control scheme, using a typical shunt regulator (b) to regulate the supply voltage to the PWM chip.

tor, C_2. The discharge current of C_2 causes Q_3 and, hence, Q_2 to turn on for a short interval to charge the timing capacitor, C_1. The moment the voltage across C_1 builds up, Q_1 turns on and activates IC_1 to overwrite the V_{CC} voltage, which D_Z initially set to a voltage—in this case, 7.02V—low enough to turn off the PWM controller (**Figure 1b**). With this action, the controller becomes temporary disabled, and the shutdown latch resets.

After C_2 completely discharges, Q_3 and Q_2 switch off, and the charge stored in C_1 continuously supplies the base drive needed to hold Q_1 on through R_1. The PWM controller then stays in sleep mode for the fixed interval, t_{SLEEP}, until the discharge current of C_1 can no longer keep Q_1 on. You can estimate this sleep-time interval (**Figure 2**) by using the following equation:

$$\frac{I_{IC1}}{h_{FEQ1}} \times R_1 = \left(V_{C1}(0) - V_{BEQ1}\right) \times e^{\frac{-t_{SLEEP}}{\tau}},$$

where I_{IC1} is the forward current of IC_1 ($\simeq$10.7 mA with V_{AUX}=12.5V), $V_{C1}(0)$ is the initial voltage stored in C_1 ($\simeq$5.05V), $\tau=R_1C_1$ ($\simeq$1.1 sec), h_{FEQ1} is the dc current gain of Q_1 ($\simeq$170 from test results), and t_{SLEEP} is the sleep time for the PWM IC ($\simeq$2 sec).

Note that, according to the 2N2222A data sheet, dc current gain can be 75 to 300. Therefore, to obtain a better prediction from the above equation, it is advisable to determine the dc gain through simple testing. To solve the equation, you must first determine $V_{C1}(0)$. This quantity depends on several factors. First, it depends on the PWM IC. The IC can discharge the soft-start capacitor either linearly (constant-current sink) or exponentially (RC discharge). Knowing this fact, you can work out the turn-on time, t_{ON}, of Q_3 and Q_2 by plugging t_{ON} and V_{CC} into the standard RC-charging equation with the time constant of $\tau_1=R_2C_1$. In **Figure 1a**, because $2.3\tau_1<t_{ON}<5\tau_1$, you can approximate $V_{C1}(0)$ by using $V_{C1}(0)=V_{IC1}-V_{BEQ4}-V_{CEQ2}-V_{D1}$.

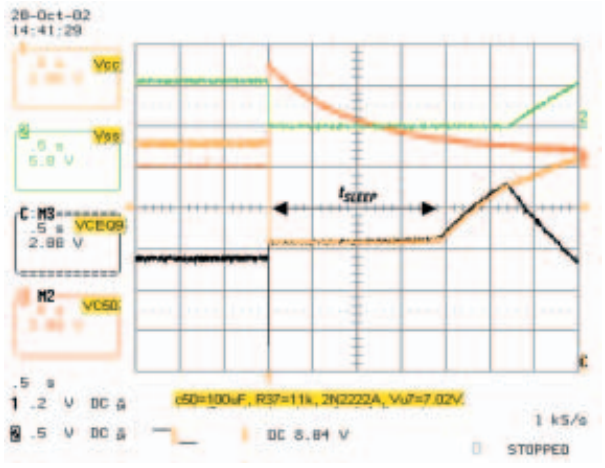

Figure 2 A scope display shows the relevant waveforms during hiccup operation. Trace 1 is the V_{CC} output voltage of the shunt regulator, Trace 2 is the soft-start voltage of the PWM controller, Trace C is the collector-emitter voltage of Q_3, and Trace B is the voltage across timing capacitor C_1.

After time period t_{SLEEP} elapses, C_1 should have discharged to a low enough voltage to turn off Q_1, thereby allowing V_{CC} to climb back to its normal value, thus enabling the PWM controller. The soft-start capacitor then charges up again. The output pulse gradually starts to generate after the soft-start voltage reaches the internal threshold. This "sleep-reboot-detect" cycle repeats until the fault disappears.□

Microcontroller provides SRAM battery backup

Dave Bordui, Cypress Semiconductor, Orlando, FL

To maintain content in the event of power loss, many designs that include SRAM require a dedicated device that can automatically switch from a standard power supply to battery operation. Microcontrollers seldom find use in power-switching applications. Because microcontrollers typically operate from the primary power supply, they stop execution if that supply drops, thereby making it impossible to perform the switching operation. However, by using a characteristic of many microcontrollers, you can perform this switching function without interruption to the SRAM (**Figure 1**). Many microcontrollers have internal protection diodes on their I/O pins. Therefore, if the V_{CC} pin is left floating, the CPU in many instances powers up and runs if you apply power only to an I/O pin. With this fact in mind, you can create an "automatic voltage switch" by connecting the main power-supply rail and a secondary battery backup to two separate I/O pins of the microcontroller. The microcontroller can then have firmware that drives a third I/O to a logic-high (source) mode or otherwise source current to an output pin. This output then provides the uninterrupted power to the external low- power SRAM device.

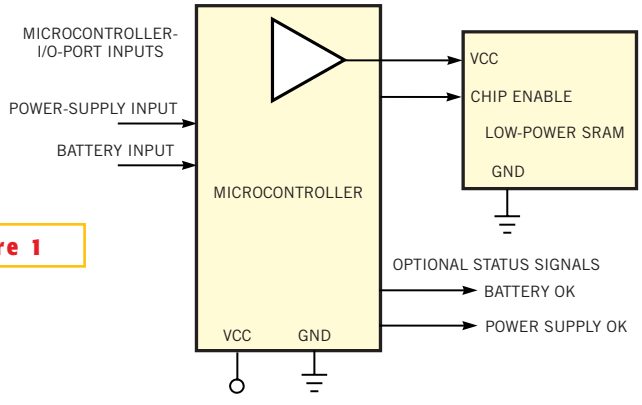

Figure 1 A microcontroller can power up and run even if its V_{CC} pin is floating.

When the V_{CC} rail is present, the mi-

crocontroller draws current from the V_{CC} pin and operates normally. If the V_{CC} rail drops below the battery-input voltage, the microcontroller automatically draws current from the battery instead. Although this scenario requires no firmware whatsoever, many microcontrollers can run firmware and continue execution throughout this power-supply transition. Continuing the microcontroller's firmware execution allows other firmware-based functions, such as deassertion of SRAM chip enable, battery- and rail-health indication, and analog-to-digital conversion. When you use this technique, you must take care to ensure that the entire design draws less current than the forward-bias-current rating of the protection diode. Also, the external SRAM circuit must draw no more current than the microcontroller's output can source. This stipulation remains true whether the V_{CC} rail or the battery provides power. It is also important to realize that, because the protection diodes are sourcing the power, a slight voltage drop exists on the microcontroller's uninterrupted-power-supply output. This voltage drop is equivalent to the one that the microcontroller's manufacturer specifies. You should consider this drop when you select the battery, V_{CC} rail, and external-SRAM voltage requirements.□

Positive regulator makes dual negative-output converter

Keith Szolusha, Linear Technology Corp, Milpitas, CA

Some systems, such as optical networks, require more than one negative voltage. A common procedure is to boost the main negative supply of −5V to −10V and then reduce it with a linear regulator to −9V. The −5V itself comes from a positive supply, typically 5 or 12V. Independently creating each of the two negative voltages requires the use of two switching-regulator ICs. However, a simpler approach uses only one step-down switching regulator and creates both a negative output with low ripple current and a second output with twice the voltage. The circuit in **Figure 1** is a positive-to-dual-negative dc/dc converter that converts 5V to both −5V and −10V, using a positive buck regulator. This configuration is not a usual application circuit of a positive buck-regulator IC, which you would typically find in single-output step-down applications. However, by rearranging the connections to ground and V_{OUT}, the dc/dc converter becomes a common positive-to-negative converter.

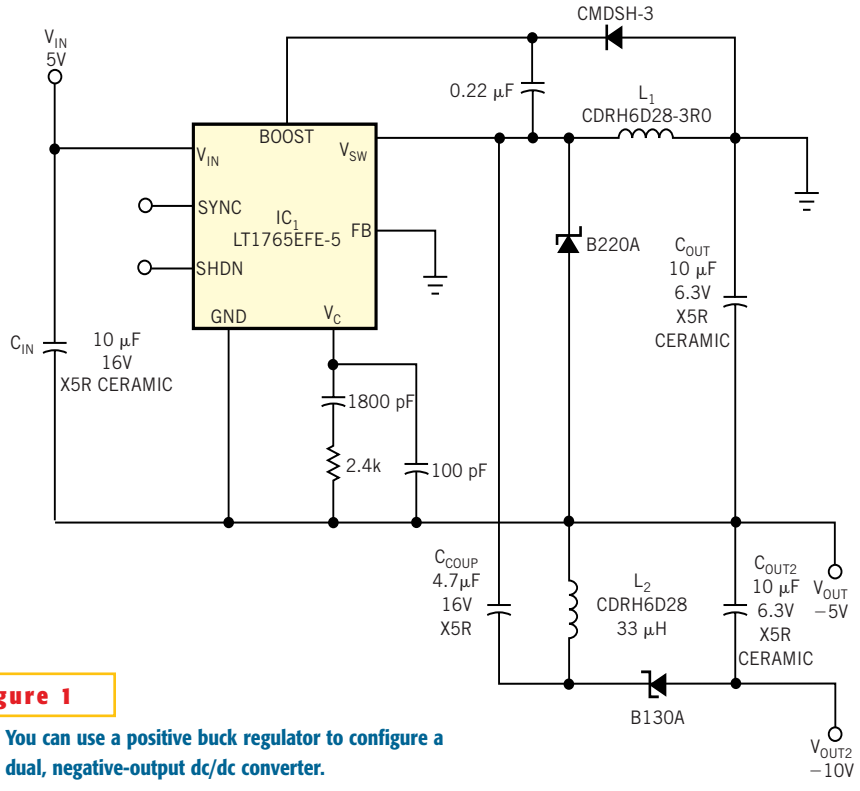

Figure 1

You can use a positive buck regulator to configure a dual, negative-output dc/dc converter.

The circuit features an additional negative-output stage with twice the voltage of the first output by using a second inductor, a catch diode, and an output capacitor. The circuit includes a coupling capacitor, C_{COUP}, for energy transfer to the second winding and offers regulation of the secondary output without feedback. The use of two inductors, as opposed to one transformer, can provide a flexible circuit layout. This circuit measures less than 3 mm high and delivers high load current (**Figure 2**). You can replace the two inductors with a single 1-to-1 transformer, but even at the high 1.25-MHz switching frequencies, it may be difficult to find a less-than-5-mm-high transformer that can do the job. The LT1765 buck regulator provides high current capabilities even with small inductors and all-ceramic coupling, input, and output capacitors, thanks to both its 1.25-MHz switching frequency and its 3A on-board power switch.

Figure 2 shows the output capability for the circuit in **Figure 1**. The load current on one output determines the maximum available load current on the other. At maximum output current, the peak

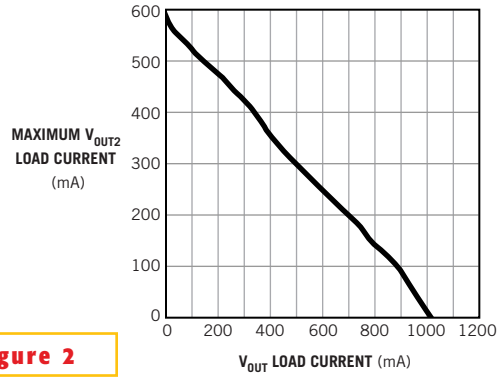

Figure 2

The circuit delivers high maximum currents available from the two outputs in the circuit of Figure 1.

switch current (the sum of the peak inductor currents) is equal to 3A. Forcing the output current higher than the maximum value can cause the output voltage on both lines to collapse and lose regulation. The single feedback signal directly monitors V_{OUT}, but the low-impedance ceramic coupling capacitor with an extremely high rms current rating keeps V_{OUT2} well-regulated. As load conditions change on both V_{OUT} and V_{OUT2}, V_{OUT2}'s regulation becomes slightly compromised over different load conditions. V_{OUT2} can become unregulated if the load current on V_{OUT2} becomes extremely small. A preload of 5 mA on V_{OUT2} is necessary to maintain regulation if the load current falls below 5 mA. Zero load current on V_{OUT} does not cause the converter to lose regulation. Cross-regulation typically stays within 1% of the typical output voltage, an excellent rating for a single-feedback, dual-output converter. **Figure 3** shows typical efficiency curves for various values of the load current on V_{OUT2}.□

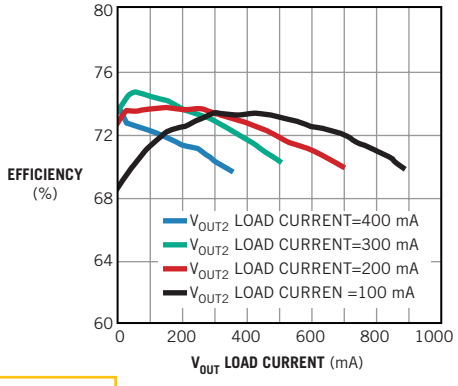

Figure 3

The circuit in Figure 1 has high conversion efficiency for various values of load current.

Analog switch frees stuck I²C bus

Bob Marshall, Philips Semiconductor, Morgan Hill, CA

THE DUAL-CHANNEL PCA9540 I²C multiplexer often breaks up an I²C or SM bus or allows you to use devices with the same addresses on the same bus. When the PCA9540 initially powers up, it comes up in a state in which both channels are deselected. The I²C- or SM-bus master can then address the control register in the PCA9540 to select either Channel 0 or Channel 1, connecting the master to the appropriate channel. The I²C bus can then address downstream devices on the selected channel. If a failure occurs in one of the downstream channels, such that the I²C bus is stuck at high or low, the I²C-bus master could become disabled. Because the PCA9540 has a power-on-reset function that initializes the multiplexer with all channels disconnected, this feature can free the bus. In some applications, however, powering down the entire system may be impractical. One way to avoid powering down the entire system is to install a low-on-resistance analog switch in series with the power-supply line of the multiplexer (**Figure 1**).

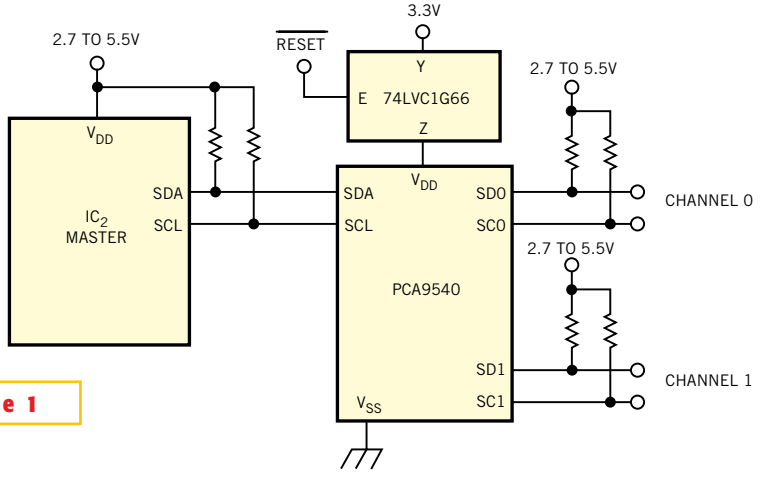

Figure 1

To free up a stuck I²C bus, this circuit controls the supply voltage to force a hardware reset.

When the enable pin of the 74LVC1G66 goes low, the supply voltage disconnects from the multiplexer, thereby freeing up the I²C bus. The I²C master or any other system controller can generate this hardware reset. The 74LVC1G66 is available in a 2-mm² package, so the circuit takes up little additional board space. This example uses the PCA9540, but you can use the 74LVC1G66, with a typical on-resistance of approximately 6Ω, to selectively control the power for any device that has a power-on-reset function. Its size and wide operating-voltage range also make it practical to selectively power down sections of any circuit in power-sensitive applications.□