design ideas

Edited by Bill Travis

DDS device produces sawtooth waveform

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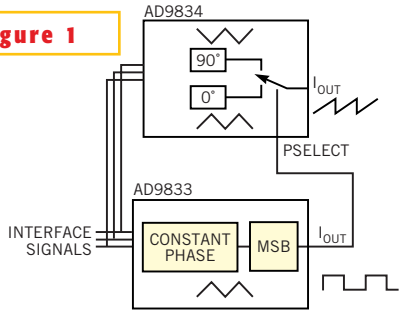
Ramp or sawtooth waveforms are useful for a broad range of applications, including automatic-test equipment, benchtest equipment, and actuator control. Discrete components typically set the waveform frequency. Unfortunately, drift in these component values over time and temperature limits the accuracy of the output frequency. Also, changing the frequency requires that you use a different set of components. This Design Idea describes a flexible implementation of a sawtooth waveform generator (**Figure 1**) using two DDS (direct-digital-synthesis) devices. The frequency of the sawtooth is digitally programmable, so the design requires no external components to set the frequency. A DDS device, a programmable waveform generator, can deliver sine, square, and triangular (up/down ramp) waveforms. You can digitally implement changes in phase or frequency by loading onboard registers. Using the phase registers, the DDS chip can generate two linear up/down ramps of the same frequency but with a 90° offset. The up ramp of one occurs at the same time as the down ramp of the other. Selecting a phase register causes the signal from that register to go to the output. A sawtooth waveform occurs when the only the "up ramp" of each signal is directed to the output. The AD9833 delivers the MSB of the phase register, thus producing a digital signal at the frequency of the up/down ramp. This signal connects to the PSELECT pin on the AD9834, which controls switching between the phase registers.

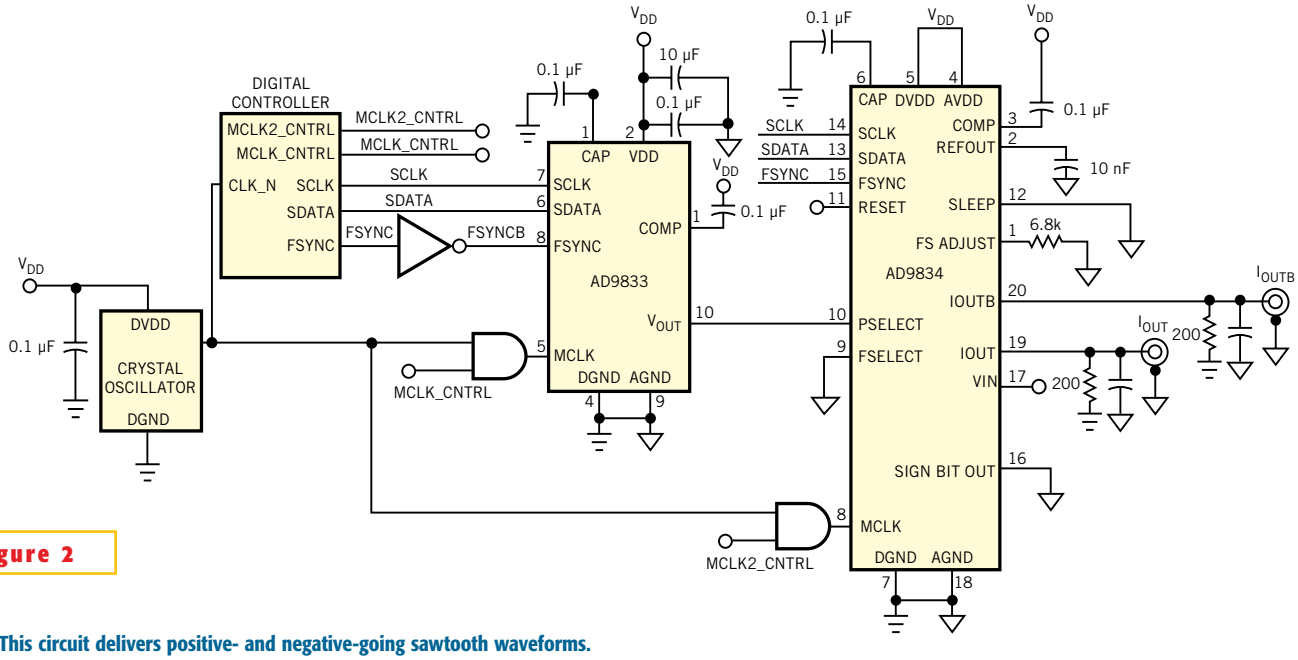
Latency in the devices means that you see the effect of switching between the phase registers on the output only after

Figure 1



Two DDS chips provide a convenient way to generate sawtooth waveforms.

Figure 2



This circuit delivers positive- and negative-going sawtooth waveforms.

seven MCLK (master clock) cycles. Controlling the MCLK signals of both devices so that one MCLK is inactive for a number of clock cycles can overcome this inherent latency. **Figure 2** illustrates how the two devices connect. The connections to the interfaces of the two devices combine so that they can accept programs from the same digital controller. The AD9833 is connected such that FSYNC is active high; the AD9834 is connected such that FSYNC is active low. In this way, the controller has to control only three signals instead of six. The AD9834 is configured so that the frequency and phase are controlled via the pins. This configuration allows the digital output from the AD9833 to control phase-register selection by simply connecting it to the PSELECT line. Two analog outputs from the AD9834, IOUT and IOUTB, deliver complementary sawtooth waveforms (**Figure 3**).

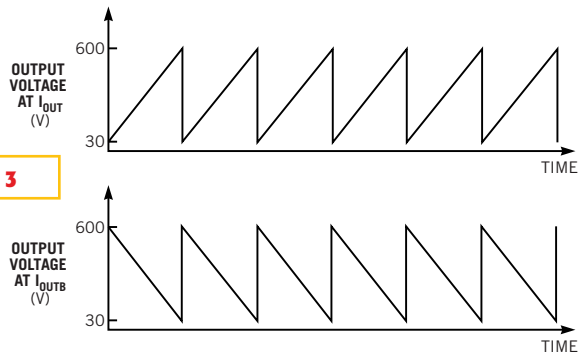


Figure 3

The up ramp of the upper waveforms occurs at the same time as the down ramp of the bottom waveform.

A RESET (Pin 11) signal initializes the devices. This initialization can occur in the same way for both devices, using the control register. This operation requires a control word with the RESET bit set to 1. The frequency and phase registers of both devices are then ready to load with data. Because of the switching involved in creating the sawtooth waveform, its frequency is twice that of an equivalent triangular waveform:

$$f_{SAWTOOTH} = \frac{F_{WORD}}{2^{27}} \times f_{MCLK},$$

where F_{WORD} is the frequency word loaded in both devices.

The AD9834 phase switches between 0 and $\pi/2$. Following instructions in the IC's data sheet, you should therefore load Phase Register 0 with 0 and Phase Register 1 with 0x800 (which corresponds to a 90° phase shift). The AD9833's phase is always set to $\pi/2$, so you should therefore load Phase Register 0 with 0x800. Once the MCLK of the AD9833 begins to run and after seven MCLKs of latency, the output of the AD9833 changes because of the $\pi/2$ phase shift in Phase Register 0. You can deactivate RESET through the control register once the registers are loaded with data. In the same control word to the AD9834, you should set the MODE bit to 1, which results in the selection of the triangular waveform as the output waveform, and you should set PIN-SW to 1, so that the pin controls phase-register-select function. And, for the AD9833, you should set the OPBITEN bit to 1 to enable the digital output. You should set the DIV2 bit to 1 so that the digital output is not divided by 2, and set the SLEEP12 bit to 1 because the DAC is not being used. For the system to implement the sawtooth, there must be an offset between the times when the MCLKs of both devices begin to run. You calculate the offset as follows:

$$\text{OFFSET} = \left[\text{ROUND}\left[\left[\frac{2^{28}}{F_{WORD}}\right] \div 4\right] - 7\right].$$

If, for example, Offset=10, then the MCLK of the AD9834 should run for 10 cycles before the MCLK of the AD9833 starts running. From then on, the ICs should be synchronous. A negative value of Offset indicates that the MCLK of the AD9833 should start running first.

This Design Idea provides a flexible method for generating a sawtooth waveform. The frequency is digitally programmable, and the design requires no external components to change the frequency. The frequency does not change with component drift over time or temperature.□

Circuit makes universal VCSEL driver

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VCSELs (vertical-cavity surface-emitting lasers) are commercially available infrared semiconductor lasers with $\lambda \simeq 850$ nm. Short-cavity-length, high-quality Bragg mirrors impart properties to VCSELs that differ from those that earlier Fabrey-Perot lasers impart. The emission characteristics—optical power, P_λ, versus diode current—shows threshold and operating currents of approximately 3 and 13 mA, respectively, for the Lasermate TSC-M85A416 VCSEL. Such values are typical for this type of laser (**Figure 1**). The current characteristics are nearly independent of temperature. Thanks to their low operating current, effective coupling to multimode fibers, high-speed switching, and low price—about one-third that of a Fabrey-Perot laser—VCSELs may replace LED light sources in short fiber-optic links. The MC10EP89 ECL coaxial VCSEL driver allows the circuit to switch current with less-than-1-nsec rise and fall times (**Figure 2**). The IC delivers a voltage swing of

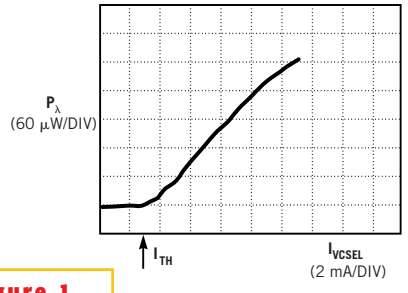

Figure 1

A VCSEL has threshold and operating currents of approximately 3 and 13 mA, respectively.

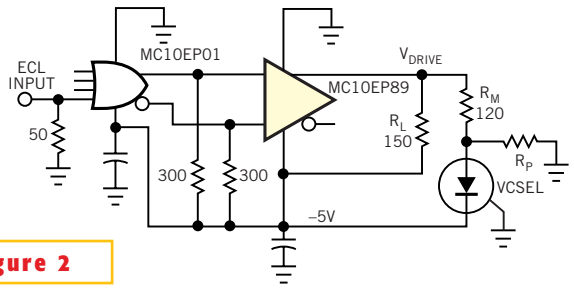

Figure 2

This universal VCSEL driver allows you optimize the circuit for any type of laser diode.

1.6V minimum to a 75Ω load (**Figure 3**).

The 120Ω resistor, R_M, limits the amplitude of the pulse current, and R_P determines the initial polarization current of the laser. For $R_P=\infty$, the laser practically switches off during the low state of the driver. You must load the MC10EP89 with resistor R_L for proper operation of the IC. You can optimize the values of R_M and R_P for each type and characteristic (individual emission parameters) of the VCSEL you select. Because of the dynamic resistance of the laser, the voltage drop across the junction varies from approximately 1.9 to 2.2V within the full current range. Therefore, you should consider this variation when you calculate R_M and R_P. In turning off the optical power of the VCSEL, you observe some residual emission (tail) in the optical-pulse response (**Figure 4**). If the current falls to zero ($R_P=\infty$), the tail is shorter and smaller, but the optical-power amplitude also decreases.

The oscillogram represents the response of a 155-Mbps laser (**Figure 4**). VCSELs for 622 and 1250 Mbps are also available from Lasermate. The MC10EP89 needs symmetrical drive; the input OR/NOR gate works as an asymmetrical/symmetrical ECL converter. The laser's good thermal properties eliminate the need to provide a complicated stabilization loop for the optical power. The entire circuit is dc-coupled and operates with constant optical power amplitude for each binary code, and the circuit is insensitive to bit patterns. A slow-start circuit is unnecessary. Because of the operating speed, you must carefully design the pc board according to high-frequency rules: Keep connections as short as possible, use surface-mount components, and carefully perform decoupling, for example. You must ground the metal case of the laser and isolate it from the chip.□

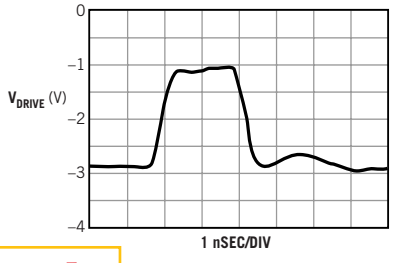

Figure 3

The driver in Figure 1 switches 1.6V into 75Ω with less-than-1-nsec rise and fall times.

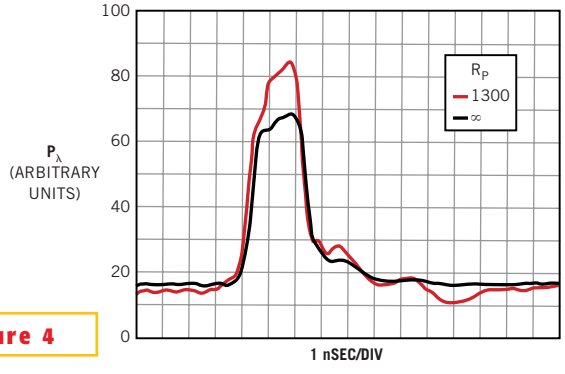

Figure 4

These curves show the VCSEL's response with R_P open and R_P=1300Ω.

Circuit level-shifts ac signals

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AC SIGNALS CAN EMANATE from many sources, and many of these sources are incompatible with the most popular interface voltages, such as TTL. A temptation always exists to capacitively couple the ac signals because capacitive coupling strips off the dc level. Capacitive coupling sometimes doesn't work, because the coupled signal's voltage swings around ground, so you have to add dc offset to make the coupled signal compatible with the interface voltage. Also, the coupled signal contains a dc content, V_{DC}, which varies with pulse width, and the dc variation interferes with the interface voltage when the signal swing is large. This circuit completes the signal interface by measuring the dc offset, adding appropriate compensation to the capacitively coupled signal and adding an adjustable-dc- level feature (**Figure 1**). R_1 and C_2 form a lowpass filter (f_{3dB}=0.312 Hz) that measures the dc content of the input signal. The transfer equation is the following:

$$V_A=\left[\frac{V_{IN}R_3+V_{REF}(R_1+R_2)}{(R_2+R_3)(R_1C_2s+1)+R_1}\right]\bullet\left[\frac{R_F+R_G}{R_G}\right].$$

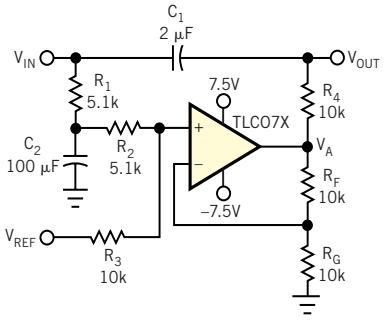

Figure 1

This circuit is a universal level shifter for ac signals; it accommodates any interface standard.

When $R_1+R_2=R_3$ and $R_F=R_G$, V_{DC} transfers to the output signal, V_A, because it is multiplied by 1/2(2)=1 or a gain of one. The output voltage for the same resistor values contains V_{REF}; thus, the output signal is level-shifted by the voltage, V_{REF}, not V_{REF} plus the V_{DC}. When the input signal's duty cycle changes, rather than the output voltage's changing with duty cycle, the op amp keeps the output-voltage level constant. The gain for the V_{DC} must be one, so that it cancels the voltage shift after ac-coupling. The gain for the reference voltage can be greater than one; for example if $R_1+R_2=3R_3$ and $R_F=3R_G$, the dc content is 1/4(4)=1, and the reference-voltage gain is 3/4(4)=3. V_{REF} can be positive or negative, so you can obtain TTL, CMOS, or ECL logic levels with this circuit. The time constant formed by C_1 and R_4 must be large enough to pass the lowest frequency signal without distortion. The value of R_4 is not critical, as long as the op amp can drive R_4 without losing too much signal swing. In some cases, you can size R_4 to present the driving-point impedance you need to eliminate near-end reflections. The circuit easily couples 400-MHz data as configured, but the data rate depends on the time constant formed by R_4 and the input impedance of the driven circuit.□

Interface a serial 12-bit ADC to a PC

DS Oberoi and Harinder Dhingra, GCET, Jammu, India

Over the years, IC manufacturers have devised various ways of effecting interfaces and paying special attention to reducing the number of ICs' interface-I/O pins. The MAX187 is one such device, a 12-bit A/D converter. You can create an interface to this ADC using serial data-communications techniques. Analog-to-digital conversion and data transfer from MAX-187 require only three digital-I/O lines. You can create a simple interface between the MAX187 and a PC using the computer's Centronics printer port (**Figure 1**). You enable or disable the MAX187 by setting the $\overline{SHDN}$ pin (Pin 3) to high or low level, respectively. If you leave this pin open, then the internal reference (4.096V) becomes disabled, and you must apply an external voltage reference to REF (Pin 4). Otherwise, this pin connects to a 4.7-µF bypass capacitor, C_1. The digital data from the MAX187 transfers to the processing unit one bit at a time by using an external clock at SCLK (Pin 8).

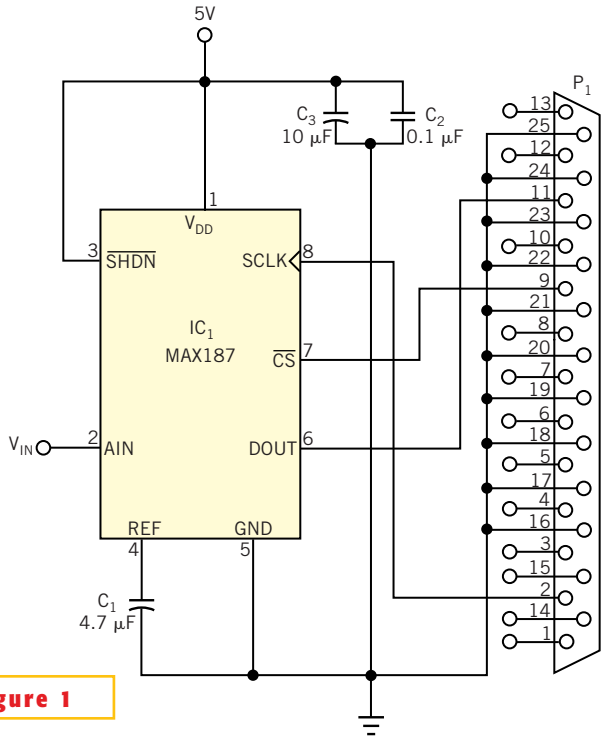

Figure 1 It's easy to effect an interface of a 12-bit serial ADC to a PC.

A complete data transfer requires 13 external clock pulses. The first clock pulse's falling edge latches the first data bit (the MSB) at the DOUT pin (Pin 6). The output data bit changes at the falling edge of the next external clock, and you can read the serial data bits until the appearance of the falling edge of the next clock cycles. The analog-to-digital conversion starts when the ADC's $\overline{CS}$ pin (Pin 7) goes low. This pin must remain in the low state until the complete cycle of conversion and subsequent serial-data transfer has taken place. A change of state in the DOUT pin from low to high level indicates the EOC (end-of-conversion) status. Then, serial 12-bit data is available for transfer. Software controls the MAX187's operation. The software should be able to generate all the control signals for successful conversion and also should be able to detect the EOC status. It should also be able to generate 13 external clock pulses to read serial 12-bit data and convert it into parallel data.

The software for the MAX-187's operation is in Turbo C++, Version 3.0 (which you can download from the Web version of this Design Idea at www.edn.com). In the code, Port defines the Centronics port of the PC to which the MAX187 interfaces. Write Port defines the port for initiating the analog-to-digital conversion and generating the external clock pulses. Read Port defines the port for reading the EOC and serial data from the ADC. After pulling CS and SCLK low, the EOC loop checks for the EOC status. If a valid EOC does not appear, this loop remains operational. As soon as a valid EOC appears, the first of the 13 clock cycles appears, which latches the first data bit (MSB). After this action, the routine calls a subroutine (get_adc()). The subroutine generates the rest of the external clock cycles to read the 12 bits of serial data. The function also converts the received serial data into parallel data (adc_val). It converts by multiplying the previous data by two by shifting adc val to the left by one bit and adding one to the parallel data if the serial bit's value is one. Once the parallel data is available, the function returns the value and displays it on the screen.□

Safety device uses GMR sensor

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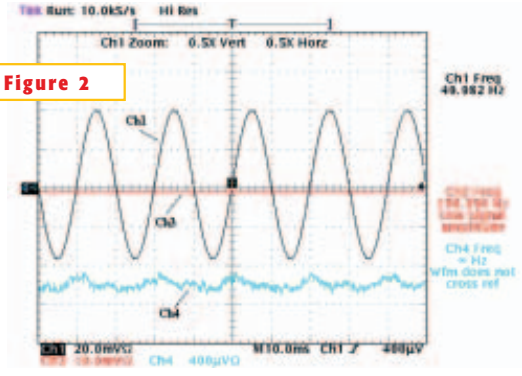
THIS DESIGN IDEA presents a differential safety device to prevent risks arising from current leakages in household applications. The proposed circuit uses a new method for differential current sensing (**Figure 1**). The method entails the use of Helmholtz coils and a magnetic sensor based on the GMR (giant-magnetoresistive) effect. The AC004-01 magnetic sensor from NVE (www.nve.com) uses GMR technology (**Reference 1**). Two Helmholtz coils carry the household's input current. If no differential current between phase and ground exists at the center of the coils, then the magnetic field is uniform and null. But, in the presence of an unbalanced magnetic field, corresponding to a leakage current to ground, a differential magnetic field appears at the center of the Helmholtz coils (**Reference 2**). Thus, the sensor's output is a nonzero voltage that the circuit in **Figure 1** amplifies and compares with a preset reference voltage. The reference voltage corresponds to the highest allowable leakage current—generally, approximately 30 mA.

The sensor's output, a differential voltage, connects via a highpass filter to an INA118 instrumentation amplifier, a device with high common-mode rejection (**Reference 3**). This stage converts the sensor's differential signal from a Wheatstone-bridge arrangement to a unipolar output with an appropriate gain figure. This output goes through a half-wave rectifier and a lowpass filter and becomes a dc signal. If this signal is greater than V_{REF1}, then the MOC3041 optotriac turns off, thereby interrupting the power to the household appliance.

Figure 2



The sensor's output (Channel 4) is zero because the differential line current is zero.

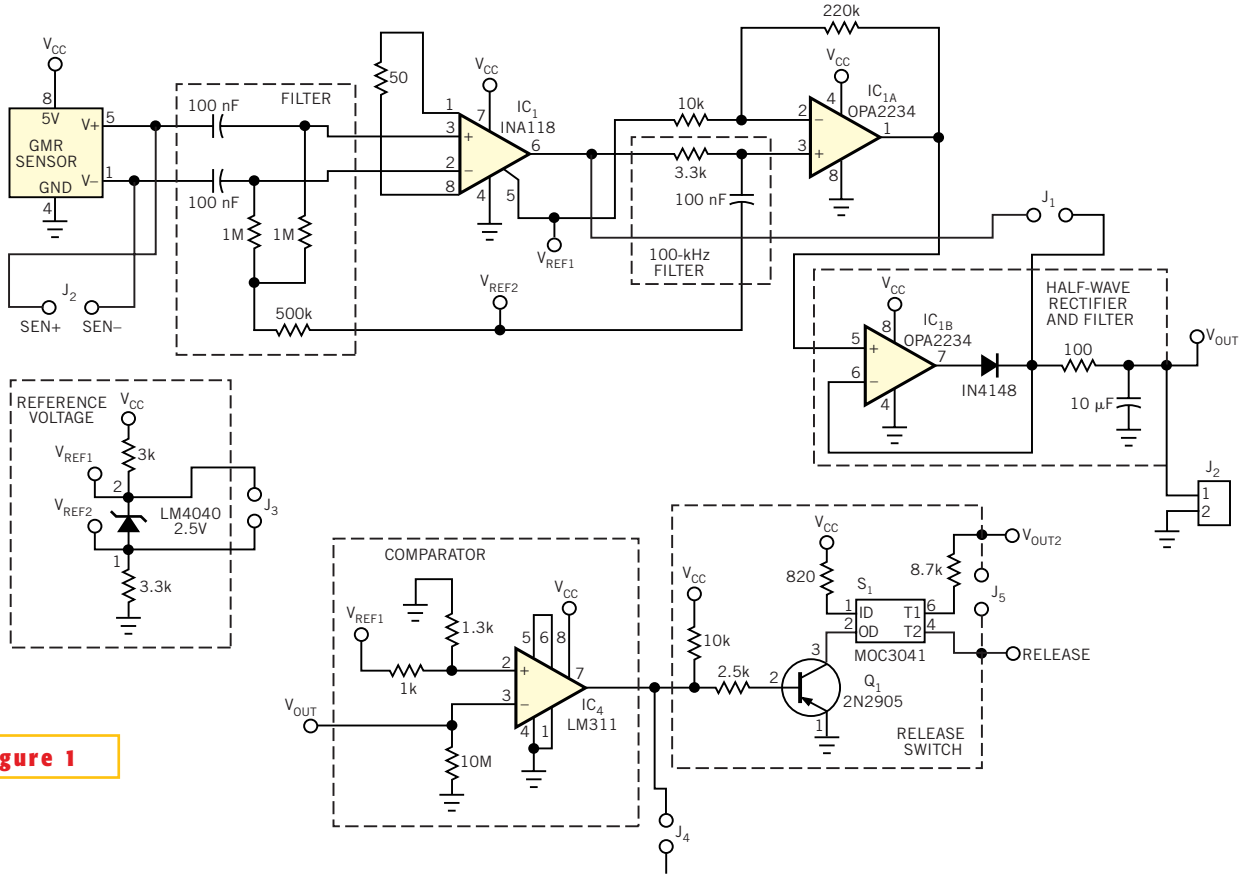
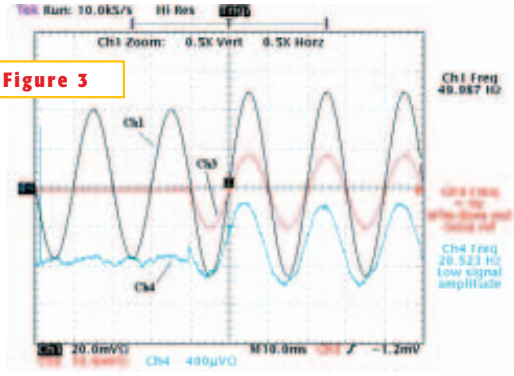


Figure 1

This circuit uses a GMR sensor to detect and disable dangerous differential line currents.

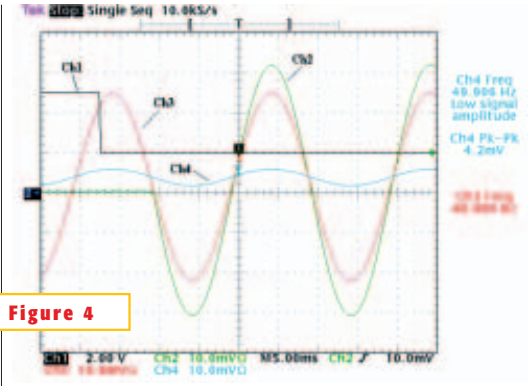
Figures 2 and **3** depict two scenarios. The Channel 1 trace represents the line current; Channel 2 shows the current circulating through the line; and Channel 4 represents the sensor's output, which is proportional to the difference between line and ground currents. In **Figure 2**, the sensor's output is zero because the current difference is null. **Figure 3** shows a ground current that generates a nonzero magnetic field in the sensor. In **Figure 4**, the ground current is greater than 30 mA. The comparator changes state, activating the optotriac (Channel 1) and turning on the relay (Channel 2, 20 mA/division). Channel 3 shows the live current, and Channel 4 shows the sensor's output (1 mV/division).□

Figure 3



A ground current generates a nonzero magnetic field in the sensor (Channel 4).

Figure 4



The ground current exceeds 30 mA. An optotriac and a relay disconnect power to the household appliance.

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