design ideas

Edited by Bill Travis

Dual comparator thermally protects lithium-ion battery

Mike Hess, Maxim Integrated Products, Sunnyvale, CA

Most manufacturers recommend that you don't change lithium-ion batteries at temperatures lower than 0°C or higher than 50°C. You can monitor both thresholds by adding a thermistor and dual (window) comparator to a lithium-ion battery charger (**Figure 1**). Set the low-temperature trip point at 2.5°C and the high-temperature trip point at 47.5°C. A precision voltage reference is unnecessary, because the comparator's resistor network is ratiometric, so variations on the supply voltage, V_{BUS}, do not affect the trip thresholds. By driving the charger's enable input, EN, the comparators' open-drain outputs ensure that charging is inhibited when the battery temperature is out of range. As an alternative, you can substitute a dual comparator with push-pull CMOS outputs, such as the MAX9032, if you also add a tiny, SOT-323 dual diode (the dashed lines in **Figure 1**). The dual comparator and the MAX9032 are available in SOT-23 packages, and both offer built-in hysteresis of 2 or 4 mV, respectively.

IC_2 is a single-cell lithium-ion battery charger that can derive its power directly from a USB port or from an external supply as high as 6.5V. The 0.5% accuracy of its battery-regulation voltage allows maximum usage of the battery's capacity. The charger's internal FET delivers as much as 500 mA of charging current, and you can configure its SELV input for charging a 4.1 or 4.2V battery. The SELI input sets the charge current to either 100 or 500 mA, and an open-drain output, CHG, indicates the charge status. For near-dead batteries, a preconditioning capability soft-starts the cell before charging. Other safety features include continuous monitoring of voltage and current and initial checking for fault conditions before charging.□

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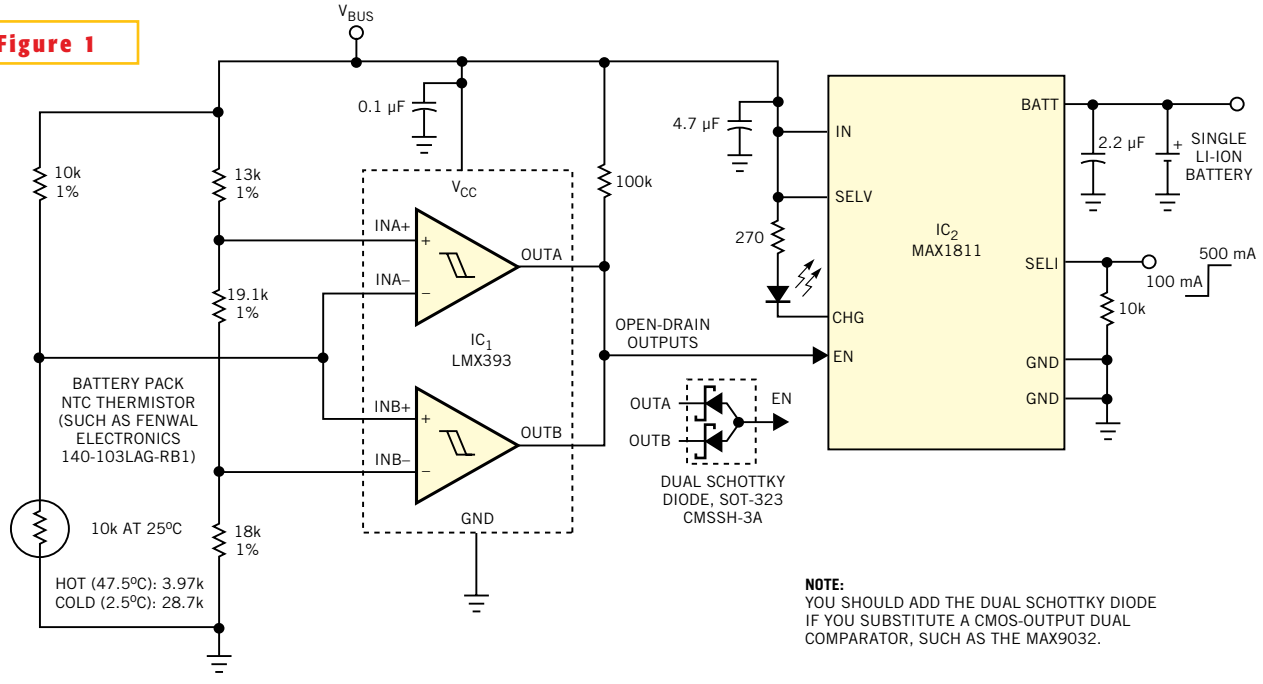
Figure 1



While charging a lithium battery from a USB port, this circuit provides thermal protection for the battery.

Lowpass filter discriminates step input from noise

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Numerous applications exist in industry, particularly with control systems, in which it is desirable to remove all but the lowest frequency components from a signal to effectively yield a dc voltage. This voltage may, for example, serve as a setpoint to a PID controller in a process-control or an HVAC application, in which the cable that is carrying the analog signal is exposed to a wide spectrum of noise, including low-frequency noise components from various sources. These sources could include variable-speed drives, ballasts, transients from switching gear, and motors. In many cases, noise reduction using a conventional lowpass filter can create adverse effects in the response time of the system, even if you use a multipole filter. As an alternative, the circuit of **Figure 1** is ideally suited to provide extensive noise reduction for applications such as these without impairing a system's ability to track rapid changes in signal level. The concept involves a lowpass filter with a slewing mechanism that has significant performance advantages over other nonlinear-lowpass-circuit topologies, given its ability to discriminate step changes in signals from noise.

The basic operation of the circuit is to momentarily increase the corner frequency of the lowpass filter formed by R_6 and C_3, using an analog switch, IC_1, upon detection of a step change in signal, allowing V_{OUT} to track V_{IN} with little delay. IC_1 has an on-resistance of about 100Ω, so when it closes across R_6, the corner frequency of the circuit changes from 0.016 Hz to approximately 160 Hz, which is ample bandwidth for the target applications for this circuit. IC_{2B}, along with R_4, R_5, and C_2, operates as an error amplifier with a corner frequency of $f_{CERR}=1/2\pi R_5C_2=1.59$ Hz. The amplifier generates an error signal, V_{ERR}, that IC_{2A} measures in reference to V_{OUT}. IC_{2A} acts as a floating window comparator that places the lowpass filter into slew mode when V_{ERR} exceeds the predetermined threshold that zener diode D_3 establishes. For values of V_{ERR} that are greater than V_{OUT}, diode D_2 conducts, causing the noninverting input of IC_{2A} to track this signal. IC_{2A} compares the signal to a threshold voltage of approximately $V_{OUT}+5.2$V at its inverting input. When a negative-step change ($V_{IN}<V_{OUT}$) to the input, V_{IN}, is of sufficient amplitude such that V_{ERR} becomes approximately 5.7V (accounting for the barrier potential of D_2), IC_{2A}'s output switches high. This action activates IC_1, causing a short circuit across R_6, thus allowing V_{OUT} to track V_{IN}.

For values of V_{ERR} below V_{OUT}, the action is similar, except that the inverting input of IC_{2A} tracks V_{ERR} through D_3 and D_4, and the comparator's output toggles high at the point at which V_{ERR} is approximately 5.2V below V_{OUT}. Although the asymmetry in the window comparator's performance is not of great significance, you could realize improved symmetry by replacing D_2 with a Schottky diode, which has a lower barrier potential. The comparator's trip points, along with the dc gain of the error-amplifier stage (IC_{2B})—determined by the ratio R_5/R_4—establish the upper and lower deadband of **Figure 1**. With the values shown in **Figure 1** the circuit triggers to slew in response to negative-step changes in V_{IN} as small as 0.260V and positive-step changes that are as small as 0.285V. You can realize better sensitivity by reducing the zener voltage of D_3 or by increasing the ratio R_5/R_4 and ensuring that the error-amplifier stage provides adequate roll-off. The roll-off must ensure that noise levels that may ex-

(continued on pg 96)

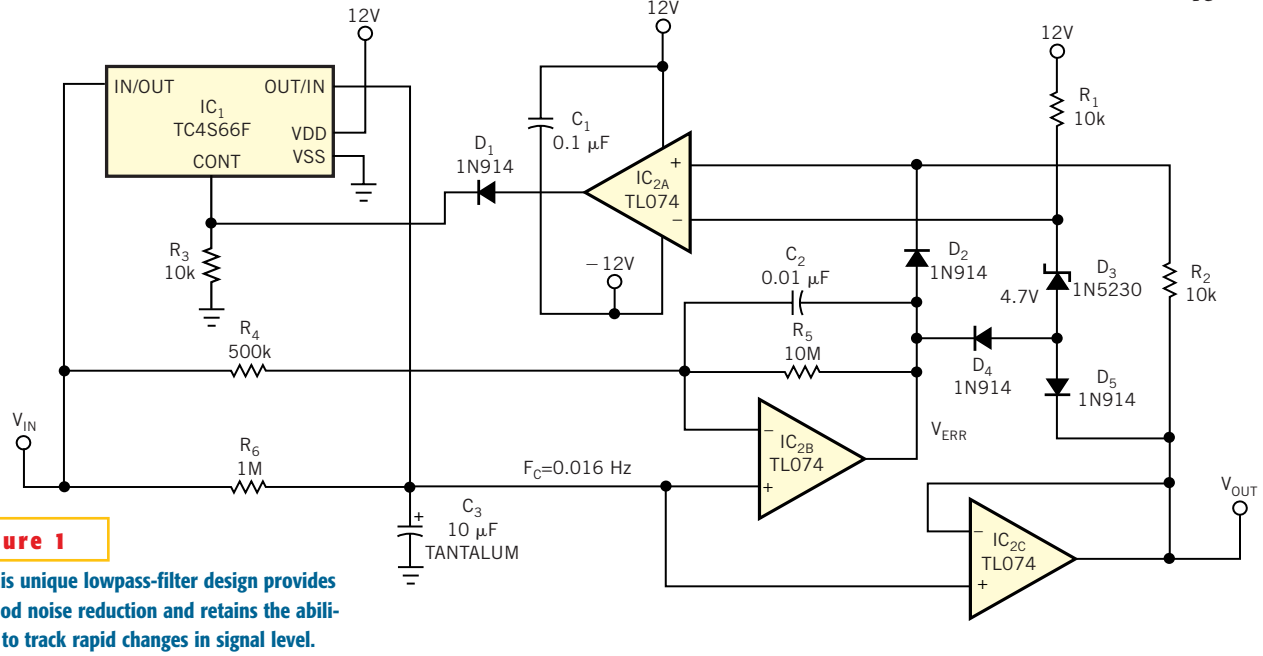


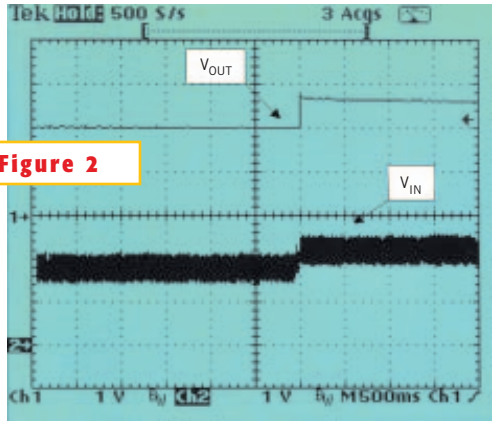
Figure 1

This unique lowpass-filter design provides good noise reduction and retains the ability to track rapid changes in signal level.

ist in a given application cannot trigger the circuit into slew mode.

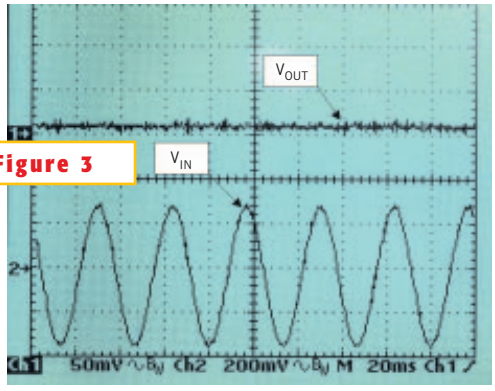
Another important parameter to consider when choosing component values for the error- amplifier stage is the step response of that circuit, because it directly impacts the overall settling time of the lowpass filter when it encounters step changes in signal. To be conservative, choose values for R_5 and C_2 such that three times the RC time constant they form is well within the settling time desired for the lowpass filter. For example, with $R_5=10\ M\Omega$ and $C_2=0.01\ \mu F$, $3\tau=0.3$ sec. This case represents the approximate worst-case delay to the response to a step change in V_{IN} that is outside the deadband of the circuit. In practice, however, the delay is much smaller for step changes in V_{IN} that are larger in magnitude, given the first-order nature of this circuit. **Figure 2** illustrates the response of the lowpass-filter design to a 600-mV step change in V_{IN}. The graphic also illustrates the circuit's significant filtering capabilities on a severe, 30-Hz, 640-mV p-p noise component superimposed on the signal. An ac-coupled view of the filter's performance at steady state illustrates more than 65 dB of attenuation at 30 Hz (**Figure 3**).□

Figure 2



The circuit in Figure 1 has good step response, even with a nasty 640-mV p-p, 30-Hz noise term superimposed on the input.

Figure 3



This ac-coupled view illustrates more than 65 dB of attenuation at 30 Hz.

Voltage-to-current converter makes a flexible current reference

Art Kay, Texas Instruments, Tucson, AZ

The voltage-to-current converter in **Figure 1** can both source and sink current. The circuit is more flexible than some traditional current references that require different topologies for current sourcing and sinking. Also, you can easily adjust the value of the current reference by simply adjusting the circuit's input voltage. Performing a simple nodal analysis generates the following equation:

$$I_{OUT}=\frac{-R_2V_{IN}}{R_1R_3A_{IC2}}.$$

You typically set R_1 equal to R_2. The output current is a function of R_3 and the gain of the instrumentation amplifier. Note that capacitor C_1 stabilizes the circuit. In this example, $R_3=10\ M\Omega$, and the instrumentation amplifier's gain is unity. Varying the input, V_{IN}, by ±10V yields a current-output range of ±1 μA. Performing a more detailed nodal analysis on the circuit in **Figure 1** yields the following equation:

$$I_{OUT}=\left[\frac{-R_2V_{IN}}{R_1R_3A_{IC2}}\right]+$$
CURRENT TERM
$$\left[\frac{R_2V_{OS1}}{R_1R_3A_{IC2}}+\frac{R_1V_{OS2}}{R_1R_3}+\frac{R_1V_{OS1}}{R_1R_3A_{IC2}}+I_{B2}\right],$$
ERROR TERM

where V_{OS1} and V_{OS2} are the offset voltages of IC_1 and IC_2, respectively, I_{B2} is the input-bias current of IC_2, and A_{IC2} is the gain of IC_2.

This second equation is useful in understanding error sources and, consequently, can aid in selecting the components that are best suited to an application. For example, for a nanoampere current reference, you should consider the error that the instrumentation amplifier's bias current generates. The example in **Figure 1** uses the INA121P FET-input instrumentation amplifier to minimize the input-bias current. A milliampere reference, on the other hand, would focus more on the input offset voltage of the instrumentation amplifier. In general, you can neglect the error that the offset voltage of the op amp generates if you use a precision, low-offset amplifier. However, resistor-mismatch and instrumentation-amplifier gain errors are inevitable, regardless of the application.□

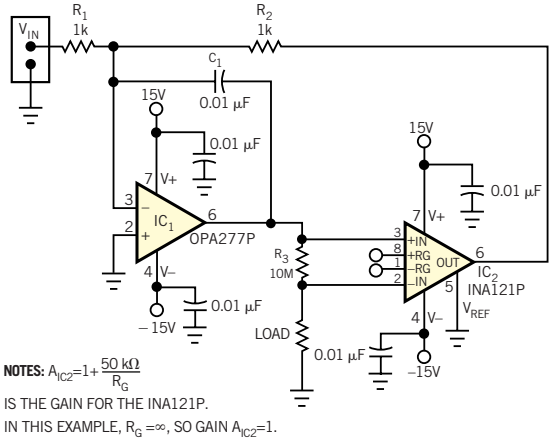


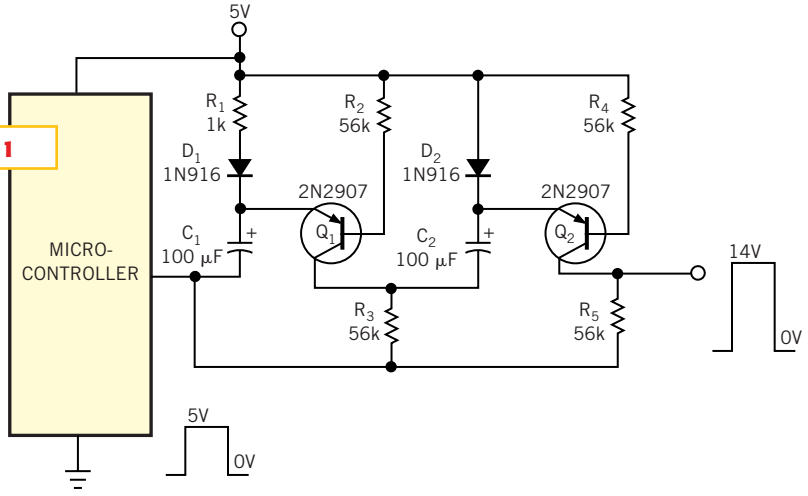
Figure 1 This current reference delivers an output that's a linear function of the input voltage.

Circuit forms single-pulse voltage multiplier

Richard Cappels, Mesa, AZ

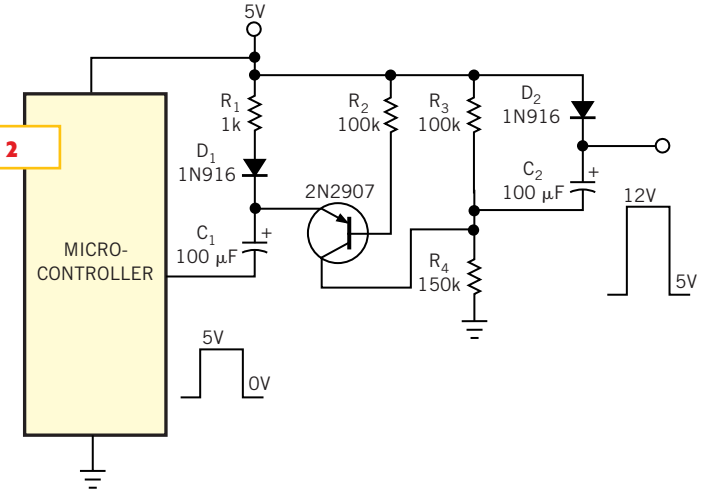
It is sometimes necessary for a microcontroller to generate a pulse whose voltage is higher than the power-supply voltage of the microcontroller. The circuit in **Figure 1** allows you to generate 14V pulses from a 5V power supply. An adaptation of the circuit provides a 5 to 12V programming pulse for programming the fuse bits in Atmel (www.atmel.com) microcontrollers (**Figure 2**). The approach is economical, in that it combines the voltage-multiplier and pulse-amplifier functions. Moreover, the technique benefits from the absence of noise that would arise from a continuously running switching power supply. In **Figure 1**, when the microcontroller's output is low, C_1 and C_2 charge in parallel to nearly 5V. When the microcontroller switches to 5V, it effectively makes the capacitors appear in series with the 5V pulse, resulting in a pulse approaching three times the power-supply voltage at the output. C_1 charges through D_1, and R_1 limits the charging current from the microcontroller's output to a few milliamperes. C_2 charges through D_2 and R_3.

Figure 1



This simple circuit provides single pulses of 14V from a 5V power supply.

Figure 2



This variation on the circuit of Figure 1 supplies fuse-programming pulses for Atmel ATV microcontrollers.

During the output pulse, C_1 must supply the base current for Q_1 and Q_2, as well as the load current. Because the voltage drop across the diodes decreases as current through them diminishes, after a charging time of several time constants, the diode drop is only a couple of hundred millivolts. Therefore, pulses of nearly three times the power-supply voltage are possible. When the pulses are continuous or when they occur within a couple of time constants of power application, diode drops of approximately 1.5V subtract from the output. Additional losses can arise from voltage drops across the resistance of the microcontroller and saturation losses in the transistors. You can reduce the saturation losses by reducing the values of R_2 and R_4, but be aware that reducing these values increases the droop rate of the output pulse. For some applications, you could omit D_1 and replace D_2 with a resistor, but the result would be longer charging and faster discharging for the capacitors. These trade-offs are acceptable for some applications.

The circuit in **Figure 2** provides a 5 to 12V programming pulse for Atmel ATV microcontrollers for the couple of hundred milliseconds the ICs require. Because the output during the time the microcontroller's output is low needs to be 5V, you omit the second transistor and take the output directly from the cathode of D_2. Because the output voltage needs to go to only 12V, C_2 charges from a voltage divider. C_2 charges to only 2V, which then appears in series with the 10V from the series combination of C_1 and the output of the microcontroller. You get no "free lunch" with this circuit. If the pulse initiation occurs before R_3 and R_4 sufficiently charge C_2 (60 kΩ×100 µF=6 sec), the voltage is lower than intended. You can reduce the charge time of the circuit by reducing the values of the capacitors. C_2 has the most effect because of the high-resistance charging path. However, reducing the capacitor values makes the output pulse droop more quickly.□

Feedback circuit eliminates CCD-driver delay mismatch

Mike Wong, Intersil-Elantec, Milpitas, CA

In a CCD (charge-coupled device), packets of charges shift across the array. The transistor array, also called a bucket-brigade shift register, receives drive from a dual-phase clock signal. Dual-phase clock signals comprise two synchronized clock signals that are 180° out of phase. High peak-output-current CCD drivers can buffer the logic-level clock signals and turn them into high-voltage and high-peak-current signals to drive the heavily capacitive gates of the many CCD transistors. Because of the speed mismatch of CCD-drivers' n- and p-channel FETs, the turn-on and -off delay times are poorly matched. **Figure 1** shows the outputs of one such current CCD driver, Intersil's EL7212 (www.elantec.com), with a dual-phase input clock. The overlap in the output stems from the turn-on and -off delay mismatches of the EL7212.

In a low-resolution system with a lower clock frequency, the delay mismatch is an insignificant part of the clock period. As CCD scan rate increases, the mismatch becomes a large part of the clock period. You need a new approach to correct the CCD-driver delay mismatch. **Figure 2** shows a circuit that uses amplifiers to sense the delay mismatch and correct it. Because $\overline{V_{OUT}}$ and V_{OUT} are 180° out of phase, if their turn-on and -off times coincide perfectly, the voltage between R_4, R_7, and C_2 is $1/2V_{CC}$. Amplifiers IC_{2A} and IC_{2B} compare voltage on C_2 with the $1/2V_{CC}$ reference voltage and adjust the voltage between R_3 and R_6. IC_{2A} provides the phase inversion, and IC_{2B} is the high-dc-gain error-correction amplifier. The output of the error amplifier drives R_3 and R_6, which shift the voltage offset of the incoming clock signal. When the offset-voltage level of the input clock signal shifts, the time at which the CCD driver is triggered also shifts. IC_{2A} and IC_{2B} guarantee that the proper offset voltage goes to the input clock signals so that the delay mismatch cancels. D_1 and D_2 rectify the input clock signals and create the supply voltage to the IC_{2A} and IC_{2B} amplifiers. When the input signals are removed, the power to the amplifiers shuts off, and the error-correction loop deactivates to prevent output oscillation with no inputs.□

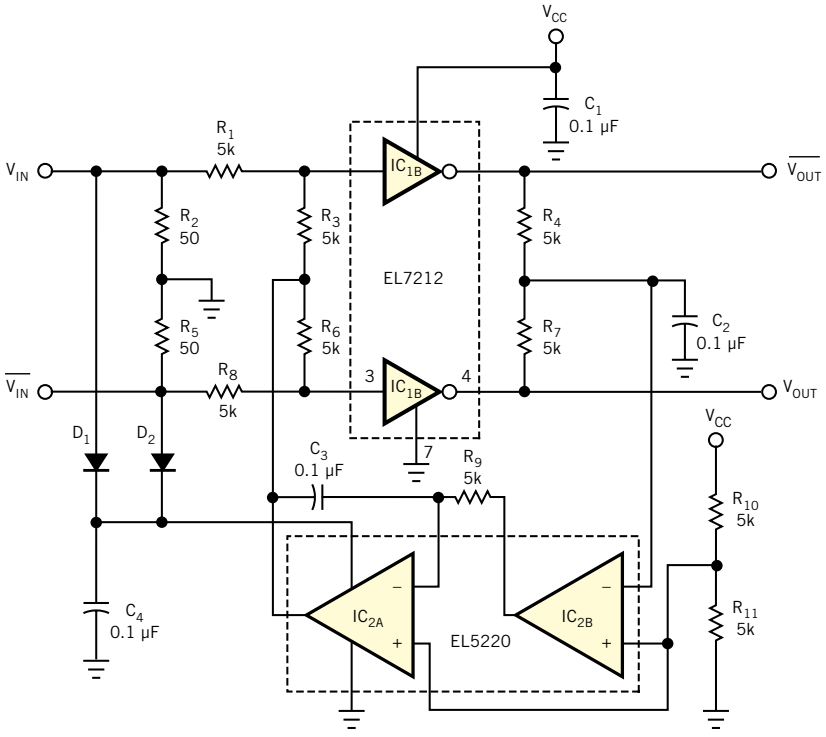


Figure 2 This circuit can correct the mismatch in turn-on and -off delays in a CCD-driver IC.

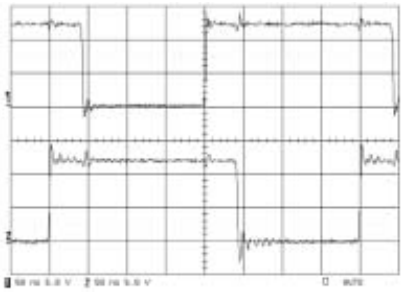


Figure 1 In a CCD driver, a mismatch may occur in the turn-on and -off delay times.

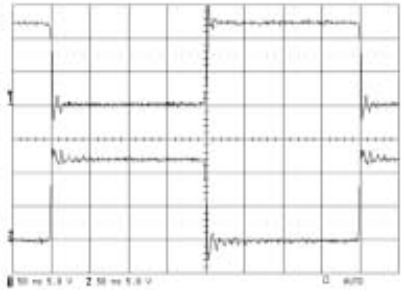


Figure 3 After the circuit in Figure 2 does its job, the turn-on and -off waveforms line up nicely.