# design ideas

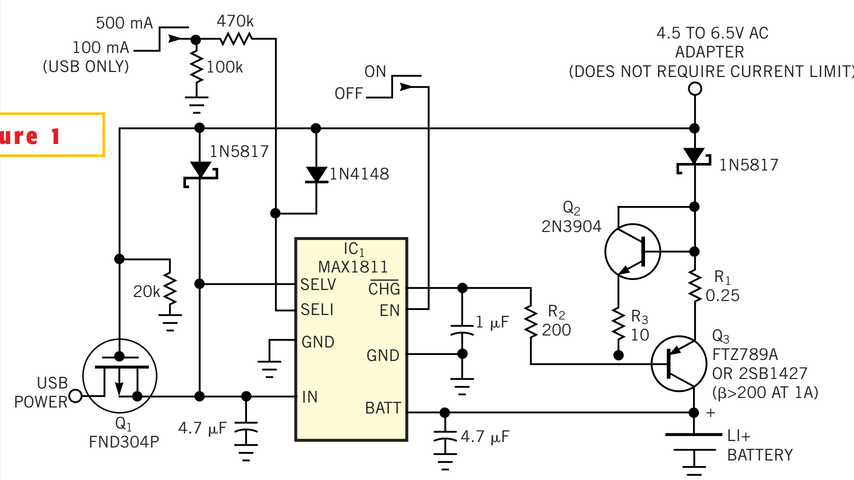
*Edited by Bill Travis*

## Add current boost to a USB charger

*Len Sherman, Maxim Integrated Products, Sunnyvale, CA*

The popular USB interface can charge a portable device while transferring data. But for high-capacity batteries, the 500-mA output current of USB hosts and powered hubs greatly extends the charging time. (Unpowered USB hubs supply no more than 100 mA.) Thus, a system that accepts charging power from an ac adapter as well as the USB port is more convenient. Such a system can charge from a notebook USB port when you're traveling, yet can charge faster via the adapter when you're at home or in the office. An external transistor current source adds dual-input capability to a single-chip lithium-cell charger (**Figure 1**). The chip, $IC_1$, operates alone when you connect to USB power and allows you to pin-program it for a maximum charging current of either 500 or 100 mA. When you plug in an ac adapter, which the 600-mA components set, the external-transistor current source, $Q_2$ and $Q_3$, turns on and sets $IC_1$'s charging current to 500 mA. Because $IC_1$ and $Q_2$ both charge the battery under that condition, the total charging current is 1100 mA.

**Figure 1**




**This battery charger delivers 100 or 500 mA (selectable) to a single lithium cell when USB power is connected and charges at 1100 mA (settable via $R_1$ or $R_2$) when ac power is present.**

$Q_2$ and $Q_3$ form a current limiter for the ac adapter. The limiter allows $Q_2$ and $R_1$ to pass the additional 600 mA. When the voltage drop across $R_1$ exceeds that across $R_2$, which $R_2$ and $R_5$ set, $Q_2$ begins to turn off. $Q_2$ cancels $V_{BE}$, enabling $R_1$ to more accurately set the maximum current. Voltage across $R_3$ sets the reference voltage, and the output current limits when the voltage drop on $R_1$ matches the voltage on $R_3$. $Q_3$ should have a beta higher than 200 at 1A, so that $IC_1$'s $\overline{CHG}$ pin can sink enough current to turn on $Q_3$. High beta also minimizes error in the transistor current source. When $IC_1$ changes from current mode to voltage mode at approximately 4.15V, $IC_1$'s $\overline{CHG}$ output turns off the transistor current source. $IC_1$ remains on and finishes off the taper to full charge. It also remains on and continues to function when USB power is gone and only ac power remains.

$IC_1$ also controls the prequalification current, which is the current level necessary to safely recover deeply discharged cells at low battery voltage. The $\overline{CHG}$ output assumes a high-impedance state during cell prequalification to ensure that the external current source remains off, and that the prequalification current of approximately 50 mA comes only from $IC_1$. When you plug in the ac power, $Q_1$ turns off to prevent back-feeding the USB input. You install $Q_1$ "backward" with the drain connected to USB input side, so that USB power remains connected to the IN pin ($IC_1$ pin 4) via $Q_1$'s body diode, even when $Q_1$ is off.

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# Transistor linearly digitizes airflow

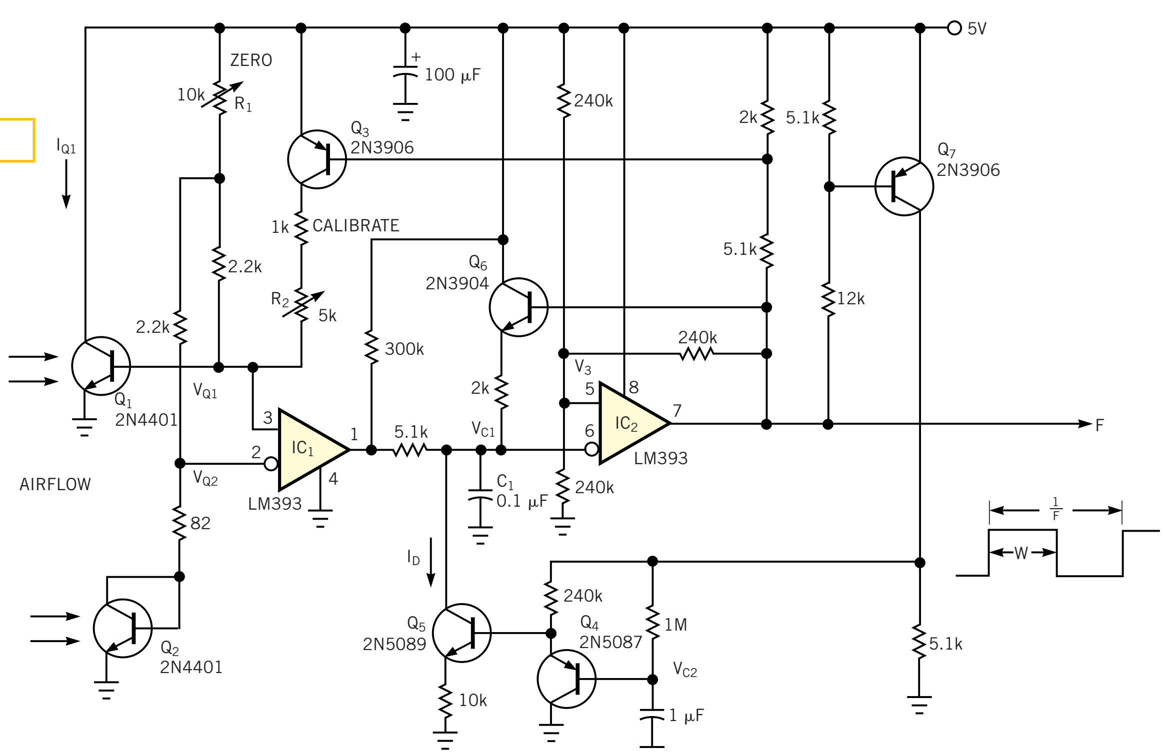
*Steve Woodward, University of North Carolina, Chapel Hill, NC*

A sensitive and reliable way to measure airflow is to take advantage of the predictable relationship between heat dissipation and air speed. The principle of thermal anemometry relies on King's Law, which dictates that the power required to maintain a fixed differential between the surface of a heated sensor and the ambient air temperature increases as the square root of air speed. The popular hot-wire anemometer exploits this principle, but it suffers from the disadvantage of using a specialized and fragile metallic filament, the hot wire, as the airflow sensor. The circuit in **Figure 1** avoids this disadvantage by using a pair of robust and inexpensive transistors instead of a flimsy wire for air-speed sensing. The $Q_1/Q_2$ front end of the circuit borrows from an earlier Design Idea (**Reference 1**). Just as in the 1996 circuit, the circuit in **Figure 1** works by continuously maintaining the condition $V_{Q1}=V_{Q2}$. To perform this task, the circuit must keep $Q_1$ approximately 50°C hotter than $Q_2$.

$V_{BE}$ balance requires this temperature difference, because $Q_1$'s collector current, $I_{Q1}$, is 100 times greater than that of $Q_2$, $I_{Q2}$. If $Q_1$ and $Q_2$ were at the same temperature, this ratio would result in $V_{Q1}$'s being greater than $V_{Q2}$ by approximately 100 mV. Proper control of $I_{Q1}$ establishes differential heating that makes $Q_1$ hotter than $Q_2$. The method thus exploits the approximate −2-mV/°C temperature coefficient of $V_{BE}$ to force $V_Q$ balance. The resulting average, $I_{Q1}$, proportional to the average power dissipated in $Q_1$, is the heat-input measurement that forms the basis for the thermal air-speed measurement. Calibration of the sensor begins with adjustment of the $R_1$ zero-adjust trim. You adjust $R_1$ such that, at zero airflow, $V_{Q1}=V_{Q2}$ with no help from $Q_3$. Then, when moving air hits the transistors and increases the heat-loss rate, $V_{Q1}$ increases and causes comparator $IC_1$ to release the reset on $C_1$. $C_1$ then charges until $IC_2$ turns on, generating a drive pulse to $Q_1$ through $Q_3$.

The resulting squirt of collector current generates a pulse of heating in $Q_1$, driving the transistor's temperature and $V_{BE}$ back toward balance. Proper adjustment of $R_2$ calibrates the magnitude of the $I_{Q1}$-induced heating pulses to establish an accurate correspondence between pulse rate and air speed. Now, consider measurement linearization. The square-root relationship of King's Law makes the relationship between heat loss and air speed nonlinear. You must iron the kinks out of the air-speed-calibration curve. You might achieve linearization in software, of course. However, depending on

Figure 1




**Using a simple transistor as sensor, this circuit yields a digitized, linear measurement of air speed.**

the flexibility of the data system the anemometer works with, a software correction is sometimes inconvenient. Another earlier Design Idea (**Reference 2**) presented an analog solution to linearization. But if you want the advantages of a digital, pulse-mode output—that is, noise-free transmission over long cable runs—you need a different fix.

The circuit in **Figure 1** provides both linearity and a digital output. The average heat the pulses deposit in $Q_1$ is $H=5V\times I\times F\times W$, where I is the amplitude of the $Q_1$ current pulses (adjusted with $R_2$), F is the output frequency, and W is the pulse width. W is inversely proportional to $I_D$, the discharge current that ramps down $V_{C1}$ and controls the on-time of $IC_2$. $Q_4$ and $Q_7$ average the output duty cycle to generate a control voltage for $Q_5$ and thus make W a function of F. In fact, the feedback loop this arrangement establishes implicitly makes $W=K/(W\times F)$, where K is a calibration constant determined by the component values. Therefore, $W^2=K/F$, and $H=5\times I\times F/\sqrt{K/F}$. This expression yields $F=(H/5I)^2/K$, making F the desired function of $H^2$ and thus linearizing the relationship between frequency and air speed.


References

1. Woodward, Steve, "Self-heated transistor digitizes airflow," *EDN*, March 14, 1996, pg 86.

2. Woodward, Steve, "Transistor and FVCs make linear anemometer," *EDN*, Sept 26, 1996, pg 72.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# Make a truly linear RF-power detector

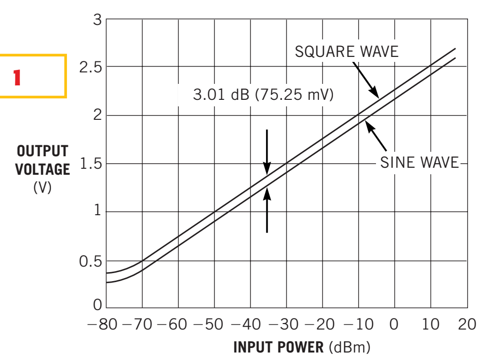
*Victor Chang and Eamon Nash, Analog Devices, Wilmington, MA*

Modern high-performance transmitters require accurate monitoring of RF power, because most cellular standards depend on strict power-transmission levels to maintain an effective network. Regulation of transmitted-signal strength also lets you build lower cost systems. **Figure 1** shows a waveform-independent circuit that provides a linear measurement of RF power. Sophisticated modulation schemes, such as CDMA (code-division multiple access) and TDMA (time-division multiple access) have obsoleted traditional approaches to RF power. Diode-based detectors have poor temperature stability, and thermal detectors have slow response times. Logarithmic amplifiers are temperature-stable and have a high dynamic range, but they exhibit a waveform-dependent response. This response causes the output to change with modulation type and, in the case of spread-spectrum technology, channel loading.

Power detection must be waveform-independent in systems that use multiple modulation schemes. These include point-to-point systems that are configurable to transmit QPSK (quadrature-phase-shift keying), 16QAM (quadrature amplitude modulation), and 64QAM, for example, and spread-spectrum systems such as CDMA and W-CDMA (wide CDMA). A logarithmic amplifier in an automatic-gain-control loop can regulate the gain of a variable-gain power amplifier, but the output voltage is waveform-dependent, because the logarithmic amplifier does not respond to the rms level of the signal. For example, sine- and square-wave inputs that have the same rms voltage levels have different logarithmic intercepts (**Figure 2**). You could use calibration factors to correct this intercept difference in a multistandard system.

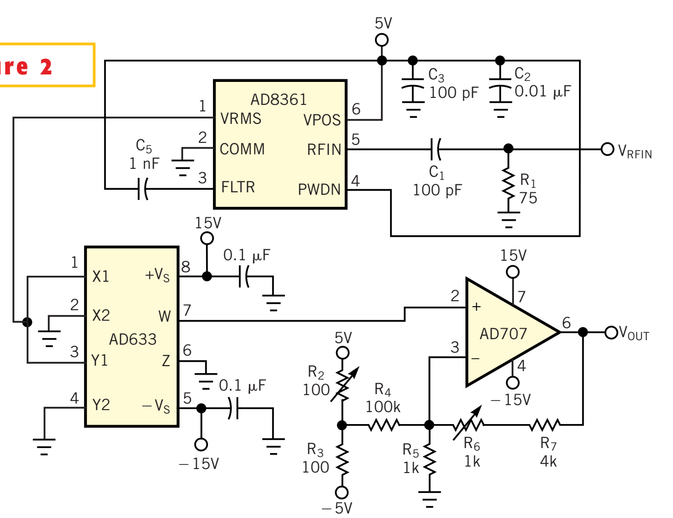
An alternative solution (**Figure 1**) uses the AD8361, a high-frequency true-power detector. Unlike the logarithmic amplifier, the AD8361 is an rms-to-dc converter and, therefore, responds to the

Figure 1




This circuit provides an output voltage that is linearly proportional to the input power in watts.

Figure 2

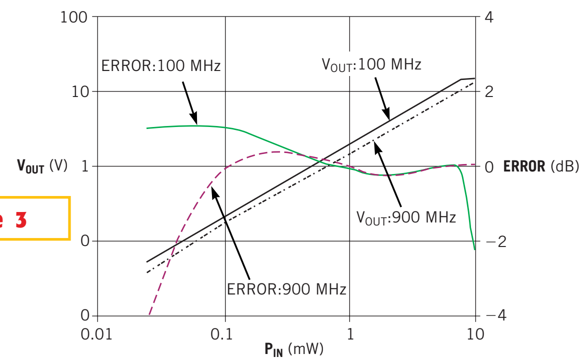



Log amps detect signals over a wide dynamic range, but are not rms-responding.

input rms voltage. Hence, a sine wave, a square wave, or any other input with the same rms level produces the same dc output, allowing you to incorporate waveform-independent measurement into a multimodulation system. With the addition of a multiplier, the circuit delivers an output voltage that is proportional to the input power level in watts. You can easily adjust gain and offset for this power meter with an op-amp circuit, thus providing an output scaled in volts per watt. A complex RF waveform feeds the input of the AD8361.

The multiplier squares the dc output to produce a voltage proportional to the power dissipated in the 50Ω input impedance of the circuit. The AD633 multiplier squares the rms output of the AD8361 and divides by 10. The AD707 provides a maximum gain of 6 [$G=(R_5+R_6+R_7)/R_5$]. This value is lower than the gain of 10 that you would need to exactly cancel the effect of the multiplier scaling and allows the circuit to have a wider dynamic range, because the output would saturate with a smaller input with a gain of 10. You can easily adjust all circuit offsets with potentiometer $R_2$. **Figure 3** shows measurements made with this power meter. The graphs plot the output voltage and error for input signals at frequencies of 100 and 900 MHz. The detector operates at frequencies as high as 2.7 GHz.

**Figure 3**




**The circuit in Figure 1 responds to rms signals, independent of waveform.**

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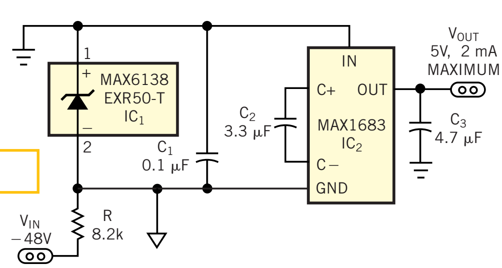
# Simple circuit provides 5V gate bias from −48V

*Will Hadden, Maxim Integrated Products, Sunnyvale, CA*

A small and simple circuit derives 5V from the −48V rail that telecomm applications typically use (**Figure 1**). Useful for gate bias and other purposes, the 5V supply delivers as much as 5-mA output current. A shunt reference, $IC_1$, defines −5V as ground reference for a charge pump, $IC_2$. The charge pump doubles this 5V difference between system ground and charge-pump ground to produce 5V with respect to the system ground. The shunt reference maintains 5V across its terminals by regulating its own current, $I_S$. $I_S$ is a function of the value of R. The current through R, $I_R$, is reasonably constant and varies only with the input voltage. $I_R$, the sum of the charge-pump and shunt-reference currents ($I_R=I_{CP}+I_S$), has maximum and minimum values set by the shunt reference.

**Figure 1**




**This small, simple circuit produces 5V at 5 mA from a −48V input.**

The shunt reference sinks as much as 15 mA and requires 60 μA minimum to maintain regulation. Maximum $I_R$ is a function of the maximum input voltage. To prevent excessive current in the shunt reference with no load on the charge-pump output, use the maximum input voltage (−48V−10%=−52.8V) to calculate the minimum value of R. The maximum reference sink current, 15 mA, plus the charge pump's no-load operating current, 230 μA, equals the maximum $I_R$ value, 15.23 mA. Thus, $R_{MIN}=(V_{IN(MAX)}-V_{REF})/I_{R(MAX)}=3.14\ k\Omega$.

Choose the next-highest standard 1% value, which is 3.16 kΩ. You calculate the guaranteed output current for the charge pump at the minimum line voltage: −48V+10%=−43.2V. The charge pump's maximum input current is $I_{CP}=(V_{IN(MIN)}-V_{REF})/R-I_{SH(MIN)}=(43.2-5)/3.16-90\ \mu A=12\ mA$, where 90 μA is the minimum recommended operating current for the shunt reference. Assuming 90% efficiency in the charge pump, the output current is $I_{OUT}=(I_{CP}/2)\times0.9=(12/2)\times0.9=5.4\ mA$. You halve the charge-pump current, because the output voltage is twice the input voltage. Be sure that R can handle the wattage under no-load conditions. A 1W resistor suffices in this example.

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# Circuit provides laser-diode control

*Michael Fisch, Agere Systems, Longmont, CO*

Laser diodes are sensitive to ESD, rapid turn-on currents, and overvoltage conditions. To address those problems, the simple laser-diode controller in **Figure 1** has several functions. The first part of the circuit comprises an 8.2V zener diode, $D_1$ that forms the heart of a constant-voltage source for the laser diode. Next, $IC_{1A}$, half of a dual FET-input op amp, forms an inverting integrator to slow the turn-on time. To turn on the laser diode, $IC_{1B}$, the other half of the op-amp IC, triggers the base of $Q_2$. This transistor forms a constant-current source for the laser diode. You can monitor the laser-diode supply voltage and the sense-diode current and voltage. You use these parameters as inputs to the differential amplifier, $IC_{2A}$, the first half of another dual FET-input op amp. When an overvoltage condition occurs, the difference amplifier detects the condition, and its output drives $IC_{2B}$, configured as an open-loop comparator. You set the threshold by using the potentiometer, $R_1$. Zener diode $D_2$ provides a constant-voltage source for that threshold setting. When the voltage reaches the threshold, the output triggers the base of $Q_1$, which instantly shuts down $IC_{1B}$, which in turn shuts down the laser diode.

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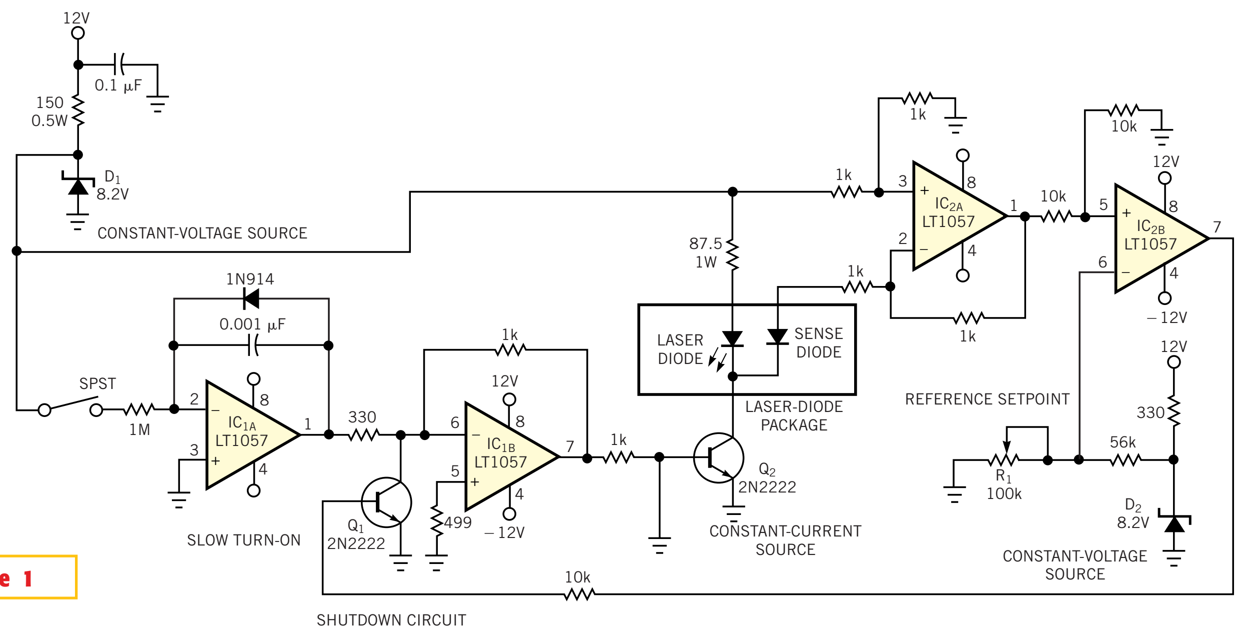
Figure 1




**Constant voltage and current and slow turn-on time are the keys to laser diodes' survival.**

# One amplifier has two gain figures

*Chuck Wojslaw, Catalyst Semiconductor, Sunnyvale, CA*

The single-supply circuit in **Figure 1** is an inverting amplifier with two outputs—one for positive output voltages, $V_{OUT(POS)}$, and the other for negative output voltages, $V_{OUT(NEG)}$. Steering diodes $D_1$ and $D_2$ split the amplifier, $IC_1$, output into the two output polarities relative to the 2.5V reference. The gain of the inverting amplifier for each of the two polarities features independent programming, using Catalyst's (www.catsemi.com) 100-tap, digitally programmable potentiometers $DPP_1$ and $DPP_2$. You configure the potentiometers as variable resistances and model them as $(1-p)R_{POT}$, where p represents the proportional position of the wiper as it moves from one end (p=0) of the DPP to the other end (p=1). $R_{POT}$ is the potentiometer's end-to-end resistance. In terms of p, the gains of the circuit are

$$V_{OUT(POS)} = -\frac{(1-p_1)R_{POT1}}{R_1}V_{IN}$$

FOR $0 < V_{IN} < 2.5V$, and

If $R_1 < R_{POT}$, the gain values can be less

$$V_{OUT(NEG)} = -\frac{(1-p_2)R_{POT2}}{R_1} V_{IN}$$

FOR $2.5V < V_{IN} < 5V$.

than one, one, or greater than one. For the circuit values shown, you can program the two gains from approximately 1/10 to 10. If you characterize the potentiometer, the measured accuracy of the circuit is approximately 1%. This implementation of the circuit uses only six components and is appropriate for signal-processing applications.

Figure 1

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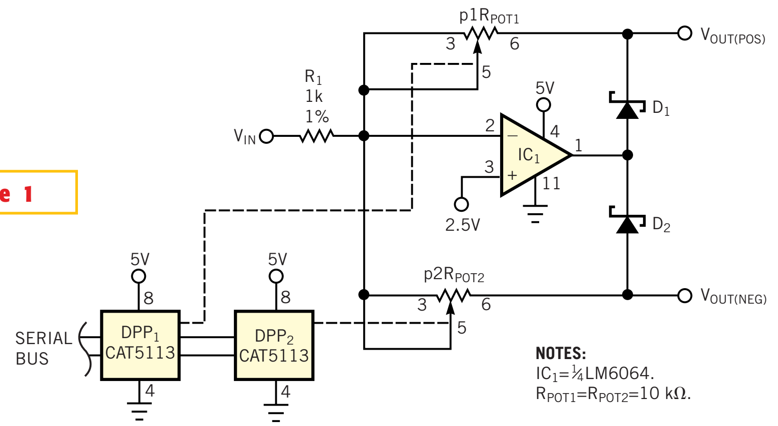



Using digitally programmable potentiometers, you can obtain two distinct gain figures from one amplifier.

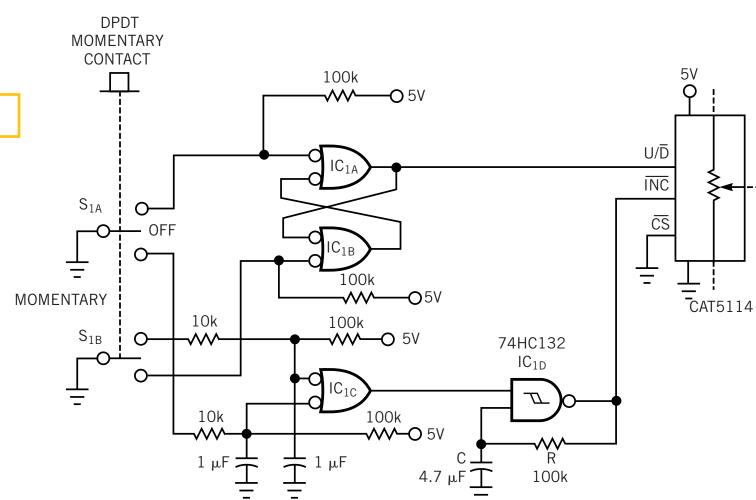
# Single switch controls digital potentiometer

*Jim Bach, Delphi Delco Electronics Systems, Kokomo, IN*

THIS DESIGN IDEA is an evolution and simplification of another (**Figure 1**, **Reference 1**). Replacing the three inverted-input NOR gates with their logical equivalents, positive-input NAND gates, makes these three gate symbols consistent with the fourth, which was drawn as a positive-input NAND gate. The 74HC132's data sheet describes the device as a quad, two-input NAND gate with hysteresis.

Figure 1

As the earlier design also describes, you can activate the DPDT rocker switch, $S_1$, to produce either a "count-up" or a "countdown" effect at the digital potentiometer, CAT5114. Moving the switch up causes $S_{1A}$ to ground the input of $IC_{1A}$, thus causing the NAND-gate flip-flop, $IC_{1A}$ and $IC_{1B}$, to switch high, thereby commanding the CAT5114 to count up. At the same time, $S_{1B}$ causes the 1-µF capacitor on $IC_{1C}$'s upper input to discharge through a 10-kΩ resistor. Eventually the output of $IC_{1C}$ also switches high, thus enabling the oscillator comprising $IC_{1D}$. Similarly, moving the switch down causes $S_{1B}$ to ground the input of $IC_{1B}$, thus causing the NAND-gate flip-flop to




This is the original circuit, as published in Reference 1.

**TABLE 1–SUMMARY OF SAVINGS**

| Component | Figure 1 count | Figure 4 count | Savings |
|---|---|---|---|
| ICs | Two | Two | Zero |
| Resistors | Seven | Four | Three |
| Resistor values | Two (10 kΩ, 100 kΩ) | One (100 kΩ) | One |
| Capacitors | Three | Two | One |
| Capacitor values | Two (1 µF, 4.7 µF) | Two (0.1 µF, 4.7 µF) | One lower value and cheaper |
| Switches | One DPDT | One SPDT | Single-pole and cheaper |

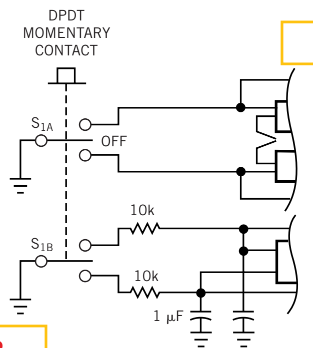
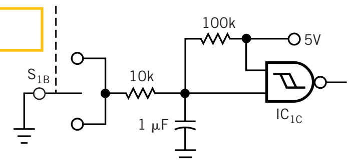



**Figure 2**

You can restructure the switch-interface circuit of Figure 1 as shown.

**Figure 3**




You can simplify the oscillator-enable structure, as shown.

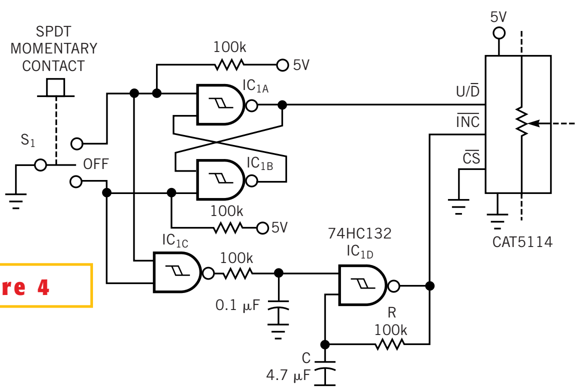



**Figure 4**

This circuit uses fewer and cheaper components than the circuit in Figure 1.

switch low, thereby commanding the CAT5114 to count down. At the same time, $S_{1A}$ causes the 1-µF capacitor on $IC_{1C}$'s lower input to discharge through a 10-kΩ resistor, thereby eventually enabling the oscillator comprising $IC_{1D}$.

The first step in simplifying this design is to rearrange the connections of $S_1$ so that the A and B sections are not cross-connected between operating the flip-flop and the oscillator-enabling circuit. You can rewire the interface structure as shown in **Figure 2**. This circuit uses $S_{1A}$ to control the flip-flop, whereas $S_{1B}$ controls the oscillator-enable circuit. This step does nothing directly to reduce the parts count of the circuit; however, it does make the subsequent step more obvious. The next step in the simplification is to recognize that the two RC networks on the inputs of $IC_{1C}$ both do the same thing but in opposite switch positions. As far as $IC_{1C}$ is concerned, either switch position performs the same function; that is, to debounce the switch contacts and eventually enable the oscillator. Thus, you need only one RC network, and you can tie it to *both* of $S_{1B}$'s active positions (**Figure 3**). Moving the switch in either direction discharges the 1-µF capacitor through the 10-kΩ resistor, eventually causing the output of $IC_{1C}$ to switch high, thus enabling the oscillator. When you release the switch, $S_{1B}$ goes to the open, or off, state, and the 1-µF capacitor recharges through the 100-kΩ resistor, thus turning off the oscillator.

The last simplification step stems from realizing that the sole purpose of $IC_{1C}$ and the RC filter on its input is to generate a high state whenever switch $S_1$ is in either of its active positions. True, the RC filter does debounce the switch contacts; however, the actual switch- closure information available at $S_{1B}$ is also available at $S_{1A}$. Thus, you can simply use $IC_{1C}$ to directly monitor the $S_{1A}$ contacts. You can move the RC filtering to the input of $IC_{1D}$. This step allows you to simplify $S_1$, changing it from a DPDT to a SPDT configuration, which means you can use a cheaper switch. Because the RC debounce filter now connects to a low-impedance gate output, $IC_{1C}$, you can increase the R, thus reducing the amount of C you need to form the same time constant. Thus, you can use smaller, cheaper capacitors. You can also use the same resistor value, 100 kΩ, in all four locations, eliminating the need to inventory two resistor values. The final circuit appears in **Figure 4**. **Table 1** summarizes the savings in component count and cost.

REFERENCE

1. Wojslaw, Chuck, "Single switch controls digital potentiometer," *EDN*, Feb 7, 2002, pg 100.

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# Instrumentation amp makes noninverting integrator

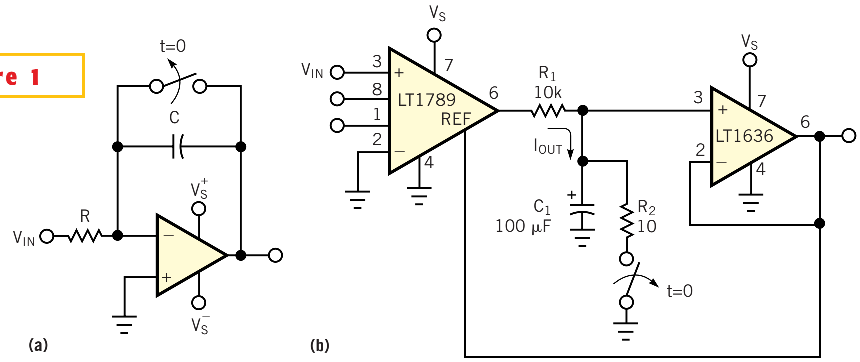
*Glen Brisebois, Linear Technology Corp, Milpitas, CA*

FIGURE 1A SHOWS the classic implementation of an integrator. The circuit has two properties that may be undesirable in same applications: It necessarily inverts, and it requires a split-supply or midsupply reference. **Figure 1b** shows an implementation of an integrator that uses an LT1789 instrumentation amplifier. This integrator does not invert, and it works with a single supply. In addition, because it has a positive-only output swing, the integrator capacitor can be a high-value, polarized electrolytic unit, as shown. Most of the circuit operates as a voltage-controlled current source. The

LT1789 is a precision micropower instrumentation amplifier that can operate from 3 to 36V total-supply spans.

With a gain setting of 1, with pins 1 and 8 open, the voltage between the inputs also appears between the Output and Reference pins. The Output pin connects to one side of $R_1$, and the voltage on the other side of $R_1$ drives the Reference. The input voltage, $V_{IN}$, appears across $R_1$, causing the current-source action, with $I_{OUT}=V_{IN}/R_1$. Dumping this current into a capacitor produces the integrator action, with the time constant $R_1C_1$. The LT1636 buffers the output voltage on $C_1$, thereby eliminating the loading effects of approximately 200 kΩ of the LT1789's Reference pin and any downstream circuitry. The wide, single-supply range and micropower operation make the circuit suitable for battery-powered systems. As a positive-output-only integrator, this circuit is not generally applicable inside control loops. Suitable applications include accumulators, adjustable ramp generators, and voltage-to-frequency converters.

**Figure 1**




The classic integrator in a inverts and requires split supplies. The circuit in b is noninverting and works with a single supply.

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