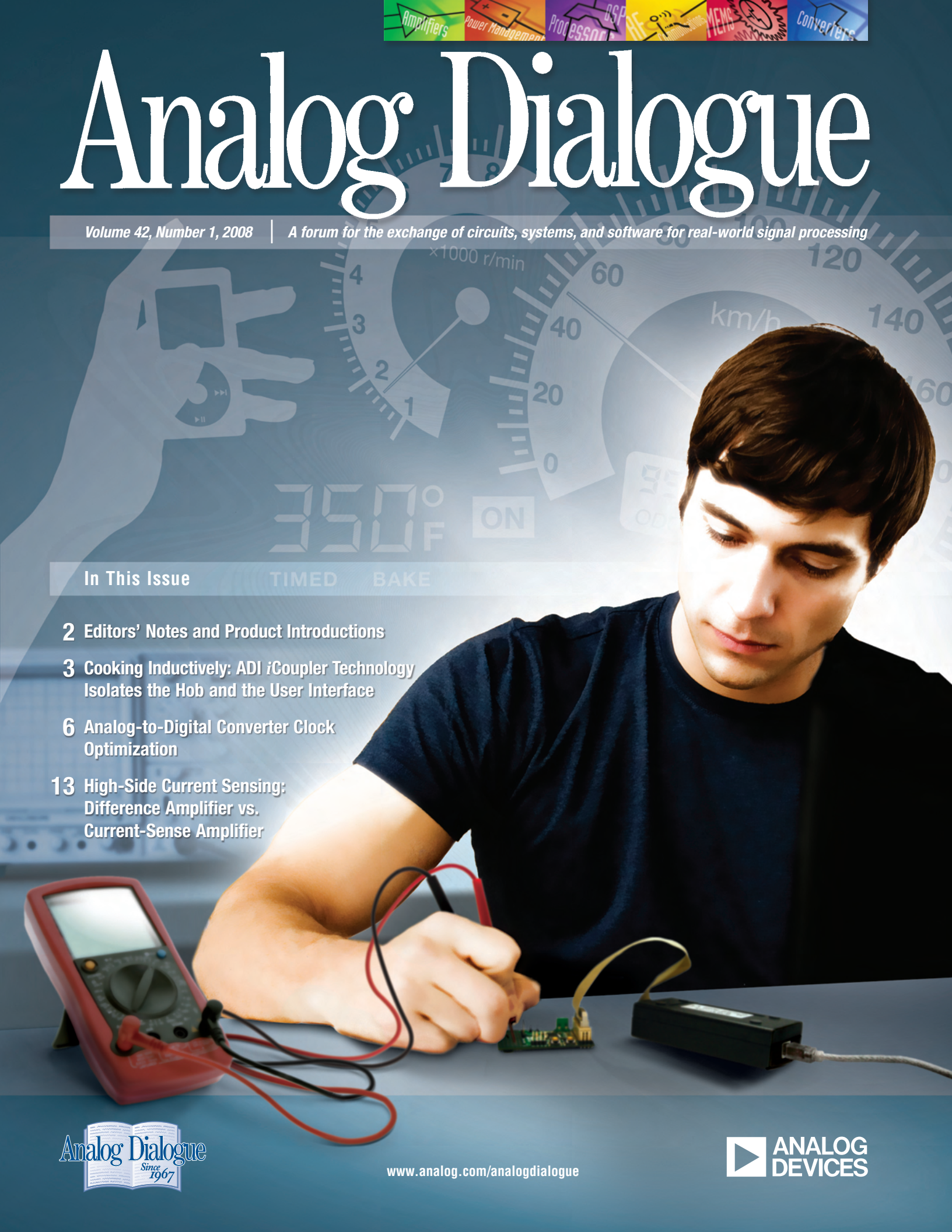

Analog Dialogue

Volume 42, Number 1, 2008 | A forum for the exchange of circuits, systems, and software for real-world signal processing

In This Issue

Analog Dialogue Since 1967

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ANALOG DEVICES

Editors' Notes

GOOD READING

You'll find the usual diversity of topics in this issue.

In "Cooking Inductively," the topic is keeping a heating ring cool while cooking electrically. The key is to let eddy currents in the metal pot produce the heat; the heating ring is just a transformer, driven by a pair of insulated-gate bipolar transistors (IGBTs). One problem in such designs is maintaining electrical isolation between the user interface, the active circuitry, and the IGBTs. Read about an effective, economical approach using ADI's *i*Coupler® technology (page 3).

You have a fast, accurate analog-to-digital converter, but it's not performing as well as you expect. Have you considered the error produced by timing jitter—contributed by the clock source and its signal chain—at the ADC's convert-start pin? The article on page 6 helps you think about this problem and its remedies.

Accurate high-side current sensing is necessary in applications such as motor control, solenoid control, and power management. The sensing circuitry must reject high common-mode voltages, while providing high gain and accuracy. The article on page 13 compares the pros and cons of two popular sensing-amplifier architectures in such applications.

HIGH-FREQUENCY COMMON MODE

The sea of RF energy in which we are immersed is often the source of mysterious offsets in measurements conducted using conventional instrumentation-amplifier circuitry. Although such amplifiers may be rated at 100 dB or more for low-frequency common-mode rejection, it is possible for ambient RF, picked up on the leads as a high-frequency common-mode signal, to drive amplifier low-level input stages into nonlinear regions, developing mysterious dc- and low-frequency errors.

This matter has been discussed in these pages a number of times, most notably in *Analog Dialogue*, Volume 37, Number 3[1] (2003), where we introduced the topic and presented a reader's observations on Page 2, then offered a set of references on Page 14. A seminal paper on the subject, presented at the 39th Annual Instrumentation Symposium in 1993 by Herman Gelbach—currently a consultant for Scanivalve Corporation—discusses the phenomenon and offers some remedies. Unfortunately, that paper is not available online—but, fortunately, the author has provided us with a revised, updated version, titled "The Contaminator of Signals—High-Frequency Common-Mode Errors,"[2] and has given us permission to place it on our website, along with a brief piece entitled "What Is This Third Signal Wire and What Do I Do with It,"[3] republished with the permission of Scanivalve Corporation.

Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 42 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. For history buffs, the *Analog Dialogue* archives include all regular editions, starting with Volume 1, Number 1 (1967), plus three special anniversary issues.

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NEW LINEAR-CIRCUIT DESIGN HANDBOOK

Effective analog circuit design requires a strong understanding of linear devices. *Linear Circuit Design Handbook*[4] bridges the gap between component theory and practical circuit design. Providing complete coverage of analog components and showing how to use them effectively, it serves as a useful reference for engineers involved in analog- and mixed-signal design. *Analog Dialogue* readers can read a sample chapter,[5] posted on our website, and get a discount when they order this book directly from Newnes.[6] Enter discount code 92222.

Dan Sheingold [dan.sheingold@analog.com]

Scott Wayne [scott.wayne@analog.com]

[1] www.analog.com/library/analogdialogue/cd/vol37n3.pdf#page=2

[2] www.analog.com/library/analogdialogue/archives/42-03/HFCM.pdf

[3] www.analog.com/library/analogdialogue/archives/42-03/third_wire.pdf

[4] www.elsevierdirect.com/product.jsp?isbn=9780750687034

[5] www.analog.com/library/analogdialogue/archives/42-03/CH03-H8703.pdf

[6] www.elsevierdirect.com/imprint.jsp?iid=73

PRODUCT INTRODUCTIONS: VOLUME 42, NUMBER 1

Data sheets for all ADI products can be found by entering the model number in the search box at www.analog.com.

January

Amplifier, Intermediate-Frequency, 20-MHz to 500-MHz ... **ADL5531**
DAC, Audio, 8-channel, 24-bit, 192-kHz, differential **AD1933**
DAC, Audio, 8-channel, 24-bit, 192-kHz, single-ended **AD1934**
DACs, Current-Output, dual, 12-/14-/16-bit, 500-MSPS **AD9780/AD9781/AD9783**
Drivers, Differential ADC, extremely low harmonic distortion **ADA4937/ADA4938**
Energy-Measurement ICs, single-phase **ADE7566/ADE7569**
Sensor, Intelligent Battery, 12-V automotive **ADuC7033**
Signal Splitters, RF, 1:3/1:4, single-ended **ADA4304-x**
Transceiver, RS-485, half-/full-duplex, isolated, ESD-protected **ADM2491E**

February

ADCs, Successive-Approximation, 4-channel, 12-/10-/8-bit, 140-kSPS **AD7991/ AD7995/AD7999**
Amplifier, Power, WiMAX, 2.5-GHz to 2.7-GHz **ADL5571**
Converter, Capacitance-to-Digital, single-electrode sensors ... **AD7148**
Detector/Controller, Logarithmic, dual, 10-GHz, 50-dB **ADL5519**
Energy-Measurement ICs, single-phase **ADE7166/ADE7169**
Modulator, Quadrature, 400-MHz to 6-GHz **ADL5375**
Transmitter, HDMI/DVI, consumer electronic control **ADV7520NK**

March

Amplifier, Audio, Class-D, 3-W, monophonic **SSM2311**
Amplifier, Difference, 2-channel, audio **AD8273**
Amplifier, Difference, 2-channel, precision **AD8270**
Amplifier, Driver, RF, 400-MHz to 2700-MHz **ADL5320**
DAC, Current-Output, 12-bit, multiplying, serial-input **AD5441**
DAC, Voltage-Output, 12-bit, serial-input **AD5626**
DACs, Current-Output, dual, 12-/14-/16-bit, 800-MSPS, 32-bit NCO..... **AD9785/ AD9787/AD9788**
DACs, Voltage-Output, 8-channel, 16-/14-bit, serial-input **AD5362/AD5363**
Driver, Gate, 4-channel, isolated, 100-mA output **ADuM1420**
Equalizer, HDMI/DVI, TMDS **ADV3003**
Gyroscope, Yaw-Rate, wideband, SPI interface **ADIS16060**
Isolators, Digital, 2-channel, 5-kV isolation **ADuM2200/ADuM2201**
Mixer, Y, high-linearity, LF to 4-GHz **ADL5350**
Monitor, Current-Shunt, high-voltage **AD8215**
Sensor, Angular Rate, high-precision **ADIS16130**
Sensor, Inertial, 3-axis, high-precision **ADIS16354**
Switch, HDMI/DVI, 4:1, equalization, pre-emphasis **AD8197B**
Switches, Temperature Trip-Point, micropower, SOT-23 ..... **ADT6503/ADT6504**
Synthesizer, Frequency, PLL, VCO **ADF4360-9**
System, Measurement and Control, 12-bit **AD7294**

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Cooking Inductively: ADI *i*Coupler Technology Isolates the Hob and the User Interface

By Jerome Patoux

Easy-to-use inductive cooking surfaces (*hobs*) are gaining acceptance by consumers as they are becoming more affordable. They are significantly safer, without flames or other direct heat sources on the hob, and they have better overall performance, including faster heating time.

Even though induction technology is well founded and proven, the design of equipment to drive the inductive plate—causing metal pots to heat up—requires designers to understand a wide variety of physical principles and design techniques. Lying below the surface of the relatively simple block diagram of an inductive hob, the required techniques include several distinct areas of analog- and digital signal processing, electrical protection, and isolation.

For example, safety standards require isolation between the user interface and the power supply. There are three primary loci of isolation:

- the low-voltage power supplies for the control logic
- between the *insulated-gate-bipolar-transistor* (IGBT) power stage and its control signals
- between the user controls and the system controller

A safe system must meet a minimum of two of these isolation requirements. This article will discuss innovative solutions that allow isolation of the IGBT gate drivers and the user interfaces.

Description of the System

As with a transformer, the inductive element generates a magnetic field. When a metal pan is placed in the field, eddy currents are generated. Their energy is dissipated as heat, causing the pan—and, by conduction, its contents—to become hot. From an electrical point of view, the inductive element drives a lossy LC resonant circuit, and the losses produce heat. Figure 1 shows the elements of an inductive heating system.

The inductor current waveform is created by a high-efficiency switched dc power supply and a pair of IGBT switches. The switches are driven by a microcontroller, which responds to a feedback loop that forces conditions monitored by sensors to correspond to settings established by the user—and to remain within safe limits.

The main sensor, a transformer in series with the inductive plate, monitors the value of the current through the inductive plate in order to maintain the appropriate current value for the selected cooking level. This prevents damage to the power stage—the inductive plate and IGBTs—by decreasing the current level as necessary to avoid an overcurrent condition.

Since the inductance and capacitance of the inductive plate, pan, and transformer constitute a resonant LC circuit, one might think that the induction frequency could be determined by setting the values of L and C. Unfortunately, the inductance and capacitance values, and hence the resonant frequency, depend on the size, shape, and material of the pan that is being used. Thus, the different heating levels selected through the user interface can't be set by fixed frequencies. A more effective way to set these working levels is based on a current measurement, which provides a measure of the dissipated power. The feedback loop allows the microcontroller to adjust the current level to correspond to the chosen heating level. The microcontroller adjusts the frequency of the *pulse-width-modulated* (PWM) waveform to adapt to the pan. The inductive-hob designer, already knowing the current that corresponds to each required heating level, simply programs the microcontroller to adjust the PWM frequency to provide the appropriate current for each heating level.

The frequency of the PWM signal that drives the IGBTs will typically range from about 20 kHz to 100 kHz. Considering that IGBTs have slower turn-off characteristics than MOSFETs, the switching frequency is limited to a few tens of kilohertz. The PWM signal from the microcontroller has a fixed duty cycle (say 50%); its frequency will be adjusted depending on the power required for the heating level selected by the user.

Due to the high voltages that can be generated in high-current inductive circuitry, it is important to provide electrical isolation at critical points in the system. In particular, it is essential to isolate the power stage of the inductive hob from the microcontroller and other digital circuitry. One way to do this is to use isolated IGBT drivers. A series of low-cost isolated gate-driver circuits, based on ADI's innovative *i*Coupler® technology, has many advantages compared to traditional isolation solutions.

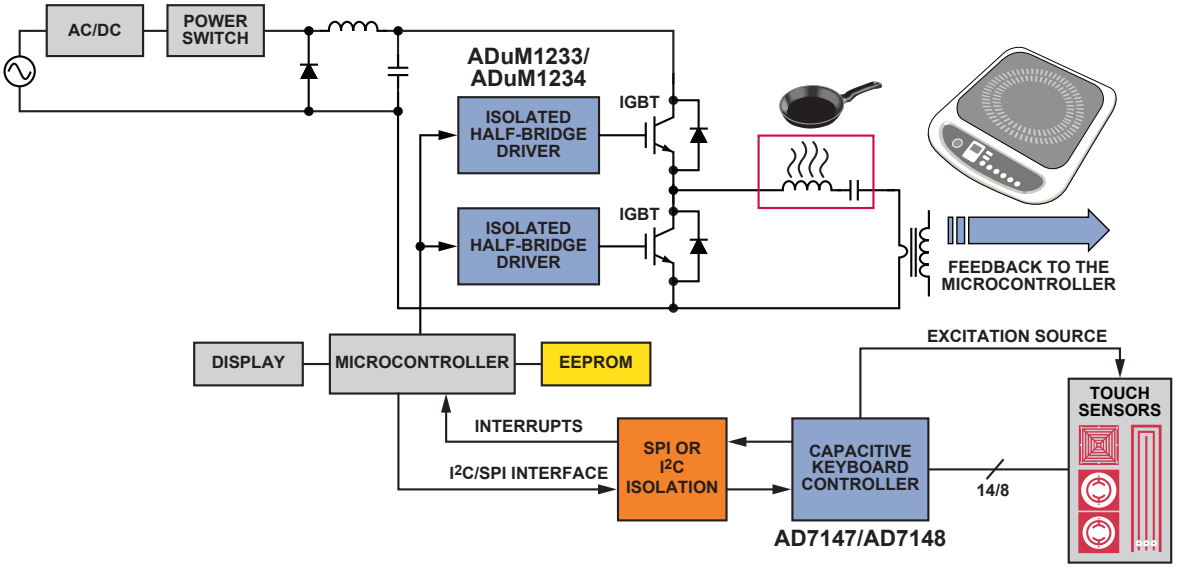

Figure 1. Inductive heating system.

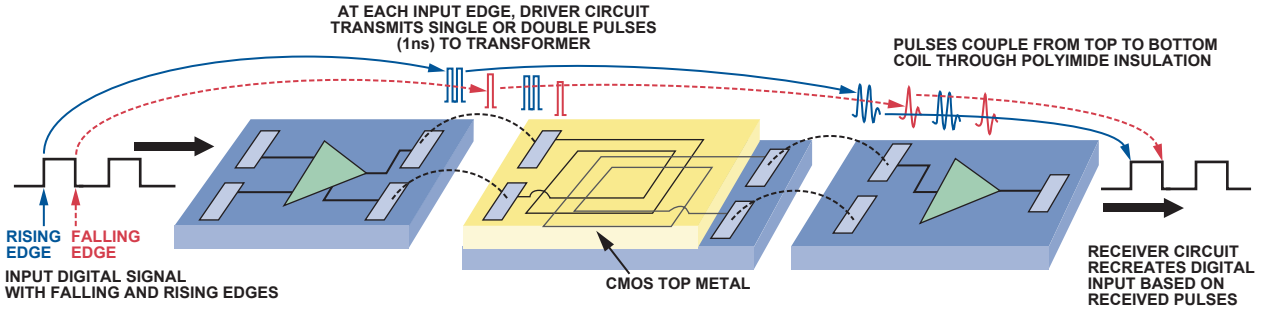

Figure 2. The anatomy of *i*Coupler technology.

Galvanic isolation is a means of preventing current from flowing directly between two communicating circuits. There are two major motivations for using isolation. The first is to protect people and equipment where there is the possibility of exposure to high operating voltages or current surges. The second is to avoid ground loops and disruptive ground currents where interconnections involve differing ground potentials. In both cases, isolation techniques prevent current flow but allow for data- or power flow between the two circuits.

*i*Coupler technology (Figure 2) is a transformer-based approach to isolation. Integrating microtransformers and electronic circuitry, it has all the advantages of optocoupler-, discrete-transformer-, and semiconductor technologies—but without the disadvantages of optocouplers and discrete transformers. Optocoupler limitations include excessive power consumption, large timing errors, data-rate limitations, and sensitivity to temperature. In *i*Coupler-based products, insulation to meet the requirements of safety agencies is achieved through the use of a 20-µm-thick polyimide insulation layer between the transformer coils. It is capable of achieving an isolation rating of greater than 5 kV rms. This technology uses patented *refresh* circuitry, which updates the output to correspond correctly to the input state when input-signal transitions are not present, thus avoiding the inherent inability of discrete transformers to achieve correct dc levels.

*i*Coupler technology[1] provides benefits in five key areas:

- Integration (size/cost)
- Performance
- Power consumption
- Ease of use
- Reliability

Isolation of IGBTs Using *i*Coupler Technology

*i*Coupler technology can be found in a family of isolated gate drivers, including the 2-channel ADuM1233[2] (Figure 3), which offers isolation between the outputs and the inputs—and also between the two outputs—making it useful for isolating the controls of the IGBTs.

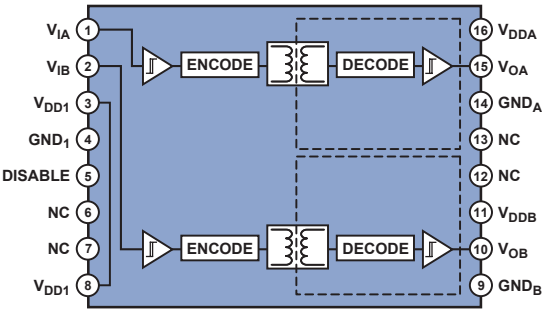

Figure 3. Functional diagram of the ADuM1233.

The input circuit's power is provided by an isolated power supply and may require one or more stages of voltage conversion. A 5-V power supply is required for the microcontroller and the rest of the system, and the IGBT circuit requires 15 V for efficient operation. The *i*Coupler-isolated gate drivers must supply up to 100 mA of peak drive current, so an additional gain stage is required, as shown in Figure 4.

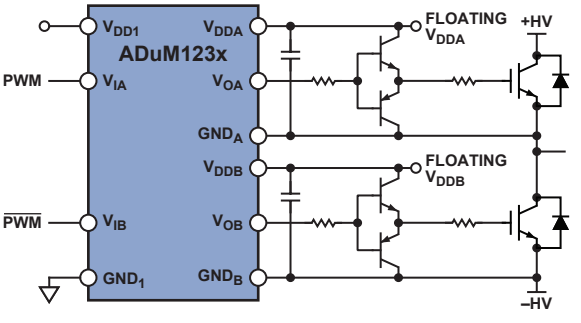

Figure 4. Driving the IGBTs using *i*Coupler isolation.

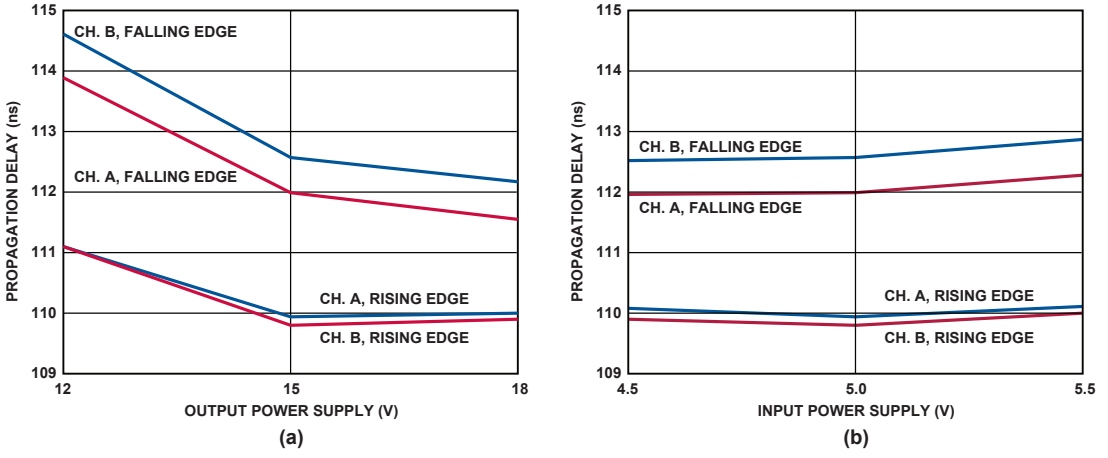

Figure 5. Propagation-delay channel matching as a function of power-supply voltage. (a) Output supply. (b) Input supply.

Because of the importance of the timing relationship between the two channels—with the IGBTs being driven by PWM signals in antiphase—the speed, stability, and reliability of the *i*Coupler technology are especially advantageous compared to LEDs and photodiodes. The curves in Figure 5 show that the propagation delays on the rising edges of the two channels are matched to about 100 ps—and on the falling edges to better than 1 ns—over the 12-V to 18-V output- and 4.5-V to 5.5-V input power-supply ranges.

The resulting timing margins ensure fully complementary switching of the IGBTs, improving the efficiency of the power stage and the overall system.

As noted, the ADuM1233 offers true galvanic isolation between the input circuitry and the outputs of the device, and between the two output circuits. Each isolated output can operate at up to ±700 V with respect to the input, thus supporting the negative voltages of the low-side power supply (–HV in Figure 4). The difference between the high- and low-side supply rails (+HV and –HV) must not be greater than 700 V; however, this is compatible with the voltage rails typically used for powering inductive cooking.

Isolation of the User Interface with *i*Coupler Technology

If a capacitive keyboard is used, the interface between the microcontroller and the AD7147[3] or AD7148[4] capacitive keyboard controller can be implemented serially with either an SPI (*serial peripheral interface*, originated by Motorola) or I²C® (*inter-integrated circuit*, a Philips Semiconductor trademark). The bidirectional I²C interface is used for relatively low data-rate communication over short distances where low cost is important. I²C enables low cost by using only two bidirectional wires. This low-cost advantage is negated, however, when the I²C bus is isolated with optocouplers, which are unidirectional and cannot handle bidirectional signals. The transmit and receive signals from each wire must thus be separated, with the resulting four wires isolated with four optocouplers. In addition, a specialized buffer is required to eliminate lockup and glitches within the isolated interface. The extra components add cost and complexity, and they consume valuable board space.

Integrated isolation solutions available in *i*Coupler technology reduce space requirements and design complexity at low cost. The ADuM1250[5] shown in Figure 6, and ADuM1251,[6] embody true bidirectional isolation and incorporate a buffer to eliminate glitches and lockup. This degree of comprehensive integration limits the required external components to two bypass capacitors and two pairs of pull-up resistors (specified in the I²C standard)—and provides an I²C interface at low cost. Details on applying these devices can be found in AN-913[7] Application Note *Isolating PC Interfaces*.

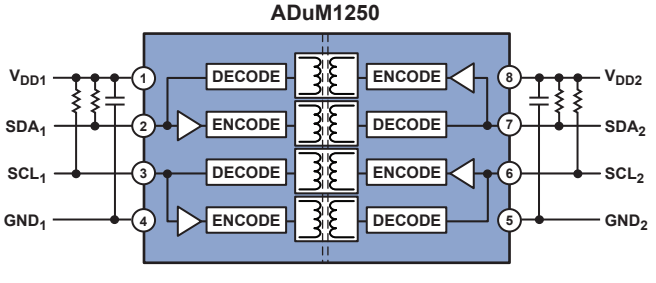

Figure 6. ADuM1250 dual hot swappable I²C isolator.

Pan Detection

It is important to detect the presence of the pan on the inductive hob. The IGBTs have to manage high voltage rails that are connected to their collector (+HV). By sampling these voltages with resistive dividers, a signal representing them can be sent to the microcontroller to detect any variation of the voltage at the collector of the IGBT. If a user chooses a heating level and places a pan on the inductive hob, the resultant energy transfer and current spike will produce a voltage variation at the collector, and thus at the resistive-divider output. When the pan is removed from the inductive hob, the change will be in the opposite direction. Thus, by comparing the voltage variation with a fixed threshold, using a comparator from the ADCMP3xx[8] family, for example, the pan's presence on the inductive hob can be detected. If no pan is detected, an interrupt is sent to the microcontroller, which will adjust the PWM frequency until the IGBTs stop providing current to the inductive element. This provides extra safety in case the user forgets to switch off the inductive hob.

CONCLUSION

Inductive cooking technology offers one example of the many useful applications of Analog Devices *i*Coupler digital-isolation devices. Today, a whole range of *i*Coupler products is available for general digital isolation and specialized applications. Some examples are shown in the selection table.[9] Further information and an overview of the *i*Coupler technology can be found at www.analog.com/*i*Coupler.

ACKNOWLEDGEMENTS

The author would like to thank Andrew Erskine (applications engineer), David Krakauer (marketing manager for *i*Coupler products), and Mark Cantrell (applications engineer for *i*Coupler products) for their great advice and help in proofreading.

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[1] www.analog.com/*i*Coupler
[2] ADI website: www.analog.com (Search) ADuM1233 (Go)
[3] ADI website: www.analog.com (Search) AD7147 (Go)
[4] ADI website: www.analog.com (Search) AD7148 (Go)
[5] ADI website: www.analog.com (Search) ADuM1250 (Go)
[6] ADI website: www.analog.com (Search) ADuM1251 (Go)
[7] ADI website: www.analog.com (Search) AN-913 (Go)
[8] ADI website: www.analog.com (Search) comparators (Go)
[9] www.analog.com/Analog_Root/static/pdf/dataConverters/SelectionGuides/Isolators.pdf

THE AUTHOR

Jerome Patoux [jerome.patoux@analog.com] is a field applications engineer for Analog Devices in Antony, France. In 2002, he graduated from ESIGETEL, France, with a master's degree in electronics and telecommunications engineering. He also has a master's degree in international project management from the University of Quebec in Hull-Gatineau, Canada, and ISMANS, Le Mans, France. Prior to joining ADI in 2005, Jerome worked as a radio engineer for SFR Group and as a department manager for SNCF.

Analog-to-Digital Converter Clock Optimization:

A Test Engineering Perspective

By Rob Reeder, Wayne Green, and Robert Shillito

System clock optimization can be both challenging and rewarding. It may be relatively easy to design an analog-to-digital converter *encode* circuit with a respectable 350 femtoseconds (fs) of jitter, but is this adequate for today's high speed requirements? For example, when testing an AD9446-100[1]—a 16-bit, 100-MHz ADC—at Nyquist with a 100-MHz sample clock, 350 fs of jitter can degrade the signal-to-noise ratio (SNR) by about 3 dB. When the same device is tested at the 3rd Nyquist zone with a 105-MHz analog input, the degradation can be as much as 10 dB. To reduce the clock jitter to a more tolerable 100 fs or less, the designer needs to understand where the clock jitter is coming from, as well as how much jitter the ADC can tolerate. It can be quite discouraging to realize—too late—that the clock-circuit performance is jitter-limited, and that this problem could have been more easily prevented during the design phase.

We will consider here the relevant clock specifications and means of achieving the expected performance of a high speed converter—employing a little know-how and experience. Starting with a typical ADC clocking scheme, such as that shown in Figure 1, we will highlight techniques that can be used to optimize the clock at each point in the signal chain—and identify some commonly used techniques that should be avoided.

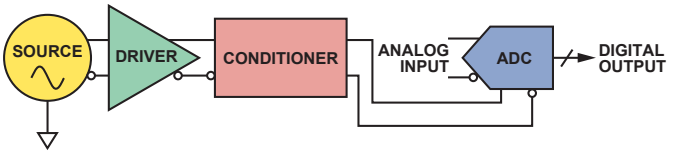

Figure 1. Typical clock signal chain.

What Is Jitter?

Jitter is probably the most important parameter in developing a good system clock circuit, so it is important to review some basics and understand what is meant by the term. Many technical papers describe the mathematics of jitter to the *n*th degree; however, design for good converter performance is not all about the exact description of jitter. One must also understand how it can get into the system and how to minimize its impact.

Jitter is variation in the placement of a clock edge; it will produce a timing error, leading directly to errors in conversion amplitude accuracy (Figure 2a). Increasing the analog input frequency increases the slope of the input signal, which magnifies the conversion error (Figure 2b). It is important to note that the magnitude of the conversion error is relative—a 0.5-LSB (least-significant-bit) conversion error for a 10-bit device is the equivalent of 32 LSBs of error for a 16-bit device. This means that jitter becomes more of a concern as both ADC resolution and analog input frequency increase.

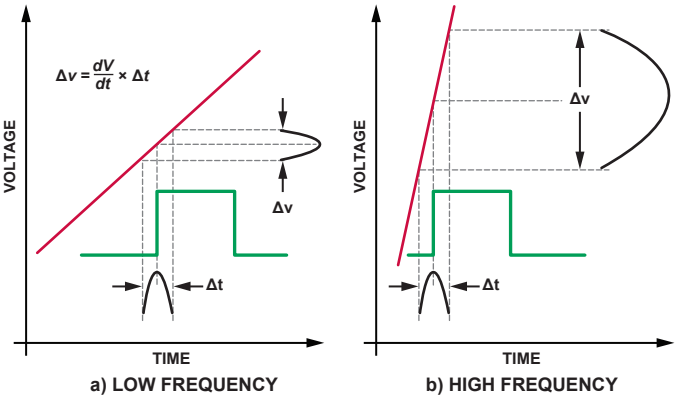

Figure 2. Conversion error as a function of clock jitter and analog input frequency.

Since this relationship is intuitively obvious, the engineer will ultimately determine how much jitter is acceptable by relating the ADC's performance to the jitter of the *encode* clock. Equation 1 defines the SNR (dB)—with frequency—of a perfect ADC having infinite resolution, while Equation 2 is the SNR (dB) of a perfect ADC with *N*- (10, 12, 14, or 16) bit resolution.

$$SNR_{ideal} = 20\log_{10}\left[\frac{1}{2\pi f t_{jitter}}\right] \quad (1)$$

(see diagonal lines of Figure 3)

$$SNR_{bits} = [6.02N + 1.76] \quad (2)$$

(see horizontal lines of Figure 3)

Figure 3 combines these two equations. The intersections allow the user to determine the amount of total clock jitter that can be tolerated for a given analog input frequency. At low frequencies, the accuracy is limited by the resolution of the converter. As the input frequency increases, however, a point is reached beyond which the performance of the ADC is dominated by the total clock jitter of the system. For input frequencies to the left of the intersections, lower jitter is unlikely to be of concern.

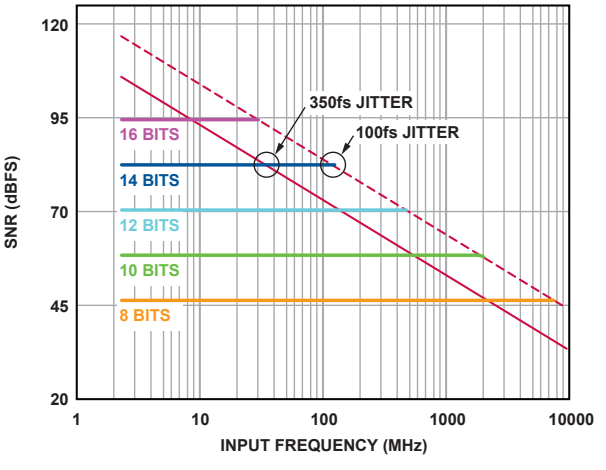

Figure 3. SNR of an ideal ADC vs. analog input frequency and jitter.

If the analog input frequency is near or to the right of an intersection, however, the frequency or resolution must be reduced—or the jitter specification must be improved. Thus, as the jitter intervals increase, the point where the SNR performance is dominated by the clock system jitter occurs at ever-lower frequencies.

For example, if a 14-bit ADC is tested using a clock that has 350 fs of jitter, the analog input frequency must be limited to frequencies below 35 MHz (the intersection of the 14-bit level and the 350 fs slope) to avoid significantly reduced performance. If the jitter can be reduced to 100 fs, input frequencies as high as 125 MHz can be handled.

In practice, this simplified model, using these first-order approximations, loses validity as the analog test frequency approaches the intersections. In order to fully understand the effect that clock jitter has on the ADC's performance, the *quantization noise and analog input amplitude* need to be considered in addition to the resolution (Equation 3, based on Further Reading 9).

$$SNR = -20\log_{10}\sqrt{\underbrace{(2\pi f_a\ t_{j\ rms})^2}_{\text{SAMPLE-CLOCK JITTER}} + \underbrace{\frac{2}{3}\left(\frac{1+\varepsilon}{2^N}\right)^2}_{\text{QUANTIZATION NOISE, DNL}} + \underbrace{\left(\frac{2\sqrt{2}\,V_{NOISE\,rms}}{2^N}\right)^2}_{\text{EFFECTIVE INPUT NOISE}}} \quad (3)$$

where

SNR = Signal-to-noise ratio in dB.
f_a = Analog input frequency of full-scale sine wave.
$t_{j\ rms}$ = Combined rms internal ADC jitter and external clock jitter.
ε = Average differential nonlinearity (DNL) of the ADC in LSBs.
N = ADC's resolution in bits.
$V_{NOISE\ rms}$ = Effective input noise of ADC.

If $t_{j\ rms} = 0$, $\varepsilon = 0$, and $V_{NOISE\ rms} = 0$, the above equation reduces to the familiar

$$SNR = 6.02N + 1.76\text{dB}$$

For example, assume that an ADC has 0.5-LSB quantization noise and that, when tested, the analog input amplitude will be 0.5 dB below full scale. Figure 4, combining Equation 2 and Equation 3, shows that the encode clock jitter will affect the SNR performance at lower frequencies than in the simplified model.

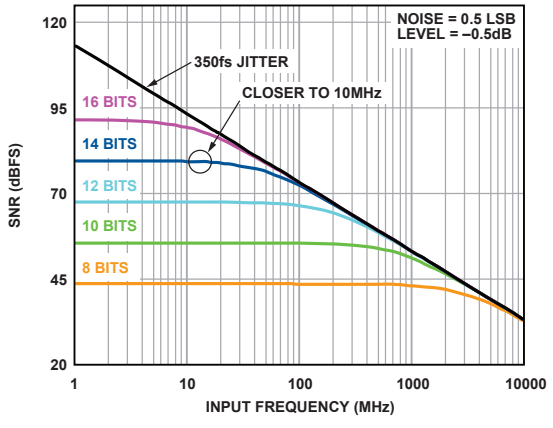

Figure 4. SNR as a function of analog input frequency, clock jitter, and quantization noise.

The earlier example showed that a clock with 350-fs jitter would not affect the SNR of a 14-bit ADC until analog input frequency approached 35 MHz. However, when the effects of quantization noise, input frequency, and input amplitude are considered, input frequencies as low as 10 MHz should be of concern. Likewise, 100 fs of jitter on the clock will also cause SNR degradation at frequencies lower than 100 MHz.

Keeping the Jitter Out

Now that the basics of jitter have been reviewed, we can consider sources of jitter. Anything that can modulate the edge transition of the ADC's clock will introduce or affect jitter. These include crosstalk, EMI (electromagnetic interference), ground effects, and supply noise.

Crosstalk-induced jitter can occur in any two adjacent traces. If one trace carries a signal, and a nearby parallel trace carries a varying current, a voltage will be induced in the signal trace; if it is a clock signal, the time at which the clock edge occurs will be modulated.

Jitter can also be induced by *EMI* radiation on sensitive signal traces. EMI is produced by switching power supplies, high-voltage power lines, RF signals, and other similar sources. EMI produces similar effects to crosstalk by means of electrical or magnetic coupling that modulates the signal or clock timing.

Figure 5 illustrates the effects of electromagnetic interference on SNR. The blue curve represents the baseline SNR-vs.-frequency of the AD9446, with an external clock and a linear power supply. The clock is not otherwise attached to the evaluation board in any way. The red curve shows the degradation that occurs when the same clock circuit is fixed or soldered onto the board, which is powered by a switching power supply. The green curve shows that substantial improvement in the converter's performance can be obtained if the oscillator is choked and filtered off this supply.

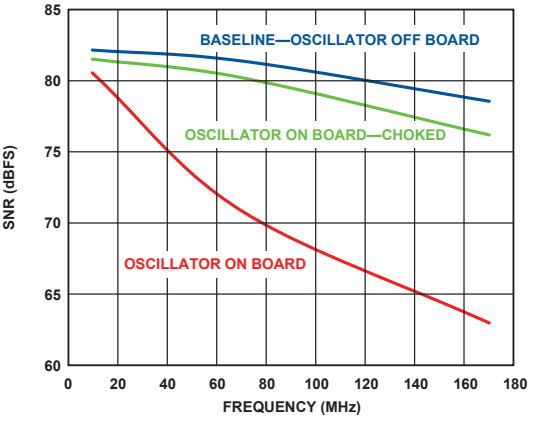

Figure 5. Converter performance vs. oscillator supply configuration and frequency.

Bouncing grounds due to switching currents or improper ground connections can also bring about jitter. Switching currents can become large when many gates are switching at the same time. This can induce current spikes on power and ground planes, level-shifting the threshold voltages on clock-circuit or analog-input signals. Consider the following example:

> Assume a gate output has a 10-pF combined load from the PCB trace and input of the receiver gate. When the gate switches, 10 mA of dynamic current can flow into or out of each output. [10 mA is derived from 10 pF × 1 V/ns, the typical slew rate of a CMOS gate ($I = C\,dV/dt$).] A midscale transition could thus account for 120 mA of dynamic current if 12 gates are switching simultaneously. This would cause a large current spike to be drawn through the supply leads, one of which may be ground. The transient voltage drop (bounce) due to the lead resistance will affect all circuits that rely on it to be at ground potential.

To diminish the jitter caused by these sources, good layout practices and proper circuit partitioning should be employed. It is essential to restrict analog circuits and digital circuits to their respective domains! This principle should be observed on every

layer to ensure good isolation. It is important to understand how return currents flow relative to their source, and to avoid any encroachments or crossovers between analog and digital circuitry. In summary, sensitive analog inputs and clock traces must be kept away from other circuitry and traces that can influence them in undesired ways.

Improving Jitter Means Improving Slew

Now that the basics of jitter and its possible deleterious influences have been covered, one might ask, "How do I make improvements to my system clock or clock circuit so as to reduce jitter?"

Recalling the initial discussion, jitter or noise can only corrupt the ADC's timing when present during the transition or threshold period of the clock, shown in Figure 6. Making this edge (and hence the threshold period) faster by increasing the slew rate will inevitably lessen the amount of time that noise can be present during the threshold period and effectively lessen the amount of rms (root-mean-square) jitter introduced to the system.

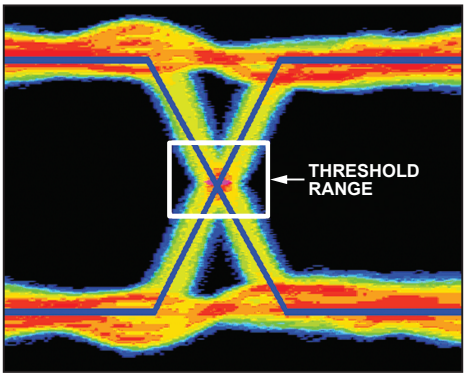

Figure 6. Expanded view of the threshold/transition region of a differential clock.

Keep in mind that increased slew rate doesn't affect the original signal quality, only the transition time through the threshold region. To confirm this statement, refer to Figure 2b. Notice that with this faster signal swing, less time is spent in the transition region. Figure 7 illustrates the inverse relationship between jitter and slew rate. Relating this to the earlier example, a 12-bit ADC requiring 100-fs minimum rms jitter for a 70-MHz analog input requires a slew rate of 1 V/ns.

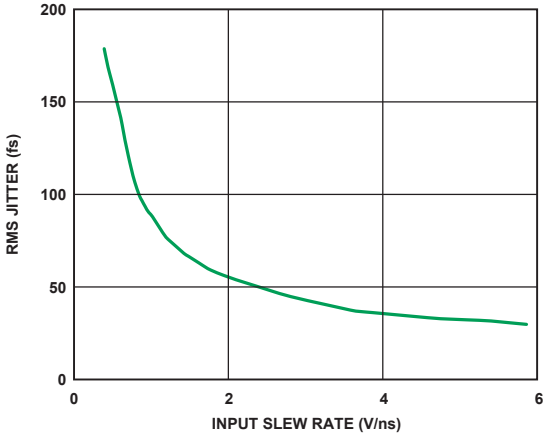

Figure 7. RMS jitter vs. slew rate.

Thus, minimizing jitter means improving the slew rate of the clock edge. One way this can be done is to improve the clock source itself. Figure 8 compares a number of different "off-the-shelf" oscillators when used as a clock source for one of ADI's highest performing ADCs, the 16-bit, 80-MSPS AD9446, over a range of analog input frequencies.

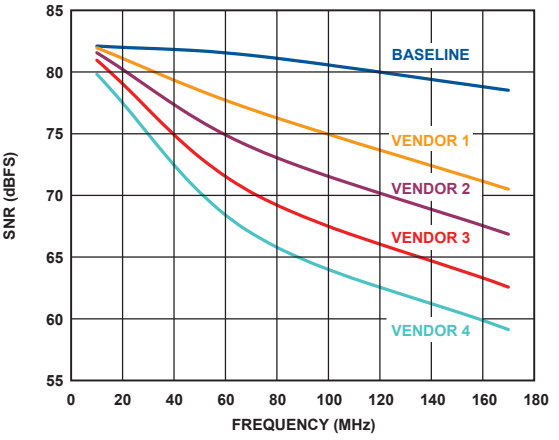

Figure 8. AD9446-80 performance is affected by the choice of oscillator source.

Typically, a custom high-performance clock oscillator is used to characterize the baseline performance achieved by Analog Devices ADCs (blue trace). Not all users of these high-speed converters can afford the cost or space required by a high-performance, oven-controlled, low-jitter oscillator, however, but available cost-effective oscillators can achieve reasonable performance, even at high analog input frequencies. Figure 8 shows the range of performance with some affordable devices.

An important point is that care should be taken when selecting an "off-the-shelf" oscillator, since oscillator vendors do not all tend to specify or measure jitter in the same way. A pragmatic way to determine which oscillator is best for the particular application is to collect a handful and test them in the system directly. By making this choice the only variable, a prediction of performance can be made (assuming that the oscillator vendor maintains reasonable standards of quality control). Better yet is to contact the oscillator manufacturer to obtain jitter- or phase-noise data, and get suggestions as to how to best terminate the device. Improper oscillator termination can seriously degrade the converter's spurious-free dynamic range (SFDR).

Further Improvements

If the best oscillator available, based on price and performance, is still not adequate, one might consider using frequency division and/or filtering. Equation 4 describes the output of a sine-wave oscillator:

$$V(t) = A\sin 2\pi ft \tag{4}$$

Two parameters affect the slew rate—signal frequency (f) and amplitude (A). Increasing either of these will increase the slew rate and reduce the system clock jitter to a more desirable number. It is generally easier to increase the clock frequency. Frequency division will then be used to produce the desired converter clock rate, as well as to feed the other stages in the system clock tree.

Frequency dividers do add cost in terms of circuit components and power requirements. They also add jitter. Each active component added to the clock signal chain will increase the total jitter.

$$j_{total} = \sqrt{j_{source1}^{\ 2} + j_{source2}^{\ 2} + \ldots j_{source\,n}^{\ 2}} \tag{5}$$

When using a divider, all the relevant specifications must be considered. Typical among ADI's clock-divider products is the AD951x[2] family, which typically add only about 250 fs. In addition to having the dividing function built right in, features such as clock distribution and duty-cycle control are also available.

It is worth noting that clock dividers must contribute, however minimally, to the overall jitter on an absolute basis; but because of the frequency reduction they provide, their output jitter becomes a smaller fraction of the output period, and thus introduces less error. For example, if a 100-MHz clock source and other members of the chain contribute 800 fs of jitter (about 12.5% of the 10-ns period), and a clock divider reduces the frequency to 10 MHz, while introducing 250 fs of jitter, the resulting 840 fs of jitter is less than 1% of the 100-ns output period.

As a consequence of Equation 5, since the largest contributor dominates the overall jitter, the maximum jitter of the clock source should be no more than one-third of the largest contributor, but not necessarily a great deal less. The actual choices depend on the application's performance requirements—such as for SNR over a given frequency range—the characteristics of available system components, and the usual limitations of size and cost.

Reducing Phase Noise

As Equation 5 indicates, *total* jitter is the root-sum-square (RSS) of the jitter from the clock cleanup circuitry, as well as the jitter in the source and any other intervening components. Thus, if the divider circuit is driven by an extremely noisy source, the full potential of the divider circuit may not be fully realized, simply because the largest jitter term dominates the equation. In this situation, consider using a passive, narrow-band *filter* between the clock source and the divider circuit.

To illustrate the advantages of filtering, consider a source having a jitter specification of 800 fs. If a clock divider circuit is placed between the source and the converter, the jitter can be reduced to roughly 500 fs even though the divider circuit is capable of much better performance. However, by placing a 5% LC band-pass filter between the source and divider circuit the jitter can be reduced to 250 fs. (See Figure 9).

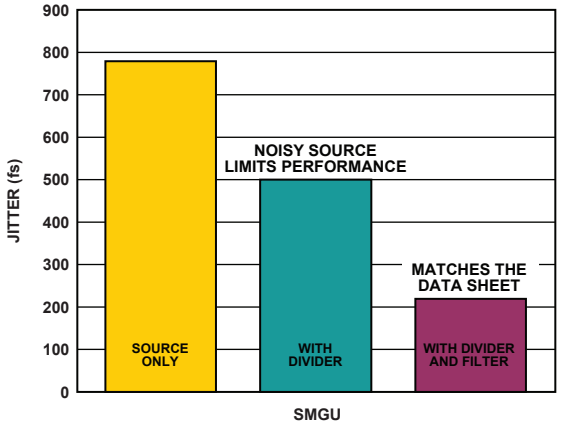

Figure 9. Jitter reduction with clock division and filtering.

In order to understand how a filter can improve the jitter of a sinusoidal source, it can be useful to think of jitter in the frequency domain and estimate its value from a phase-noise plot. Although the calculation is straightforward and provides a good method of comparison, it doesn't take into account nonlinear factors such as slew rate. As a result, this model will often predict more jitter than is actually present.

To perform the calculation, the phase-noise plot is divided into frequency regions, and the integrated noise power of each region is calculated, as shown in Figure 10. This permits identification of the jitter contribution from each region, as well as the total jitter of the source (by RSS summation). For these equations, f_0 is the carrier frequency. The integrated phase noise is multiplied by the square root of 2 because the plot represents one of the two sidebands.

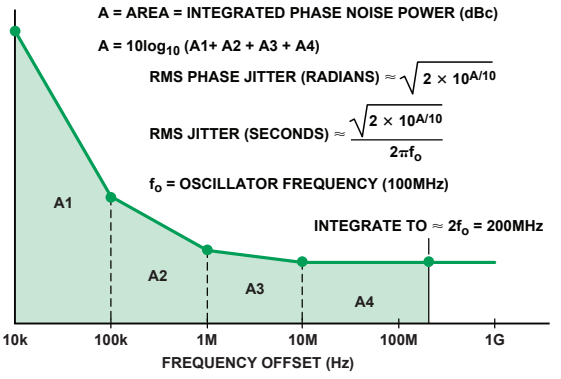

Figure 10. Calculating jitter from phase noise.

Consider now a source with 800-fs jitter. Plotting the phase noise of the source (Figure 11) makes it easy to determine where in the frequency domain most of the jitter is coming from. In the case of the clock with 800-fs jitter, it can be seen that the dominant part of the jitter in the spectrum is wideband. Therefore, emphasis in reducing wideband noise is paramount in sampled-type systems.

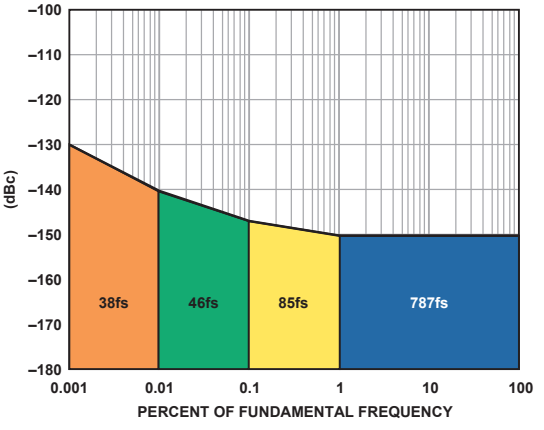

Figure 11a. Phase-noise plot of an 800-fs source.

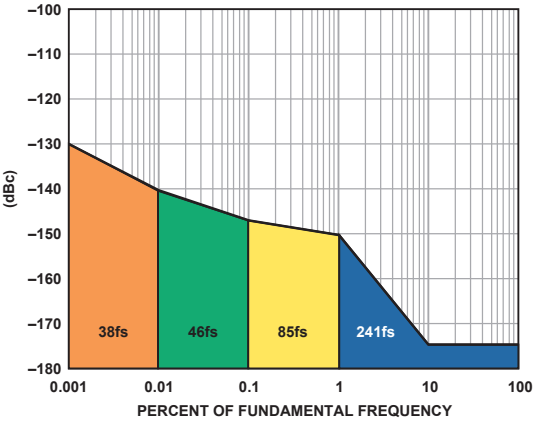

Figure 11b. Phase noise of the 800-fs source with a band-pass LC multipole filter with a 5% pass band applied.

The use of a simple band-pass LC multipole filter with a 5% pass band (5% LCBP) on the output of the clock source can greatly improve the performance, as shown in Figure 11b. Note the improvement from 800 fs to less than 300 fs. That corresponds to an SNR improvement of over 12 dB.

Five-percent LCBP filters can be easily obtained, but they can be big and expensive. An alternative is to use a crystal-type filter. Figure 12 shows the improvement in phase noise from 800 fs to less than 100 fs. This represents an additional 3-dB improvement over the 5% LCBP filter's 12 dB, for a total of 15 dB!

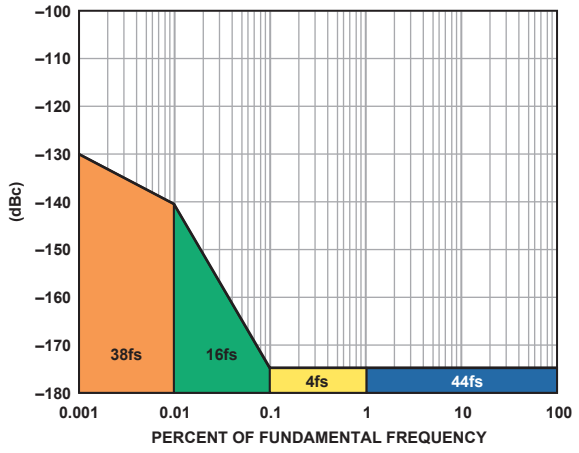

Figure 12. Phase-noise of an 800-fs source with a crystal filter.

To demonstrate the effectiveness of cascading crystal filters with a noisy source, an experiment was performed using an old benchtop pulse generator to clock the 16-bit, 100-MHz AD9446-100 ADC. Unfiltered, the generator exhibited greater than 4 ps of jitter, resulting in an SNR degradation of over 30 dB. With the crystal filter applied the calculated jitter was close to 50 fs, providing an improvement in SNR approaching data-sheet typical performance (Figure 13).

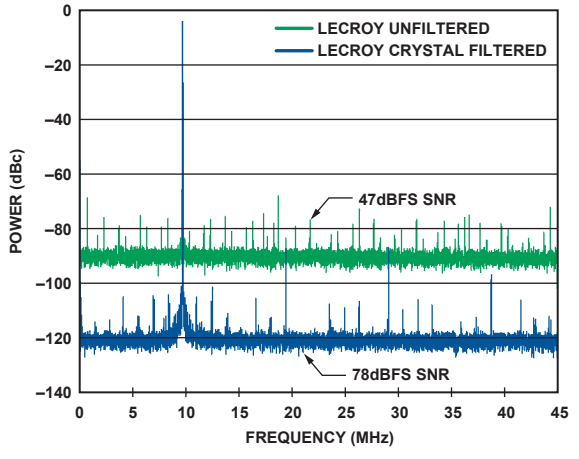

Figure 13. Crystal filters are helpful—even with noisy sources.

Crystal filters, with their very narrow pass-band region—usually <1%—can reduce jitter from many sources to less than 100 fs, but they add expense and are bulkier than active filters. It is also worth noting that crystal filters have a limited input/output range of 5 dBm to 10 dBm. Pushing them beyond their specified range will result in distortion, possibly degrading the ADC's SFDR. Finally, some crystal filters may require external components for impedance matching. Filters can do the job, but they require additional parts, tricky matching, and extra cost.

A quick summary of divider and filter solutions to improve the slew rate is shown in Table 1.

It is desirable to clip the signal before it approaches the ADC clock inputs using back-to-back Schottky diodes. This allows the source amplitude to be increased, thus increasing the slew rate, yet keeping the clock's amplitude at a level compatible with the converter's clock inputs.

If the clocking system is small or the last stage has short trace lengths, consider using a transformer in concert with the clipping diode. The transformer is passive and won't add jitter to the overall clock signal. Transformers can also be used to provide gain for the oscillator's signal voltage, increasing the A term (amplitude) in Equation 4. Lastly, transformers inherently provide pass-band filtering. Those with gain (1:2 or 1:4 impedance ratios) have narrower bandwidth, providing even better filtering of the clock signal. Transformers can also convert that single-ended signal into a differential signal—common and highly recommended in today's ADC clock input interfaces.

Keep in mind that not all diodes will perform equally well (Figure 14). The "baseline" condition is the performance of the best-performing diode, relative to all the other diodes in this test batch, measured under the same conditions. Read the specifications carefully and pay particularly close attention to the dynamic resistance and total capacitance specifications. Diodes with low R and C values can improve clipping speed.

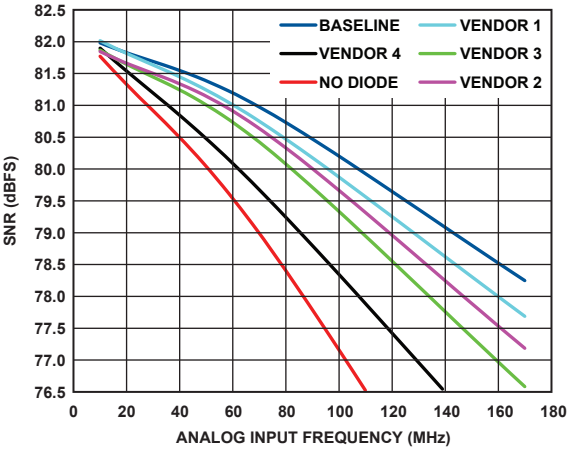

Figure 14. AD9446-80 performance is affected by choice of clipping Schottky diodes.

Table 1. Summary of Divider and Filter Trade-Offs

	Divider	5% LCBP Filter	Crystal Filter
Pros	• Low cost ($5 to $20). • High slew rate at low frequencies. • Can vary the duty cycle. • Clock distribution chips = more outputs available.	• With proper source, can achieve <100 fs jitter. • Short lead times. • High max input power.	• Ultralow jitter for all sources. • Very small (also available 50 Ω matched).
Cons	• Best case jitter ~ 200 fs to 250 fs.	• Encode limited to the pass-band frequency. • Duty cycle limited to 50%. • More expensive than dividers (~$300).	• Encode limited to the pass-band frequency. • Duty cycle limited to 50%. • Custom cost results in a 50% cost increase over LCBP.
Don't Forget	• For best performance, place a band-pass filter before the divider.	• Dividers can make matters worse. • Max output power is limited by filter insertion loss and max specified input power.	• Max output power is limited by filter insertion loss and max specified input power. • Request high max power when ordering custom filters.

Here the AD9446, 16-bit, 80-MSPS ADC was used as a test platform; the only change was in the source of back-to-back diodes. The circuit used for this evaluation is shown in Figure 15.

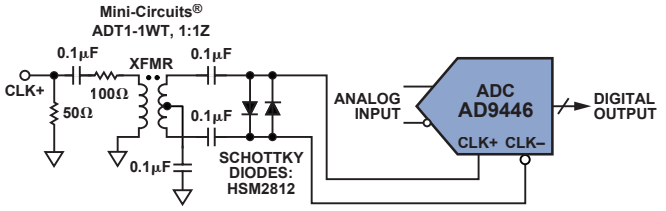

Figure 15. AD9446 clock circuit for data of Figure 14.

Jitter Reduction in Clock Hardware Interfaces

There are many circuits and solutions that can be used when interfacing to the ADC's clock input pins. However, a review of Equation 5

$$j_{total} = \sqrt{j_{source1}^{\ 2} + j_{source2}^{\ 2} + \ldots j_{source\,n}^{\ 2}}$$

reminds us that a valid expectation is that each active component (oscillator source, driver or fanout gate, divider, etc.) in the signal chain will increase the total amount of jitter presented to the ADC's clock input pins. Figure 16 shows that the addition of two gates, each contributing 700 fs of jitter, to a source with 300 fs of jitter can degrade resolution from about 12 bits to less than 10 bits at 140 MHz.

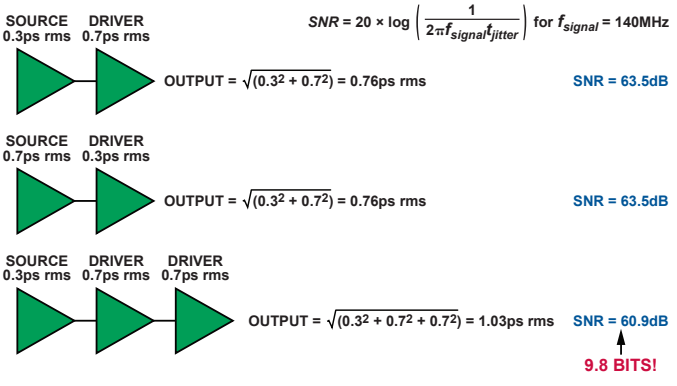

Figure 16. Multiple driver gates increase jitter and reduce SNR.

Thus, minimizing the number of components in the clock signal chain can help keep the total RSS jitter low.

The type of clock gates chosen is also worth noting. Simple logic gates are probably not the best choice when seeking to obtain good performance at high analog input frequencies. It is best to carefully read the data sheets of candidate devices and understand the pertinent specifications, such as jitter and skew. This is especially important when they are to work with sources that have extremely low jitter. For example, in Figure 17, Source A has 800 fs of jitter and Source B has 125 fs of jitter. With a crystal filter, the respective jitter levels can be reduced to 175 fs and 60 fs. However, a divider (or a gate with comparable jitter specifications) can increase the jitter to above 200 fs in both cases. This underscores the fact that proper selection and placement of clock drivers in the clock signal chain is important.

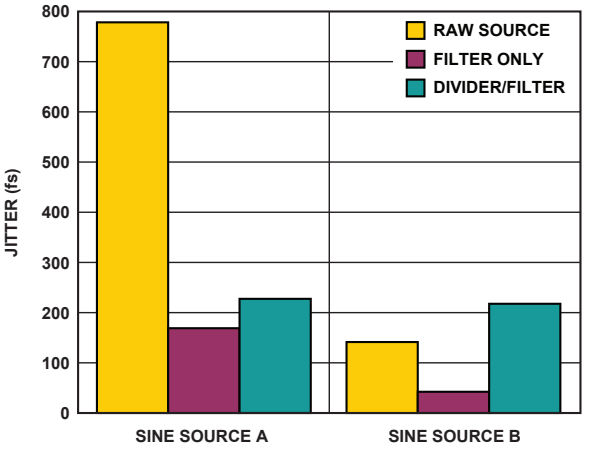

Figure 17. Gates will add jitter.

Another common approach leads to manifest inability to achieve data sheet performance. A flexible gate driver can be achieved fairly simply using an FPGA (often with a *digital clock manager*—DCM, which provides clock division). However, as Figure 18 shows, this approach has huge costs in degradation of SNR using the AD9446-80 (80-MSPS ADC); capable of achieving 13 bits ENOB, for example. The high-performance oscillator establishes the baseline SNR performance over a range of frequencies, as shown by the red curve. The green curve shows the difference in performance using the same clock, but with an FPGA as the gate driver between the high-performance oscillator and the converter. At 40 MHz, the FPGA reduces the SNR to 52 dB (8.7-bit performance) while the DCM contributes an additional 8-dB (1.3-bit) reduction of SNR. That performance difference is pretty alarming with 29-dB degradation in SNR, which means that the FPGA driver gate alone has an additive jitter of roughly 10 ps using Equation 1!

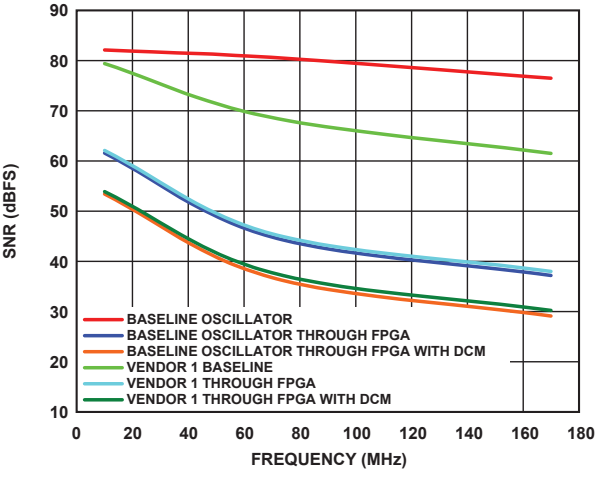

Figure 18. AD9446-80 performance is affected by FPGA gate drive circuits.

Choosing the best clock driver gate can be difficult. Table 2 gives a rough comparison of the additive jitter of a number of driver gates on the market. The suggestions on the lower half of the table may be helpful in attaining good ADC performance.

Table 2. Summary of Clock-Driver Gates and Their Additive Jitter

Logic Family	Comments
FPGA	33 ps to 50 ps (driver gates only, not including internal gates of DLL/PLL)[1]
74LS00	4.94 ps[2]
74HCT00	2.2 ps[2]
74ACT00	0.99 ps[2]
MC100EL16 PECL	0.7 ps[1]
AD951x Family	0.22 ps[1]
NBSG16, Reduced Swing ECL (0.4 V)	0.2 ps[1]
ADCLK9xx, ECL Clock Driver Family	0.1 ps[1]

[1]Manufacturer's specification.

[2]Calculated value based on degradation of ADC SNR.

CONCLUSION

It is critical to understand the entire clock system in order to achieve the best possible performance of the converter. Figure 3 and Equations 1 and 2 are helpful guides to clock requirements for applying either a jitter-limited ADC having very high resolution or a "perfect" N-bit ADC. If the analog input frequency is not well below the intersection of these lines, one must consider a clock source and associated circuitry with reduced jitter.

Decreasing the jitter of the system clock circuit can be achieved in many ways, including improving the clock source, filtering, and/or frequency-dividing, as well as proper choice of clock circuit hardware. Remember to pay attention to the slew rate of the clock. This will determine the amount of noise that can corrupt the converter during the transition time. Minimizing this transition time can improve the converter's performance.

Use only necessary circuitry to drive and distribute the clock because each component in the signal chain will increase the overall jitter. Finally, don't use "cheap" hardware gates; their performance is likely to be disappointing. One can't expect championship performance from a $70,000 car outfitted with $20 tires.

FURTHER READING

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ACKNOWLEDGEMENTS

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[1]ADI website: www.analog.com (Search) AD9446-100 (Go)
[2]ADI website: www.analog.com (Search) AD951x (Go)

THE AUTHORS

Rob Reeder [rob.reeder@analog.com] is a senior converter-applications engineer working in the High-Speed Converter Group in Greensboro. He has published numerous papers on converters and converter testing. Formerly, Rob was a designer for ADI's Multichip Products group, designing converter modules for space- and military applications. Rob received his MSEE and BSEE in 1998 and 1996, respectively, from Northern Illinois University in DeKalb, IL. In his spare time he enjoys mixing music, art-airbrushing, and building Hot Wheels® race tracks with his two boys.

Wayne Green [wayne.green@analog.com] works as a test development engineer for the High-Speed Converter Group in Greensboro. Wayne has developed test solutions for digital-to-analog converters, high-speed comparators, pin drivers, and high-speed analog-to-digital converters. Currently his development work involves test solutions for ADI's family of multichannel, multiresolution, ultrahigh-speed ADCs.

Robert Shillito [robert.shillito@analog.com] is a product-test development engineer with the High-Speed Converter Group in Greensboro. In June 2006, he joined Analog Devices—after graduating from North Carolina State University with a BSEE. He primarily works with 12- and 14-bit high-performance ADCs, with speeds ranging from 50 MSPS to 250 MSPS.

High-Side Current Sensing: Difference Amplifier vs. Current-Sense Amplifier

By Henri Sino

Accurate high-side current sensing is necessary in many applications, including motor control, solenoid control, and power management (for example, dc-to-dc converters and battery monitoring). In such applications, monitoring of current on the high side—instead of the return—permits improved diagnostic capabilities, such as determining shorts to ground and continuous monitoring of the recirculation-diode current—and maintains the integrity of the ground path by avoiding the introduction of shunt resistance. Figures 1, 2, and 3 depict typical high-side current-shunt configurations for solenoid- and motor control.

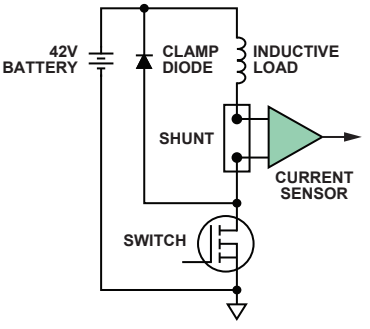

Figure 1. High-side shunt in typical solenoid control.

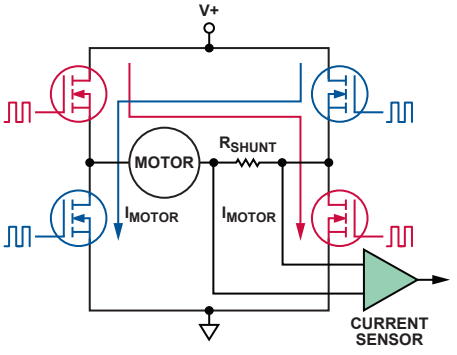

Figure 2. High-side shunt in H-bridge motor control.

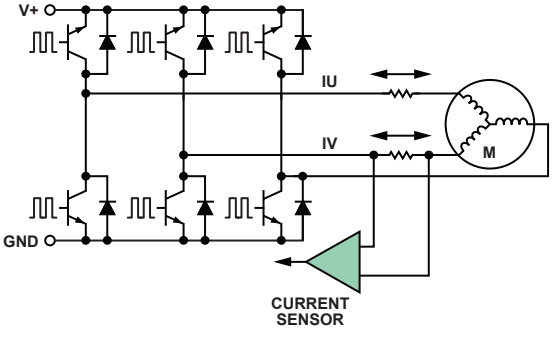

Figure 3. High-side shunts in 3-phase motor control.

In all configurations shown above, the *pulse-width-modulated* (PWM) common-mode voltage at the shunt resistor—which monitors the load current—is swinging *over the whole range* from ground to battery. This PWM input signal will have a period, frequency, and rise/fall time established by the control signal from the power stage to the FET. Therefore, the difference-measurement circuitry that monitors the voltage across the shunt resistor will require the stringent combination of very high common-mode rejection and high-voltage handling capability, plus high gain, high accuracy, and low offset—all in order to deliver a true representation of the load-current value.

In solenoid control[1] (Figure 1) that uses a single control FET, the current is always flowing in the same direction, so a unidirectional current sensor will be sufficient. In motor-control configurations (Figures 2 and 3), placing the shunt on the motor phase means that current in the shunt resistor could flow both ways; therefore, a bidirectional current sensor is necessary.

The designer who studies the choices for the high-side current-sensing function will find a variety of options from many semiconductor vendors. However, a key finding will be that the choices among these integrated-circuit devices can be classified in terms of two quite different high-voltage architectures: *current-sense amplifiers* and *difference amplifiers*.

We will identify and explain here some of the key differences between these architectures to help the designer in need of high-side current sensing to choose a device best-suited to the application. We will compare two high-voltage parts, the AD8206[2] bidirectional difference amplifier and the AD8210[3] bidirectional current-sense amplifier. Both devices offer the same pinout, and both perform high-side current-shunt monitoring, yet their specifications and architectures are different. So, how does one consider which device is best-suited for the application?

HOW THEY WORK

The AD8206 (Figure 4), an *integrated high-voltage difference amplifier*, withstands common-mode voltages up to 65 V by using input resistors to attenuate the input voltage by 16.7:1 so as to keep the common-mode voltage within the input range of amplifier A1. Unfortunately, the input resistance network also attenuates the differential signal by the same value. To achieve the AD8206's featured gain of 20 V/V, amplifiers A1 and A2 must actually amplify the differential signal by approximately 334 V/V.

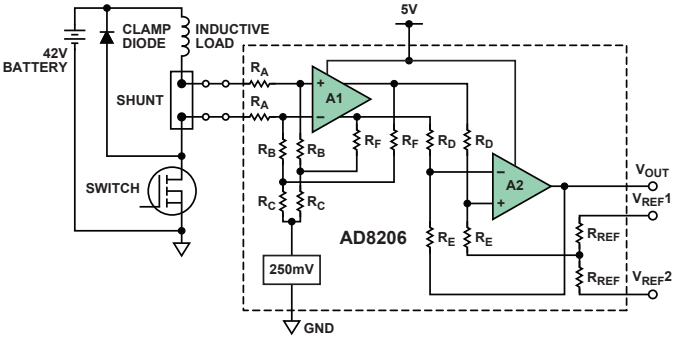

Figure 4. AD8206 simplified schematic.

This device implements bidirectional input measurements by offsetting the output amplifier to a suitable voltage within the supply range. The offset is achieved by applying an external low-impedance voltage to a precisely trimmed resistance divider connected to the positive input of A2. A useful feature of this device is its ability to correctly amplify the differential input voltage when the common-mode voltage goes *negative* by as much as 2 V—a consequence of the 250-mV common-mode bias circuit shown in the figure.

The AD8210 (Figure 5), a recently introduced *high-voltage current-sense amplifier*, offers the same functional relationship as the AD8206 and uses the same pin connections. However, it works in a different way, and the resulting specifications are unlike those of a difference amplifier.

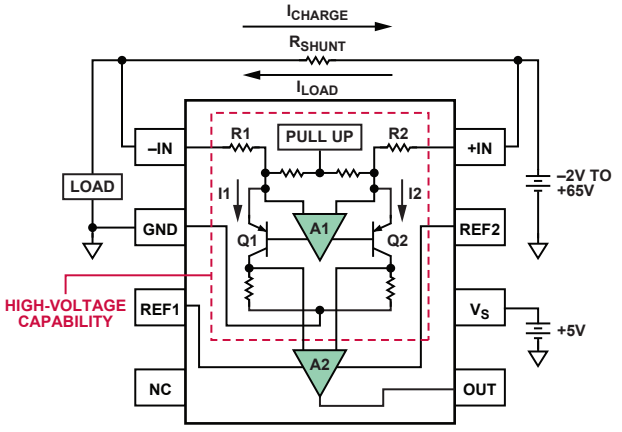

Figure 5. AD8210 functional diagram.

An obvious distinction is that the input structure does not rely on a resistive attenuation network to deal with the large common-mode voltage. The input amplifier comprises high-voltage transistors, available on the XFCB IC fabrication process. Because the V_{CE} breakdown of all transistors exposed to this voltage is beyond 65 V, the common-mode voltage at the input can be as great as 65 V.

Current-sense amplifiers such as the AD8210 amplify the small differential input voltage in the following manner. The input terminals are connected to the differential amplifier, A1, by R1 and R2. A1 nulls the voltage appearing across its own input terminals by adjusting the current through R1 and R2 with transistors Q1 and Q2. When the input signal to the AD8210 is 0 V, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal. The differential currents through Q1 and Q2 are converted to a ground-referenced differential voltage via two internal precision-trimmed resistors. This voltage can then be amplified by amplifier A2, this time using low-voltage transistors powered by the device's 5-V (typically) supply, to produce the final output with an overall gain of 20.

Current-sense amplifiers with this architecture are generally useful only if input common-mode voltage remains above 2 V or 3 V, and if the application doesn't require that the input common-mode voltage go all the way to ground (or below). However, the AD8210 uses a pull-up circuit to hold the inputs of amplifier A1 near the 5-V power supply, *even when the input common-mode drops below 5 V*, and all the way down to –2 V. Thus, accurate differential input-voltage measurement is possible at common-mode voltages well below the device's 5-V supply.

It is apparent that current-sense amplifiers and difference amplifiers perform the same function while operating quite differently. A difference amplifier attenuates high input voltages to bring the signal to a level the amplifier can tolerate. A current-sense amplifier converts the differential input voltage to a current, and then back to a ground-referenced voltage; its input amplifier is able to withstand large common-mode voltages due to its high-voltage manufacturing process. The disparity between the two architectures naturally leads to performance differences that designers must consider when choosing a high-side current-monitoring solution. Manufacturers' data sheets typically provide most of the information needed to make the right judgment on which type of device to use, based on accuracy, speed, power, and other parameters. However, some key differences inherent in device architecture are not immediately obvious when reading a data sheet, yet they can be essential design considerations. The following are key points engineers must be aware of to arrive at the best solution.

Bandwidth: Because of the input attenuation, the bandwidth of many difference amplifiers is typically about one-fifth that of current-sense amplifiers. However, the lower bandwidth of the difference amplifier is still sufficient for most applications. For example, many solenoid-control applications run at less than 20 kHz, but motor control typically must run at or above 20 kHz due to noise considerations. Solenoid control typically involves looking at the *average* current, an application for which the bandwidth of difference amplifiers is well suited. For motor control, on the other hand, *instantaneous* current is key, especially when measuring on the motor phase; therefore, the current-sensor architecture, with its higher bandwidth, will yield a truer representation of the actual motor current.

Common-Mode Rejection: The difference in the input structure between these two architectures also leads to a difference in CMR performance. The difference amplifiers typically have trimmed input resistors with a tracking accuracy of 0.01%. This degree of matching typically results in a guaranteed 80-dB CMR at dc. The current-sense amplifiers, with their transistor input structure, can obtain a better match, so that CMR, no longer dependent on input resistor matching, can typically be specified above 100 dB, except at low values of common-mode voltage. For example, the AD8210 offers the same 80 dB as a difference amplifier when the input common-mode voltage is less than 5 V. At this voltage range, the input structure becomes resistive, due to the internal pull-up circuit mentioned above; so, the CMR once again becomes a function of the 0.01% precision-trimmed resistor matching. Over the whole range, though, the current-sense architecture will offer better common-mode rejection.

Effect of External Input Filtering: If input filtering is to be used in a high-side current-sensing application, the architecture can be highly influential. An input filter, intended to smooth out effects of input noise and current spikes, is typically implemented as shown in Figure 6.

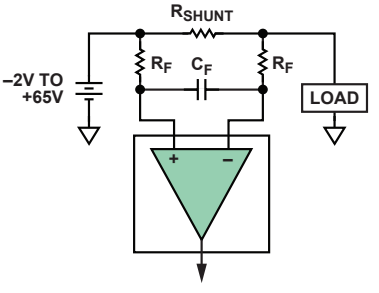

Figure 6. Input filter options.

Since each part, regardless of its architecture, has some trimmed input resistance, any external resistance added in series will produce mismatches leading to both gain- and CMR errors, typically calculated as follows (R_{in} is the specified amplifier input resistance):

$$Gain\ error\ (\%) = 100 - 100\frac{R_{in}}{R_{in} + R_F}$$

$$CMR\ error\ (\text{dB}) = 20\log\frac{R_F \times (R_F\ \%\ error) \times 2}{R_{in}}$$

The difference amplifiers have an input resistance greater than 100 kΩ. For the AD8206, where R_{in} = 200 kΩ, if a 200-Ω filter resistor is used, the additional gain error will be ~0.1%. The common-mode error due to these external components, assuming a 1% resistor tolerance, will be –94 dB, making its contribution irrelevant since it is essentially buried in the 80-dB specified CMR error of the device.

The current-sense amplifiers, while having much higher common-mode input impedance, feature input series resistors typically lower than 5 kΩ, in order to convert the differential input voltage into a current. For the AD8210, the equations above must be recalculated using R_{in} = 3.5 kΩ (differential input impedance). In this case, the additional gain error due to the filter resistors could be as high as 5.4%! Also, the CMR could drop down to 59 dB, assuming a worst-case external resistor mismatch. This is a major blow to performance for a device whose typical accuracy provides a maximum total error of less than 2%.

Therefore, care must be used when introducing input filters with *current-sense* architecture. Use a filter resistor that is less than 10 Ω when the internal resistance is 5 kΩ or less. This will ensure that the high original accuracy of the current-sense amplifier is maintained. As shown above, a wider range of input filter resistor values can be used with a *difference amplifier*, as the high value input resistors are less susceptible to external mismatching.

Overdriving the Inputs: In high-side current-sensing applications, the designer must carefully consider potential events that could cause the amplifier to operate outside of its specified range. In typical use, the inputs to the amplifier are meant to differ by only the few hundred millivolts caused by the flow of load current through the shunt resistor, but could the device survive fault conditions where several volts appear across the inputs? In such cases the difference amplifier architecture is inherently more robust and more likely to continue to function as expected once the system is back in order. The input resistor network can simply source the current to ground; at 65 V, the AD8206, with 200 kΩ per input, will have 325 μA flowing to ground.

If the current-sense architecture is used, the designer must be concerned with such potential problems. In the case of the first example, a device like the AD8210 would not be able to survive large voltage swings across the inputs. Such devices usually include an ESD protection diode between the inputs. This diode is forward-biased by a voltage difference greater than about 0.7 V. The actual breaking point of this diode varies, but large differential voltages, such as those available from an automotive battery, typically leads to damage to the device due to electrical overstress.

Negative Voltage Protection: In many cases it is necessary to protect the current sensor against reversed battery voltage, especially in automotive applications. The *difference amplifier's* resistance-bridge input is potentially an important survival factor. However, designers must check the device's absolute ratings to ensure that the input ESD diodes are also designed to turn on, but only at large negative voltages.

However, the *current-sense* architecture is not optimal in such cases because the input amplifier and its corresponding input transistors will be directly connected to the large negative voltage. Because the inputs should not be subjected to large negative dc voltage, the input ESD diodes of current sense amplifiers are typically designed to turn on just outside the specified low end of the input voltage range.

In addition to negative *dc* voltage, however, such current monitors can also be subject to *negative input transients*. This is typically the case in a PWM system, where the current-shunt monitor's input common-mode voltage swings from ground to battery as the control FET switches on and off. Again, it is essential to carefully consider the absolute maximum ratings, which are principally determined by the device's input ESD diodes. The difference amplifiers, as before, are protected by the high input resistance and are essentially impervious to the negative transients; therefore, the ESD diodes typically are designed to clamp at large negative voltages. But when the current-sense architecture is used, negative transients of even very short duration can trip the input ESD protection, which is designed to turn on at voltages close to the input common-mode rating of the device. Although such pulses typically do not carry enough energy to damage the ESD cells of the AD8210, performance in this regard will vary from device to device. To ensure that no complications arise, this parameter should be tested in the actual system.

Input Bias Current: In applications where power management is important and even small leakages must be considered, the differing input structures of the two architectures require that input bias current be considered. For example, in a battery-current sensing system, both architectures will monitor the current on the high side. However, when the system is *off* and the power supply to the current monitor is *off*, while the inputs are still connected to battery, the path to ground inherent in the resistive input network of a difference amplifier (like the AD8206) will require a bias current that continues to drain current from the battery. On the other hand, with their very high input common-mode impedance (>5 MΩ for the AD8210), devices using the current-sense architecture will not drain the battery current, since almost no current will flow via its inputs to ground.

CONCLUSION

High-side current sensing is a pervasive requirement in automotive, telecom, consumer, and industrial applications. Integrated high-voltage difference- and current-sense amplifiers are now offered in the marketplace to perform this function. Depending on the accuracy- and survival requirements in the application, systems engineers need to look carefully at which type of current sensor is best suited for their system. Typical considerations are summarized in the table below.

Both types of current monitors can do the job, yet the advantages offered by their different architectures are accompanied by distinct trade-offs. For instantaneous current monitoring, the wide bandwidth of current-sense amplifiers is most suitable, while applications monitoring average current can be easily served by a difference-amplifier topology. In addition, power-management applications sensitive to current consumption benefit by a current-sense amplifier with its minimal input power-off bias-current drain. However, the input structure of high-side current sense amplifiers may limit performance when implementing external filters and require careful scrutiny to ensure that their absolute input ratings are not exceeded in hostile application environments.

Features	Current-Sense Amplifiers	Difference Amplifiers
Speed is Ideal for Monitoring...	Instantaneous current	Average current
Input CMR (DC)	>100 dB	About 80 dB
Input CMR (PWM)	About 80 dB	About 80 dB
"Off" Input Bias-Current Consumption	Very low	Continuous leakage in input resistance divider
External Filtering	Primarily "post"	"Pre" or "post"
Input Stress Susceptibility	External stresses need careful consideration	Typically robust

REFERENCES—VALID AS OF JANUARY 2008

[1]www.analog.com/library/analogdialogue/archives/38-04/solenoids.pdf
[2]ADI website: www.analog.com (Search) AD8206 (Go)
[3]ADI website: www.analog.com (Search) AD8210 (Go)

THE AUTHOR

Henri Sino [henri.sino@analog.com] is an applications engineer in the Integrated Amplifier Products (IAP) Group at Analog Devices in Wilmington, MA. Henri has been with ADI for four years, since obtaining a BSEE from Worcester Polytechnic Institute. During his time at ADI, Henri has mainly focused on supporting products and customers relating to the automotive market.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA
02062-9106 U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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