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In This Issue

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ANALOG DEVICES

Editors' Notes

At the time of this writing, Dan Sheingold, our friend and colleague, and Editor of this publication, is home recuperating from a lower back injury. The staff and readers of *Analog Dialogue* want to extend our best wishes to Dan for his swift, easy, and complete recovery, and for his quick return to work. In the meantime, I hope that I have been able to adequately fill his rather large shoes over the past few months.

TECHNOLOGY AND HAPPINESS

In his 1902 lecture *On the Principles of Mechanics*, Ludwig Boltzmann responded to the question "Has mankind been made happier by all the advances in culture and technology?" by saying:

> Indeed, a ticklish question. Certainly a mechanism for making humans happy has not yet been invented. Each must seek and find happiness within himself. However, science and civilization have succeeded in eliminating influences disturbing happiness by overcoming the danger of lightning, national plagues, and illnesses of individuals in many cases. Furthermore, it has been made easier to journey over, and to come to know, our beautiful Earth, to imagine vividly the structure of the starred skies, and to glean dimly at least the eternal laws of Nature as a whole. In this way it [science] has allowed an ever greater development of the physical and mental powers of mankind and an ever-growing dominion over all the rest of Nature; and it has enabled those who found inner peace to enjoy it in a heightened unfolding of life and a greater perfection.

Although Boltzmann believed that people must seek happiness within themselves, he proposed that technology makes it easier by providing improved safety, better medical care, and easier methods of transportation.

With its integrated circuits, Analog Devices seeks to improve our quality of life and to protect our environment. In audio/video applications, for example, ADI's precision amplifiers, converters, digital signal processors, and MEMS devices allow viewers and listeners to experience vivid, lifelike pictures and sound from their high-definition home theater systems, cell phones, and automotive infotainment systems.

In automobiles, our devices enhance safety by implementing functions such as adaptive cruise control, advanced driver assistance, crash detection, electronic stability control, intelligent battery monitoring, navigation systems, remote keyless entry, and security systems.

In medical instrumentation, our analog, digital, and mixed-signal processing and MEMS technologies are delivering better resolution in MRI and CT scanners, lower power ultrasound systems, and more accurate and reliable home monitoring equipment.

In industrial applications, ADI's ICs are used to monitor and control solar and wind power systems, water desalinization plants, and nuclear power plants; and smart metering technologies result in more efficient energy utilization. In addition, each generation of devices consumes less power than the previous generation, contributing to a greener environment.

These are but a few examples of the wide variety of products that use Analog Devices' components. The average person might not buy our ICs, but they are likely to buy or use a piece of equipment that does, to gain the benefits of these devices, and, hopefully, to lead happier lives.

FEMTOCELLS, MULTIPLIERS, AND SHORT-RANGE WIRELESS

Imagine a device that can provide high-quality cellular reception within your home, allowing you and your family unlimited voice and data usage for a low monthly fee. A femto base station, usually referred to as a femtocell, provides all that and more. This small wireless device, which improves local wireless coverage when placed in a home or office, is poised to dramatically change the wireless infrastructure landscape. Read about femtocells in the article on Page 3.

Multipliers exploiting translinear loops, current mirrors, current conveyors, and linear g_m cells continue to be indispensable more than 60 years since the very first fully monolithic ICs were fabricated in 1967. In this futuristic tale, Drs. Newton Leif and Niku Chen discuss multiplier topologies, uses, and history. Leif also provides some hints as to how neurons, which are translinear, behave exactly like bipolar junction transistors. Consider multipliers when implementing your next design. Read more in the article on Page 8. In case you missed any of the earlier articles, the complete *Wit and Wisdom of Dr. Leif* series can be found in the *Analog Dialogue* online archives at www.analog.com/library/analogDialogue/archives.html#leif.

The broad acceptance of standards developed for short range wireless connectivity has been one of the notable features of the semiconductor market in the past few years. These standards include Bluetooth, various flavors of Wi-Fi, ZigBee, and new emerging standards, such as Wibree/Bluetooth ULP and Ultra Wideband. The available wireless standards are not always the best fit for the application's requirements, however. The article on Page 15 shows you how to design, simulate, and document your own proprietary wireless system.

PAST, PRESENT, AND FUTURE

Over the past year, *Analog Dialogue* articles have covered products and applications ranging from motor control to inductive cooking, from biometric identification to blood analysis, and from cell phone base stations to in-home femtocells. Over the next year, look forward to reading articles about smart metering technologies, MEMS microphones, industrial process control, base station power monitoring, and automotive video systems. As always, your comments and suggestions are welcome.

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Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 42 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. For history buffs, the *Analog Dialogue* archives include all regular editions, starting with Volume 1, Number 1 (1967), plus three special anniversary issues.

If you wish to subscribe to the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

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Analog Front End for 3G Femto Base Stations Brings Wireless Connectivity Home

By Thomas Cameron and Peadar Forbes

INTRODUCTION

Imagine a device that can provide high-quality cellular phone reception within your home, allowing you and your family unlimited voice and data usage for a low monthly fee. A femto base station, usually referred to as a femtocell, provides all that and more. This small wireless device, which improves local wireless coverage when placed in a home or office, is poised to dramatically change the wireless infrastructure landscape.

Figure 1 illustrates the femtocell concept. While traditional base stations provide wide area coverage, a femtocell provides wireless coverage in a small area such as a residence. The femtocell routes mobile traffic to the network through the user's broadband Internet connection, thus offloading traffic from the radio network. The femtocell improves the capacity of the network, while reducing backhaul, power, and maintenance costs for the operator. It also enables operators to compete for services in homes that have limited signal coverage. In exchange for a subsidized femtocell, the operator adds an additional fee to the customer's monthly cellular plan. When in the femtocell zone, all mobile usage would be covered under the home billing plan, allowing unlimited voice and data usage in the home without incurring large monthly bills. The proximity of the femtocell enables a high quality link, while simultaneously reducing handset battery usage. The femtocell overcomes the limitation of 3G signals from the base station to penetrate walls, enabling high-speed access to mobile data services such as browsing the Internet, downloading music, and streaming video on the handset.

The femtocell, similar to a Wi-Fi router, is based on proven wireless infrastructure standards (UMTS, CDMA). Compatible with emerging standards, it provides an efficient, robust wireless link using operator-owned spectrum. Compatibility with existing handsets makes the connection transparent to the user. Unlike a macrocell network, which aggregates tens or hundreds of base stations onto the core network, a femtocell gateway must manage thousands or even millions of femtocell nodes.

Femtocells, which must provide the quality of service (QoS) expected from a base station at a cost similar to a handset, present unique challenges to the radio designer. The femtocell must provide both high-quality voice service and high-speed mobile data services (EVDO and HSPA) at a fraction of the cost of a macronode. In order to meet these challenges, the femtocell design must take advantage of low-cost manufacturing techniques and highly integrated circuits that minimize calibration and test time. Femtocells reside in the home, so they must be small, low cost, and user installed. Transmitting at low power—on the order of 100 mW—femtocells must be aware of the wireless environment to mitigate interference and meet regulatory requirements. 3G femtocells must monitor UMTS channels to detect base stations in the vicinity, as well as GSM channels to establish cells that might be appropriate for handover when a user leaves the femtocell zone.

The femtocell can be viewed as two distinct functions: the analog front end and the baseband processor. The front end, which is the topic of this article, converts the digital data stream into an RF signal in the *transmit* circuit, and vice versa in the *receive* chain. The front-end design entails trade-offs between integration and performance. Although discrete solutions can be tailored to provide the best performance, the cost would be prohibitive for a femtocell design. Conversely, a fully integrated solution may provide the lowest cost, but the performance may not be sufficient.

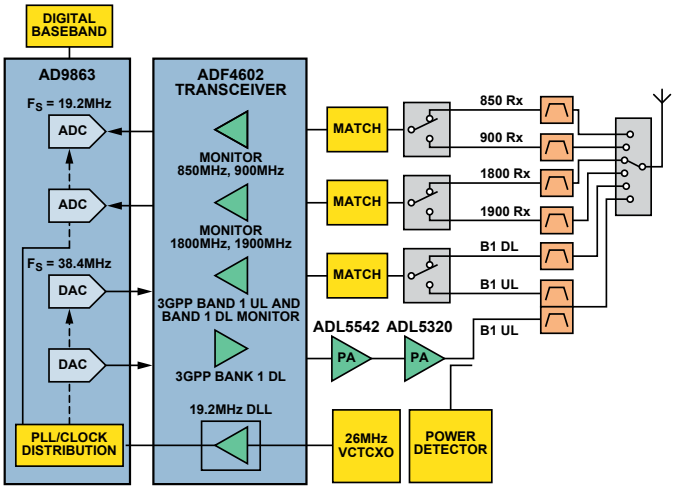

Figure 2. Femtocell analog front-end implementation based on ADI chipset.

Figure 2 illustrates a high-level block diagram of a femtocell designed to support local base station operation in UMTS band 1 as well as monitor signals in the 850-MHz, 900-MHz, 1800-MHz, 1900-MHz, and 2100-MHz bands. Together, the AD9863[1] mixed-signal front-end (MxFE®) baseband transceiver, ADF4602[2] integrated radio transceiver, ADL5542[3] and ADL5320[4] linear amplifiers, switches, filters, and other associated support circuitry form a compact, high-performance front end for the femtocell. A detailed description of the highlighted blocks follows.

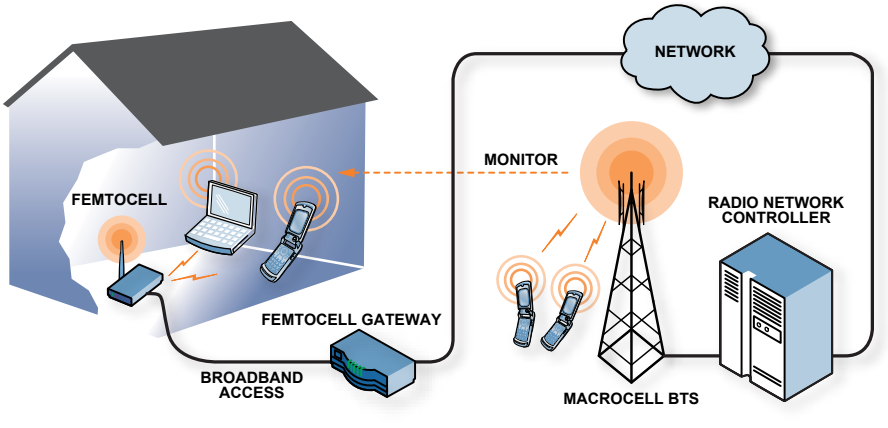

Figure 1. Femto base station compared to macro base station.

On the *transmit* side, the digital baseband feeds a 12-bit parallel data stream to the AD9863, which converts it to an analog I/Q baseband signal. The baseband signal is converted to RF by the ADF4602, amplified by the ADL5542 and ADL5320 gain stages, and sent to a duplexer. A power detector monitors the RF output. A single-pole, six-throw (SP6T) switch selects which *transmit* or *receive* monitoring chain is connected to the single antenna. This signal chain provides 13 dBm output power at the RF output connector, while meeting transmit ACLR specifications as defined in 3GPP standard TS25.104.

The *receive* chain includes surface acoustic wave (SAW) filters and SPDT switches for monitoring the main path. The matching blocks consist of a simple series/shunt inductor for each receive port. The ADF4602 has three receiver input pins: one for band 1, and one each for high- and low band monitoring functions. The band-1 *receive* function may be switched between 1960 MHz to receive the uplink signal and 2140 MHz to monitor the downlink frequency. The ADF4602 downconverts and filters the selected RF signal to a baseband I/Q signal. The baseband signal is sampled by the dual ADCs in the AD9863 and converted to dual 12-bit parallel bit streams for the digital baseband.

This functional partition provides the designer with flexibility, ensures high performance in the signal chain, and allows the data converter's speed and resolution to be chosen to fit the application's requirements. The ADI solution enables the designer to combine the analog front end with a commercially available baseband function, accelerating time to market of the femtocell design, while maintaining the benefit of future integration of ADI technology as the femtocell market matures.

ADF4602 Integrated Radio Transceiver

The ADF4602, shown in Figure 3, is a 3G transceiver offering unparalleled integration and a feature set well-suited to high-performance 3G femtocells. The receiver, based on the direct-conversion architecture, is the ideal choice for highly integrated wideband CDMA (W-CDMA) receivers, reducing the bill of materials (BOM) by fully integrating all interstage filters. The *receive* baseband filters offer selectable bandwidth, enabling reception of both W-CDMA and GSM-EDGE radio signals. The selectable bandwidth, coupled with the multiband LNA input structure, allow GSM/EDGE signals to be monitored as part of a UMTS home base station.

The ADF4602 contains two fully integrated programmable frequency synthesizers for generation of *transmit* and *receive* local oscillator (LO) signals. The design uses a fractional-N architecture for low noise and fast lock-time. All necessary components, including loop filters, VCOs, and tank components, are fully integrated for both *transmit* and *receive* synthesizers. The VCOs run at twice the high-band frequency and four times the low-band frequency, minimizing VCO leakage power at the wanted frequency and the tuning range requirements of the VCO. The VCOs use a multiband structure to cover the wide operating frequency range. The design incorporates both frequency- and amplitude calibration to ensure that the oscillator is always operating at optimum performance. The fully self-contained calibrations, which occur during the 200-µs PLL lock time, require no user inputs. The on-chip VCO outputs are fed to tuned buffer stages and then to the quadrature-generation circuitry. The tuned buffers ensure that minimum current and LO-related noise are generated in the VCO transport. The quadrature generators create the highly accurate phased signals required to drive the modulator and demodulator. Special precautions have been taken to provide the isolation demanded by frequency division duplex (FDD) systems between the *transmit* and *receive* chains.

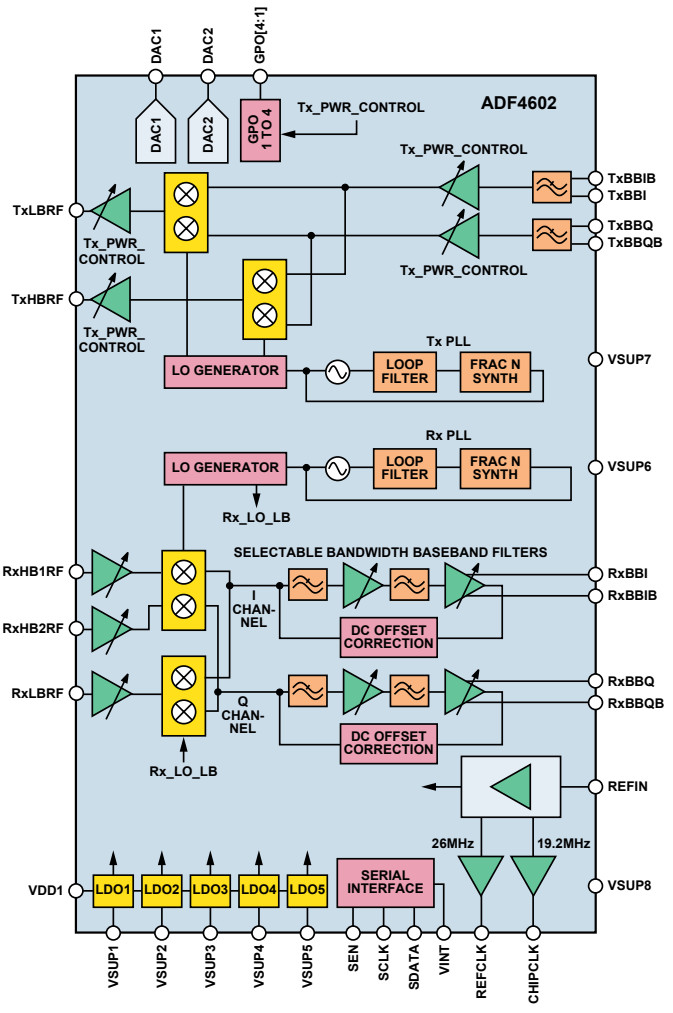

Figure 3. ADF4602 block diagram.

The receiver front-end includes three high-performance, single-ended, low-noise amplifiers (LNAs), allowing the device to support tri-band applications. Two are suitable for high-band operation from 1800 MHz to 2170 MHz, while one is suitable for operation from 824 MHz to 960 MHz. Interstage RF filtering is fully integrated, ensuring that external out-of-band blockers are suitably attenuated prior to the mixer stages. The single-ended 50-Ω input structure eases interfacing and reduces the matching components required for small footprint single-ended duplexers. The excellent device linearity ensures good performance with a large range of SAW- and ceramic filter duplexers.

High linearity demodulator circuits are used to convert the RF signal to baseband in-phase and quadrature components. Two demodulator sections are included: one optimized for the high-band LNA outputs and one optimized for the low band. The high-band- and low-band outputs are combined to drive directly into the first stage of the baseband low-pass filter, which reduces the largest blocking signals prior to baseband amplification. The receiver synthesizer section provides quadrature LO drive to the mixers from the VCO distribution system. A programmable divider allows the same VCO to be used for both high- and low bands. Excellent 90° quadrature phase- and amplitude match are achieved by careful design and layout of the demodulators and VCO distribution circuits.

The baseband section, which includes distributed gain and filtering, is designed to provide a maximum of 54-dB gain with a 60-dB gain-control range. Through careful design, pass-band ripple, group delay, signal loss, and power consumption are

kept to a minimum. Filter calibration is performed during the manufacturing process, resulting in a high degree of accuracy and ease of use. Two selectable 7th-order baseband filters are available: one with a 1.92-MHz cutoff for W-CDMA and one with a 100-kHz cutoff for GSM.

In W-CDMA mode, the ADF4602 is capable of providing 102-dB gain with a 90-dB gain-control range distributed throughout the *receive* signal chain. The RF front-end contains 30-dB of control range: 18 dB in the LNA and 12 dB in the mixer transconductance stage. The two baseband active filter stages each provide an 18-dB gain-control range in 6-dB steps. This results in a 36-dB total gain control range in three 12-dB steps. The variable-gain amplifier (VGA) implements a 24-dB gain control range in 1-dB steps. To simplify programming and ensure optimum receiver performance and dynamic range, simply program the total desired *receive* gain; the ADF4602 decodes the gain setting and automatically distributes the gain between the various blocks.

The transmitter uses an innovative direct-conversion modulator, which achieves high linearity and low noise while eliminating the need for external *transmit* SAW filters. The differential, dc-coupled baseband interface for I and Q channels supports a wide range of input common-mode voltages (VCM) from 1.05 V to 1.4 V. The maximum allowed signal swing is 550 mV peak, which corresponds to a differential range of 1.1 V p-p on either I or Q channels. Prior to the quadrature modulator, the baseband inputs' signals pass through a 2nd-order Butterworth filter with a cutoff frequency of 4 MHz to suppress out-of-band spurs. Calibration techniques maintain accurate I/Q balance and phase across frequency and environmental conditions, ensuring that 3GPP carrier leakage, EVM, and ACLR requirements are met with good margin under all conditions. The ADF4602 achieves a –163-dBm/Hz broadband noise floor at a 190 MHz offset and –8-dBm output power, while meeting TS25.104 requirements for EVM and ACLR. The output is matched to 50 Ω to enable a simple connection to the power amplifier.

AD9863 Mixed-Signal Front-End Baseband Transceiver

The AD9863, a member of the MxFE family of integrated converters for the communications market, is ideally suited for low-cost, high-performance femtocell applications. It integrates dual 12-bit analog-to-digital converters and dual 12-bit TxDAC® digital-to-analog converters. The ADCs are optimized for sampling at 50 MSPS or less. The DACs, which operate at speeds up to 200 MHz, include a bypassable 2× or 4× interpolation filter. Packaged in a 64-lead LFCSP package, the AD9863 is only 9 mm × 9 mm × 0.9 mm. The AD9863 is highlighted here, but other members of the MxFE family (AD9860, AD9861, and AD9862) offer the designer flexibility in choice of performance and auxiliary converters for control circuits.

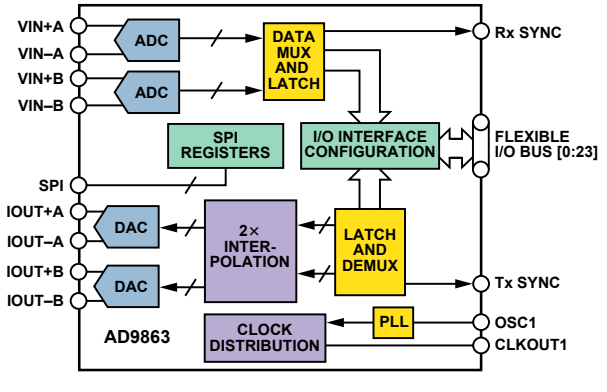

Figure 4. AD9863 MxFE block diagram.

A flexible, bidirectional 24-bit I/O bus accommodates a variety of commercially available baseband ASICs or DSPs. In half-duplex systems, the interface supports 24-bit parallel transfers or 12-bit interleaved transfers. In full-duplex systems, the interface supports a 12-bit interleaved ADC bus and a 12-bit interleaved DAC bus. The flexible I/O bus reduces pin count and package size. For frequency division duplex (FDD) W-CDMA, the AD9863 operates *transmit* and *receive* channels simultaneously. This requires the use of full duplex mode—one 12-bit interleaved Rx data bus and one 12-bit interleaved Tx data bus.

The DAC core converts the 12-bit data into two complementary differential current outputs, providing them to the ADF4602 using a resistor network, as shown in Figure 5. R_{DC} is set to 120 Ω for a 1.2-V common-mode voltage, and R_L is set to 63 Ω for a 1-V p-p differential input swing.

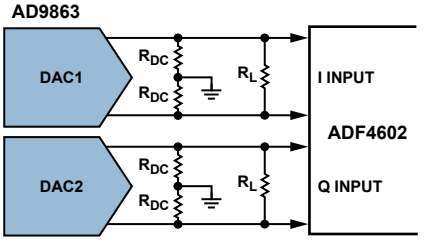

Figure 5. Simple interface between the AD9863 and ADF4602.

The DACs contain programmable fine-gain- and dc-offset controls that can be used to compensate for mismatches between I and Q channels to suppress LO feedthrough and improve EVM performance. The 10-bit dc-offset controls can be used independently to provide up to ±12% of offset to either differential pin, thus allowing calibration of any system offsets.

The ADC input consists of a 2 kΩ differential input resistance and a switched capacitor circuit. The input can be self biased to midsupply, or it can be programmed to accept an external dc bias. It is thus recommended that the ADF4602 *receive* baseband outputs be connected directly to the AD9863 ADC inputs. The ADC input full-scale level is 2 V p-p differential.

Clock Solution for the Femtocell

The femtocell requires a very accurate reference clock—±0.1 ppm—in order to meet 3GPP specifications. Methods for implementing this very fine clock control are outside the scope of this article—but a number of possibilities exist, including GSM macrocell synchronization via the monitoring receivers, GPS synchronization, and IEEE 1588 precision timing protocol. In some instances, a combination of the above methods may be implemented by femtocell vendors. Ultimately, the reference timing control circuitry will regulate the reference frequency source. On the ADI evaluation board, this 26-MHz VCTCXO is used as the reference to the ADF4602. A delay-locked loop (DLL) generates 19.2 MHz, which is a multiple of the 3.84-MHz W-CDMA chip clock. This 19.2-MHz clock is used as the clock input for the AD9863.

The AD9863 has a versatile clocking configuration with many variables. The ADC clock rate, DAC clock rate, PLL, and interpolator settings are software controllable, allowing optimization of power vs. performance to suit the requirements. In the recommended configuration, the PLL multiplier is set to 2×, giving a PLL output frequency of 38.4 MHz. The ADC is clocked at half this frequency. On the *transmit* side, the 38.4-MHz PLL output is used to clock the DAC. *Transmit* interpolation is set to 2× in order to suppress DAC images. Other combinations of clock frequencies are also possible. The AD9863 data sheet provides

a complete description of the operating modes. Using the above clock scheme, the femtocell does not require any discrete frequency conversion PLLs, as are often found in macrocell base stations. All frequency conversion is integrated, helping the femtocell to meet the price point demanded by the market.

RF Amplifiers

The amplifiers chosen for the RF power stage are low-cost, high-performance, broadband linear amplifiers fabricated on an InGaP process. They linearly amplify the output of the ADF4602 and compensate for losses in the RF duplexer and switching networks. The ADL5542 contains internal biasing and matching; the ADL5320 requires external matching, and is packaged in an industry-standard plastic SOT-23 package. Both amplifiers run directly off a 5-V rail, so no external bias circuitry is required. Key specifications for the amplifiers are shown in Table 1. Proprietary techniques applied to the design of the ADI RF amplifiers provide exceptional linearity vs. supply current.

Table 1. Key Specifications for the ADF5542 and ADL5320 (@ 2 GHz)

Specification	ADL5542	ADL5320
Gain	19 dB	13.2 dB
P1dB	18.9 dBm	25.7 dBm
Output IP3	37 dBm	42 dBm
Noise Figure	3.1 dB	4.4 dB
Supply Current (5 V Supply)	97 mA	104 mA

Transmit Output Power and Interference Mitigation

To mitigate interference, the femtocell must set its output power flexibly and intelligently to account for deployments where multiple femtocells operating on the same frequency are located in close proximity to each other (e.g., in an apartment complex). Here, each femtocell will need to transmit at lower output powers to avoid same-frequency interference. Also, the femtocell cannot cause interference to geographically neighboring macrocell base stations operating on the adjacent channel, as this would create dead spots for nearby mobile phones connected to the macrocell network. The femtocell will thus have an *adjacent channel protection* requirement, forcing it to measure the power in the adjacent downlink channel and set its own power according to a predetermined formula so as not to obstruct the macrocell signal.[i]

To allow the femtocell to meet the price point required and for ease of customer installation, these interference mitigation techniques must be automatic and must not require input from a trained field technician or the home user. This process should be automatically initiated when the box is first turned on by the user, and updated at regular intervals thereafter. Together, the band 1 monitoring receiver on the ADI design and the large *transmit* dynamic range available on the ADF4602 allow the femtocell vendor to implement these interference mitigation techniques automatically without external input. The monitoring receiver allows the power in the adjacent channel to be measured accurately and the output power to be adjusted accordingly. About 30 dB of total *transmit* power dynamic range will be required.

Radio Performance Measurements

To evaluate the transceiver chipset against the TS25.104 radio systems specifications, the transceiver lineup described above has been incorporated into an evaluation board design. The evaluation platform, shown in Figure 6, enables the independent testing of *transmit* and *receive* chains, as well as individual component testing. The evaluation board includes the functionality of the block diagram in Figure 1 as well as power conditioning. The radio portion, including ADF4602, AD9863, ADL5542, ADL5320, VCTCXO, and all associated front-end switches and filters, occupies a 1" × 2" space on the board. Note that this board has not been optimized for space savings as it is provisioned for testing purposes, but a more compact design can be achieved for production. Some of the key test results against the TS25.104 specifications are included below to illustrate the performance of the ADI chipset on the evaluation board.

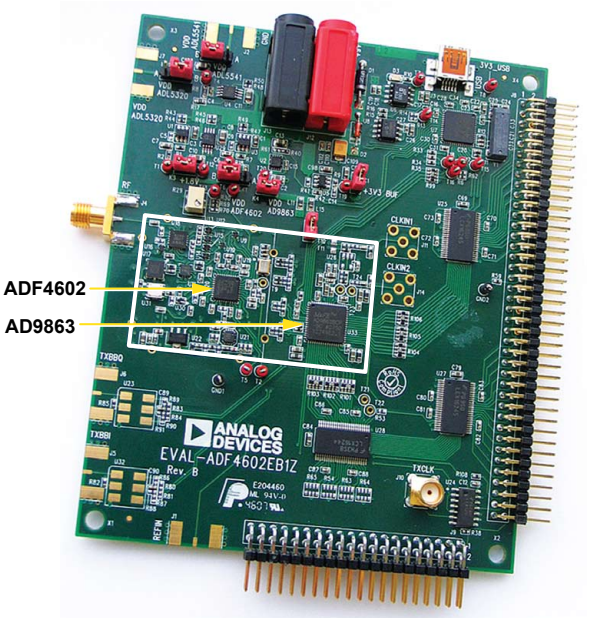

Figure 6. ADF4602/AD9863 evaluation board.

Figure 7 shows the band 1 receiver sensitivity measurement. Receiver sensitivity is a measure of how well the receiver can detect a low-level signal, and is an indicator of the noise figure of the receiver. In this measurement, a 12.2 kHz reference is used. The ADF4602 gain is set to 80 dB. The receiver sensitivity exceeds the TS25.104 specification by 6 dB or more across the band.

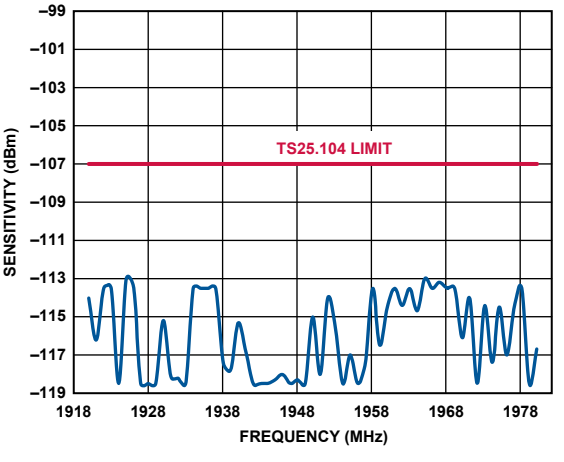

Figure 7. Band 1 receiver sensitivity.

Another key specification for the receiver is the performance under blocking conditions. The blocking tests simulate the ability to receive the wanted signal in the presence of large unwanted signals in adjacent channels. The UL 12.2-kHz reference signal is set to –101 dBm, and blocking signals are injected until a BER of 10^{-3} is measured. As shown in Table 2, the ADF4602 exceeds the TS25.104 with some margin in all three cases.

[i]TSG R4#48 - TSG-RAN Working Group 4 (Radio) meeting #48. October 2008.

Table 2. Summary of Receiver Blocking Testing vs. TS25.104 Specifications

Receiver Blocking Specifications	TS25.104 Specification Limit	ADF4602 Evaluation Board Test Results
Adjacent Channel Selectivity	–38 dBm	–31 dBm (7 dB margin)
10 MHz WCDMA Blocker	–30 dBm	–21 dBm (9 dB margin)
20 MHz Out of Band CW Blocker (1900 MHz)	–15 dBm	–11 dBm (4 dB margin)

Key indications of transmit chain quality are adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM). In both cases these tests are key indicators of the linearity of the combined *transmit* chain. Table 3 compiles the measurements taken on the ADI evaluation board compared to the TS25.104 specifications. It also includes peak code domain error, an EVM measurement that ensures even spreading of errors over the code domain.[ii] In all cases, the ADF4602 evaluation board exceeds the TS25.104 specifications with margin. A plot of the output spectrum used in the ACLR measurements is shown in Figure 8.

Table 3. Summary of Transmitter Testing vs. TS25.104 Specifications

Transmitter Specification	TS25.104 Specification Limit	ADF4602 Evaluation Board Test Results
Error Vector Magnitude (EVM)	<12%	4%
Peak Code Domain Error (PkCDE)	<–33 dB	–46 dB
Adjacent Channel (5 MHz) ACLR	<–45 dB	–49 dB
Alternate Channel (10 MHz) ACLR	<–50 dBm	–72 dB

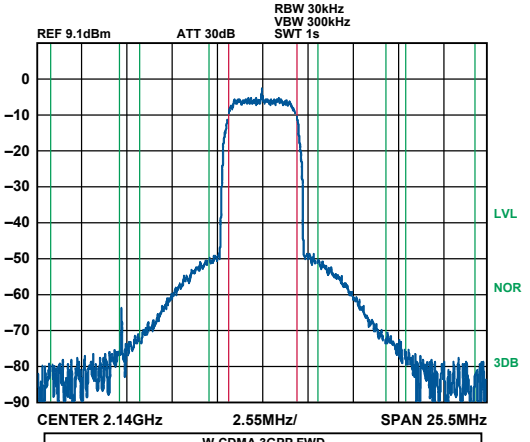

Figure 8. ACLR measurement for W-CDMA band 1 signal with 13 dBm output power.

Figure 9 shows a transmit EVM plot for a typical femtocell configuration involving two HSDPA channels and a number of voice/data channels. The composite EVM is below 4%. Evaluation of the circuit has shown that the EVM is dominated by the LO leakage introduced by the I/Q offsets voltage at the input of the modulator—a feature of direct-conversion transmitters. As mentioned above, these offsets may be calibrated out by using the AD9863 dc-offset controls.

[ii]TSG R4#8 (99)705 - TSG-RAN Working Group 4 (Radio) meeting #8. October 1999.

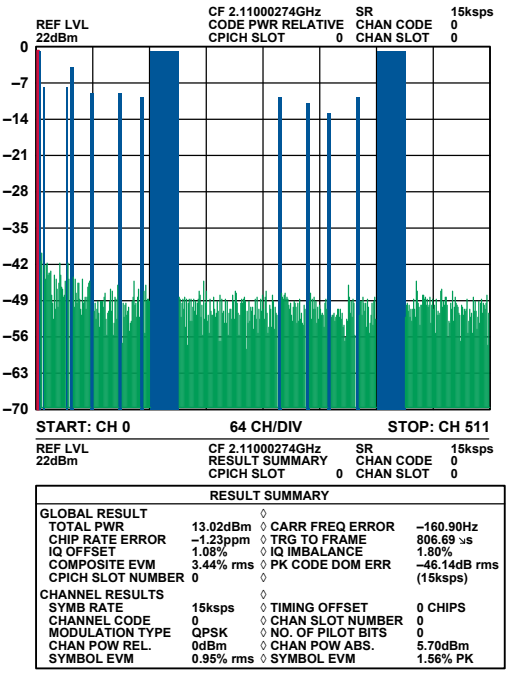

Figure 9. EVM measurement for a typical femtocell configuration.

CONCLUSION

The emerging femtocell application presents a unique challenge to the radio designer to minimize cost while maintaining base-station performance. The ADI 3G femtocell chipset comprised of the ADF4602 integrated radio transceiver, AD9863 MxFE baseband transceiver, and ADL5542 and ADL5320 RF amplifiers enables the femtocell designer to meet the TS25.104 specifications in a compact form factor.

REFERENCES

[1] www.analog.com/AD9863
[2] www.analog.com/ADF4602
[3] www.analog.com/ADL5542
[4] www.analog.com/ADL5320

THE AUTHORS

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Considering Multipliers (Part 1)

[The Wit and Wisdom of Dr. Leif—7]

By Barrie Gilbert

You may recall that Newton Leif joined Analog Devices as a young designer, bringing with him a wealth of experience and insights from his prior work. Now, in 2028, Dr. Leif continues to be active in mentoring the younger engineers at our design center located in Solna, near Stockholm. One, for whom he has a special affection, is the young Niku Chen, already well on her way to a stellar career at this company.

Throughout her life, Niku has been developing that critical aptitude—predicated on an *attitude*—essential for sustained success as a designer of integrated circuits: the ability to visualize, propose, promote, and then develop refreshingly novel concepts from the *engineering side of the fence*. In this regard, Leif's own courageous inclination to launch ideas for long-neglected functions has been her inspiration. Time and again, the naysayers declared them to be of "no value" in the current marketplace; and yet, steadily and stealthily, he would find the resources needed to develop them.

Young Niku has this stubborn flair for *imagineering* from the trenches and, with but the barest of hints from Leif, she's been busy designing nanopower analog array processors for use in neuromorphic systems, employing many thousands of slow, low-accuracy, and—frankly—rudimentary multiplier cells. To the surprise of all the blind spear throwers (the most dangerous kind!), multipliers continued to be indispensable over 60 years since the very first fully monolithic ICs were fabricated in 1967 at Tektronix (for use as gain-control elements **[1]**) by another youthful and aspiring imagineer, to whom Dr. Leif invariably referred as "that rascally irrepressible Tinkerer."

Cells based on the bipolar junction transistor (BJT) became the Tinkerer's lifetime passion, after his exposure to the very first production transistors in 1954—frail, expensive little guys, and as different from one another as siblings. He joined forces with Analog Devices in 1972, and, like Niku, enjoyed the freedom to work proactively in a focused, but fiercely independent-minded and entrepreneurial, fashion. One outcome: he had proposed, and then developed, an extensive family of products loosely known as "functional" circuits—an ambiguous term, but no more so than the notion of an "operational" amplifier.

Many of these early parts were *multipliers*, which remained in production well into the 2010s. They exploited current-mode *translinear* (TL) loops **[2,3,4]**, current-mirrors **[5]**, and current *conveyors* (conceived and named by the Tinkerer during the Tektronix years), aided by linear g_m cells **[6]** (Figure 1). Another novel and ubiquitous cell from that era, later named a "KERMIT" **[7]**, meaning a *Kommon-EmitteR MultI-Tanh*, was used as the kernel of a 2008 product, the ADL5390† RF vector multiplier (Figure 2), and in an elaborated form in the ADL5391 dc-to-2-GHz multiplier, the latter providing exact symmetry in the time delay from its *X* and *Y* inputs, for the first time.

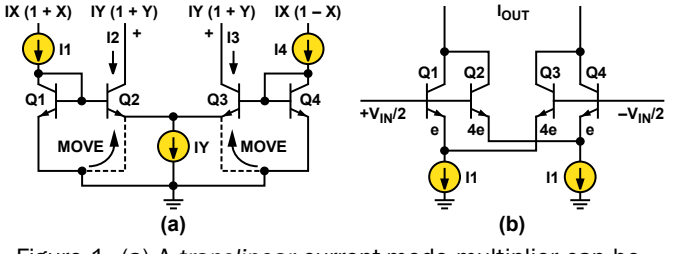


Figure 1. (a) A *translinear* current-mode multiplier can be viewed as two current mirrors with the inner emitters tied together, and its simple math. (b) One of many multi-*tanh* cells, the doublet, a g_m-based multiplier.

Today, well into the second quarter of this century, there is no disagreement, among the experts in *neuromemic*[1] intelligence systems, regarding the indispensable role of *analog* multipliers and numerous other nonlinear *analog* functions in this field. But at one time, during the century's first quarter, well before the recent breakthroughs in practical neuromorphic hardware, there *were* legitimate reasons for doubting this outcome. Now, lacking these (the most distinctive aspect of our massively parallel hybrid, yet essentially analog, hypercessors), we'd still be squeezing miserable little on-again off-again bits through tiny pipes, a mere handful at a time. *Michaday*[2] and kin are evidence of their many beneficiaries.

Citizens at large were never much aware of how technological upheavals occur and change society. For example, these days, we think nothing of conversing with people across the nations, using real-time language translation, and yet this wasn't always possible; it had to await the deep power of hypercessors, power totally beyond the scope of the old sequential bit-dribblers of 20 years ago—ample evidence of how far we've come.

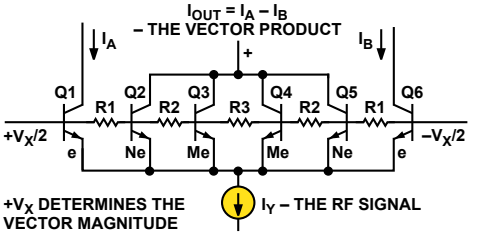


Figure 2. A KERMIT core of the type used in the ADL5390 RF vector multiplier, called a SCAM—steerable-current analog multiplier.

Following the general collapse of Moore's Law around 2016, some 20 years ahead of predictions based on fundamental quantum considerations **[9]**, it took researchers quite a while to realize that *binary computers were not the road to high-level intelligence*; and it took far longer than originally expected to emulate human intelligence to any significant degree and on a significant scale of practical value. There was much to learn about these highly parallel, continuous-time nonalgorithmic computational systems, before issues of *imagination*, *interest*, *visualization*, and *independence* could be addressed. Crucially, the ability to make the millions of neural interconnections remained out of reach until the development of *peristrephic electrofibers*, which could grow the necessary meters in length, each to its individual intracoded destination, in just a few days.

Because the numerous nonlinear cells in today's Companions, like Michaday, are deeply woven into the machine's tapestry, even the experts are inclined to forget the critical role of all the analog array multipliers and array normalizers **[10]** that make their nests in this colorful fabric, utilizing a concept that the Tinkerer named "Super-Integration" (S^{u}I). For example, in his curious S^{u}I multiplier, conceived and fabricated in 1975 **[11]**, all elements and local functions are inextricably merged into a unity, making it impossible to provide a schematic or generate a netlist. Numerous other S^{u}I devices and techniques have been developed over the years **[12,13,14]**. The old I^{2}L was one such.

During November of 2028, over at the campus GalaxyBux, we happened to capture a fascinating discussion between Dr. Leif and Dr. Chen about their work related to analog multipliers in neurocomputers—a topic of great interest to Leif, ever since he first picked up the thread spun by the Tinkerer and stretched it further. As an outcome of her own work, Niku is now writing a piece on multipliers for *Analog Dialogue*. What follows is the last 20 minutes of that hour-long discussion.

† Information and data sheets on all products mentioned here may be found on the Analog Devices website, www.analog.com.

[1] From "meme," the *unit of imitation* **[8]**; used in this adjectival way since 2018.

[2] See *D-Day: The Wit and Wisdom of Dr. Leif* [Analog Dialogue 40-3, p. 3.]

"So, Prof …" (she had always felt awkward about persistently addressing her mentor as "Doctor Leif," and yet since she was disinclined to use his first name, Newton, far less "Newt," she had settled on "Prof"—which, the first time she'd tried it, had generated a broad grin across his rugged Scandinavian face), "I think this piece I'm writing for *A-D* needs to begin with a review of the key attributes of our latest family of nanopower multipliers for neuromorphics—the block diagram, principal system specifications, key applications, that sort of thing."

"Well, ah ... maybe; though perhaps you should start with a bit of the history, going back to their earliest applications **[15]**, and such basic questions as: What were electronic multipliers first used for during the WWII years—the late 1930s through to the mid-1940s? How did their value and use differ in the closing years of the 20th century? And in what ways was multiplication achieved prior to the advent of the *translinear* technique? Then provide examples of IC multipliers developed at ADI over the years, like the seminal and versatile AD534, with its innovative output-summing feature, the '*Z*' pin, which surfaced later in an 8-pin IC, the AD633 (Figure 3).

"And, of course, a review of this sort must mention the 10-MHz AD734—still the *most accurate multiplier ever developed*, by anyone, in any technology, other than the outdated and slow-as-molasses pulse-time-height **[16]** and hybrid multipliers, using DACs. There were early wideband multipliers, such as the AD834 and AD835, and then …"

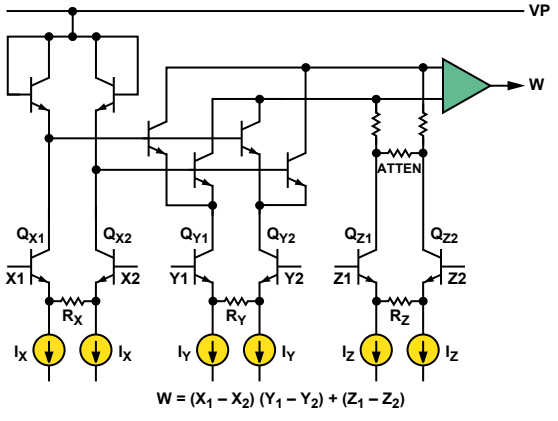


Figure 3. The Z input: an innovation in the AD534, used subsequently in most ADI multipliers, including the 8-pin AD633.

"Whoa, Prof! ... Don't you think that's rather a lot to cram into one article? I mean, isn't its purpose to demonstrate the value of our *newest* parts for neurocomputers: like the ADNm22577 nanowatt analog array processor, the ADNm22585 order- statistics filter, or the ADNm22587 frame-capture correlator, all of which are used in Micha? Today's readers will find these far more useful and can easily understand their functions. I'd really like to cut to the *good stuff* as quickly as possible!"

"Those are certainly valid concerns. But Nicky, keep in mind that the simple multipliers of the late 20th and early 21st century provided the foundation for what you are so expertly designing today. Don't you think you should first say a bit about how *they* work? I'll tell you what: I think I can rummage up a few lecture notes from the catacombs that you might wish to draw upon. We ought to have them readily at hand, anyway."

With just a few gestures on the Actablet touch-panel/display that forms the glass top of every table at GalaxyBux, and the transparent connectivity of a campus-wide local net operating in the 35-GHz arena, supervised (and healed, when necessary) by neuromorphs like Michaday, Leif quickly located his old notes. He was relieved to discover that they still made good sense after so many years. "All *right!!* So, Mitch, please speak them," he directed the Companion, who obliged, streaming via the Actablet to the pair's permanently implanted earceivers, while Leif's annotated text also scrolled on the TableScreen.

Solving Hard Equations in Real Time

"Before neuromorphics," began Michaday, "before binary computers of the sort that were in the ascendancy in the fifty years from 1960 to 2010, going back to World War II years, problems in mission-critical dynamical systems were solved using modeling techniques, with *analog computing* circuits, whose specific functions and connectivity *embodied* simultaneous (and often nonlinear) integro-differential equations. One simply let the network solve them—*autonomously* and *asynchronously*—and in some cases, interactively. Indeed, many such problems could *only* be solved by some kind of *analogous* device. This explains the 18th- and 19th-century fascination with mechanical differential analyzers **[17]**, which very cleverly implemented summation/integration, addition/subtraction, and the like. As an aside, mainly because of noise considerations, the later electronic computers only sparingly used different initiators …"

"That's *differentiators*, Micha," chided Niku, chuckling.

"Sorry." Continuing: "The *structure* of the equations determined the actual physical connections, which were often made at a patch panel, just like the manual telephone exchanges of the time. The fixed *coefficients* were set up in part as R-C *time-constants*, and in part by *weighting factors*, as gain or attenuation, sometimes using potentiometers. The equations also involved calculation of *products* (sometimes *quotients*) of the *variables*, all of which were represented by fairly high voltages ... *High voltages*?! Oh ... That's not still true of *me*, is it?" quivered Michaday, who recalled having been terrified, during his installation days, by some sparks in a power unit that a negligent technician caused.

"Well ... not so *terribly* large, in your case, Mitch," joked Leif. "More like 25 millivolts. Actually, you use both voltage-mode and current-mode representations, whichever is appropriate at the functional level **[19]**. By the way, our human neurocircuits are just the same in this regard. Okay. Now, please proceed, and quit breaking the thread with self-indulgent observations!"

Niku hid an empathic grin behind her slender hand.

"Some of the nominally *fixed* coefficients may have needed to be *altered*, as the accuracy of the solution improved, using the potentiometers, which adjusted voltages acting on *coefficient multipliers*, and which were also of about a hundred volts full-scale," gulped Michaday. "Do you wish me to continue?"

"Yes, Mitch, at least a couple more paragraphs."

"Contrary to the popular myth, analog computers never died. They just went underground. All monolithic analog ICs—not just the multipliers—developed from 1965 onward, inherited the genes of those powerful early techniques. Thus, the term *operational*, as applied to an amplifier, declared that it was designed for the implementation of *mathematical operations*, such as integration or signal summation, ensuring as nearly as practicable that the function was solely a consequence of the *external* components, by placing full reliance on its (fairly) high open-loop gain, its (reasonably) low input offsets, and its (relatively) wide bandwidth.

"First-generation vacuum-tube *op amps* **[18]** were used by the thousands. Today, countless billions of virus-sized elements of their kind are doing much the same thing—with incomparably greater accuracy, speed, and efficiency. However, to *multiply* two variables was once a challenging quest; it required more than a few

'linear' op amps and external networks, due to the fundamental nature of this function. Many solutions devised at the time were hilariously crude by modern standards, scarcely up to the task. For example ..."

"Okay, Micha," interjected Niku. "Let's pause here. Prof, as I see from the descriptions of the almost desperate methods used to approximate multiplication in the text that follows, their designers believed accuracies of 1% and bandwidths of a few kilohertz were regarded as the cat's pajamas! We *have* come a long way! Some of the techniques that were concocted to do multiplication are scarcely credible. They're in sharp contrast to the translinear principle that later was universally adopted for multiplication. It's so very simple, inevitable, and elegant; even *inherently obvious*."

"Heh! Perhaps that's because I brainwashed you! But keep in mind that, for one thing, reliable silicon planar transistors, with their natural but gleefully fortuitous log-exponential properties, were decades into the future. What's more, even the translinear multipliers of the last century had an Achilles' heel: they were *asymmetrical in the time-domain responses* from their *X* and *Y* inputs, as well as in the linearity of these two signal paths. That remained a problem for some of the competition's multipliers. Be sure to explain in your *A-D* article why *time-symmetry* and *signal linearity* are important. And, don't leave the matter of *quadrants of operation* until too late in the piece."

"I won't. By the way, can you tell me where the labels, *X* and *Y*, used for a multiplier's input ports, came from?"

"No, I really don't know when that first became the custom. Of course, they are commonly used for the two axes of a surface. Perhaps it was the choice of George Philbrick **[20]**. But I'm pretty sure that it was the Tinkerer who introduced today's naming convention at ADI for the other variables associated with modern multiplier-dividers. I think it was at about the time the AD534 was being developed, which was the first analog multiplier designed expressly to be fully calibrated using laser-trimming *at the wafer level*. He used the notation

$$V_W = V_X V_Y / V_U + V_z \tag{1}$$

"The *denominator voltage*, V_U, was internally fixed at 10 V, using a *buried Zener*.[3] The provision for adding in a further signal, V_Z, to the *XY* product was another of his innovations. It's a rather nice example of the genesis of *pragmatic novelty* coming from *thinking like the customer*. You know, envisioning yourself slipping yourself into the shoes of several imaginary users of a new IC, persistently asking '*In such-and-such a devious circumstance*, what would *I myself* like this product to do?' Here, while the main utility of the V_Z input was for adding a further variable to the product—for example, the output(s) of one or more other multipliers, as in correlation—the Tinkerer had much else in mind. I expect your article will explain its value in structuring a multiplier as a divider, and some of its many other uses."

Niku said, enthusiastically: "Yes, of course! I remember now that this neat feature was found in almost all of the other multipliers designed by the Tinkerer. It also allowed several signals to be summed progressively simply by *daisy-chaining* the 'next' V_Z to the previous V_W ... But, the wideband AD834 was a bit different, wasn't it? As I recall, it had a differential *current-mode* output. But these can just as easily be summed, in an analog correlator, as I did recently in the ADNm22587, using directly paralleled output connections. However, the utility of that V_Z terminal goes far beyond such basic uses."

[3] An idea he imported into ADI, during the mid-1970s, but revealed to him, without preconditions, by Bob Dobkin, later of LTC, during a long, aprés-ISSCC bar chat.

"Yes," agreed Leif. "Remember this example? General-purpose multipliers were often used to *square the amplitude* of a signal. The *X* and *Y* ports received the same signal, V_{IN}, setting up the output $V_W = V_{IN}^2/V_U$. Then, in the special case of a sinusoidal input, the output is a *raised cosine* at twice the frequency.

$$V_W = \frac{E^2 \sin^2 \omega t}{V_U} = \frac{E^2}{V_U} \times \frac{1}{2}\left(1 + \cos 2\omega t\right) \tag{2}$$

"In a 1976 article illustrating the numerous applications of the AD534 **[21]**, the Tinkerer included a neat way to avoid that dc offset at the output, for a single frequency, without ac-coupling the output. He used just one CR network with $\omega_0 = 1/CR$, and the two inputs were phase-shifted by +45° and –45°, with each attenuated by $\sqrt{2}/2$ at ω_0. Their 90° relative phase shift eliminates the output offset for inputs at ω_0 (see Figure 4).

$$V_W = (E^2/4V_U)\cos 2\omega t \qquad \text{at } \omega = \omega_0 \tag{3}$$

"And here's where the V_Z input served another useful function—*not to add* another signal to the output, in this case, but rather to *raise the gain* by a factor of 4, by feeding only a quarter of V_W to the *Z* pins, so realizing the full ±10-V output swing for a ±10-V sine input. This idea can also be implemented using an AD633, even though its 8-pin format limits the '*Z*' function to just one pin (Figure 4). The ratio $R_{F2}/(R_{F2} + R_{F1})$ determines the feedback factor. Of course, the frequency doesn't have to be as low as 1 kHz, nor exactly $1/2\pi CR$, and there are many things that can be done to reduce the variation of output amplitude over frequency. You might mention these in your article."

"Hmm, it seems I *will* have to say quite a bit about all these ancient parts and their manifold applications in my article. By the way, I also read that article by the Tinkerer. It's a terrific resource, but probably hard to find today. I was intrigued to discover how simple it is to synthesize novel functions using the *normalized* relationship, $w = xy + z$, where $w = V_W/V_U$, $x = V_X/V_U$, and so on. Constantly having to divide variables by that denominator is no fun, and nothing but a time-wasting distraction when you're pursuing invention with just a Ziptip and a sketch-pad on your knee."

"You're right about the idea-enabling potential of $w = xy + z$, Nicky; but be careful never to fall into complacency about the importance of establishing *and preserving* scaling parameters in a nonlinear circuit. As a designer, whenever a scalar, such as V_U, appears in your target function, you'd better be absolutely sure you can vouch for it—that *you* are in full control of both its initial value and its environmentally threatened stability."

"I certainly understand that's something for us IC designers to worry about," replied Niku. "But surely it's less relevant for the user of the part. Can I rewind to an earlier point? All of today's 'vanilla' multipliers operate in *four quadrants*. You know: V_W is the true *algebraic product* of V_X and V_Y, either of which may be positive or negative. But that *wasn't* true of all those early IC multipliers you alluded to, was it?"

"No, it wasn't. Our AD538, for example, was a *one-quadrant* multiplier; it could only accept unipolar inputs at its *X* and *Y* ports. But the primary appeal of such parts was that they were usually more accurate at dc and low frequencies; and in addition, that one-of-a-kind AD538 had several other tricks up its sleeve, including *multiple-decade* operation, keying off the BJT's wide-range log-exponential properties, as well as being able to generate both integral and fractional *powers* and *roots* of input signals and various less-common nonlinear functions." (Figure 5 is an example of what Leif probably had in mind.)

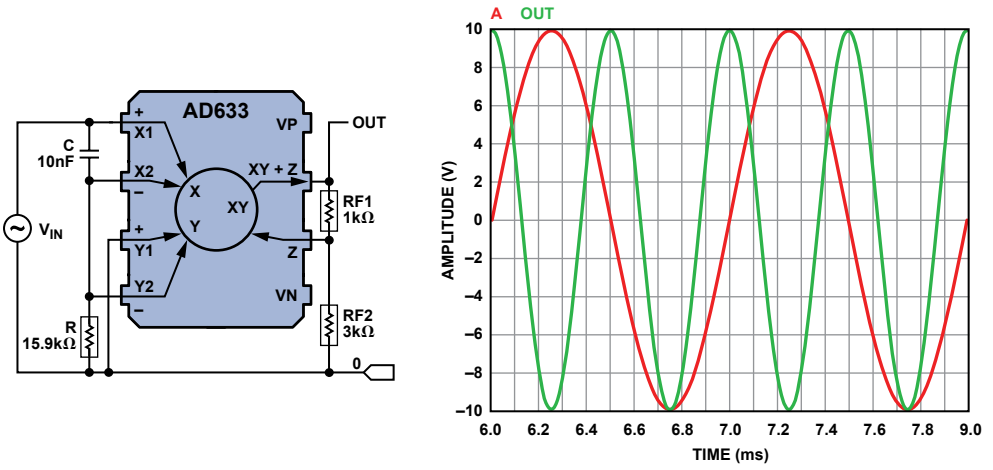


Figure 4. A frequency-doubler using the 8-pin AD633. Here f_0 = 1 kHz.

"So ... what about *two-quadrant* multiplication?" asked Niku.

"The AD538 could be connected to work in that fashion. But today, two-quadrant multipliers are more likely to be known as *variable-gain amplifiers* (VGAs). Their *Y*-channel desirably has *low noise*, *very low distortion*, and *wide bandwidth*, while the former *X*-channel is used to control the *gain* of that signal path.[4] Only a few multipliers optimized for gain control were developed, mostly during the mid-1970s. The 70-MHz AD539 was one such. That part featured *dual*, closely matched signal paths, for *in-phase/quadrature* (I/Q) signal processing."

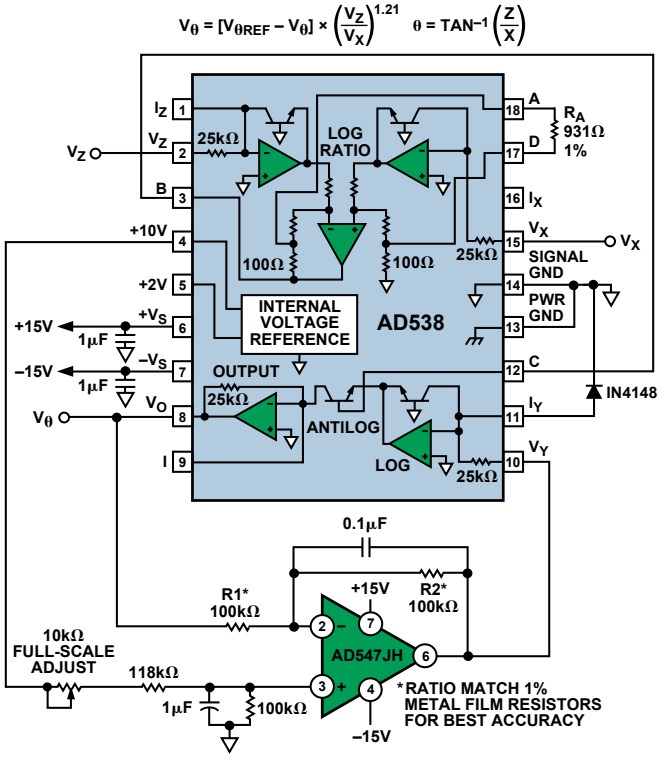


Figure 5. Using the AD538 to generate the arc-tangent function.

So ... Aren't VGAs Just Analog Multipliers?

"Prof, you once mentioned that it was the IC designers, rather than the user community, who first recognized that, in a VGA, the gain-control function is preferably *linear in decibels*—in other words, *exponential*—rather than *linear in magnitude*."

"Right. Optimized VGAs actually are multipliers, in a certain sense, but they more usefully implement the function

$$V_W = V_Y A_0 \exp(x) \tag{4}$$

"A_0 is simply the gain when x = 0. Recall that $x = V_X/V_U$, but V_U now represents something a bit different—although it's still a very important *reference voltage*. If we focus on the *gain* as a function of x we have

$$\text{Gain Magnitude: } A_{LIN}(x) = A_{0\,LIN} \times \exp(x) \tag{5}$$

$$\text{Gain Magnitude: } A_{dBS}(x) = A_{0\,dBS} + x \text{ dB} \tag{6}$$

reusing the variable, x, liberally rather than literally. The gain increases by a number of decibels proportional to V_X, with a slope (which may be gain-increasing or gain-decreasing, as either fixed or user-selectable modes) dependent on V_U."

Niku said, "I recall that the Tinkerer gave the name *X-AMP*® to his novel VGA topology (Figure 6), stressing that the '*X*' doesn't mean 'experimental' or 'mysterious,' but refers to the *exponential* aspect of the gain-control function. He and his team left a rich legacy of X-AMP devices, starting with the AD600/AD602/AD603/AD604/AD605/AD606/AD607 series, followed by the AD8331/AD8332/AD8334/AD8335/AD8336/AD8337 group, and, in modified form, the ADL5330. In other parts, such as the AD8362/AD8363/AD8364 family, X-AMP architecture was embedded into dc-to-GHz rms-responding measurement functions having true power-response even for microwaves, as well as in RF transceivers and demodulators."

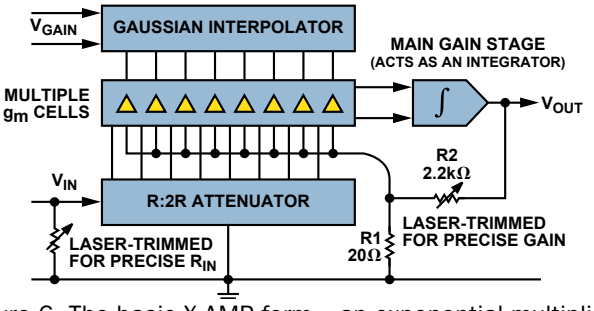


Figure 6. The basic X-AMP form—an exponential multiplier.

"True. And yet other ADI teams adopted the X-AMP idea, as in the 8-channel AD9271 X-AMP device, which included eight independent ADCs, for use in medical and industrial ultrasound.

[4] By the Tinkerer's convention, wherever this distinction arose, "*Y*" was used for the more linear "signal-oriented" path, while "*X*" referred to the slower, and either less-critically linear, or in some cases deliberately nonlinear, gain-control function. This naming convention evaporated as general-purpose multipliers slowly morphed first into general-purpose VGAs and then into even more specialized types.

At the time of its introduction, it was regarded as *state-of-the-art* analog VLSI and won a 'Product of the Year' award in 2008. Really, these all were based on specialized spins of some sort of analog multiplier core; but we called 'em *VGAs*, as soon as that older, worn-out theme ran out of steam!" joked Leif.

"In fact," he continued, "some of the voltage-controlled VGAs utilized a topology other than the X-AMP idea, harking back to the translinear-multiplier roots. While functioning as exponential amplifiers from a user's perspective, internally they used the familiar *current-mode* gain-cells, augmented by elaborate and accurate circuitry for linear-in-dB gain-shaping.

"A classy example of an alternative form was the AD8330. Its core consisted of nothing more (well, perhaps a little bit more) than the four-transistor translinear multiplier, like this." Leif pointed to a circuit on the Actablet, reproduced here as Figure 7. "The key idea is that the *ratio of the currents* in an input pair of transistors (Q1/Q2) forces the *identical ratio* of currents in the output pair (Q3/Q4). But those tail currents, I_D and I_N, are, in general, very different. The input current, I_{IN} (V_{IN} divided by the input resistance, R_1), is multiplied *up* or *down* by the ratio I_N/I_D, resulting in a linearly amplified, current-mode output. This is converted back to voltage-mode by R_O, with a gain of $(I_N/I_D)(R_O/R_1)$. The great appeal of this topology is that the shot noise of the input pair falls as the gain is increased, due to the reduction of the tail current, I_D.

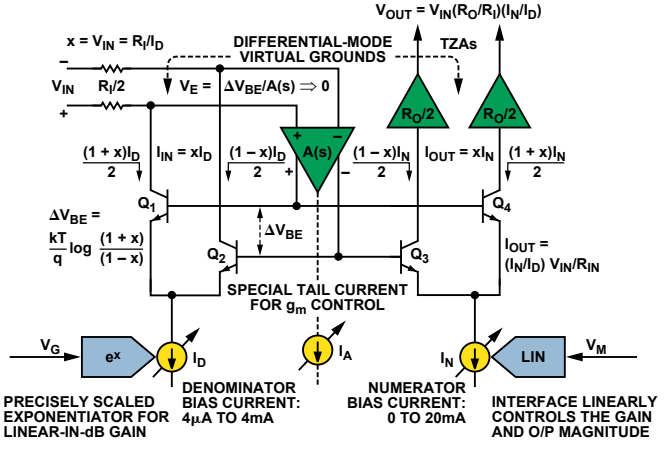


Figure 7. The essentials of the AD8330: A multiplier? or a VGA?

"What makes the AD8330 so different is that I_A is arranged to be a temperature-stable *exponential* function of the primary (input-related) gain-control voltage, V_{dBS}, over a span of at least 50 dB, while on the other hand, I_B is *simply proportional* to a second (output-related) gain-control voltage, VLIN. This unique fusion of a 'linear-in-dB' VGA and 'multiplier-style' control of gain achieved, in effect, the combination of what the Tinkerer referred to as an 'IVGA'—a VGA optimized to cope with a large dynamic range at its signal *input*—with an 'OVGA,' one optimized to provide a widely variable *output* amplitude. If the output's gain-span were used in tandem with the input's 50-dB gain-span, an unprecedented continuous gain-span of >115 dB could be realized, under the control of a single voltage.

"But the intrepid Tinkerer didn't let it rest there. He solved one of the most pernicious problems of VGAs, namely, that *the high-frequency response was invariably a strong function of the gain*. At high gain settings, it tended to roll off—generally in a fairly benign way. But for low gains, most VGAs of that time eventually exhibited a *strongly rising* HF response. This problem was so severe in many competing products that at some high frequency above the specified bandwidth, the actual gain didn't depend at all on the control voltage!"

Niku said: "Yes, I remember once doing some measurements of my own, on a drawer-full of old samples in the lab, and saw this effect. I also checked for myself the data-sheet claim that the AD8330 didn't suffer from this problem at all." Using the Actablet to locate her early work, she found Figure 8. "Ah-ha, here's what I'm looking for. So ... the left panel shows the HF response of the ... should I mention the part's manufacturer?"

"Better not," Leif grinned broadly, "though they and a lot of other standard analog-IC outfits faltered in the early 2000s."

"Okay. On the right is the AD8830's frequency response. I was amazed by how closely all the samples met the data sheet's promises. I've often wondered why it took so long for this part to become popular. It was a great little VGA, with good all-around specs and tremendous versatility, hiding a lot of deeply elegant design—not a bit like the simple repeated cells used in Michaday's parallel-array processors and correlators ..."

Niku was deliberately teasing Michaday—still remotely paying close attention to this flow of information, for possible future use. However, over at GalaxyBux, neither Niku nor Leif could see the expression on its animatrix face. While quite irrelevant to its function, this feature was often left in operation, for the amusement of visitors to the Michael Faraday auditorium, on ADI's Solna campus. And if ever a neuromorph could 'put on a pout,' this would very aptly describe its visage just then. But due to a technical oversight, while he (or 'she'?—apart from the masculine name, it could be either, or neither) could clearly see Leif and Niku, its facial views were not replicated in the down-link data to any of the remote Actablets. And today, a neuromorph's capacity to interpret the expressions of humans is very good **[23]**.

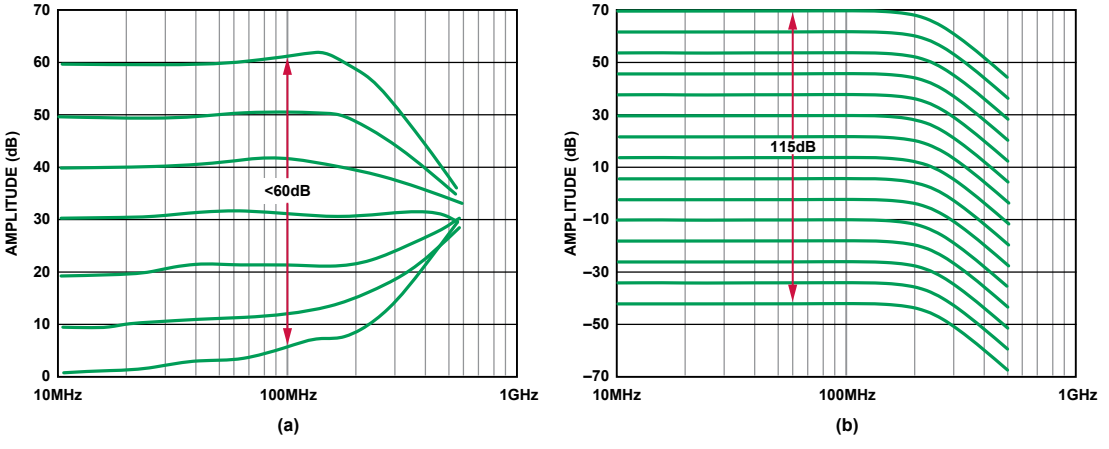


Figure 8. (a) The frequency response of a nameless VGA compared with (b) the response of the AD8330 over its full 115-dB gain-span.

Initially, only the most rudimentary pattern-recognition tasks (such as "Is that a face or a hot dog?") were possible. However, Neuromorphics, Inc. machines are far more sensitive, and can discern the most subtle facial nuances. And, right then and there, Michaday wasn't at all pleased by the conspiratorial grins that glimmered across the coffee cups.

"Excuse me ... Will you be needing any further services, today? I am *rather* busy," he said peevishly in their earceivers.

Leif said, "Alright, Mich, since you have managed to wriggle back into the story line, I'll mention here that your multipliers are in fact not-so-ordinary, if for no other reason than they are quite unlike anything we have discussed. They use full-scale values of mere millivolts for their voltage-mode state-variables, and only a few nanoamps for current-mode variables. Such low-level representations are possible only because of the massively parallel nature of your hypercessors, the miles of your interconnects, and the sheer ameliorative power of abundant redundancy. As the term 'neuromorphic' implies, Mich, *Companions* like you are modeled on human systems, including this reliance on concurrency and parallelism. But what is probably much less well-known is that your state-variables are almost identical in magnitude to those found in organic neurons. You know, it's an intriguing fact that ..."

Neurons Are ... *Translinear*!?

Here, Leif hesitated, weighing the imminence of mentioning an absolutely fascinating aspect of neural behavior against the risk of totally losing the 'multiplier' thread—which had already become slender. But, countenancing the fact that, sooner or later, the pivotal topic of the bipolar junction-transistor's V_{BE} would have to be raised by Niku somewhere in her article, in order to explain translinear concepts from first principles, he leaned out far in the direction of indiscretion.

"Niku, you won't need to mention this in your article, but there is this thing called *Nernst's Law* **[22]**, an important application of which is the quantification of the current-flow that diffuses across the cell membrane of a neuron, the key decision element found everywhere in living systems. The relationship is usually stated in terms of the variables of chemistry, rather than those of electronics. Consequently, I had to do a bit of speculation, at first, regarding the matter of its scaling dimensions; but the outcome of my research was gratifying." (Figure 9.)

"I found that, in the chemistry of weak aqueous solutions of, say, sodium chloride, NaCl, the positively charged Na^+ ions can be regarded as roughly equivalent to the holes in the base of a transistor, while—rather more similarly—electrons are in correspondence to singly ionized Na^-. These are atoms, of course, but in the neuron, they are carriers of charge, much like holes and electrons, and they diffuse in concentration gradients.

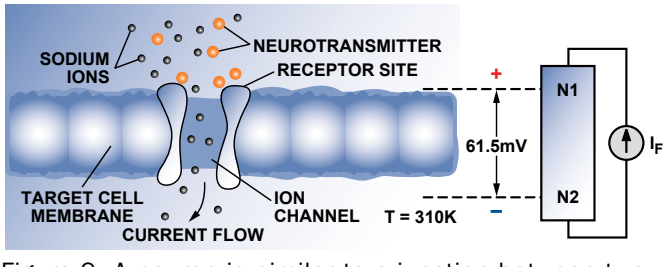


Figure 9. A neuron is similar to a junction between two semiconductor layers of the same polarity type but having different doping concentrations, N1 and N2.

"Now, the question arises: for a given charge concentration on either side of the neuron's cell membrane, what is the potential established across this barrier after ions have diffused across it to establish equilibrium? The answer, in chemistry—after one wakes up to the fact that an obscure scaling quantity, RT/Fzs, is just our old friend, kT/q, in disguise—is truly astonishing:

$$\Delta V = V_{OUTSIDE\ CELL} - V_{INSIDE\ CELL} = (kT/q)\log(Na_O/Na_I) \quad (7)$$

"Here, Na_O and Na_I are the sodium ion concentrations outside and inside the neuron respectively. In this respect, the neuron is behaving *very much* like the ΔV_{BE} of a BJT! It even exhibits a slope, roughly equivalent to the transistor's *transconductance*! Not just some vague transconductance like the old CMOS transistors, but one just like a modern BJT: one that is linear with a concentration gradient—a current-density, a current flow! So is it putting too fine a sheen on all this, to view neurons as *translinear* elements?

"The underlying physical principles are the same: both involve similar processes of diffusion and mobility; both conform to Fick's equation and invoke the Einstein relationship, familiar to semiconductor specialists. Since this aspect of the behavior of a neuron so closely parallels that of a semiconductor device, it should not be surprising that this same relationship is used over and over again in the neuromorphic decision elements of Michaday as well as in most of your recent ICs, Niku. Consider this: for an ion ratio of 10 in the cell of Figure 9, the membrane potential in a neuron is 61.5 mV!"

"All this is fascinating! But, wait a minute. Wouldn't a charge concentration ratio of 10 generate **59.525** mV, proportional to absolute temperature: PTAT, to use the Tinkerer's term? **[24]**"

"Nicky, I have never been inclined to call you a 'hot-head'... but your brain operates at 310 K. The value of 25.85 mV for kT/q is for an assumed temperature of 300 K, close to 27°C. In our bodies, kT/q is (310/300) × 25.85 mV. So for an ion ratio of 10, the human neuronal difference potential is **61.51** mV."

"Of course! Still … might a better comparison to the neuron be, say, a multiple-gate MOS transistor operating in subthreshold? I mean ... a neuron has this capacity for *linear multiplication*, based on its translinear qualities, but it also can perform such things as *integration*, even with *recursion*, *signal summation* with discretionary weighting—all the functions that are at the heart of solving equations in analog computers! It's no wonder that today's neurocomputers are so powerfully intelligent! And I can see clearly now—after having worked with you these past months—why you're always so passionate about stressing the 'Fundaments.' It really is crucial to have a firm grasp on all of them, and be aware of interdisciplinary truths like these.

"By the way, Prof, I've been doing a bit of my *own* research … well, with Micha's help ..." (was that a sigh of appreciation in the downlink?) "and I found that the Tinkerer anticipated the future relevance of translinear elements to neural hardware as far back as 1988, 40 years ago! During his presentation at the first Workshop on Neural Hardware **[25]** in San Diego, he predicted today's nanowatt computing elements, the role of translinear concepts, and he even noted Nernst's Law and its astonishing similarity to the equation for the key voltage-current relationship in a BJT—the same rock-solid foundation of translinear theory. Micha's just located for me a 1990 essay by him **[26]** in which he observed that, just as carrier injection at the emitter-base of a BJT is affected by quantum fluctuations in the band energies, thus generating shot noise,[5] so likewise must neurons be affected. He said it's lucky for us that neurons are not entirely deterministic, since we'd be very dull people!"

[5] Leif says it's improperly called "*collector* shot noise" because it's due principally to statistical fluctuations at the *emitter* junction. These variations in the mean current travel across the base to the collector junction (which is *not a barrier*, but more like a waterfall). Some extra noise might be generated here, but only when the field strength is high enough to cause ionization (avalanche multiplication).

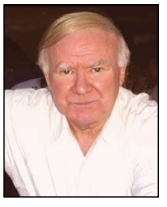
"I also learned that in any cluster of neurons, there are multiple feedback paths, like those sometimes associated with op amp circuitry, and many of them are nonlinear, too. It seems this is the fertile soil from which sprouts chaotic behavior in neurons, which is quasi-deterministic, leading to the original thought. The Tinkerer argued that *human creativity actually depends on moderate amounts of stochastic noise*—and *that* idea would go a long way toward explaining the ephemeral, *unpredictable* quality of the sudden flash of insight. Isn't that a *hoot*!?"

"Well, Niku," said the elder, "between us, we've drifted a long way from the topic of analog multipliers! Tell you what. I have a three-PM with the Director, and it's getting close to that time, so why don't you finish up your ideas for your next *A-D* article back in the lab? I'm really looking forward to seeing it!"

Leif and Niku rose from the still-glowing Actablet and strolled to the door. The unfailingly irritating GalaxyBux AutoGreeter opened it, and the disembodied voice said, in that cheery, ding-dong fashion "Glad to be of *ser*-vice to you!" They exchanged a giggly glance. "See how far the science of neuromemics has gotten us!" joked Leif. Lacking ears (they assumed, as being irrelevant to its prosaic function) the Greeter had nothing more to say ... just then, anyway.

(to be continued)

THE AUTHOR



Barrie Gilbert (barrie.gilbert@analog.com), the first ADI Fellow, has "spent a lifetime in the pursuit of analog elegance." He joined Analog Devices in 1972, was appointed ADI Fellow in 1979, and manages the Northwest Labs in Beaverton, Oregon. Barrie was born in Bournemouth, England, in 1937. Before joining ADI, he worked with first-generation transistors at SRDE in 1954, and at Mullard, Ltd.; later at Tektronix and Plessey Research Labs. Barrie is an IEEE Fellow (1984) and has received numerous awards. He has some 50 issued patents, has authored about 40 papers, is coauthor of several books, and is a reviewer for several journals. He was awarded an honorary doctorate of engineering from Oregon State University in 1997.

ENDNOTES

[1] Gilbert, B. "A DC-500 MHz Amplifier/Multiplier Principle." *ISSCC Technical Digest*. Feb 1968. pp. 114–115. This was the first public disclosure of circuits exploiting what later would be called "The Translinear Principle." [3]

[2] Gilbert, B. "A Precise Four-Quadrant Multiplier with Subnanosecond Response." *IEEE Jour. Solid State Circuits*, Vol. SC-3, No. 4. pp. 365–373.

[3] Gilbert, B. "Translinear Circuits: A Proposed Classification." *Electron Lett.*, Vol. 11, No. 1. pp. 14–16. Jan 1975.

[4] Gilbert, B. "Translinear Circuits: An Historical Overview." *Analog Integrated Circuits and Signal Processing* 9-2. Mar 1996. pp. 95–118.

[5] Toumazou, C., G. Moschytz, B. Gilbert, and G. Kathiresan. *Trade-Offs in Analog Circuit Design, The Designer's Companion*, Part Two. Springer US. 2002. ISBN 978-1-4020-7037-2.

[6] Gilbert, B. "The Multi-tanh Principle: A Tutorial Overview." *IEEE Jour. Solid-State Circuits*, 33-1. 1998. pp. 2–17.

[7] KERMIT, meaning "Kommon-EmitteR MultI-Tanh," is an extremely versatile cell form, in which N > 2 emitters (or sources) are joined and supplied with one current source. An early example (though not yet named that) appears as the vector scanner, in the paper: "Monolithic Analog Read-Only Memory for Character Generation," by Gilbert, B. *IEEE Jour. Solid-State Circuits*, Vol. SC-6, No. 1. pp. 45–55. 1971.

[8] Blackmore, Susan. *The Meme Machine*. Oxford University Press. 1999. ISBN 0-19-286212-X. An excellent introduction to the idea of memetic growth.

[9] Powell, J. R. "The Quantum Limit to Moore's Law." *Proc. IEEE*, Vol. 96, No. 8. Aug 2008. pp 1247–1248.

[10] Gilbert, B. A Monolithic 16-Channel Analog Array Normalizer." *IEEE Jour. Solid-State Circuits*, 19-6. Dec 1984. pp. 956–63.

[11] Gilbert, B. "A New Technique for Analog Multiplication." *IEEE Jour. Solid-State Circuits*, 10-6. Dec 1975. pp. 437–447.

[12] Gilbert, B. "A Super-Integrated 4-Decade Counter with Buffer Memory and D/A Output Converters." ISSCC Tech Digest. 1970. pp 120–121.

[13] Wiedmann, S. K. "High-Density Static Bipolar Memory." *ISSCC Tech. Digest*. 1973. pp. 56–57.

[14] Gilbert, B. "Novel Magnetic-Field Sensor using Carrier Rotation." *Electronics Letters*, Vol. 12, No. 31. Nov 1976. pp 608–611.

[15] Paynter, H. M., ed. *A Palimpsest on the Electronic Art (Being a collection of reprints of papers & other writings which have been in demand over the past several years)*. 1955. Boston: George A. Philbrick Researches, Inc. Fascinating, authoritative, and relevant to this day. Although long out of print, it is worth seeking out on eBay.

[16] Korn, G.A., and T.M. Korn. *Electronic Analog Computers*. NY: McGraw Hill Book Company. 1952.

[17] For an extensive history, see http://everything2.com/e2node/Differential%2520analyzer. For an intriguing account of a differential analyzer built with Meccano, see www.dalefield.com/nzfmm/magazine/Differential_Analyser.html.

[18] Gilbert, B. "Current Mode, Voltage Mode, or Free Mode? A Few Sage Suggestions." *Analog Integrated Circuits and Signal Processing*, Vol. 38, Nos. 2-3, Feb 2004. pp. 83–101.

[19] A fragment of an early article about "Analog Computors," written by G.A. Philbrick, can be found at http://www.philbrickarchive.org/dc032_philbrick_history.htm.

[20] X,Y,Z and W were used in specifying the Philbrick SK5-M four-quadrant multiplier, but in the form W = XY/Z, rather than the later usage W = XY/U + Z. See www.philbrickarchive.org/sk5-m.htm. Incidentally, this magnificent machine needed 200 W to light it up!

[21] Gilbert, B. "New Analogue Multiplier Opens Way to Powerful Function Synthesis." *Microelectronics*. Vol. 8, No. 1. pp. 26–36. 1976. May be hard to find, but Niku dips into her copy in Part 2.

[22] Aityan, S.K. and C. Gudipalley. "Image Understanding with Intelligent Neural Networks." *World Congress on Neural Networks*. Portland, OR. Jun 1993. Vol. 1. pp. 518–523. A milestone event. Other papers in this extensive five-volume resource will be of interest to anyone interested in the status of neuroelectronics in the early 1990s.

[23] Partridge, Lloyd D. and L. Donald. *The Nervous System*. MIT Press. 1992. ISBN 0-262-16134-6. This is a very well-written book, providing an excellent introduction for the electronics engineer to the design and function of neurons. Appendix I derives Nernst's Law from the starting point of ionic diffusion in a weak solution.

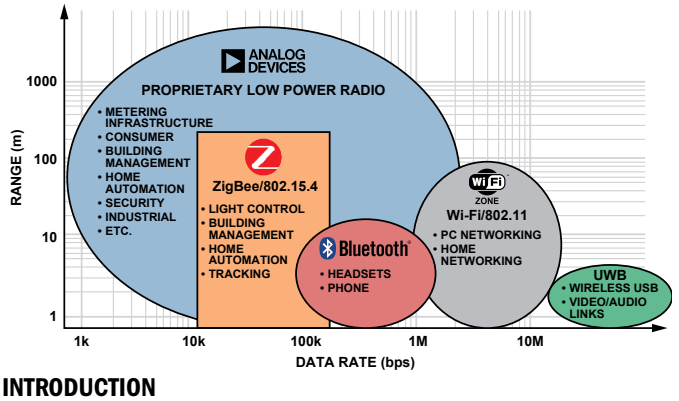
[24] The abbreviation "PTAT" was first used in Section B (p. 854) of the paper by Gilbert, B. "A Versatile Monolithic Voltage-to-Frequency Converter." *Jour. Solid-State Circuits*. Vol. 11. No. 6. Dec 1976. pp. 852-864.

[25] Gilbert, B. "Nanopower Nonlinear Circuits Based on The Translinear Principle." In workshop notes *Hardware Implementation of Neuron Nets and Synapses*. First Workshop on Neural Hardware. San Diego. Jan 1988. pp. 135–170.

[26] *Coming Next Week! The Elements of Innovention*. An early version of this rambling essay, concerning the root sources of creativity, was mounted without the author's permission on the Internet during the mid-1990s. An update is available from barrie.gilbert@analog.com.

Design, Simulate, and Document Proprietary Wireless Systems

By Austin Harney



INTRODUCTION

The broad acceptance of standards developed for the short range wireless connectivity market has been one of the notable features of the semiconductor market in the past few years. These standards include Bluetooth, the various flavors of Wi-Fi, ZigBee, and new emerging standards, such as Wibree/Bluetooth ULP and Ultra Wideband.

A sensible designer faced with the task of wirelessly connecting two or more devices will usually look to these standards for a solution, but the available wireless standards are not always the best fit for the application's requirements.

One reason is that these standards mainly specify operation in the license-free band at 2.4 GHz—due to its worldwide acceptance and approximately 84-MHz bandwidth. The 2.4-GHz band suffers from nontrivial coexistence issues and lower propagation distances for a given power budget, however, causing increased interest in the lower UHF bands. Common frequencies include 868 MHz and 433 MHz in Europe, 902 MHz to 928 MHz in the United States, and 426 MHz in Japan. These are usually collectively termed the *sub-GHz bands*, and they include other unlicensed bands below 1 GHz. Due to the shortage of wireless standards below 1 GHz, designers tend to use a proprietary physical layer (PHY) and communication protocol stack, which can then be tailored to their specific needs.

Figure 1 shows the locations where most of the unlicensed sub-GHz bands are utilized.

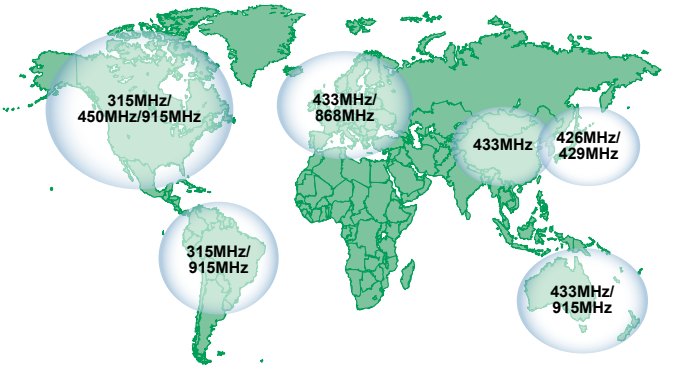


Figure 1. Worldwide sub-GHz bands.

Simulation of Sub-GHz Wireless Connectivity Systems

The advantage of using a wireless standard like Wi-Fi or Bluetooth is that the standards working groups have already defined the data rate, modulation type, output power, and frequency plan, so designers need not be concerned with the underlying national regulations. Bluetooth designers, for example, can be confident that standard reference designs meet the maximum allowed radiated power, maximum modulation bandwidth, emission mask, and minimum number of hop channels to meet EN 300 440 and FCC Part 15 regulations covering the 2.4-GHz ISM band.

At sub-GHz frequencies, however, the problem is a little different. The fragmented nature of the bands results in fewer standards at sub-GHz, so most system designers operating at sub-GHz tend to use proprietary wireless protocols, exercising the freedom to choose the various system parameters themselves. The risk of doing so is that a given set of parameters may not meet national regulations. Thus, the ADI SRD Design Studio™ tool was developed to allow users to simulate various scenarios before going to the lab; it guides the user through the design process, while keeping the underlying regulations in mind. A graphical overview of the main tasks it performs is shown in Figure 2.

The range of subsystem operations and parameters to be considered in the development process includes PLL optimization, RF filtering and matching, data rate and modulation type, demodulation process, packet-data formatting, and average power consumption. System designers typically rely on a combination of spreadsheet-based tools and iterative lab work to help with the optimization of these parameters. Conventionally, time domain analysis can be performed using a SPICE-based simulator, but performing

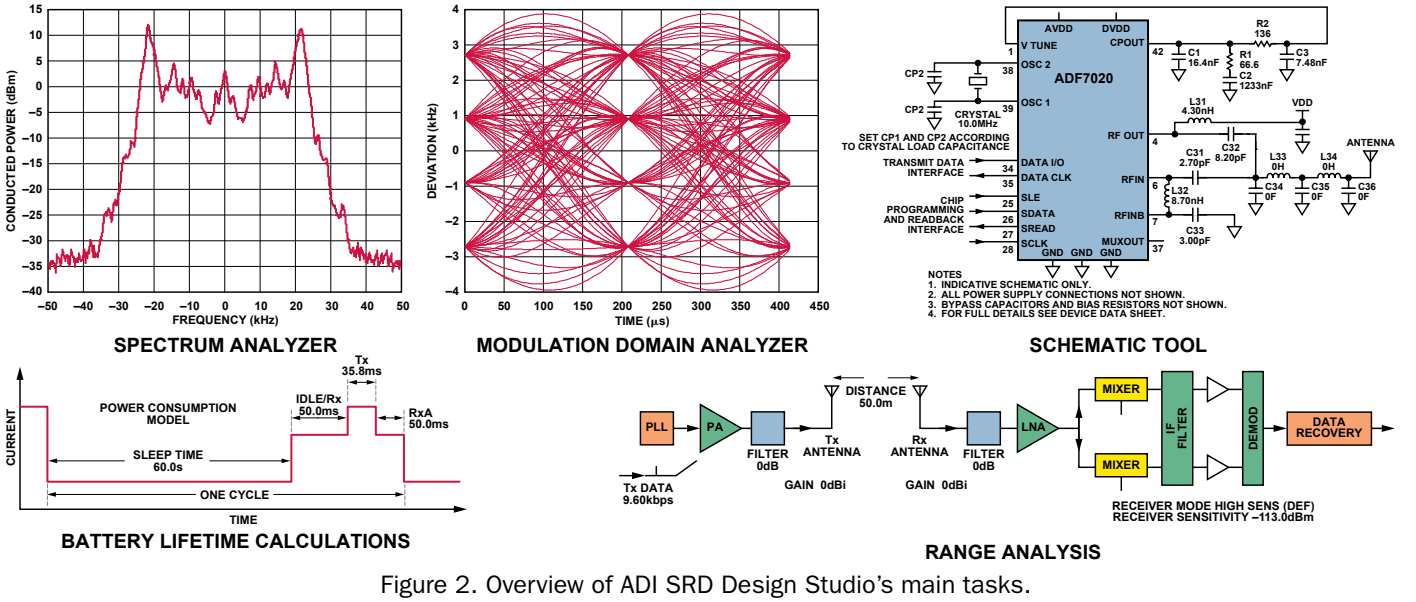


Figure 2. Overview of ADI SRD Design Studio's main tasks.

accurate phase-noise simulations in the frequency domain is usually possible only by using specialized software. Alternatively, designers can make multiple trips to a local regulatory test-house to optimize the system, but this can be expensive.

To help with these challenges, Analog Devices has released a free software package called ADI SRD Design Studio to allow real-time simulation and optimization of various system parameters using the ADF7xxx family of transceivers and transmitters. The development tool is based on the popular ADIsimPLL™ software, enhanced to allow users to view modulation in both the time and frequency domains using a virtual spectrum analyzer. Beyond this, ADI SRD Design Studio greatly simplifies the overall development process, creating a path along which a user can be guided and breaking down the design workflow into a number of distinct tasks, summarized in Table 1.

	Task Name	Description
1	New Design Wizard	Includes default settings for the various regional regulations (FCC, ETSI, ARIB, etc.).
2	Link Budget	Allows range estimation using different propagation models and fade margins.
3	Frequencies Worksheet	Aids in choice of XTAL and PFD for various combinations of data rates and frequencies.
4	Transmitter Spectrum	Extremely flexible spectrum analyzer (FFT based).
5	Packet Formatting	Enter in your packet structure to see effect on battery life and packet error rate (PER).
6	Sync Detection	Helps choose sync byte with good auto correction properties to minimize false triggers.
7	Power Consumption	Different sleep-Tx-Rx scenarios possible. Used for battery life calculation.
8	Schematic	Gives external schematic based on system parameters (for example, loop filter, VCO inductor, XTAL, and matching).

Table 1. List of tasks available in ADI SRD Design Studio.

Basic Overview of Operation

The core of ADI SRD Design Studio is a library of ADF7xxx device models that contains parameterized data for each device, including, for example, the VCO and synthesizer phase noise, VCO gain, frequency range, available data-filter types, sensitivity, and noise figure. Using these models, a *nonlinear time-domain analysis* is performed with the baseband data used to modulate the RF carrier to obtain a time-series output of the VCO. The baseband data can be chosen to be pseudorandom (PRBS) or a periodic (010101) pattern. Unlike conventional linear analysis, nonlinear effects like VCO pulling, nonlinear VCO gain curves, and charge-pump saturation are accurately modeled. An FFT is then performed on the time domain waveform to obtain the spectrum-analyzer output.

The versatile spectrum analyzer allows the user to adjust resolution bandwidth, detector type, and number of sweeps like a commercial spectrum analyzer. The resolution bandwidth can be set from 100 Hz to 300 kHz, while the span is selectable from 1 kHz to 3 MHz. Users can also choose whether to use peak- or average detectors, instructing the analyzer to take the maximum or average number, respectively, in each FFT bin. Having these parameters adjustable is useful because each regulatory standard specifies different measurement conditions—including the resolution bandwidth, span, and detector type that should be used in the measurement equipment. The simulator takes all of these into account in the various preset tests available in the spectrum analyzer mode. These useful preset tests, listed in Table 2, mean that users can quickly test to the relevant standard without poring over the documentation.

Test #	Regulation	Preset Measurement
1	ETSI EN 300 220	Modulation Bandwidth
2	ETSI EN 300 220	Adjacent Channel Power
3	ETSI EN 300 220	Occupied Bandwidth
4	FCC 15.231	–20 dB Bandwidth
5	FCC 15.247	–20 dB Bandwidth
6	FCC 15.247	–6 dB Bandwidth
7	FCC 15.247	3 kHz Power Spectral Density
8	FCC 90.210	Emission Mask D
9	FCC 15.249	–20 dB Bandwidth
10	FCC 15.231 (b)	Field Strength
11	FCC 15.231 (e)	Field Strength
12	ARIB STD-T67	Occupied Bandwidth (25 kHz)
13	ARIB STD-T67	Occupied Bandwidth (12.5 kHz)

Table 2. List of preset measurements in spectrum-analyzer mode.

In addition to the transient- and spectrum-analyzer modes, a PLL frequency-domain analysis is performed to calculate PLL loop filter components and estimate phase- and gain margin. By adjusting the PLL loop bandwidth in the simulation, users can see the effect on the *transmit* modulation spectrum and phase-plot eye opening. This allows a proper optimization of the loop filter without having to rely on a small subset of vendor filter tables or basic guidelines. All three of these main simulations run in less than two seconds in a typical setup.

Propagation Models

One of the other useful tools in the ADI SRD Design Studio package is the *link-analysis worksheet*, which is used to estimate link budget and range under various conditions. Like all of the other tasks, it is integrated into the main simulator. A change in the data rate to conform to an emission mask will cause a corresponding change in sensitivity, affecting the link budget and ultimately the propagation range. This capability provides an advantage over a set of standalone tools, as a change in one parameter—such as data rate—will ripple through to the other worksheets.

The link analysis first calculates the link budget, that is, the difference between the *transmit* power and the *receive* sensitivity, taking any filter- or antenna loss into account. The device setup for this simulation is shown in Figure 3.

The range can then be determined by increasing the distance between the antennas in the simulation until the path loss equals the link budget, that is the point at which the link margin is 0 dB. The path loss is calculated using a user-selected propagation model; three different propagation models are supported: free-space, over-ground, and simple-indoor.

A. Free-Space Propagation Model

The free-space model assumes that there are no obstructions, nor any significant reflecting objects (including the ground), between the transmitter and receiver. With spacing between transmitter and receiver, R, wavelength, λ, and path loss, P_L, the following formula tends to give optimistic propagation ranges for most practical emitter/receiver placements.

$$P_L = 20\log_{10}\frac{\lambda}{4\pi R}$$

B. Over-Ground Propagation Model

Here, the transmitter is at height, h_T, above flat ground, the receiver is at height, h_R, and the spacing is R. This formula gives quite accurate results for clear line-of-sight (LOS) conditions—for

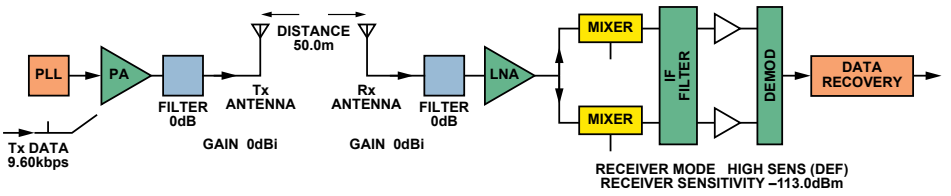


Figure 3. Link analysis blocks.

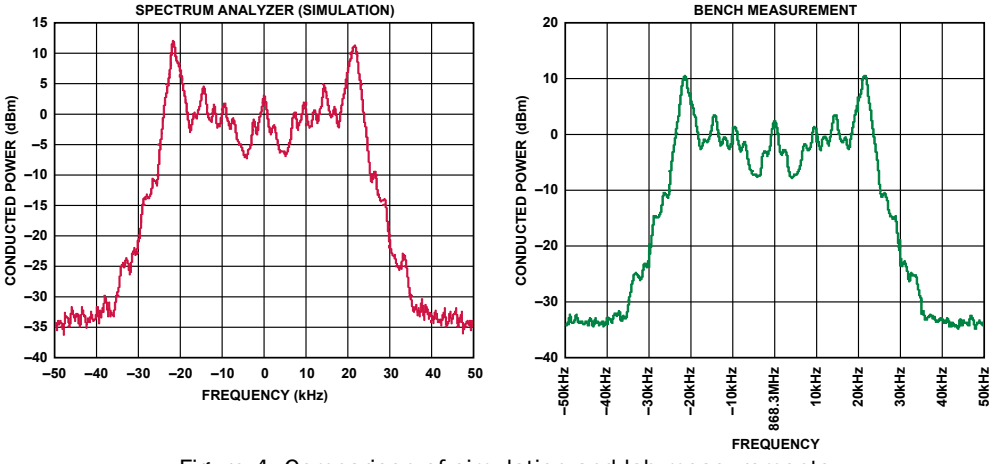


Figure 4. Comparison of simulation and lab measurements.

example, on a beach or a relatively wide piece of road. This simulation shows that propagation ranges of greater than 3 km are possible using the ADF7xxx devices, without the need for an external power amplifier (PA) or low-noise amplifier (LNA).

$$P_L = 20\log_{10}\frac{h_T h_R}{R^2}$$

C. Simple-Indoor Propagation Model

$$P_L = 10\log_{10}(P_0 R^{-n})$$
$$= 20\log_{10}\frac{\lambda}{4\pi R} - 10n\log_{10} R$$

where P_0 is the path loss at 1 m, and n is an exponent whose value depends on the environment. Reference 3 lists some reported values for n in various environments, such as a factory floor, multistory office building, etc. Most designers simply insert a value of n based on empirical results.

Another useful task in ADI SRD Design Studio is the packet-formatting worksheet. This allows users to input a given packet format and see the effect of packet length on battery life, choose a sync word that will result in low false-trigger probability, and translate the *bit error rate* (BER) into a corresponding *packet error rate* (PER), based on the packet length. The BER-to-PER conversion is useful because some IC vendors specify sensitivity in terms of BER—and others specify it in terms of PER.

Testing a Simulation Setup in the Lab

Once the simulation has been completed and the results are acceptable, the file can be saved and the simulation settings exported to the Analog Devices ADF7xxx programming software. Then, a bench test can be run using the *program device utility*. This function will export the frequency, data rate, modulation type, etc. to the ADF7xxx programming software—which will allow quick device configuration in the lab. Bench measurements compare quite well with simulated results, as shown in Figure 4. The simulated and bench measurements for a 9.6-kbps GFSK signal at 868 MHz agree quite closely. When running these comparisons, care should be taken that the simulator uses the same PLL loop filter as on the board, as it will affect the shape of the output spectrum.

SUMMARY

ADI SRD Design Studio was released in July 2007 and has received over 5,000 downloads at the time of this writing. Because Analog Devices is committed to improving the software, an online forum allows users to post suspected bugs, issues, or suggestions for the next revision of the software. This forum is hosted on the Radiolab website, which can be accessed via ADI SRD Design Studio. Users should also check this website periodically for patches or upgrades to the software.

New wireless devices will be added to the software tool as Analog Devices expands its portfolio, including devices at different frequencies—and supporting different modulation schemes. ADI SRD Design Studio should become a very useful part of the wireless connectivity designer's toolkit and a must for anyone designing with the Analog Devices ADF7xxx family of transmitters or transceivers.

REFERENCES

1. Analog Devices website: www.analog.com/srddesign.
2. Harney, A. and C. O'Mahony. "Wireless Short-Range Devices: Designing a Global License-Free System for Frequencies < 1 GHz." *Analog Dialogue*. Vol. 40, No. 1. March 2006. pp. 18–22.
3. Hashemi, H. "The Indoor Radio Propagation Channel." *Proc. IEEE*. Vol. 81, No. 7. July 1993. pp. 943–968.

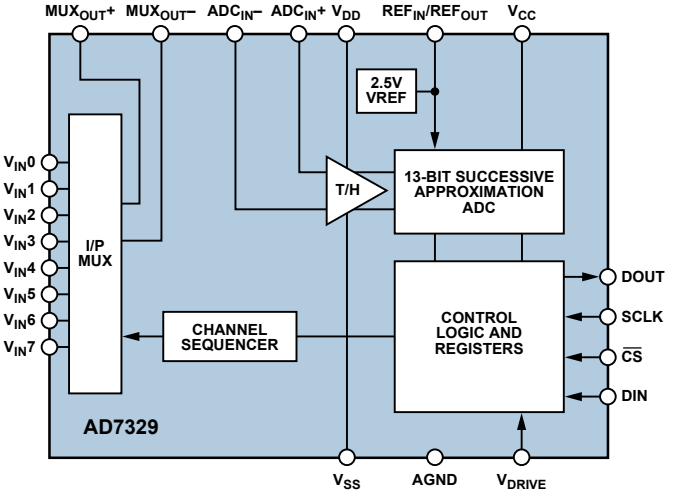
THE AUTHOR

Austin Harney [austin.harney@analog.com] graduated in 1999 with a BEng from University College, Dublin, Ireland, and joined Analog Devices following graduation. He is currently an applications engineer for the ISM-band wireless product line, based in Limerick. In his spare time, Austin enjoys football, music, and spending time with his daughters.

Tales From the Back Burner

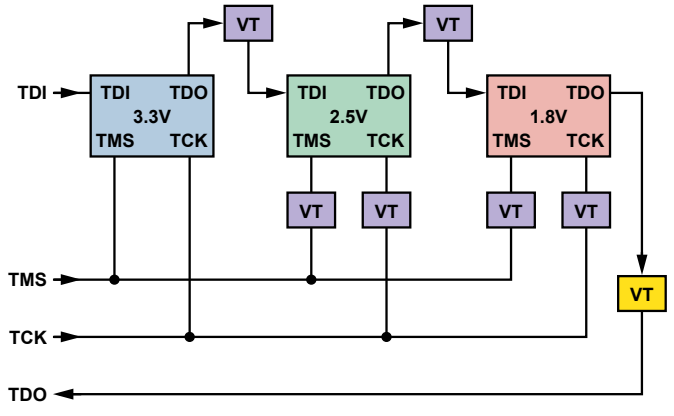
8-Channel Data Acquisition

The principal factors that affect *data-acquisition systems* are: speed, accuracy, power dissipation, package size, and component cost, with varying factors becoming critical depending upon the application requirements. In conjunction with the AD7329 13-bit, 1-MSPS successive-approximation analog-to-digital converter, a single op amp can be used to implement an 8-channel data-acquisition system, reducing the cost and size of the overall system. An article describing a simple, low-cost, 8-channel data-acquisition system can be found at www.analog.com/library/analogdialogue/archives/42-12/8_channel_das.html.



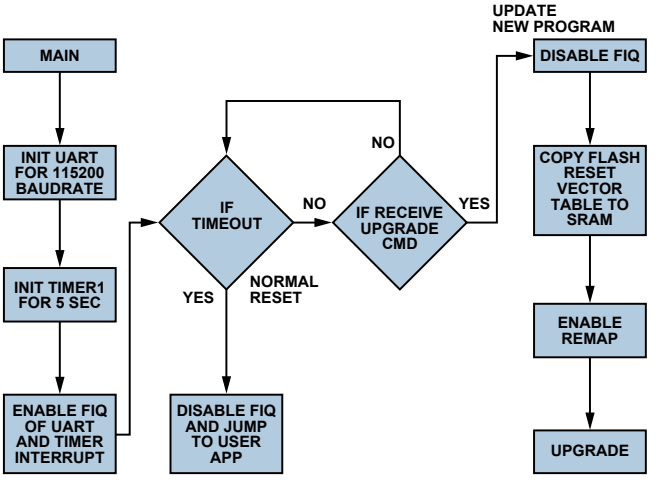
Multivoltage JTAG Chains

As low-power, handheld devices become more prevalent, printed circuit boards with a mixture of 5-V, 3.3-V, 2.5-V, and 1.8-V devices have become common, making the design of a *JTAG chain* challenging. The designer must determine both the operating voltage and the order to place devices that operate at different voltages. An article that provides some tips and techniques for making a robust JTAG design can be found at www.analog.com/library/analogdialogue/archives/42-12/multi_voltage_jtag.html.



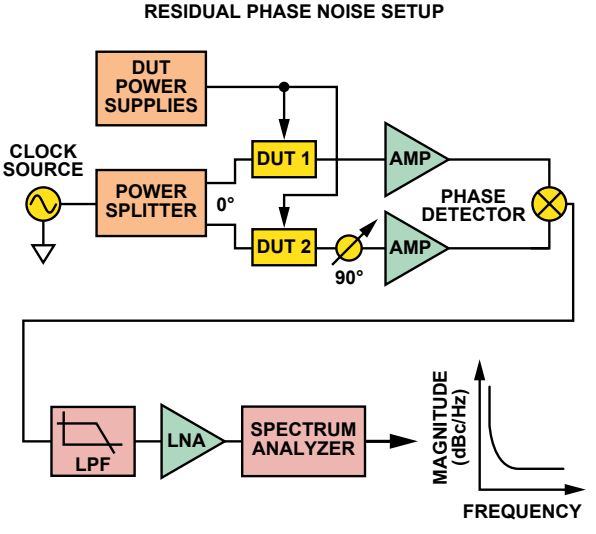
In-Application Programming

The ADuC702x *precision analog microcontroller* provides a serial downloader for loading an assembled program into on-chip memory, but this requires a user to manually tie a pin low during reset or power on. *In-application programming* allows upgrades without touching the board. An article that describes an easy method for upgrading ADuC703x programs can be found at www.analog.com/library/analogdialogue/archives/42-11/ADuC702x_IAP.html. The application code is provided, making implementation quick and easy.



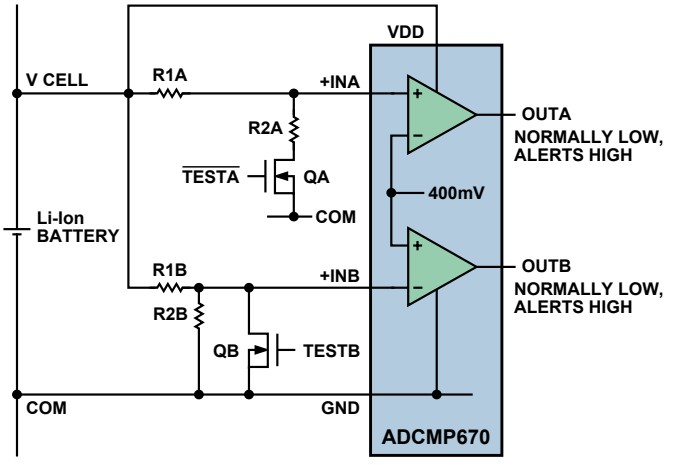
Residual Phase Noise Measurement

Residual phase noise measurement cancels the effect of power supplies, input clocks, or other external noise sources. An article that highlights the attributes of the residual phase noise setup and demonstrates how additive phase noise can be used to identify the source of noise-related issues can be found at www.analog.com/library/analogdialogue/archives/42-11/residual_phase_noise.html.



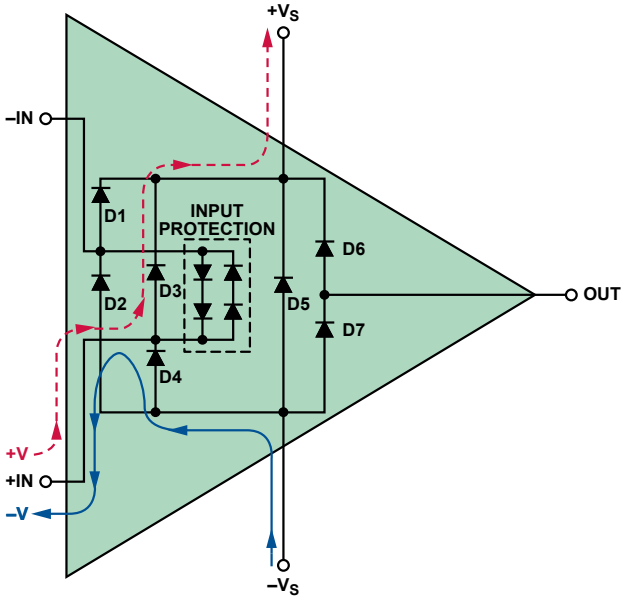
Testing Window Comparators

It probably wasn't too long after comparators were invented that someone thought to put two of them together to make a *window comparator*. An externally controlled test function can be added to a window comparator in order to test whether the circuit is working properly or not. An article that shows an easy way to accomplish this can be found at www.analog.com/library/analogdialogue/archives/42-10/testing_comparators.html.



Protecting Off-Amps

The best reason to be an applications engineer is the wide variety of customers, applications, circuits, and questions encountered, all of which provide daily opportunities to learn something new. Each year applications engineers receive questions regarding the kind of performance users might expect from ADI amplifiers when their power supply is *off*. Amplifiers in this condition are sometimes referred to as "*off-amps*." An article that shows how amplifiers can be protected against current-induced failures can be found at www.analog.com/library/analogdialogue/archives/42-10/off_amps.html.



PRODUCT INTRODUCTIONS: VOLUME 42, NUMBER 4

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

October

Amplifier, Difference, precision, low distortion **AD8274**
Amplifier, Instrumentation, programmable gain **AD8253**
DACs, Current Output, dual, 8-/10-/12-/14-bit, 125-MSPS **AD911x**
Decoder, Video, 10-bit, SDTV, RGB graphics digitizer .. **ADV7181C**
Filter, Video, 6-channel HD/SD **ADA4420-6**
Generator, Clock, 12 LVPECL/24 CMOS outputs **AD9520-x**
Isolator, Digital, 2-channel, enhanced ESD protection .. **ADuM3210**
Isolator, Digital, 5-channel **ADuM1510**
Switch, CMOS, quad SPDT, 0.6-Ω on resistance **ADG858**
Transceiver, RS-485, isolated, 500-kbps, ESD protected **ADM2484E**

November

Amplifier, Operational, dual, ultralow-noise **ADA4075-2**
Amplifier, Operational, quad, micropower **ADA4505-4**
Buffer, Clock/Data, ultrafast, HVDS outputs **ADCLK914**
Codec, Audio, 24-bit, 192-kHz, PLL, 4 ADCs, 8 DACs ... **AD1937**
DACs, Current Output, dual, 8-/10-/12-/14-bit, 125-MSPS **AD971x**
IC, System Management, monitors four voltages **AD5100**
I/O Port, Analog, 16-channel, 12-bit, 8 op amps **AD5590**
Switch, CMOS, SPDT, 0.8-Ω on resistance **ADG852**

December

ADC, Sigma-Delta, 24-bit, 4.8-kHz, PGA **AD7190**
ADC, SAR, 8-channel, 16-bit, 500-kSPS **AD7699**
ADCs, SAR, dual, 12-bit, 3-/5-MSPS **AD7352/AD7356**
Amplifier, Audio, 3-W, Class-D, monophonic **SSM2335**
Amplifier, Instrumentation, low cost, single-supply **AD8223**
Amplifiers, Low-Noise, 400-MHz to 4000-MHz **ADL5521/ADL5523**
Amplifier, Operational, dual, low power, JFET input .. **ADA4062-2**
Amplifier, Operational, dual, low power, rail-to-rail .. **ADA4091-2**
Amplifier, Operational, ultralow noise and distortion **AD8597**
Codec, Audio, high-definition audio **AD1882A**
Controller, Touch-Screen, low voltage **AD7879**
Converter, Capacitance-to-Digital, 2-channel, 12-bit ... **AD7156**
Converter, DC-to-DC, isolated **ADuM5000**
Converter, DC-to-DC, step-down, 600 mA loads **ADP2108**
DACs, Voltage Output, dual, 12-/14-/16-bit **AD50x5**
DACs, Voltage Output, quad, 14-/16-bit, serial input **AD57x4R**
Detector/Controller, Logarithmic, 1-MHz to 4-GHz .. **ADL5513**
Driver, ADC, 16-bit, level translation, gain of 0.2 ..... **AD8275**
Drivers, ADC, differential, low power **ADA4932-x**
Driver, Backlight, programmable, ambient-light input .. **ADP5501**
Front-End, Analog, 8-channel, low noise **AD9272**
Front-End, Analog, 8-channel, low power **AD9273**
Generator, Clock, 12 LVDS/24 CMOS outputs **AD9522-x**
IC, Pin Electronics, 200-MHz, DCL and PMU **ADATE304**
IC, RF Tuner, DVB-H, DVB-T, DTMB, and CMMB .. **ADMTV102**
Isolators, Digital, 2-channel, 500-mW dc-to-dc **ADuM520x**
Processor, Blackfin Embedded **ADSP-BF54x**
Regulator, Low-Dropout, 100-mA loads **ADP120**
Sensor, Intelligent Battery, 12-V automotive **ADuC7036**
Switches, Analog Crosspoint, 300-MHz, 32 × 32 ..... **ADV3200/ADV3201**
Switches, Analog Crosspoint, 300-MHz, 32 × 16 ..... **ADV3202/ADV3203**
Switch, *i*CMOS®, SPST, 1.6-Ω on resistance **ADG1517**

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