Volume 43, Number 2, 2009

A forum for the exchange of circuits, systems, and software for real-world signal processing

Analog Dialogue

In This Issue

www.analog.com/analogdialogue

ANALOG DEVICES

Editors' Notes

IN THIS ISSUE

PLC Evaluation Board Simplifies Design of Industrial Process-Control Systems

The applications for industrial process-control systems range from simple traffic control to complex electrical power grids, from environmental control systems to oil-refinery process control. The intelligence of these systems lies in their measurement and control units. The two most common computer-based systems to control machines and processes are programmable logic controllers and distributed control systems. Page 3.

Skin Impedance Analysis Aids Active and Passive Transdermal Delivery

Pharmaceutical firms are developing alternatives to injections. Transdermal methods, which feature noninvasive delivery of medication through a patient's skin, overcome the protective barrier in one of two ways: passive absorption and active penetration. Skin impedance analysis facilitates proper dosing. Page 11.

Accelerometers—Fantasy and Reality

High sensitivity, small size, low cost, rugged packaging, and the ability to measure both static and dynamic acceleration have made numerous new applications of surface micromachined accelerometers possible. Many of these were not anticipated because they were not thought of as classic accelerometer applications. New applications are limited only by the imagination of designers. Page 13.

Digital Isolator Simplifies USB Isolation in Medical and Industrial Applications

Despite its low speed and point-to-point nature, RS-232 was tolerated in medical and industrial applications because it was universally available, well supported, and allowed easy implementation of the required isolation. The ADuM4160 digital isolator allows simple, inexpensive isolation of full- and low-speed USB peripherals—including the D+ and D– lines—increasing the usefulness of USB in medical and industrial applications. Page 15.

Automated Calibration Technique Reduces DAC Offset to Less Than 1 mV

The AD5360 16-bit, 16-channel DAC is factory trimmed, but an offset of several millivolts can still exist. This idea shows how a simple software algorithm can reduce an unknown offset to less than 1 mV. This technique can be used for factory calibration, or for offset correction at any point in the DAC's life cycle. Page 19.

"Rules of the Road" for High-Speed Differential ADC Drivers

Most modern high-performance ADCs use differential inputs to reject common-mode noise and interference, increase dynamic range by a factor of two, and improve overall performance. ADC drivers—circuits often specifically designed to provide differential signals—perform many important functions including amplitude scaling, single-ended-to-differential conversion, buffering, common-mode offset adjustment, and filtering. Page 21.

Dan Sheingold [dan.sheingold@analog.com]

Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 43, NUMBER 2

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

April

DAC, current-output, 14-bit, 2500-MSPS **AD9739**
Multiplexer, *i*CMOS, 4:1, 1-Ω **ADG1604**
Switch, *i*CMOS, dual SPDT, 1-Ω **ADG1636**
Switches, *i*CMOS, quad SPST, 1-Ω **ADG14611/ADG1612/ADG1613**

May

Accelerometer, gyroscope, and magnetometer, 3-axis **ADIS16405**
Buffer, clock, ultrafast, 2-input, 12-output **ADCLK954**
Comparator, voltage, very fast, LVDS **AD8465**
Controller, touch-screen, low-voltage **AD7889**
DACs, current-output, 12-/16-bit **AD5410/AD5420**
DAC, voltage-output, quad, 12-bit **AD5724R**
Energy Meters, single-phase **ADE5566/ADE5569**
Gyroscope, yaw-rate **ADXRS622**

June

Accelerometer, gyroscope, and magnetometer, 3-axis **ADIS16400**
Amplifier, audio, Class-D, 2 × 2-W **SSM2356**
Amplifier, difference, unity-gain, wide supply range **AD8276**
Amplifier, instrumentation, micropower **AD8236**
Amplifier, operational, dual, wideband **ADA4692-2**
Amplifiers, RF/IF, ultralow-distortion **ADL5561/ADL5562**
Amplifier, variable-gain, 1 MHz to 1.2 GHz **ADL5331**
Amplifier, variable-gain, quad, 235-MHz **AD8264**
ADC, pipelined, quad, 12-bit, 170-MSPS/210-MSPS **AD9639**
ADC, Σ-Δ, 24-bit, 4.8-kHz **AD7192**
ADC, Σ-Δ, 24-bit programmable gain, data rate **AD7191**
ADC, successive-approximation, 18-bit, 2-MSPS **AD7986**
ADC, successive-approximation, dual, 14-bit, 4.2-MSPS **AD7357**
ADCs, pipelined, dual, 14-/16-bit, 125-MSPS **AD9258/AD9268**
ADCs, Σ-Δ, 24-/20-bit, pin-programmable **AD7780/AD7781**
Buffer, clock fanout, 6 LVPECL outputs **ADCLK946**
Buffer, clock fanout, 12 LVDS/24 CMOS outputs **ADCLK854**
Controller, digital, isolated power supplies **ADP1043**
Converter, dc-to-dc, step-down, 600 mA **ADP2109**
Converter, dc-to-dc, synchronous, step-down, 600 mA **ADP2121**
Converters, dc-to-dc, step-up, 650 kHz/1300 kHz .. **ADP1612/ADP1613**
DAC, RF, 14-bit, 2400-MSPS, 4-channel QAM **AD9789**
DACs, current- and voltage output, 12-/16-bit **AD5412/AD5422**
Detector, rms power, 50-dB, 50 Hz to 6 GHz **AD8363**
Driver, 7-channel LED **ADP8860**
Drivers, differential ADC, single and dual **ADA4950-1/ADA4950-2**
Generator, multiservice clock **AD9551**
Generator/synchronizer, network clock **AD9548**
Isolators, digital, 4-channel, 5-kV **ADuM4400/ADuM4401/ADuM4402**
Microcontroller, precision analog, two 24-bit ADCs **ADuC7060**
Potentiometers, digital, 256-/1024-position **AD5291/AD5292**
Potentiometer, digital, 1024-position **AD5293**
Processor, digital audio, flexible routing matrix **ADAU1446**
Processors, embedded, Blackfin **ADSP-BF52x/ADSP-BF52xC**
Power Management Unit, imaging **ADP5020**
Sensor, impact, programmable **ADIS16240**
Sensors, temperature, 16-bit **ADT7310/ADT7410**
Tuner, mobile TV, ISDB-T **ADMTV202**

Analog Dialogue

Analog Dialogue, www.analog.com/analogdialogue, the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 43 years—starting in 1967—it is currently available in two versions. Monthly editions offer technical articles; timely information including recent application notes, new-product briefs, pre-release products, webinars and tutorials, and published articles; and potpourri, a universe of links to important and relevant information on the Analog Devices website, www.analog.com. Printable quarterly issues feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. If you wish to subscribe, please go to www.analog.com/analogdialogue/subscribe.html. Your comments are always welcome; please send messages to dialogue.editor@analog.com or to *Dan Sheingold*, Editor [dan.sheingold@analog.com] or *Scott Wayne*, Publisher and Managing Editor [scott.wayne@analog.com].

ISSN 0161-3626

PLC Evaluation Board Simplifies Design of Industrial Process-Control Systems

By Colm Slattery, Derrick Hartmann, and Li Ke

Introduction

The applications for industrial process-control systems are diverse, ranging from simple traffic control to complex electrical power grids, from environmental control systems to oil-refinery process control. The intelligence of these automated systems lies in their measurement and control units. The two most common computer-based systems to control machines and processes, dealing with the various analog and digital inputs and outputs, are *programmable logic controllers*[1] (PLCs) and *distributed control systems*[2] (DCS's). These systems comprise power supplies, central processor units (CPUs), and a variety of analog-input, analog-output, digital-input, and digital-output modules.

The standard communications protocols have existed for many years; the ranges of analog variables are dominated by 4 mA to 20 mA, 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. There has been much discussion about wireless solutions for next-generation systems, but designers still claim that 4 mA to 20 mA communications and control loops will continue to be used for many years. The criteria for the next generation of these systems will include higher performance, smaller size, better system diagnostics, higher levels of protection, and lower cost—all factors that will help manufacturers differentiate their equipment from that of their competitors.

We will discuss the key performance requirements of process-control systems and the analog input/output modules they contain—and will introduce an industrial process-control evaluation system that integrates these building blocks using the latest integrated-circuit technology. We also look at the challenges of designing a robust system that will withstand the electrical fast transients (EFTs), electrostatic discharges (ESDs), and voltage surges found in industrial environments—and present test data that verifies design robustness.

PLC Overview with Application Example

Figure 1 shows a basic process-control system building block. A process variable, such as flow rate or gas concentration, is monitored via the input module. The information is processed by the central control unit; and some action is taken by the output module, which, for example, drives an actuator.

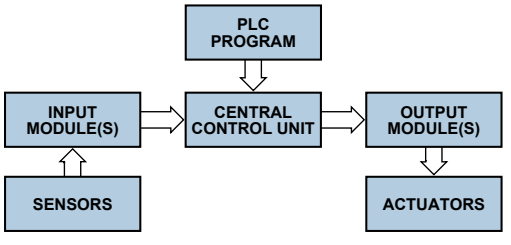


Figure 1. Typical top-level PLC system.

Figure 2 shows a typical industrial subsystem of this type. Here a CO_2 gas sensor determines the concentration of gas accumulated in a protected area and transmits the information to a central control point. The control unit consists of an analog input module that conditions the 4 mA to 20 mA signal from the sensor, a central processing unit, and an analog output module that controls the required system variable. The current loop can handle large capacitive loads—often found on hundreds-of-meters long communications paths experienced in some industrial systems. The output of the sensor element, representing gas concentration levels, is transformed into a standard 4 mA to 20 mA signal, which is transmitted over the current loop. This simplified example shows a single 4 mA to 20 mA sensor output connected to a single-channel input module and a single 0 V to 10 V output. In practice, most modules have multiple channels and configurable ranges.

The resolution of input/output modules typically ranges from 12- to 16 bits, with 0.1% accuracy over the industrial temperature range. Input ranges can be as small as ±10 mV for bridge transducers and as large as ±10 V for actuator controllers—or 4 mA to 20 mA currents in process-control systems. Analog output voltage and current ranges typically include ±5 V, ±10 V, 0 V to 5 V, 0 V to 10 V, 4 mA to 20 mA, and 0 mA to 20 mA. Settling-time requirements for digital-to-analog converters (DACs) vary from 10 µs to 10 ms, depending on the application and the circuit load.

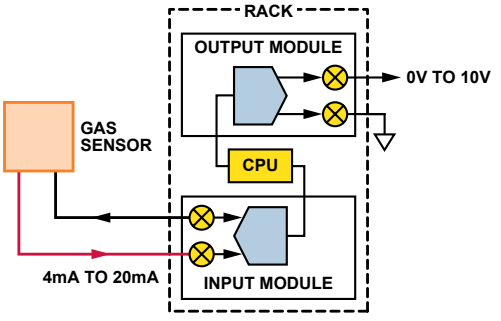


Figure 2. Gas sensor.

The 4 mA to 20 mA range is mapped to represent the normal gas detection range; current values outside this range can be used to provide fault-diagnostic information, as shown in Table 1.

Table 1. Assigning Currents Outside the 4 mA to 20 mA Output Range

Current Output (mA)	Status
0.0	Unit fault
0.8	Unit warm-up
1.2	Zero drift fault
1.6	Calibration fault
2.0	Unit spanning
2.2	Unit zeroing
4 to 20	Normal measuring mode
4.0	Zero gas level
5.6	10% full scale
8.0	25% full scale
12	50% full scale
16	75% full scale
20	Full scale
>20	Overrange

PLC Evaluation System

The PLC evaluation system[3] described here integrates all the stages needed to generate a complete input/output design. It contains four fully isolated ADC channels, an ARM7™ microprocessor with RS-232 interface, and four fully isolated DAC output channels. The board is powered by a dc supply. Hardware-configurable input ranges include 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, 4 mA to 20 mA, 0 mA to 20 mA, ±20 mA, as well as thermocouple and RTD. Software-programmable output ranges include 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, 4 mA to 20 mA, 0 mA to 20 mA, and 0 mA to 24 mA.

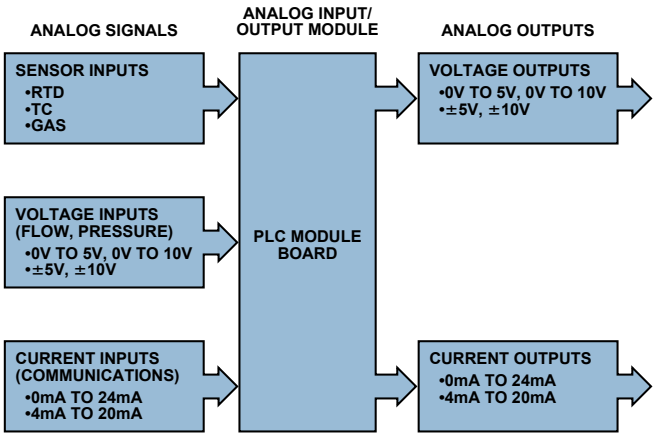


Figure 3. Analog input/output module.

Output Module: Table 2 highlights some key specifications of PLC output modules. Since the true system accuracy lies within the measurement channel (ADC), the control mechanism (DAC) requires only enough resolution to tune the output. For high-end systems, 16-bit *resolution* is required. This requirement is actually quite easy to satisfy using standard digital-to-analog architectures. Accuracy is not crucial; 12-bit integral nonlinearity (INL) is generally adequate for high-end systems.

Calibrated accuracy of 0.05% at 25°C is easily achievable by overranging the output and trimming to achieve the desired value. Today's 16-bit DACs, such as the AD5066,[4] offer 0.05 mV typical offset error and 0.01% typical gain error at 25°C, eliminating the need for calibration in many cases. *Total accuracy* error of 0.15% sounds manageable but is actually quite aggressive when specified over temperature. A 30 ppm/°C output drift can add 0.18% error over the industrial temperature range.

Table 2. Output Module Specifications

System Specification	Requirement
Resolution	16 bits
Calibrated Accuracy	0.05%
Total Module Accuracy Error	0.15%
Open-Circuit Detection	Yes
Short-Circuit Detection	Yes
Short-Circuit Protection	Yes
Isolation	Yes

Output modules may have current outputs, voltage outputs, or a combination. A classical solution that uses discrete components to implement a 4 mA to 20 mA loop is shown in Figure 4. The AD5660 16-bit *nano*DAC® converter provides a 0 V to 5 V output that sets the current through sense resistor, R_S, and therefore, through R_1. This current is mirrored through R_2.

$$V_{DAC} / R_S = I_S = V_{R1} / R_1 = V_{R2} / R_2 = I_{R2}$$

$$I_{R2} = (V_{DAC} / R_S) \times R_1 / R_2$$

Setting R_S = 15 kΩ, R_1 = 3 kΩ, R_2 = 50 Ω and using a 5-V DAC will result in I_{R2} = 20 mA max.

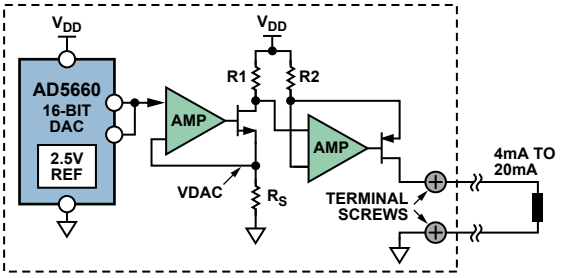


Figure 4. Discrete 4 mA to 20 mA implementation.

This discrete design suffers from many drawbacks: Its high component count engenders significant system complexity, board size, and cost. Calculating total error is difficult, with multiple components adding varying degrees of error with coefficients that can be of differing polarities. The design does not provide short-circuit detection/protection or any level of fault diagnostics. It does not include a voltage output, which is required in many industrial control modules. Adding any of these features would increase the design complexity and the number of components. A better solution would be to integrate all of the above on a single IC, such as the AD5412/AD5422 low-cost, high-precision, 12-/16-bit digital-to-analog converters. They provide a solution that offers a fully integrated programmable current source and programmable voltage output designed to meet the requirements of industrial process-control applications.

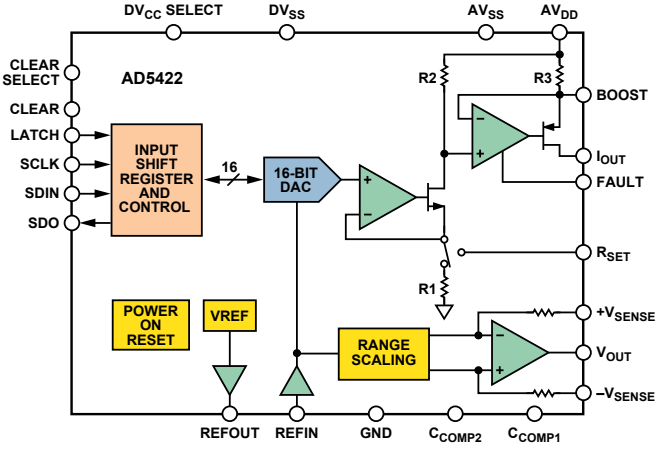


Figure 5. AD5422 programmable voltage/current output.

The output current range is programmable to 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA overrange function. A voltage output, available on a separate pin, can be configured to provide 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V ranges, with a 10% overrange available on all ranges. Analog outputs are short-circuit protected, a critical feature in the event of miswired outputs—for example, when the user connects the output to ground instead of to the load. The AD5422 also has an open-circuit detection feature that monitors the current-output channel to ensure that no fault has occurred between the output and the load. In the event of an open circuit, the FAULT pin will go active, alerting the system controller. The AD5750 programmable current/voltage output driver features both short-circuit detection and protection.

Figure 6 shows the output module used in the PLC evaluation system. While earlier systems typically needed 500 V to 1 kV of isolation, today >2 kV is generally required. The ADuM1401 digital isolator uses *i*Coupler®[5] technology to provide the necessary isolation between the MCU and remote loads, or between the input/output module and the backplane. Three channels of the ADuM1401 communicate in one direction; the fourth channel communicates in the opposite direction, providing isolated data readback from the converters. For newer industrial designs, the ADuM3401 and other members of its family of digital isolators provide enhanced system-level ESD protection.

The AD5422 generates its own logic supply (DVCC), which can be directly connected to the field side of the ADuM1401, eliminating the need to bring a logic supply across the isolation barrier. The AD5422 includes an internal sense resistor, but an external resistor (R1) can be used when lower drift is required. Because the sense resistor controls the output current, any drift of its resistance will affect the output. The typical temperature coefficient of the internal sense resistor is 15 ppm/°C to 20 ppm/°C, which could add 0.12% error over a 60°C temperature range. In high-performance system applications, an external 2-ppm/°C sense resistor could be used to keep drift to less than 0.016%.

The AD5422 has an internal 10-ppm/°C max voltage reference that can be enabled on all four output channels in the PLC evaluation system. Alternatively, the ADR445 ultralow-noise XFET® voltage reference, with its 0.04% initial accuracy and 3 ppm/°C, can be used on two output channels, allowing performance comparison and a choice of internal vs. external reference, depending on the total required system performance.

Input Module: The input module design specifications are similar to those of the output module. High resolution and low noise are generally important. In industrial applications, a differential input is required when measuring low-level signals from thermocouples, strain gages, and bridge-type pressure sensors to reject common-mode interference from motors, ac power lines, or other noise sources that inject noise into the analog inputs of the analog-to-digital converter (ADCs).

Sigma-delta ADCs are the most popular choice for input modules, as they provide high accuracy and resolution. In addition, internal programmable-gain amplifiers (PGAs) allow small input signals to be measured accurately. Figure 7 shows the input module design used in the evaluation system. The AD7793 3-channel, 24-bit sigma-delta ADC is configured to accommodate a large range of input signals, such as 4 mA to 20 mA, ±10 V, as well as small signal inputs directly from sensors.

Care was taken to allow this universal input design to be easily adapted for RTD/thermocouple modules. As shown, two input terminal blocks are provided per input channel. One input allows for a direct connection to the AD7793. The user can program the internal PGA to provide analog gains up to 128. The second input allows the signal to be conditioned through the AD8220 JFET-input instrumentation amplifier. In this case, the input signal is attenuated, amplified, and level shifted to provide a single-ended input to the ADC. In addition to providing the level shifting function, the AD8220 also features very good common-mode rejection, important in applications having a wide dynamic range.

The low-power, high-performance AD7793 consumes <500 μA, and the AD8220 consumes <750 μA. This channel is designed to accept 4 mA to 20 mA, 0 V to 5 V, and 0 V to 10 V analog inputs. Other channels in the input module have been designed for bipolar operation to accept ±5 V and ±10 V input signals.

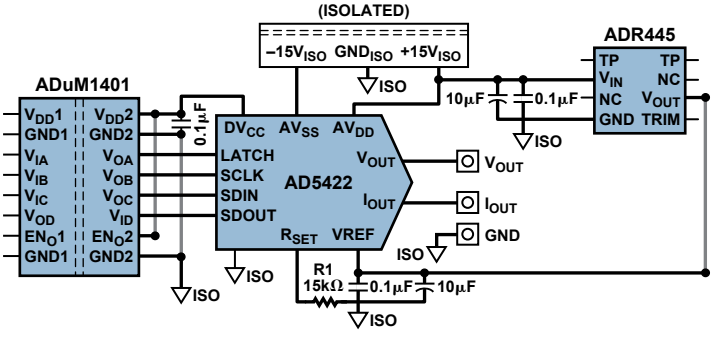


Figure 6. Output module block level.

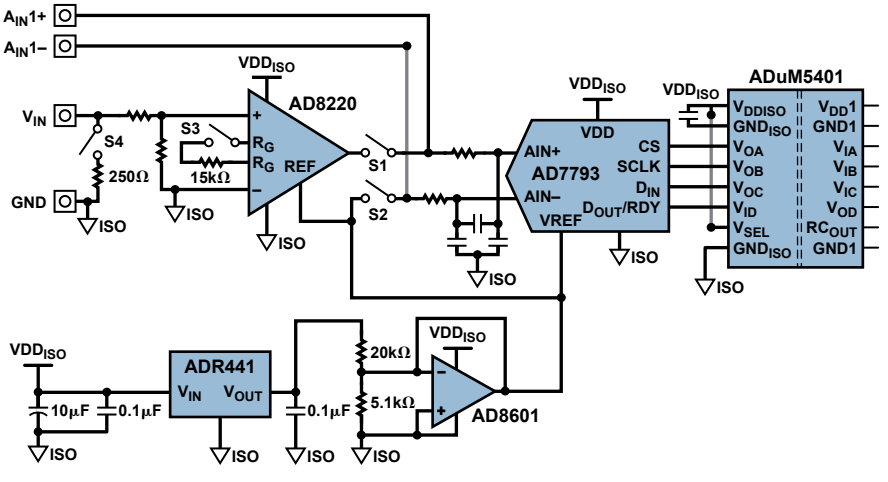


Figure 7. Input module design.

To measure a 4 mA to 20 mA input signal, a low-drift precision resistor can be switched (S4) into the circuit. In this design, its resistance is 250 Ω, but any value can be used as long as the generated voltage is within the input range of the AD8220. S4 is left open when measuring a voltage.

Isolation is required for most input-module designs. Figure 7 shows how isolation was implemented on one channel of the PLC evaluation system. The ADuM5401 4-channel digital isolator uses *iso*Power®[6] technology to provide 2.5-kV rms signal and power isolation. In addition to providing four isolated signal channels, the ADuM5401 also contains an isolated dc-to-dc converter that provides a regulated 5-V, 500-mW output to power the analog circuitry of the input module.

Complete System: An overview of the complete system is shown in Figure 8. The ADuC7027 precision analog microcontroller[7] is the main system controller. Featuring the ARM7TDMI® core, its 32-bit architecture allows easy interface to 24-bit ADCs. It also supports a 16-bit *thumb* mode, which allows for greater code density if required. The ADuC7027 has 16 kB of on-board flash memory and allows interfacing to up to 512 kB external memory. The ADP3339 high-accuracy, low-dropout regulator (LDO) provides the regulated supply to the microcontroller.

Communication between the evaluation board and the PC is provided via the ADM3251E isolated RS-232 transceiver. The ADM3251E incorporates *iso*Power technology—making a separate isolated dc-to-dc converter unnecessary. It is ideally suited to operation in electrically harsh environments or where RS-232 cables are frequently plugged in or unplugged, as the RS-232 pins, Rx and Tx, are protected against electrostatic discharges of up to ±15 kV.

Evaluation System Software and Evaluation Tools: The evaluation system is very versatile. Communication with the PC is achieved using LabVIEW.™[8] The firmware for the microcontroller (ADuC7027) is written in C, which controls the low-level commands to and from the ADC and DAC channels.

Figure 9 shows the main screen interface. Pull-down menus on the left side allow the user to choose active ADC and DAC channels. Under each ADC and DAC menu there is a pull-down range menu, which is used to select the desired input and output ranges to be measured and controlled. The following input and output ranges are available: 4 mA to 20 mA, 0 mA to 20 mA, 0 mA to 24 mA, 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. Small signal input ranges can also be accommodated directly on the ADC by using its internal PGA.

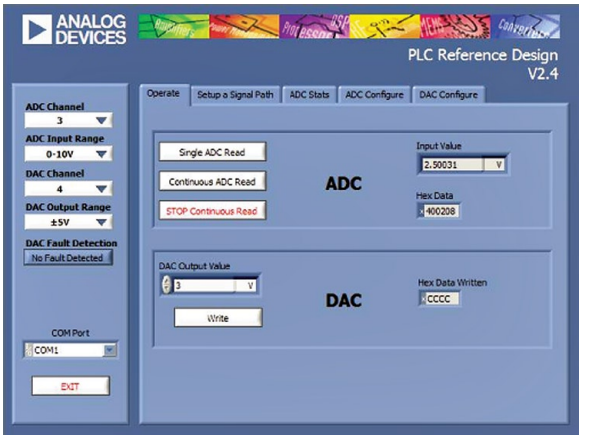


Figure 9. Evaluation software main screen controller.

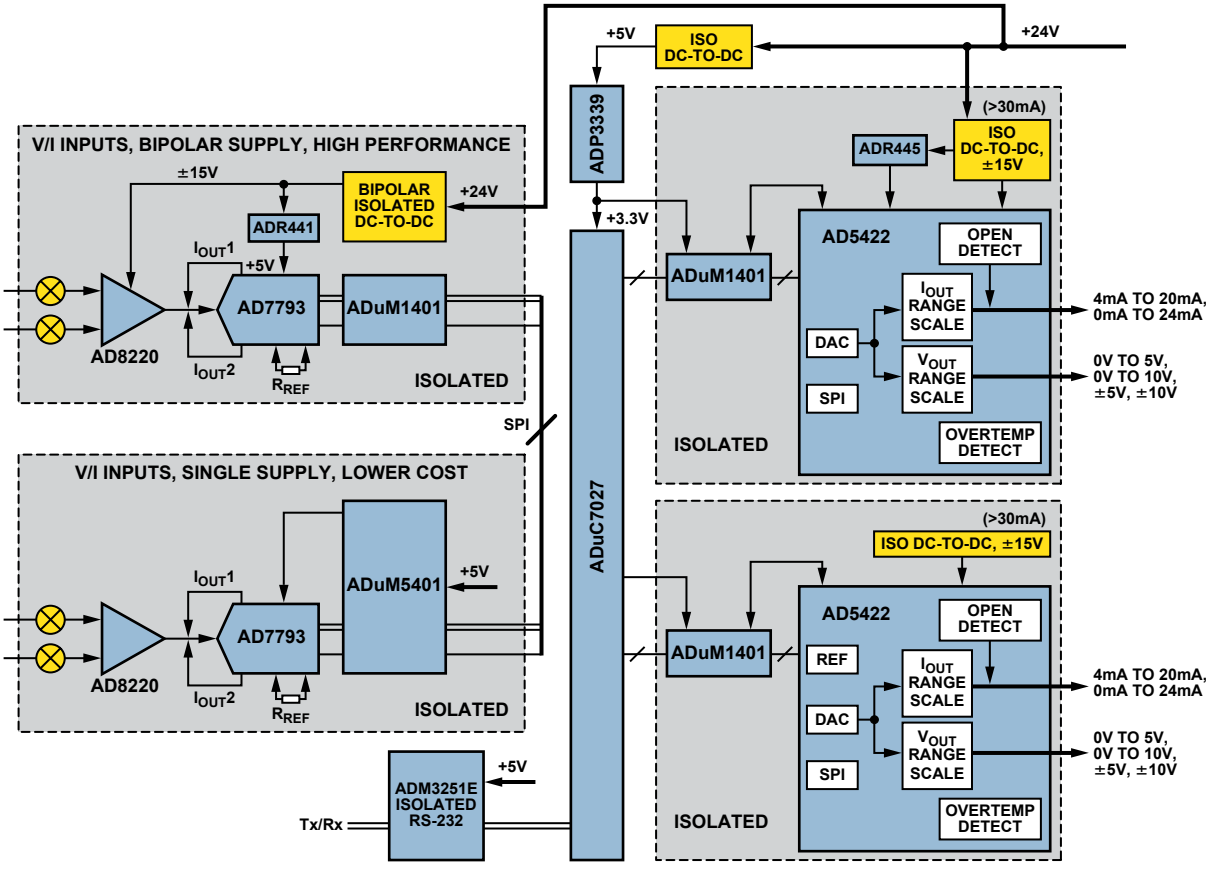


Figure 8. System-level design.

The *ADC Configure* screen, shown in Figure 10, is used to set the ADC channel, update rate, and PGA gain; to enable or disable excitation currents; and for other general-purpose ADC settings. Each ADC channel is calibrated by connecting the corresponding DAC output channel to the ADC input terminal and adjusting each range. When using this method of calibration, therefore, the offset and gain errors of the AD5422 dictate the offset and gain of each channel. If these provide insufficient accuracy, ultrahigh-precision current and voltage sources can be used for calibration if desired.

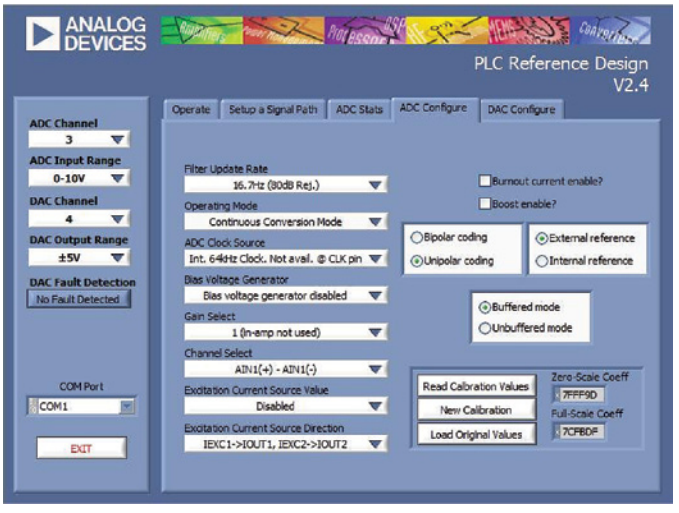


Figure 10. ADC Configure screen.

After selecting the ADC's input channel, input range, and update rate, we can now use the *ADC Stats* screen, shown in Figure 11, to display some measured data. On this screen, the user chooses the number of data points to record; the software generates a histogram of the selected channel, calculates the peak-to-peak and rms noise, and displays the results. In the measurement shown here, the input is connected through the AD8220 to the AD7793: gain = 1, update rate = 16.7 Hz, number of samples = 512, input range = ±10 V, input voltage = 2.5 V. The peak-to-peak resolution is 18.2 bits.

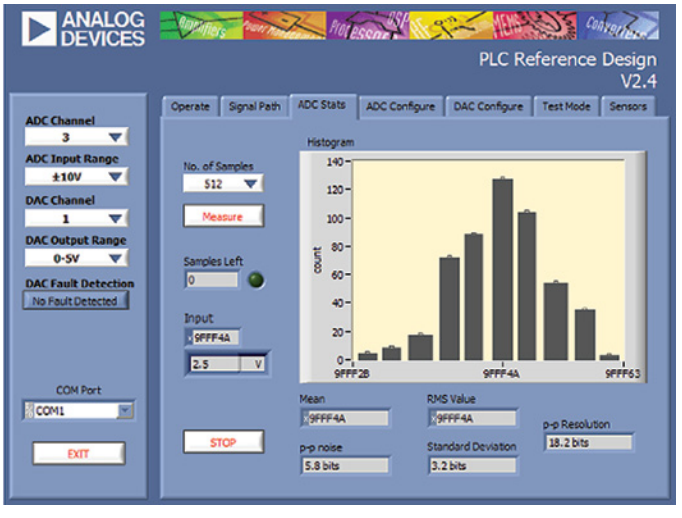


Figure 11. ADC Stats screen.

In Figure 12, the input is connected directly to the AD7793, bypassing the AD8220. The on-chip 2.5-V reference is connected directly to the AIN+ and AIN– channels of the AD7793, providing a 0-V differential signal to the ADC. The peak-to-peak resolution is 20.0 bits. If the ADC conditions remain the same but the 2.5-V input is connected through the AD8220, the peak-to-peak resolution degrades to 18.9 bits for two reasons: at low gains, the AD8220 contributes some noise to the system; and the scaling resistors that provide the input attenuation result in some range loss to the ADC. The PLC evaluation system allows the user to change the scaling resistors to optimize the ADC's full-scale range, thereby improving the peak-to-peak resolution.

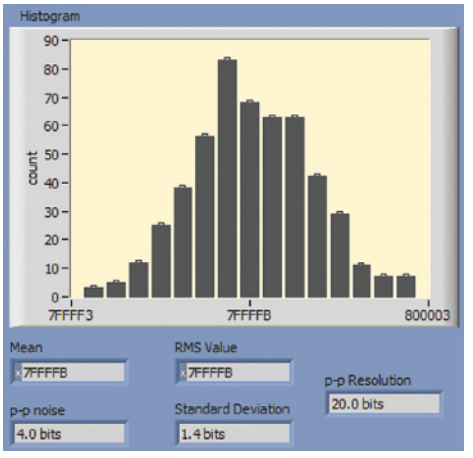


Figure 12. AD7793 performance.

Power Supply Input Protection: The PLC evaluation system uses best practices for electromagnetic compatibility (EMC). A regulated dc supply (18 V to 36 V) is connected to the board through a 2- or 3-wire interface. This supply must be protected against faults and electromagnetic interference (EMI). The following precautions, shown in Figure 13, were taken in the board design to ensure that the PLC evaluation system will survive any interference that may be generated on the power ports.

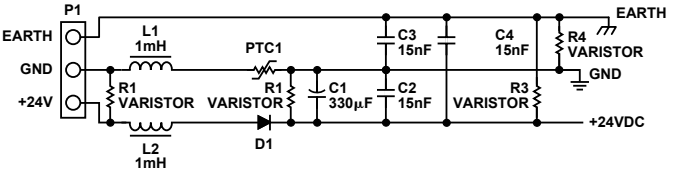


Figure 13. Power supply input protection.

- A varistor, R1, is connected to ground adjacent to the power input ports. During normal operation, the resistance of R1 is very high (megohms), so the leakage current is very low (microamperes). When an electric current surge (caused by lightning, for example) is induced on the port, the varistor breaks down, and tiny voltage changes produce rapid current changes. Within tens of nanoseconds, the resistance of the varistor drops dramatically. This low-resistance path allows the unwanted energy surge to return to the input, thus protecting the IC circuitry. Three optional varistors (R2, R3, and R4) are also connected in the input path to provide protection in cases when the PLC board is powered using the 3-wire configuration. The varistors typically cost well under one US dollar.
- A positive temperature coefficient resistor, PTC1, is connected in series with the power input trace. The PTC1 resistance appears very low during normal operation, with no impact to the rest of the circuit. When the current exceeds the nominal, PTC1's temperature and resistance rapidly increase. This high-resistance mode limits the current and protects the input circuit. The resistance returns to its normal value when the current flow decreases to the nominal limit.

- *Y capacitors* C2, C3, and C4 suppress the common-mode conductive EMI when the PLC board operates with a connection to EARTH. These safety capacitors require low resistance and high voltage endurance. Designers must use Y capacitors that have UL or CAS certification and comply with the regulatory standard for insulation strength.
- Inductors L1 and L2 filter out the common-mode conducted interference coming in from the power ports. Diode D1 protects the system from reverse voltages. A general-purpose silicon or Schottky diode specifying a low forward voltage at the working current can be used.

Analog Input Protection: The PLC board can accommodate both voltage and current inputs. Figure 14 shows the input structure. Load resistor R5 is switched in for current mode. Resistors R6 and R7 attenuate the input. Resistor R8 sets the gain of the AD8220.

These analog input ports can be subjected to electric surge or electrostatic discharge on the external terminal connections. Transient voltage suppressors (TVS's) provide highly effective protection against such discharges. When a high-energy transient appears on the analog input, the TVS goes from high impedance to low impedance within a few nanoseconds. It can absorb thousands of watts of surge power and clamp the analog input to a preset voltage, thus protecting precision components from being damaged by the surge. Its advantages include fast response time, high transient power absorption, low leakage current, low breakdown voltage error, and small package size.

Instrumentation amplifiers are often used to process the analog input signal. These precision, low-noise components are sensitive to interference, so the current flowing into the analog input should be limited to less than a few milliamperes. External Schottky diodes generally protect the instrumentation amplifier. Even when internal ESD protection diodes are provided, the use of external diodes allows smaller limiting resistors and lower noise and offset errors. Dual series Schottky barrier diodes D4-A and D4-B divert the overcurrent to the power supply or ground.

When connecting external sensors, such as thermocouples (TCs) or resistance temperature devices (RTDs), directly to the ADC, similar protection is needed, as shown in Figure 15.

- Two quad TVS networks, D5-C and D5-D, are put in after the J2 input pins to suppress transients coming from the port.
- C7, C8, C9, R9, and R10 form the RF attenuation filter ahead of the ADC. The filter has three functions: to remove as much RF energy from the input lines as possible, to preserve the ac signal balance between each line and ground, and to maintain a high enough input impedance over the measurement bandwidth to avoid loading the signal source. The –3-dB differential-mode and common-mode bandwidth of this filter are 7.9 kHz and 1.6 MHz, respectively. The RTD input channel to AIN2+ and AIN2– is protected in the same manner.

Analog Output Protection: The PLC evaluation system can be software-configured to output analog voltages or currents in various ranges. The output is provided by the AD5422 precision, low-cost, fully integrated, 16-bit digital-to-analog converter, which offers a programmable current source and programmable voltage output. The AD5422 voltage and current outputs may be directly connected to the external loads, so they are susceptible to voltage surges and EFT pulses.

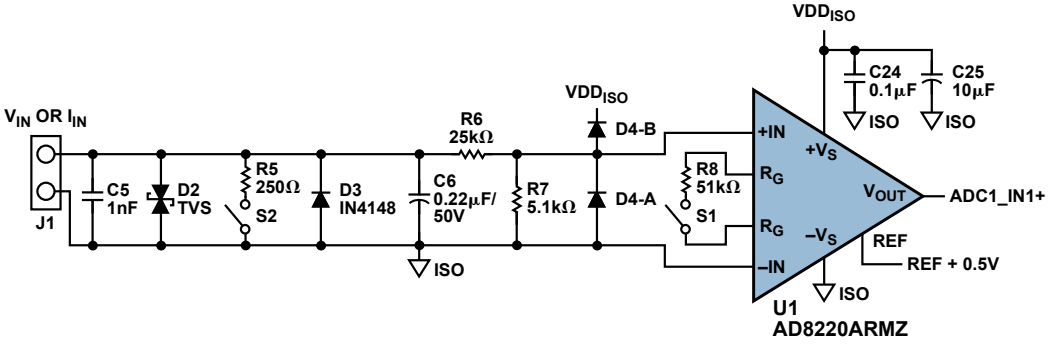


Figure 14. Analog input protection.

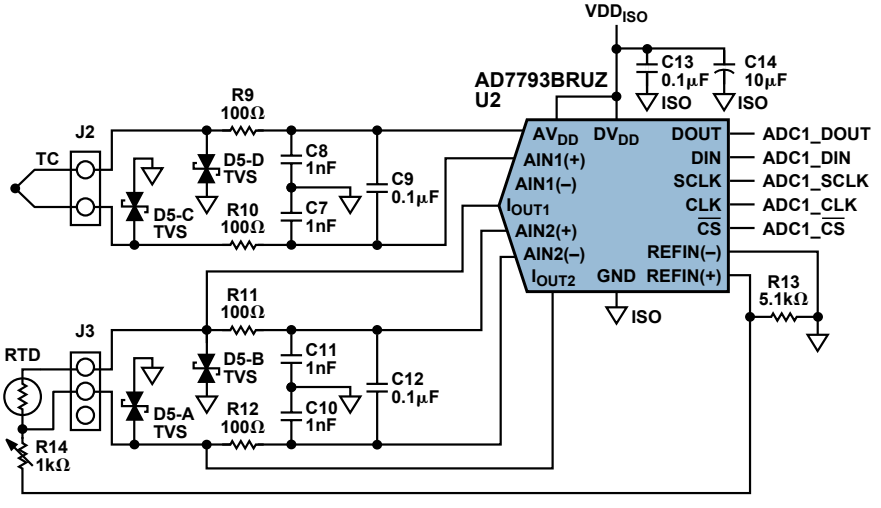


Figure 15. Analog input protection.

The output structure is shown in Figure 16.

- A TVS (D11) is used to filter and suppress any transients coming from Port J5.
- A nonconductive ceramic ferrite bead (L3) is connected in series with the output path to add isolation and decoupling from high-frequency transient noises. At low frequencies (<100 kHz), ferrites are inductive; thus, they are useful in low-pass LC filters. Above 100 kHz, ferrites become resistive, an important characteristic in high-frequency filter designs. The ferrite bead provides three functions: localizing the noise in the system, preventing external high frequency noise from reaching the AD5422, and keeping internally generated noise from propagating to the rest of the system. When ferrites saturate, they becomes nonlinear and lose their filtering properties. Thus, the dc saturation current of the ferrites must not go over their limit, especially when producing high currents.
- Dual series Schottky barrier diodes D9-A and D9-B divert any overcurrent to the positive or the negative power supply. C22 provides the voltage output buffer and the phase compensation when the AD5422 drives capacitive loads up to 1 μF.
- The protection circuitry on the current output channel is quite similar to that on the voltage output channel except that a 10-Ω resistor (R17) replaces the ferrite bead. The current output from the AD5422 is boosted by the external discrete NPN transistor Q1. The addition of the external boost transistor will reduce the power dissipated in the AD5422 by reducing the current flowing in the on-chip output transistor. The breakdown voltage BV_{CEO} of Q1 should be greater than 60 V. The external boost capability is useful in applications where the AD5422 is used at the extremes of the supply voltage, load current, and temperature range. The boost transistor can also be used to reduce the amount of temperature-induced drift, thus minimizing the drift of the on-chip voltage reference and improving the device's drift and linearity.
- A 15-kΩ, precision, low-drift current-setting resistor (R15) is connected to R_{SET} to improve stability of the current output over temperature.
- The PLC demo system can be configured to provide a voltage output higher than 15 V when the AD5422 is powered by an external voltage. A TVS is used to protect the power input port. Diodes D6 and D7 provide protection from reverse biasing. All the supplies are decoupled by 10-μF solid tantalum electrolytic and 0.1-μF ceramic capacitors.

IEC Tests and Results: The results in Table 3 show the deviations of the DAC output that occurred during the testing. The output recovered to the original values after the tests were completed. This is generally referred to as Class B. Class A means that the deviation was within the allowed system accuracy *during* the test. Typical industrial control system accuracies are approximately 0.05%.

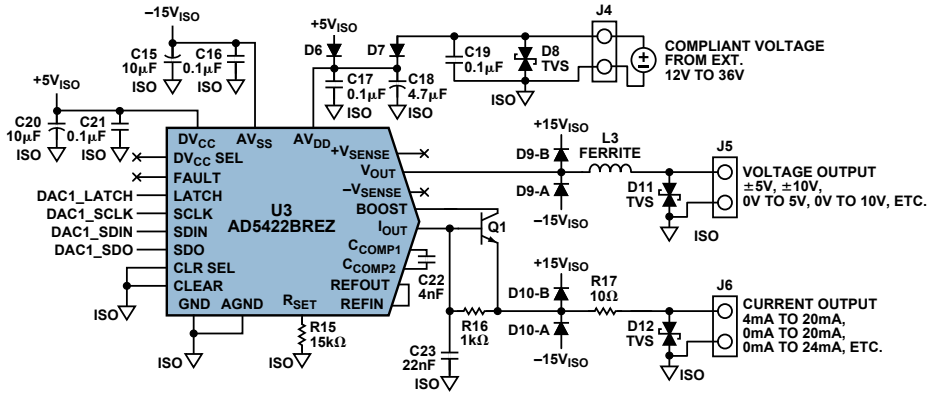


Figure 16. Analog output protection.

Table 3. IEC Test Results

Test Item	Description	Result
EN and IEC 61000-4-2	Electrostatic discharge (ESD) ±4 kV VCD	Max deviation 0.32% for CH3 Class B
	Electrostatic discharge (ESD) ±8 kV HCD	Max deviation 0.28% for CH3 Class B
EN and IEC 61000-4-3	Radiated immunity 80 MHz to 1 GHz 10 V/m, vertical antenna polarization	Max deviation 0.09% for CH1, 0.30% for CH3 Class B
	Radiated immunity 80 MHz to 1 GHz 10 V/m, horizontal antenna polarization	Max deviation −0.04% for CH1, 0.22% for CH3 Class B
	Radiated immunity 1.4 GHz to 2 GHz 3 V/m, vertical antenna polarization	Max deviation 0.01% for CH1, −0.09% for CH3 Class B
	Radiated immunity 1.4 GHz to 2 GHz 3 V/m, horizontal antenna polarization	Max deviation 0.01% for CH1, 0.09% for CH3 Class B
EN and IEC 61000-4-4	Electrically fast transient (EFT) ±2 kV power port	Max deviation −0.12% for CH3 Class B
	Electrically fast transient (EFT) ±1 kV signal port	Max deviation −0.02% for CH3 Class A
EN and IEC 61000-4-5	Power line surge, ±0.5 kV	No board or part damage occurred, passed with Class B
EN and IEC 61000-4-6	Conducted immunity test on power cord, 10 V/m for 5 minutes	Max deviation 0.09% for CH3 Class B
	Conducted immunity test on input/output cable 10 V/m for 5 minutes	Max deviation −0.93% for CH3 Class B
EN and IEC 61000-4-8	Magnetic immunity horizontal antenna polarization	Max deviation −0.01% for CH3 Class A
	Magnetic immunity vertical antenna polarization	Max deviation −0.02% for CH3 Class A

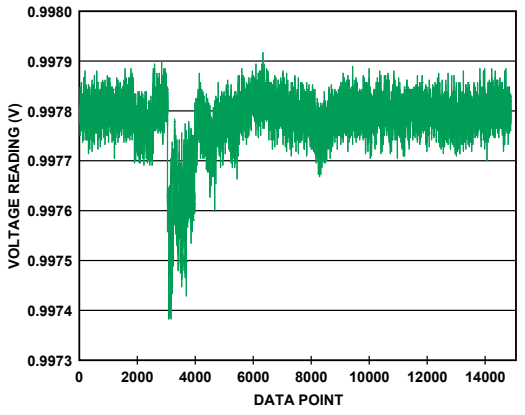


Figure 17. DAC channel dc voltage output. Radiated immunity 80 MHz to 1 GHz @ 10 V/mH.

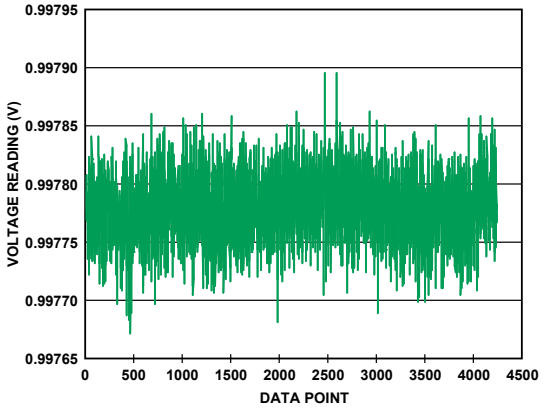


Figure 18. DAC channel 1 dc voltage output. Radiated immunity 1.4 GHz to 2 GHz @ 3 V/mH.

Typical System Configuration: Figure 19 shows a photo of the evaluation system and how a typical system might be configured. The input channels can readily accept both loop-powered and nonloop-powered sensor inputs, as well as the standard industrial current and voltage inputs. The complete design uses Analog Devices converters, isolation technology, processors, and power-management products, allowing customers to easily evaluate the whole signal chain.

Authors

Colm Slattery [colm.slattery@analog.com] graduated from the University of Limerick with a bachelor's degree in engineering. In 1998, he joined Analog Devices as a test engineer in the DAC group. Colm spent three years working for ADI in China and is currently working as an applications engineer in the Precision Converters group in Limerick, Ireland.

Derrick Hartmann [derrick.hartmann@analog.com] is an applications engineer in the DAC group at Analog Devices in Limerick, Ireland. Derrick joined ADI in 2008 after graduating with a bachelor's degree in engineering from the University of Limerick.

Li Ke [li.ke@analog.com] joined Analog Devices in 2007 as an applications engineer with the Precision Converters product line, located in Shanghai, China. Previously, he spent four years as an R&D engineer with the Chemical Analysis group at Agilent Technologies. Li received a master's degree in biomedical engineering in 2003 and a bachelor's degree in electric engineering in 1999, both from Xi'an Jiaotong University. He has been a professional member of the Chinese Institute of Electronics since 2005.

References

[1] http://en.wikipedia.org/wiki/Programmable_logic_controller.
[2] http://en.wikipedia.org/wiki/Distributed_control_system.
[3] www.analog.com/en/digital-to-analog-converters/products/evaluation-boardstools/CU_eb_PLC_DEMO_SYSTEM/resources/fca.html.
[4] Information on all ADI components can be found at www.analog.com.
[5] www.analog.com/en/interface/digital-isolators/products/CU_over_iCoupler_Digital_Isolation/fca.html.
[6] www.analog.com/en/interface/digital-isolators/products/overview/CU_over_isoPower_Isolated_dc-to-dc_Power/resources/fca.html.
[7] www.analog.com/en/analog-microcontrollers/products/index.html.
[8] www.ni.com/labview.

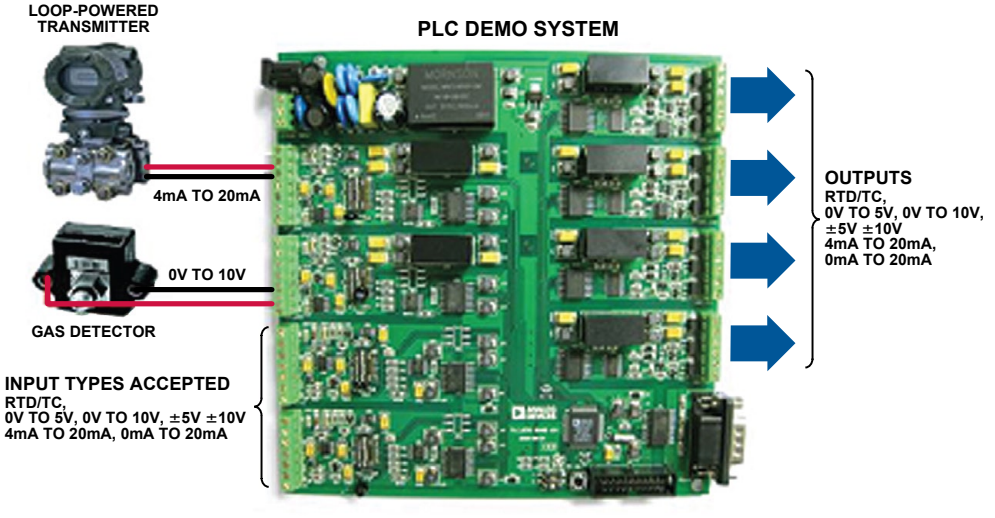


Figure 19. Industrial control evaluation system.

Skin Impedance Analysis Aids Active and Passive Transdermal Delivery

By Liam Riordan

Drug delivery is one of the fastest growing areas in the pharmaceutical industry, with leading firms actively developing alternatives to injections. Options such as oral, topical, pulmonary (inhaler type), nanotechnology enabled, and transdermal drug delivery systems are all current research areas. Transdermal methods, which feature noninvasive delivery of medication through the patient's skin, overcome the skin's protective barrier in one of two ways: passive absorption or active penetration.

The transdermal patch is one of the most common methods of passive drug delivery. Applied to a patient's skin, it safely and comfortably delivers a defined dose of medication over a controlled period of time. The drug is absorbed through the skin into the bloodstream. The nicotine patch is a prime example, but other common uses include motion sickness, hormone replacement therapy, and birth control. Passive delivery has two major disadvantages: the speed of drug absorption is dependent on the skin impedance, and only a limited number of drugs are capable of diffusing through the skin's protective barrier at acceptable rates. As a result, major investment has been undertaken on active methods of transdermal drug delivery. Active methods include using ultrasonic energy to speed up drug diffusion, using RF energy to create microchannels through the stratum corneum (outer layer of the epidermis), and *iontophoresis*.

Iontophoresis uses electrical charge to actively transport a drug through the skin into the bloodstream. The device consists of two chambers that contain charged drug molecules. The positively charged anode will repel a positively charged chemical, while the negatively charged cathode will repel a negatively charged chemical. The electromagnetic field developed between the two chambers actively propagates the medicine through the skin in a controlled manner.

Skin impedance is a key variable for transdermal delivery. The complex impedance, which depends on age, race, weight, activity level, and other factors, is frequency dependent and difficult to model. Dynamic measurement of skin impedance offers an accurate and practical solution for optimal drug delivery.

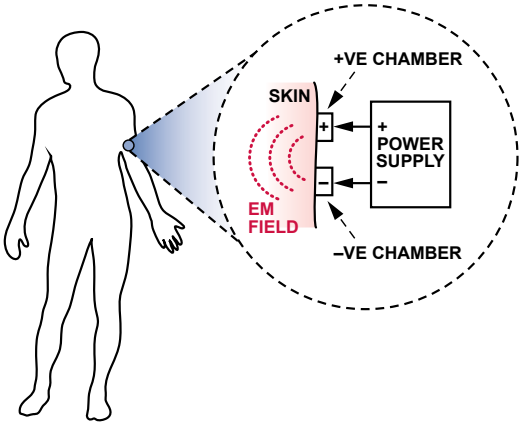


Figure 1. Iontophoresis.

Impedance spectroscopy facilitates accurate analysis of complex impedances such as human skin, leveraging the fact that resistor, capacitor, and inductor impedances vary differently with frequency. As frequency increases, a resistor's impedance remains constant; a capacitor's impedance decreases; and an inductor's impedance increases. Exciting a test impedance with a known ac waveform makes it possible to determine the resistive, inductive, and capacitive components of the unknown impedance. Direct digital synthesizers[1] (DDS) have flexible phase, frequency, and amplitude; sweep capability; and programmability—making them ideal for exciting unknown impedances. Embedded digital signal processing and enhanced frequency control allow the devices to generate synthesized analog or digital frequency-stepped

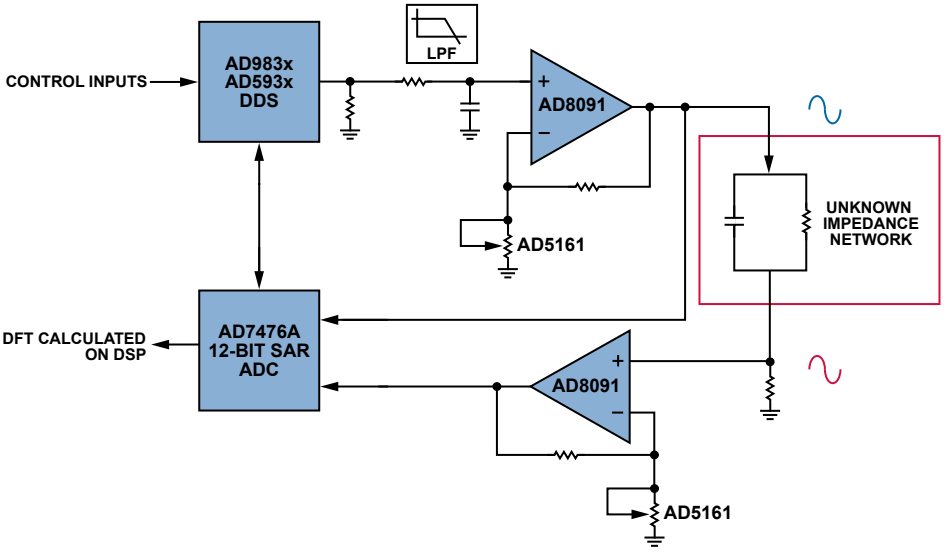


Figure 2. Simple impedance analyzer.

waveforms. Figure 2 shows a block diagram of a simple impedance analyzer. The ac waveform generated by the AD9834[2] complete, low-power, 75-MHz DDS is filtered, buffered, and scaled by the AD8091 high-speed, rail-to-rail op-amp. Another AD8091[3] buffers the response signal and scales it to match the input range of the AD7476A[4] 12-bit, 1-MSPS, successive-approximation ADC.

This simple signal chain masks some underlying challenges, however. First, the ADC must synchronously sample the excitation and response waveforms over frequency so that phase information can be maintained. Optimizing this process is key to overall performance. In addition, numerous discrete components are involved, so varying tolerances, temperature drift, and noise will degrade measurement accuracy, particularly when working with small signals.

The AD5933[5] 12-bit, 1-MSPS integrated impedance converter network analyzer overcomes these limitations by combining the DDS waveform generator and the SAR ADC on a single-chip, as shown in Figure 3.

The AD5933 has an output impedance of a few hundred ohms, depending on the output range. This impedance could swamp the unknown impedance, so an AD8531[6] op amp buffers the signal, as shown in Figure 4. Note that the receive side of the AD5933 is internally biased to $V_{DD}/2$, so this same voltage must be applied to the noninverting terminal of the external amplifier to prevent saturation. For safety, all excitation voltages and currents need to be signal conditioned, attenuated, and filtered before they are applied to human tissue.

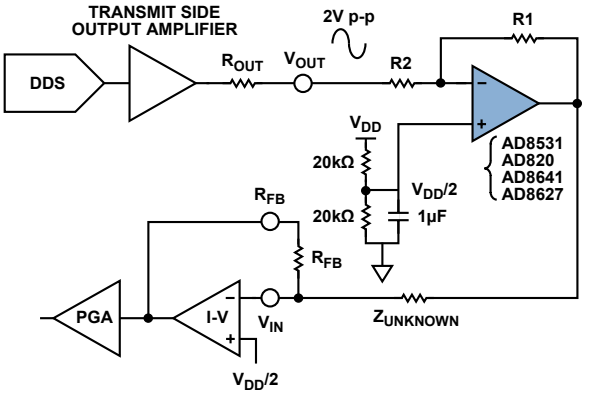


Figure 4. Low-impedance measurement configuration.

References

[1] www.analog.com/en/rfif-components/direct-digital-synthesis-dds/products/index.html.

[2] www.analog.com/en/rfif-components/direct-digital-synthesis-dds/ad9834/products/product.html.

[3] www.analog.com/en/audiovideo-products/video-ampsbuffersfilters/ad8091/products/product.html.

[4] www.analog.com/en/analog-to-digital-converters/ad-converters/ad7476a/products/product.html.

[5] www.analog.com/en/rfif-components/direct-digital-synthesis-dds/ad5933/products/product.html.

[6] www.analog.com/en/audiovideo-products/display-driver-electronics/ad8531/products/product.html.

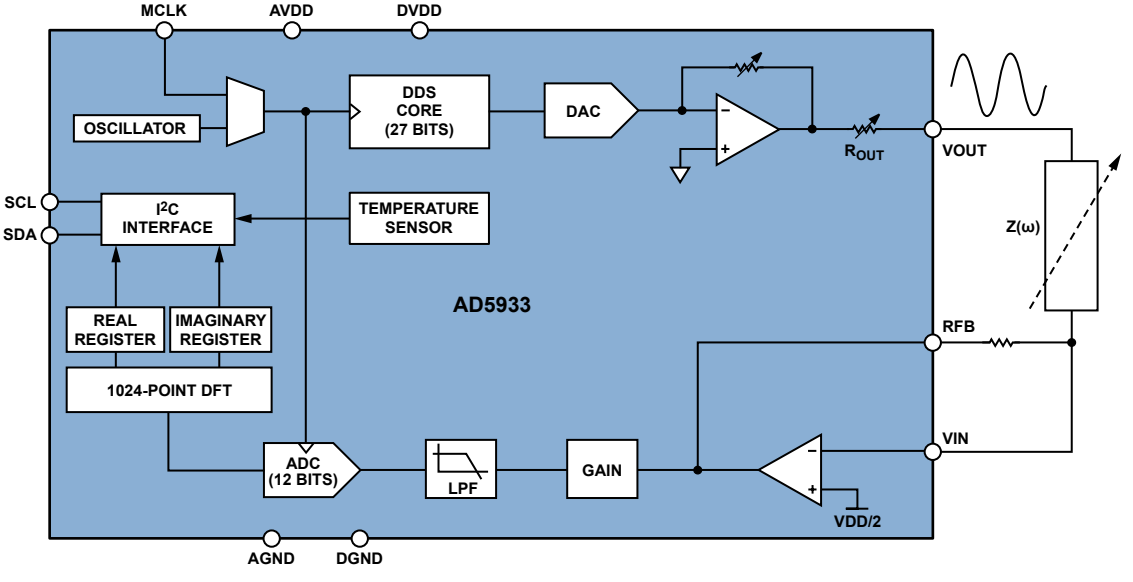


Figure 3. AD5933 functional block diagram.

Accelerometers—Fantasy and Reality

By Harvey Weinberg

As applications engineers supporting ADI's compact, low-cost, gravity-sensitive *i*MEMS® accelerometers,[1] we get to hear lots of creative ideas about how to employ accelerometers in useful ways, but sometimes the suggestions violate physical laws! We've rated some of these ideas on an informal scale, from real to dream land:

- **Real** – A real application that actually works today and is currently in production.
- **Fantasy** – An application that could be possible if we had much better technology.
- **Dream Land** – Any practical implementation we can think of would violate physical laws.

Washing Machine Load Balancing. Unbalanced loads during the high-speed spin-cycle cause washing machines to shake and, if unrestrained, they can even "walk" across the floor. An accelerometer senses acceleration during the spin cycle. If an imbalance is present, the washing machine[2] redistributes the load by jogging the drum back and forth until the load is balanced.

Real. With better load balance, faster spin rates can be used to wring more water out of clothing, making the drying process more energy efficient—a good thing these days! As an added benefit, fewer mechanical components are required for damping the drum motion, making the overall system lighter and less expensive. Correctly implemented, transmission and bearing service life is extended because of lower peak loads present on the motor. This application is in production.

Machine Health Monitors. Many industries change or overhaul mechanical equipment using a calendar-based preventive maintenance schedule. This is especially true in applications where one cannot tolerate unscheduled downtime. So, machinery with plenty of service life left is often prematurely rebuilt at a cost of millions of dollars across many industries. By embedding accelerometers in bearings or other rotating equipment, service life can be extended without risking sudden failure. The accelerometer senses the vibration of bearings or other rotating equipment to determine their condition.

Real. Using the vibration[3] "signature" of bearings to determine their condition is a well proven and industry-accepted method of equipment maintenance, but wide measurement bandwidth is needed for accurate results. Before the release of the ADXL001,[4] the cost of accelerometers and associated signal conditioning equipment had been too high. Now, its wide bandwidth (22 kHz) and internal signal conditioning make the ADXL001 ideal for low-cost bearing maintenance.

Automatic Leveling. Accelerometers measure the absolute inclination of an object, such as a large machine or a mobile home. A microcontroller uses the tilt information to automatically level the object.

Real to Fantasy (depending on the application). Self-leveling is a very demanding application, as absolute precision is required. Surface micromachined accelerometers have impressive resolution, but absolute tilt measurement with high accuracy (better than 1° of inclination) requires temperature stability and hysteresis performance that today's surface-micromachined accelerometers cannot achieve. In applications where the temperature range is modest, high stability accelerometers like the ADXL203[5] are up to the task. Applications needing absolute accuracy to within ±5° over a wide temperature range can be handled as well. However, more precise leveling over a wide temperature range requires external temperature compensation. Even with external temperature compensation absolute accuracy of better than ±0.5° of inclination is difficult to achieve. Some applications are currently in production.

Human Interface for Mobile Phones. The accelerometer allows the microcontroller to recognize user gestures, enabling one-handed control of mobile devices.

Real. Mobile phone[6] screens eat up most of the available real estate for controls. Using an accelerometer for user interface functions allows mobile phone makers to add "buttonless" features such as Tap/Double Tap (emulating a mouse click/double click), screen rotation, tilt controlled scrolling, and ringer control based on orientation—to name just a few. In addition, mobile phone makers can use the accelerometer to improve accuracy and usability of navigation functions and for other new applications. This application is currently in production.

Car Alarm. The accelerometer senses if a car is jacked up or being picked up by a tow truck and sets off the alarm.

Real. One of the most popular methods of auto theft is to steal the car by simply towing it away. Conventional car alarms[7] do not protect against this. Shock sensors cannot measure changes in inclination, and ignition-disabling systems are ineffectual. This application takes advantage of the high-resolution capabilities of the ADXL213[8]. If the accelerometer measures an inclination change of more than 0.5° per minute, the alarm is sounded—hopefully scaring off the would-be thief. Good temperature stability is needed as no one wants their car alarm to go off because of changes in the weather, making the highly stable ADXL213 an ideal choice. This application is currently in production in OEM and after-market automotive anti-theft systems.

Ski Bindings. The accelerometer measures the total shock energy and signature to determine if the binding should release.

Fantasy. Mechanical ski bindings are highly evolved, but limited in performance. Measuring the actual shock experienced by the skier would accurately determine if a binding should release. Intelligent systems could take each individual's capability and physiology into account. This is a practical accelerometer application, but current battery technology makes it impractical. Small, lightweight batteries that perform well at low temperature will eventually enable this application.

Personal Navigation. In this application, position is determined by dead reckoning (double integration of acceleration over time to determine actual position).

Dream Land. Long-term integration results in a large error due to the accumulation of small errors in measured acceleration. Double integration compounds the errors (t^2). Without some way of resetting the actual position from time to time, huge errors result. This is analogous to building an integrator by simply putting a capacitor across an op amp. Even if an accelerometer's accuracy could be improved by ten or one hundred times over what is currently available, huge errors would still eventually result. They would just take longer to happen.

Accelerometers can be used with a GPS navigation system[9] when the GPS signals are briefly unavailable. Short integration periods (a minute or so) can give satisfactory results, and clever algorithms can offer good accuracy using alternative approaches. When walking, for example, the body moves up and down with each step. Accelerometers can be used to make very accurate pedometers that can measure walking distance to within ±1%.

Subwoofer Servo Control. An accelerometer mounted on the cone of the subwoofer provides positional feedback to servo out distortion.

Real. Several active subwoofers with servo control are on the market today. Servo control can greatly reduce harmonic distortion and power compression. Servo control can also electronically lower the *Q* of the speaker/enclosure system, enabling the use of smaller enclosures, as described in *Loudspeaker Distortion Reduction*.[10] The ADXL193[11] is small and light; its mass, added to that of the loudspeaker cone, does not change the overall acoustic characteristics significantly.

Neuromuscular Stimulator. This application helps people who have lost control of their lower leg muscles to walk by stimulating muscles at the appropriate time.

Real. When walking, the forefoot is normally raised when moving the leg forward, and then lowered when pushing the leg backward. The accelerometer is worn somewhere on the lower leg or foot, where it senses the position of the leg. The appropriate muscles are then electronically stimulated to flex the foot as required.

This is a classic example of how micromachined accelerometers have made a product feasible. Earlier models used a liquid tilt sensor or a moving ball bearing (acting as a switch) to determine the leg position. Liquid tilt sensors had problems because of sloshing of the liquid, so only slow walking was possible. Ball-bearing switches were easily confused when walking on hills. An accelerometer measures the differential between leg back and leg forward, so hills do not fool the system and no liquid slosh problem exists. The low power consumption of the accelerometer allows the system to work with a small lithium battery, making the overall package unobtrusive. This application is in production.

Car-Noise Cancellation. The accelerometer senses low-frequency vibration in the passenger compartment; the noise-cancellation system nulls it out using the speakers in the stereo system.

Dream Land. While the accelerometer has no trouble picking up the vibration in the passenger compartment, noise cancellation is highly phase dependent. While we can cancel the noise at one location (around the head of the driver, for example), it will probably increase at other locations.

Conclusion

Because of their high sensitivity, small size, low cost, rugged packaging, and ability to measure both static and dynamic acceleration forces, surface micromachined accelerometers have made numerous new applications possible. Many of them were not anticipated because they were not thought of as classic accelerometer applications. The imagination of designers now seems to be the limiting factor in the scope of potential applications—but sometimes designers can become too imaginative! While performance improvements continue to enable more applications, it's wise to try to stay away from "solutions" that violate the laws of physics.

References

[1] www.analog.com/en/sensors/inertial-sensors/adxl193/products/product.html.

[2] www.analog.com/en/industrial-solutions/white-goods/applications/index.html.

[3] www.analog.com/en/industrial.

[4] www.analog.com/en/sensors/inertial-sensors/adxl001/products/product.html.

[5] www.analog.com/en/sensors/inertial-sensors/adxl203/products/product.html.

[6] www.analog.com/en/wireless-solutions/featurephonesmartphone/applications/index.html.

[7] www.analog.com/static/imported-files/application_notes/50324364571097434954321528495730car_app.pdf.

[8] www.analog.com/en/sensors/inertial-sensors/adxl213/products/product.html.

[9] www.analog.com/en/automotive-solutions/navigation/applications/index.html.

[10] Greiner, Richard A. and Travis M. Sims, Jr. *Loudspeaker Distortion Reduction*. JAES Vol. 32, No. 12. www.aes.org/e-lib/browse.cfm?elib=4467.

[11] www.analog.com/en/sensors/inertial-sensors/adxl193/products/product.html.

Digital Isolator Simplifies USB Isolation in Medical and Industrial Applications

By Mark Cantrell

The personal computer (PC), currently the standard information-processing device for office and home use, communicates with most peripherals using the *universal serial bus* (USB). Standardization, cost, and the availability of software and development tools have made the PC very attractive as a host-processor platform for medical and industrial applications, but the safety and reliability requirements of these growing markets—especially regarding electrical isolation—are very different from the office environment that has historically driven the design of the personal computer.

In the early days, personal computers were provided with serial and parallel ports as standard interfaces to the outside world. These legacy standards had been inherited from the earliest mainframe computers. Another available communication standard, RS-232, though slow, fit well into medical and industrial environments because it allowed easy implementation of the required robust isolation. Its low speed and point-to-point nature were tolerated because it was universally available and well supported.

USB, which has come to replace RS-232 as a standard port in personal computers and their peripherals, has features that are far superior to the older serial port in nearly every respect. It has been difficult and costly to provide the necessary isolation for medical and industrial applications, however, so USB has been principally used for diagnostic ports and temporary connections.

This article discusses various ways of applying isolation with USB. In particular, a new option, the ADuM4160[1] USB isolator, is now available from Analog Devices. This breakthrough product allows simple, inexpensive isolation of peripheral devices—especially including the D+ and D– lines—increasing the usefulness of USB in medical and industrial applications.

About the Universal Serial Bus (USB)

USB is the serial interface of choice for the PC. Supported by all common commercial operating systems, it enables on-the-fly connection of hardware and drivers. Up to 127 devices can exist on the same hub-and-spoke-style network. Many data transfer modes handle everything from large bulk data transfers for memory devices, to isochronous transfers for streaming media, to interrupt-driven transfers for time-critical data such as mouse movements. USB operates at three data transfer rates: *low speed* (1.5 Mbps), *full speed* (12 Mbps), and *high speed* (480 Mbps). When this system was created, consumer applications were emphasized; connections had to be simple and robust, with controllers and physical-layer signaling absorbing the complexity.

The USB physical layer consists of only four wires: two provide 5-V power and ground to the peripheral device; the other two, D+ and D–, form a twisted pair that can carry differential data (Figure 1). These lines can also carry single-ended data, as well as *idle* states that are implemented with passive resistors. When a device is attached to the bus, currents in the passive resistor configuration negotiate for speed, as well as establish a nondriven idle state. The data is organized into data frames or packets. Each frame can contain bits for clock synchronization, data type identifier, device address, data payload, and an end-of-packet sequence.

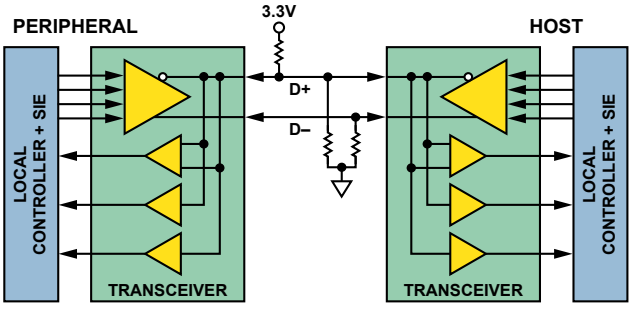


Figure 1. Standard elements of USB.

Control of this complex data structure is handled at each end of the cable by a *serial interface engine* (SIE). This specialized controller—or portion of a larger controller, which usually includes the USB transceiver hardware—takes care of the USB protocol. During *enumeration*,[2] when a peripheral is first connected to the cable, the SIE provides the host with the configuration information and power requirements. During operation, the SIE formats all data according to the required transfer type, as well as provides error checking and automatic fault handling. The SIE handles all flow of control on the bus, enabling and disabling the line drivers and receivers as required. The *host* initiates all transactions, which then follow a well-defined sequence of data exchanges between host and peripheral, including provisions for when data is corrupted and other fault conditions. The SIE may be built into a microprocessor, so it may provide only the D+ and D– lines to the peripheral. Isolating this bus presents several challenges:

1. Isolators are nearly always unidirectional devices, while the D+ and D– lines are bidirectional.
2. The SIE does not provide an external means to determine data transmission direction.
3. Isolators must be compatible with the pull-up and pull-down functions of passive resistors, making them match across the barrier.

Typical approaches to isolate the USB largely seek to sidestep the above challenges.

A First Approach: Move the USB interface completely out of the device that requires isolation (Figure 2). Many devices interface generic serial buses to USB; an RS-232-to-USB interface is shown in this example. The SIE provides a generic serial-interface function; isolation is implemented in the low-speed serial lines. This approach does not capitalize on the advantages of USB, however. All that has been created is a serial port that can be loaded on-the-fly. The interface IC could be customized through firmware changes to identify the peripheral, allowing a custom driver to be created; but each peripheral would require a custom adaptor. Unless the adaptor was permanently affixed to the peripheral, it would be a servicing nightmare. In addition, the speed of the interface would be limited to that of standard RS-232—not close to the throughput of even low-speed USB.

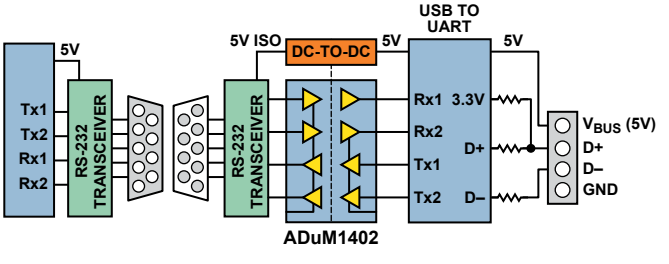


Figure 2. Isolating through RS-232.

A Second Approach: Use a standalone SIE that has an easily isolated interface (Figure 3). Several products on the market use fast unidirectional interfaces, such as SPI, to connect an SIE to a microprocessor. Digital isolators, such as the ADuM1401C 4-channel digital isolator, will allow full isolation of an SPI bus. The SIE contains buffer memory that can be filled by the SPI bus, so the operating speed of the SPI can be largely independent of the speed of the USB. The SIE will negotiate with the USB host for its highest possible connection speed and will dispense data at the negotiated bus speed until it runs out of buffered data. The SIE will then tell the host to retry if more data is expected, allowing time for the SPI interface to refill the buffers for another transfer cycle. Though very effective, this scheme usually requires modifications to peripheral drivers, as well as bypassing existing USB facilities built into the peripheral's microprocessor. This solution is expensive in terms of components and board space.

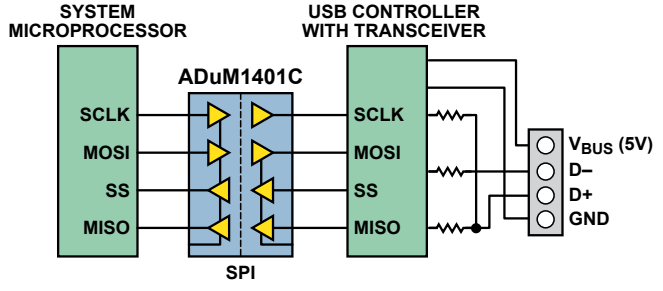


Figure 3. Isolated SIE through an SPI interface.

A Third Approach: If the microprocessor's SIE uses an external transceiver, the data and control lines to the transceiver can be isolated (Figure 4). But USB requires as many as nine unidirectional data lines between an SIE and its transceiver. This represents a significant expense in high-speed digital isolators. In addition, the fastest available digital isolator works at about 150 Mbps. Though much faster than low- and full-speed USB, it can't handle high-speed data, limiting the speed range of the USB interface. This solution is fully compatible with the USB drivers provided for the microprocessor's SIE, lowering development costs, but the many isolation channels required make it expensive to implement. Market trends toward increased integration will obsolete this type of transceiver interface.

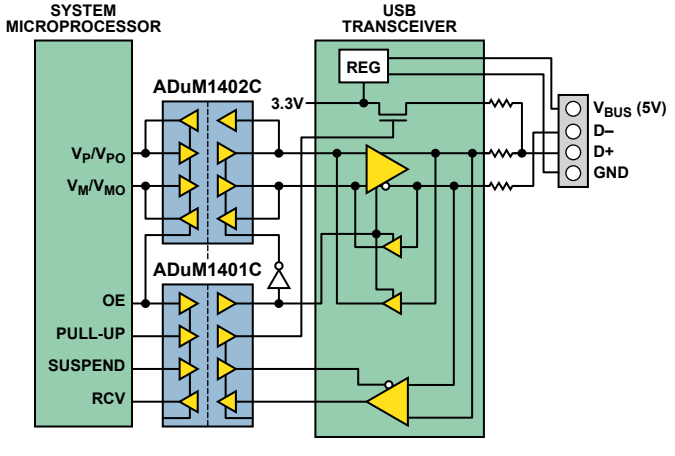


Figure 4. Isolated external USB transceiver.

A Fourth Approach: Insert the isolation *directly* into the D+ and D– lines (Figure 5). This allows D+/D– isolation to be added to existing USB applications without rewriting drivers or adding a redundant SIE, a significant advantage over the other approaches. Isolating the D+ and D– lines complicates the situation, however, as the device must be able to handle flow of control like an SIE, as well as permit application of pull-up resistors and speed determination across its isolation barrier. It should also operate without calling for the overhead of additional device drivers.

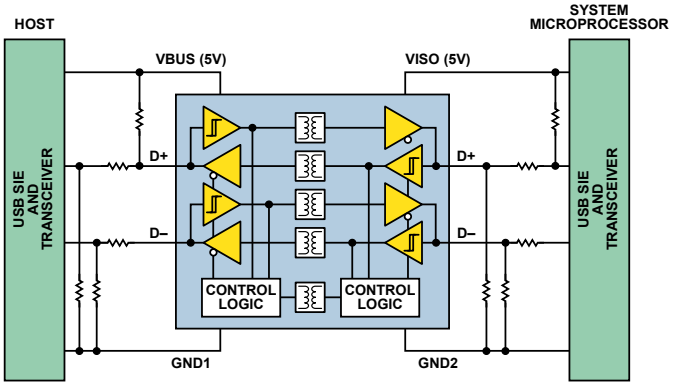


Figure 5. Isolating the D+/D– lines.

These challenges have been met with the ADuM4160 USB isolator (Figure 6), a new chip-scale device that supports direct isolation of low- and full-speed USB D+ and D– lines.

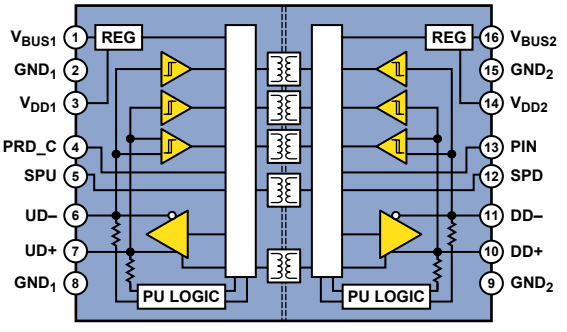


Figure 6. ADuM4160 block diagram.

Analog Devices *i*Coupler® technology[3] is particularly well-suited to construction of a USB isolator. The primary challenges in developing a USB isolator are properly determining the direction of data transmission—and when to disable drivers to allow an idle bus state. The packet-oriented nature of USB data allows a simple method of determining data direction without the overhead of a complete SIE. When the bus is idle, pull-up and pull-down resistors hold the USB in an idle state with no buffers driving the bus.

The ADuM4160 monitors the upstream and downstream segments of the bus, waiting for a transition from either direction. When a transition is detected, it is encoded and transmitted across the barrier. The data is decoded, and the output drivers are enabled to transmit on the other cable segment. From this first transition, the direction of data flow is identified, and the reverse-direction isolation channels are disabled. The isolator continues to transmit data in the same direction as long as data continues to be received. When the USB packet is complete, special data, the end-of-packet (EOP) sequence, is transmitted. The EOP contains a nondifferential signal that should not be included in any data structure. The isolator can distinguish an EOP marker from valid data. This signals that the bus should be returned to the *idle* state. The output drivers are disabled, and the isolator begins to monitor its upstream and downstream inputs for the next transition—which will set the next direction for data transmission.

In addition, watchdog timers return the isolator to its idle state when a bus error occurs. The ADuM4160 takes advantage of the transition-based isolation scheme, one of the core capabilities of *i*Coupler technology.

The isolator must also provide support for pull-up and pull-down resistors. Each side of the isolator supports an independent USB bus segment, with all of the bias resistors present in the idle state. The pull-up resistor signals that a new device on the bus needs to go through the initialization sequence, called *enumeration*. Knowing the operating speed of the peripheral and the time when the pull-up should be connected allows enumeration to begin in a controlled manner. Several factors can affect the status of the upstream pull-up resistor. Different combinations of available upstream and downstream power-supply voltage are possible. The isolator is designed to give predictable operation in all specified combinations of available power. A peripheral would want to delay application of the upstream pull-up resistor at times—if it needs to complete its own local initialization prior to starting the USB enumeration, for example. The ADuM4160 provides a control pin on the downstream side of the part to allow the peripheral to determine when enumeration occurs.

Other features available in the device include the ability to run from either a 5-V or 3.3-V power source. So only one power supply is required in the peripheral; it can be either voltage. The ADuM4160 has also been designed with rugged ESD protection to allow hot plugging of D+ and D– pins to connectors without external protective circuitry in most cases.

The ADuM4160 will likely be used in one of three ways:

- It will be installed in a peripheral to isolate its upstream port. The ADuM4160 was designed with this configuration as the base application. It leads to the simplest power and control configurations (Figure 7).
- It can be used to isolate a hub and therefore all of the peripherals downstream of the hub (Figure 8).
- It can be used in an isolated cable configuration (Figure 9).

The following illustrations show how the ADuM4160 will be connected in each of these applications.

In the peripheral application (Figure 7), where the peripheral has its own source of power, almost no power is required from the USB cable—about 10 mW to run the isolator's upstream side and the pull-up resistor. Since the peripheral operates at a single speed, the isolator is hardwired for the desired speed setting, either *full speed* or *low speed*. If the peripheral port happens to be *high-speed*-capable, then it sends a high-speed "chirp" pattern during enumeration. This would normally initiate negotiations for high-speed operation, but the ADuM4160 blocks the chirp signal and automatically forces the high-speed peripheral to operate at *full speed*. For low-power peripherals that don't have their own supply, an isolated dc-to-dc converter, such as the ADuM5000, can be used to supply the peripheral and the ADuM4160, drawing power from the USB cable.

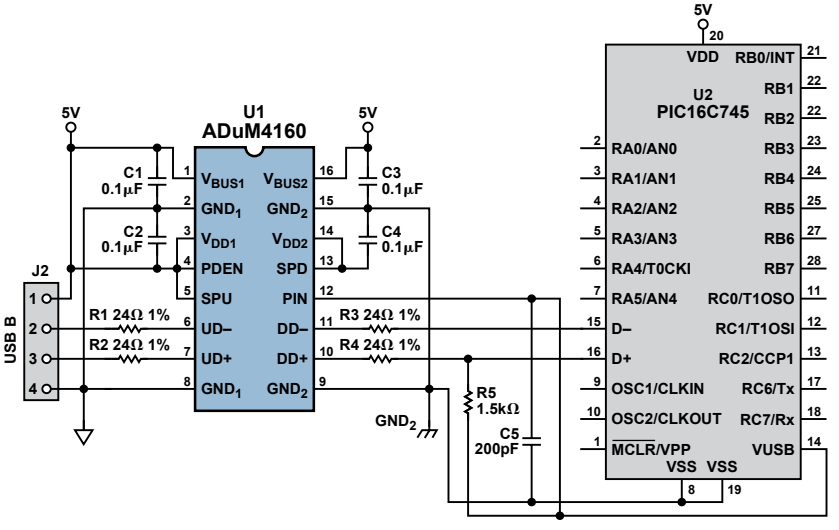


Figure 7. Isolated peripheral port.

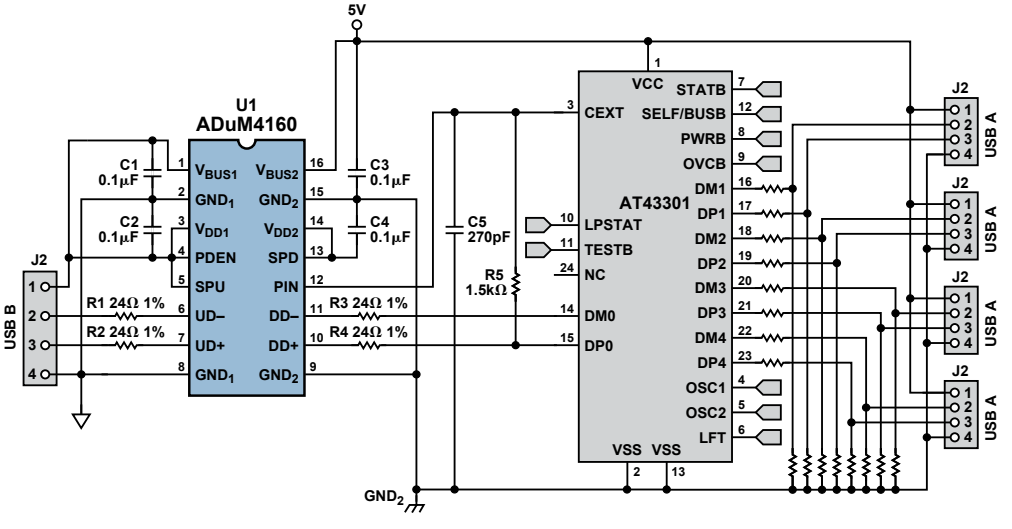


Figure 8. Isolated hub.

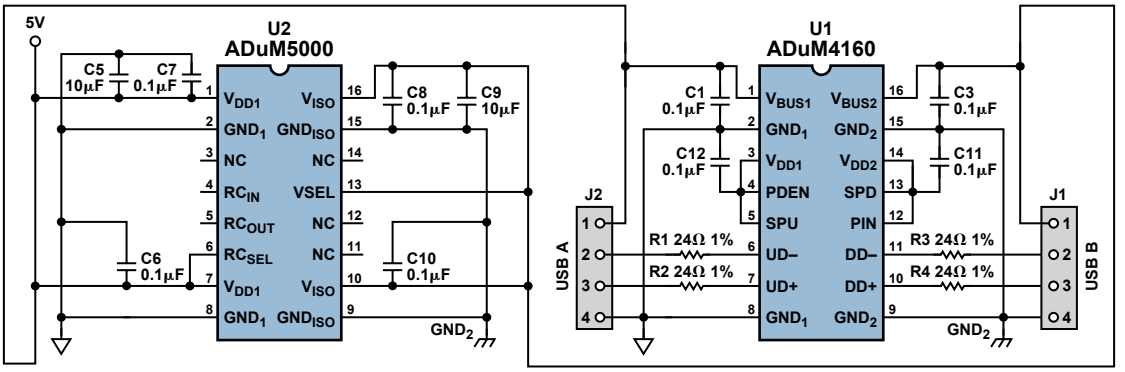


Figure 9. Isolated cable interface including *iso*Power.

Used as a hub isolator (Figure 8), the ADuM4160 treats the hub as its peripheral. The ADuM4160 is set to full speed; the rest of the application is similar to the standard peripheral case discussed above. The hub will be forced to operate at full speed by the isolator's intervention in its chirp function. The hub IC will allow connection to combinations of low- and full-speed devices, even though the isolator runs at a fixed speed. The hub provides power to the isolator's downstream port, and enumeration can begin either at power-up or on a delayed basis. The hub usually requires more power than can be supplied by the upstream cable via an isolated dc-to-dc converter.

Driving an isolated USB cable (Figure 9) requires use of a dc-to-dc converter to supply power to the downstream port and cable. To satisfy the requirements of the USB specification, the downstream segment of the cable must provide 5-V power to the pull-up of the peripheral device. An isolated dc-to-dc converter, such as the ADuM5000, can provide this power with enough left over to provide power for downstream devices with low power requirements. Figure 9 shows the use of an ADuM5000 *iso*Power® device.[4] In this application, the hard-wired speed pins of the ADuM4160 become somewhat inconvenient. The cable will only operate at one USB speed at a time; it must be rewired to switch speed modes, either manually, by simple switches, or with more elaborate circuits, depending on the end-user's requirements.

Conclusion

USB is here to stay. The ADuM4160, a breakthrough isolation product, will allow simple and inexpensive isolation of peripheral devices in USB applications. This, in turn, will increase the penetration of USB into the medical and industrial application space well beyond diagnostic ports and temporary connections. The ADuM4160's focus on providing isolation in the D+/D– lines makes implementation extremely simple. Support for both *full-speed* and *low-speed* operation provides sufficient bandwidth for a wide range of applications.

Author

Mark Cantrell [mark.cantrell@analog.com] provides applications engineering support for the *i*Coupler product line at Analog Devices. Prior to joining ADI, Mark spent six years at California Eastern Laboratories, where he was responsible for applications support for NEC's optocoupler and solid-state-relay product lines. Mark's experience also includes 17 years at Lockheed Martin Missiles and Space, where his job as a radiation-effects test engineer included work on the Gravity Probe B satellite program. Mark received his MS in physics from Indiana University.

References

[1] Information on all ADI components can be found at www.analog.com.

[2] www.lvr.com/usbcenum.htm.

[3] www.analog.com/en/interface/digital-isolators/products/CU_over_iCoupler_Digital_Isolation/fca.html.

[4] www.analog.com/en/interface/digital-isolators/products/overview/CU_over_isoPower_Isolated_dc-to-dc_Power/resources/fca.html.

Automated Calibration Technique Reduces DAC Offset to Less Than 1 mV

By Ken Kavanagh

The transfer function for an N-bit bipolar digital-to-analog converter (DAC) is

$$A = \left(\frac{D}{2^{N-1}} \times G \times V_{FS}\right) - V_{FS} + V_{OS},$$

where A is the analog output, D is the digital input, G is the gain, V_{FS} is the nominal full-scale voltage, and V_{OS} is the offset voltage. For an ideal DAC, $G = 1$ and $V_{OS} = 0$.

The offset error specification, combined with the system requirements, will determine if calibration is needed. The AD5360[1] 16-bit, 16-channel DAC is factory trimmed, but an offset of several millivolts can still exist. The following example shows how a simple software algorithm can reduce an unknown offset to less than 1 mV (typical). This technique can be used for factory calibration, or for offset correction at any point in the DAC's life cycle.

The AD5360's offset DACs are used to set the output range, which can be unipolar positive, unipolar negative, bipolar centered, or bipolar skewed. The default value of the offset DACs set a ±10-V output range when a 5-V reference is used. The offset DACs also have an offset error. The 16 DAC outputs are factory trimmed with the offset DACs at their default value, so these errors are trimmed out. As the offset DACs are changed, their offset error affects the offset errors of the main DAC outputs.

Two features of the AD5360 simplify offset calibration: a GPIO pin, which can have its status determined by reading a register; and an integrated monitor multiplexer, which allows any of the 16 DAC outputs or two external voltages to be switched to a single pin under software control.

Theory of Operation

The offset calibration procedure is as follows: A comparator monitors two voltages: MON_OUT, the DAC output containing an unknown offset, and SIGGND, the ground reference for the DACs. The comparator output indicates whether the unknown offset is above or below SIGGND. The output of the DAC is incremented or decremented until the comparator output toggles, indicating that the DAC output is as close to SIGGND as the comparator can detect. The comparator output is connected to the GPIO pin; its status can be determined by reading the appropriate register. Figure 1 shows the circuit diagram.

The AD5360's multiplexer connects the selected DAC output to MON_OUT. Its switches have a low but finite RDSON, so any current drawn from MON_OUT creates a voltage drop across R_{DS} and, hence, an output error. To prevent this, MON_OUT is buffered by an AD8597[2] low-noise amplifier. The low-pass filter following the amplifier reduces the amount of noise seen by the AD790[3] fast, precision comparator and prevents false triggering. The AD790 can be operated from ±15V supplies, making it compatible with the AD5360. In addition, the AD790 has a 15-V maximum differential input voltage, so it can tolerate the output voltages from the AD5360 without attenuation. In Figure 1, the comparator output will be low if the channel offset is positive, indicating that the output voltage needs to be reduced to remove the offset. The comparator output will be high if the channel offset is negative, indicating that the output voltage needs to be increased to remove the offset.

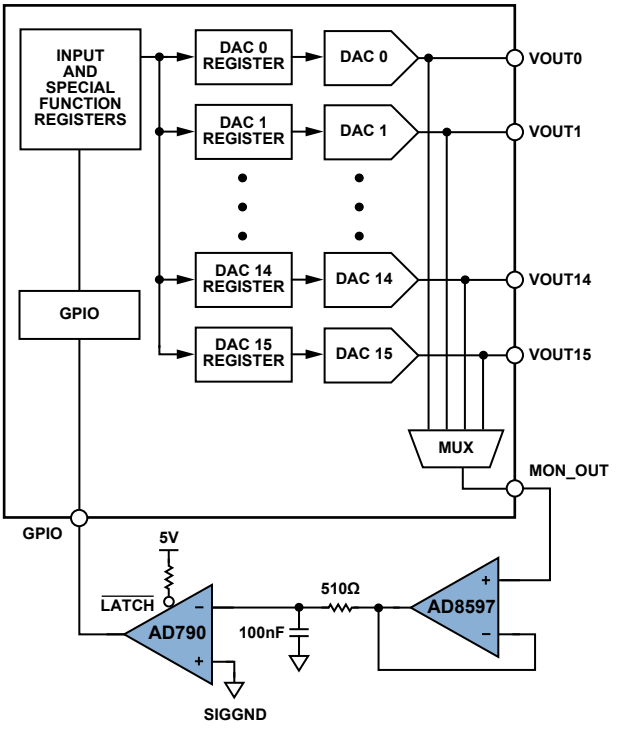


Figure 1. Circuit diagram.

Configuring the Monitor Multiplexer and GPIO of the AD5360

Writing 0x0C002X, where X is the required output channel, to the Monitor Special Function Register enables the monitor multiplexer and selects the required channel. When this is done, MON_OUT will give the same output voltage as the selected channel. Bit 0 of the GPIO Special Function Register indicates the status of the GPIO pin. Consult the AD5360 data sheet for information on reading and writing registers.

Calibrating a Channel

Figure 2 shows the calibration routine. The DAC channel is loaded with 0x8000, which should ideally provide a voltage equal to SIGGND (i.e., 0 V). In this example, the DAC channel is assumed to have a negative offset. Reading the GPIO register shows that the comparator output is low, indicating that the input must be incremented until the output toggles. As progressively higher codes are written to the DAC input register, the GPIO register is read until the comparator toggles. Figure 2 shows that this happens at code 0x8009. The AD790 has a maximum hysteresis band of 0.65 mV, so reducing the DAC code again allows a more accurate determination of the DAC offset. The comparator output toggles again at code 0x8006. The value that puts the output closest to SIGGND thus lies somewhere between codes 0x8006 and 0x8009. In this example, code 0x8007 is the better choice, but there is no way to determine which code will give the best output using this system. The comparator and op-amp offsets make it impossible to determine which code within the two comparator trip points gives the best result, but in either case the DAC channel is typically <1 mV from SIGGND.

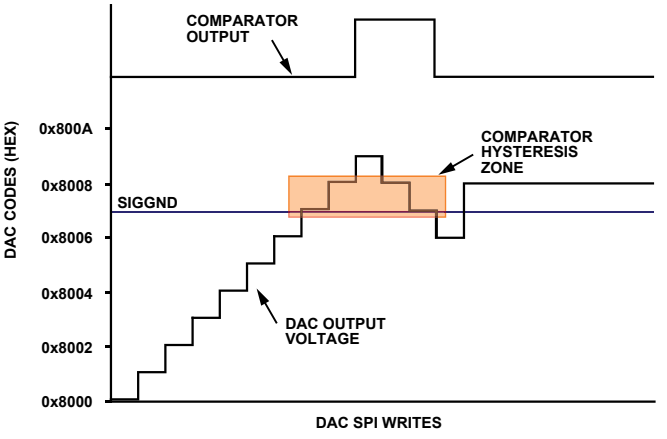


Figure 2. Calibration routine.

Conclusion

This technique makes it possible to reduce an unknown offset error to less than 1 mV using a software algorithm and a few external components.

References

[1] www.analog.com/en/other-products/automatic-test-equipment/ad5360/products/product.html.

[2] www.analog.com/en/amplifiers-and-comparators/operational-amplifiers-op-amps/ad8597/products/product.html.

[3] www.analog.com/en/other-products/militaryaerospace/ad790/products/product.html.

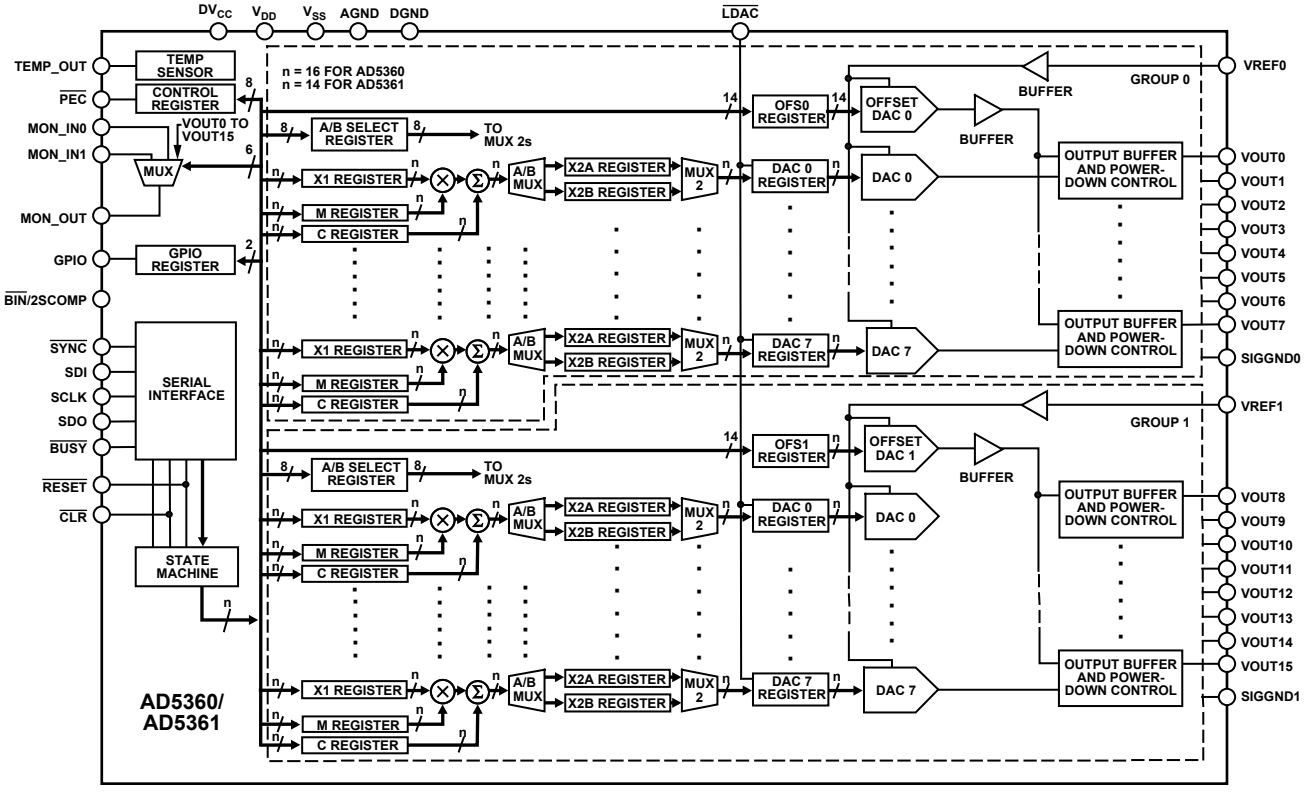


Figure 3. AD5360 functional block diagram.

"Rules of the Road" for High-Speed Differential ADC Drivers

By John Ardizzoni and Jonathan Pearson

As applications engineers, we are constantly bombarded with a variety of questions about driving high-speed analog-to-digital converters (ADCs) with differential inputs. Indeed, selecting the right ADC driver and configuration can be challenging. To make the design of robust ADC circuits somewhat easier, we've compiled a set of common "road hazards" and solutions. In this article, the circuit that actually drives the ADC—variously known as an ADC driver, differential amplifier, or diff amp—is assumed to be capable of handling high-speed signals.

Introduction

Most modern high-performance ADCs use differential inputs to reject common-mode noise and interference, increase dynamic range by a factor of two, and improve overall performance due to balanced signaling. Though ADCs with differential inputs can accept single-ended input signals, optimum ADC performance is achieved when the input signal is differential. ADC drivers—circuits often specifically designed to provide such signals—perform many important functions including amplitude scaling, single-ended-to-differential conversion, buffering, common-mode offset adjustment, and filtering. Since the introduction of the AD8138,[1] differential ADC drivers have become essential signal conditioning elements in data-acquisition systems.

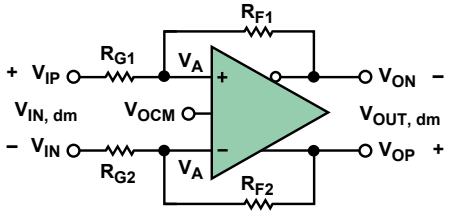


Figure 1. Differential amplifier.

A basic fully differential voltage-feedback ADC driver is shown in Figure 1. Two differences from a traditional op-amp feedback circuit can be seen. The differential ADC driver has an additional output terminal (V_{ON}) and an additional input terminal (V_{OCM}). These provide great flexibility when interfacing signals to ADCs that have differential inputs.

Instead of a single-ended output, the differential ADC driver produces a balanced differential output—with respect to V_{OCM}—between V_{OP} and V_{ON}. "P" indicates *positive* and "N" indicates *negative*. The V_{OCM} input controls the output common-mode voltage. As long as the inputs and outputs stay within their specified limits, the output common-mode voltage must equal the voltage applied to the V_{OCM} input. Negative feedback and high open-loop gain cause the voltages at the amplifier input terminals, V_A+ and V_A–, to be essentially equal.

For the discussions that follow, some definitions are in order. If the input signal is *balanced*, V_{IP} and V_{IN} are nominally equal in amplitude and opposite in phase with respect to a common reference voltage. When the input is *single-ended*, one input is at a fixed voltage, and the other varies with respect to it. In either case, the input signal is defined as $V_{IP} - V_{IN}$.

The *differential-mode* input voltage, $V_{IN,\,dm}$, and *common-mode* input voltage, $V_{IN,\,cm}$, are defined in Equation 1 and Equation 2.

$$V_{IN,\,dm} = V_{IP} - V_{IN}, \quad V_{IN,\,cm} = \frac{V_{IP} + V_{IN}}{2} \qquad (1, 2)$$

This common-mode definition is intuitive when applied to balanced inputs, but it is also valid for single-ended inputs.

The output also has a differential mode and a common mode, defined in Equation 3 and Equation 4.

$$V_{OUT,\,dm} = V_{OP} - V_{ON}, \quad V_{OUT,\,cm} = \frac{V_{OP} + V_{ON}}{2} \qquad (3, 4)$$

Note the difference between the actual output common-mode voltage, $V_{OUT,\,cm}$, and the V_{OCM} input terminal, which establishes the output common-mode level.

The analysis of differential ADC drivers is considerably more complex than that of traditional op amps. To simplify the algebra, it is expedient to define two feedback factors, β_1 and β_2, as given in Equation 5 and Equation 6.

$$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}, \quad \beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}} \qquad (5, 6)$$

In most ADC driving applications $\beta_1 = \beta_2$, but the general closed-loop equation for $V_{OUT,\,dm}$, in terms of V_{IP}, V_{IN}, V_{OCM}, β_1, and β_2, is useful to gain insight into how beta mismatch affects performance. The equation for $V_{OUT,\,dm}$, shown in Equation 7, includes the finite frequency-dependent open-loop voltage gain of the amplifier, A(s).

$$V_{OUT,\,dm} = \left[\frac{2}{\beta_1 + \beta_2}\right]\left[\frac{V_{OCM}(\beta_1 - \beta_2) + V_{IP}(1 - \beta_1) - V_{IN}(1 - \beta_2)}{1 + \frac{2}{A(s)(\beta_1 + \beta_2)}}\right] \qquad (7)$$

When $\beta_1 \neq \beta_2$, the differential output voltage depends on V_{OCM}—an undesirable outcome, since it produces an offset and excess noise in the differential output. The gain-bandwidth product of the voltage-feedback architecture is constant. Interestingly, the gain in the gain-bandwidth product is the reciprocal of the averages of the two feedback factors.

When $\beta_1 = \beta_2 \equiv \beta$, Equation 7 reduces to Equation 8.

$$\frac{V_{OUT,\,dm}}{V_{IN,\,dm}} = \left[\frac{R_F}{R_G}\right]\left[\frac{1}{1 + \frac{1}{A(s)(\beta)}}\right] \qquad (8)$$

This is a more familiar-looking expression; the ideal closed-loop gain becomes simply R_F/R_G when $A(s) \rightarrow \infty$. The gain-bandwidth product is also more familiar-looking, with the "noise gain" equal to $1/\beta$, just as with a traditional op amp.

The ideal closed-loop gain for a differential ADC driver with matched feedback factors is seen in Equation 9.

$$A_V = \frac{V_{OUT,\,dm}}{V_{IN,\,dm}} = \frac{R_F}{R_G} \qquad (9)$$

Output balance, an important performance metric for differential ADC drivers, has two components: *amplitude* balance and *phase* balance. Amplitude balance is a measure of how closely the two outputs are matched in amplitude; in an ideal amplifier they are exactly matched. Output phase balance is a measure of how close the phase difference between the two outputs is to 180°. Any imbalance in output amplitude or phase produces an undesirable common-mode component in the output. The *output balance error* (Equation 10) is the log ratio of the output common-mode voltage produced by a differential input signal to the output differential-mode voltage produced by the same input signal, expressed in dB.

$$Output\ Balance\ Error = 20\log_{10}\left[\frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}}\right] \quad (10)$$

An internal common-mode feedback loop forces $V_{OUT,\,cm}$ to equal the voltage applied to the V_{OCM} input, producing excellent output balance.

Terminating the Input to an ADC Driver

ADC drivers are frequently used in systems that process high-speed signals. Devices separated by more than a small fraction of a signal wavelength must be connected by electrical transmission lines with controlled impedance to avoid losing signal integrity. Optimum performance is achieved when a transmission line is terminated at both ends in its characteristic impedance. The driver is generally placed close to the ADC, so controlled-impedance connections are not required between them; but the incoming signal connection to the ADC driver input is often long enough to require a controlled-impedance connection, terminated in the proper resistance.

The input resistance of the ADC driver, whether differential or single-ended, must be greater than or equal to the desired termination resistance, so that a termination resistor, R_T, can be added in parallel with the amplifier input to achieve the required resistance. All ADC drivers in the examples considered here are designed to have balanced feedback ratios, as shown in Figure 2.

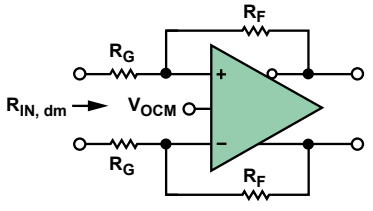


Figure 2. Differential amplifier input impedance.

Because the voltage between the two amplifier inputs is driven to a null by negative feedback, they are virtually connected, and the differential input resistance, R_{IN}, is simply $2 \times R_G$. To match the transmission-line resistance, R_L, place resistor, R_T, as calculated in Equation 11, across the differential input. Figure 3 shows typical resistances $R_F = R_G = 200\ \Omega$, desired $R_{L,\,dm} = 100\ \Omega$, and $R_T = 133\ \Omega$.

$$R_T = \frac{1}{\frac{1}{R_L} - \frac{1}{R_{IN}}} \quad (11)$$

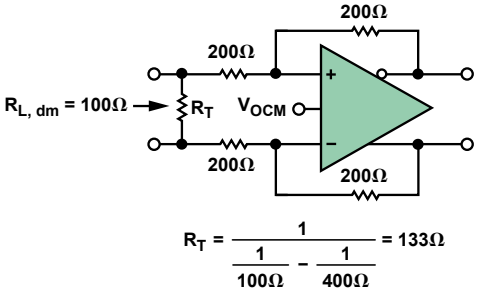


Figure 3. Matching a 100-Ω line.

Terminating a single-ended input requires significantly more effort. Figure 4 illustrates how an ADC driver operates with a single-ended input and a differential output.

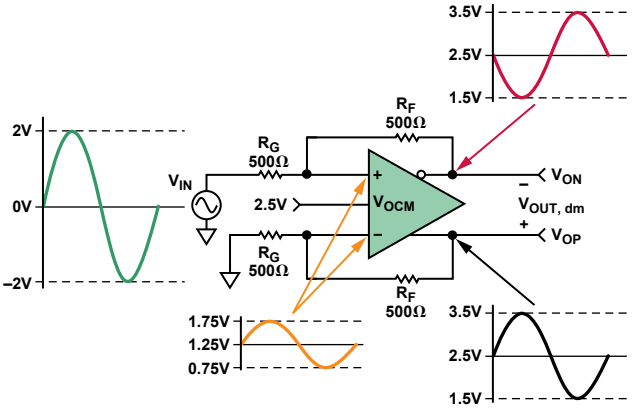


Figure 4. Example of single-ended input to ADC driver.

Although the input is single-ended, $V_{IN,\,dm}$ is equal to V_{IN}. Because resistors R_F and R_G are equal and balanced, the gain is unity, and the differential output, $V_{OP} - V_{ON}$, is equal to the input, that is, 4 V p-p. $V_{OUT,\,cm}$ is equal to V_{OCM} = 2.5 V and, from the lower feedback circuit, input voltages V_{A+} and V_{A-} are equal to $V_{OP}/2$.

Using Equation 3 and Equation 4, $V_{OP} = V_{OCM} + V_{IN}/2$, an in-phase swing of ±1 V about 2.5 V. $V_{ON} = V_{OCM} - V_{IN}/2$, an antiphase-swing of ±1 V about 2.5 V. Thus, V_{A+} and V_{A-} swing ±0.5 V about 1.25 V. The ac component of the current that must be supplied by V_{IN} is (2 V – 0.5 V)/500 Ω = 3 mA, so the resistance to ground that must be matched, looking in from V_{IN}, is 667 Ω.

The general formula for determining this single-ended input resistance when the feedback factors of each loop are matched is shown in Equation 12, where $R_{IN,\,se}$ is the single-ended input resistance.

$$R_{IN,\,se} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}}\right) \quad (12)$$

This is a starting point for calculating the termination resistance. However, it is important to note that amplifier gain equations are based on the assumption of a zero-impedance input source. A significant source impedance that must be matched in the presence of an imbalance caused by a single-ended input inherently adds resistance only to the upper R_G. To retain the balance, this must be matched by adding resistance to the lower R_G, but this affects the gain.

While it may be possible to determine a closed-form solution to the problem of terminating a single-ended signal, an iterative method is generally used. The need for it will become apparent in the following example.

In Figure 5, a single-ended-to-differential gain of one, a 50 Ω input termination, and feedback and gain resistors with values in the neighborhood of 200 Ω are required to keep noise low.

Equation 12 provides the single-ended input resistance, 267 Ω. Equation 13 indicates that the parallel resistance, R_T, should be 61.5 Ω to bring the 267-Ω input resistance down to 50 Ω.

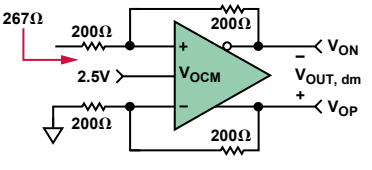


Figure 5. Single-ended input impedance.

$$R_T = \frac{1}{\frac{1}{50\Omega} - \frac{1}{267\Omega}} = 61.5\Omega \quad (13)$$

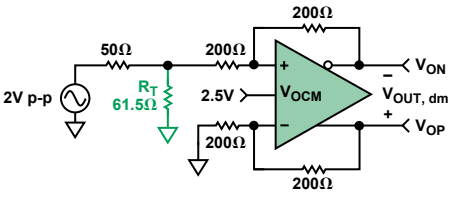


Figure 6. Single-ended circuit with source and termination resistances.

Figure 6 shows the circuit with source and termination resistances. The open-circuit voltage of the source, with its 50-Ω source resistance, is 2 V p-p. When the source is terminated in 50 Ω, the input voltage is reduced to 1 V p-p, which is also the differential output voltage of the unity-gain driver.

This circuit may initially appear to be complete, but an unmatched resistance of 61.5 Ω in parallel with 50 Ω has been added to the upper R_G alone. This changes the gain and single-ended input resistance, and mismatches the feedback factors. For small gains, the change in input resistance is small and will be neglected for the moment, but the feedback factors must still be matched. The simplest way to accomplish this is to add resistance to the lower R_G. Figure 7 shows a Thévenin equivalent circuit in which the above parallel combination acts as the source resistance.

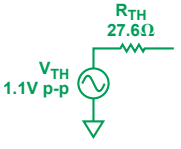


Figure 7. Thévenin equivalent of input source.

With this substitution, a 27.6-Ω resistor, R_{TS}, is added to the lower loop to match loop feedback factors, as seen in Figure 8.

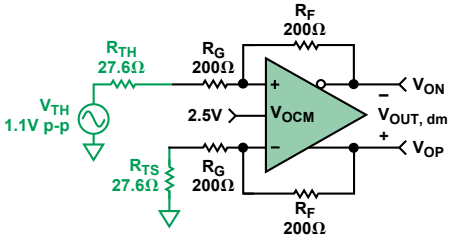


Figure 8. Balanced single-ended termination circuit.

Note that the Thévenin voltage of 1.1 V p-p is larger than the properly terminated voltage of 1 V p-p, while the gain resistors are each increased by 27.6 Ω, decreasing the closed-loop gain. These opposing effects tend to cancel for large resistors (>1 kΩ) and small gains (1 or 2), but do not entirely cancel for small resistors or higher gains.

The circuit in Figure 8 is now easily analyzed, and the differential output voltage is calculated in Equation 14.

$$V_{OUT,dm} = 1.1\text{ V p-p}\left(\frac{200\Omega}{227.6\Omega}\right) = 0.97\text{ V p-p} \quad (14)$$

The differential output voltage is not quite at the desired level of 1 V p-p, but a final independent gain adjustment is available by modifying the feedback resistance as shown in Equation 15.

$$R_F = 227.6\Omega\left(\frac{Desired\ V_{OUT,dm}}{1.1\text{ V p-p}}\right) = 227.6\Omega\left(\frac{1.0\text{ V p-p}}{1.1\text{ V p-p}}\right) = 206.9\Omega \quad (15)$$

Figure 9 shows the completed circuit, implemented with standard 1% resistor values.

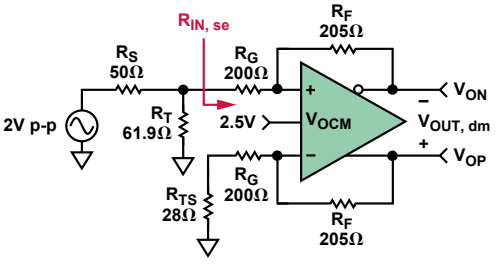


Figure 9. Complete single-ended termination circuit.

Observations: Referring to Figure 9, the single-ended input resistance of the driver, $R_{IN,se}$, has changed due to changes in R_F and R_G. The driver's gain resistances are 200 Ω in the upper loop and 200 Ω + 28 Ω = 228 Ω in the lower loop. Calculation of $R_{IN,se}$ with differing gain resistance values first requires two values of beta to be calculated, as shown in Equation 16 and Equation 17.

$$\beta_1 = \frac{R_G}{R_F + R_G} = \frac{200\Omega}{405\Omega} = 0.494 \quad (16)$$

$$\beta_2 = \frac{R_G + R_{TS}}{R_F + R_G + R_{TS}} = \frac{228\Omega}{433\Omega} = 0.527 \quad (17)$$

The input resistance, $R_{IN,se}$, is calculated as shown in Equation 18.

$$R_{IN,se} = \frac{R_G(\beta_1 + \beta_2)}{\beta_1(\beta_2 + 1)} = 271\Omega \quad (18)$$

This differs little from the original calculated value of 267 Ω, and does not have a significant effect on the calculation of R_T, since $R_{IN,se}$ is in parallel with R_T.

If a more-exact overall gain were necessary, higher precision or series trim resistors could be used.

A single iteration of the method described here works well for closed-loop gains of one or two. For higher gains, the value of R_{TS} gets closer to the value of R_G, and the difference between the value of $R_{IN,se}$ calculated in Equation 18 and that calculated in Equation 12 becomes greater. Several iterations are required for these cases.

This should not be arduous: Recently released differential amplifier calculator tools, ADIsimDiffAmp™ (Reference 2) and ADI Diff Amp Calculator™ (Reference 3) downloadable, do all the heavy lifting; they will perform the above calculations in a matter of seconds.

Input Common-Mode Voltage Range

Input common-mode voltage range (ICMVR) specifies the range of voltage that can be applied to the differential-amplifier inputs for normal operation. The voltage appearing at those inputs can be referred to as ICMV, V_{acm}, or $V_{A\pm}$. This specification is often misunderstood. The most frequent difficulty is determining the actual voltage at the differential amplifier inputs, especially with respect to the input voltage. The amplifier input voltage ($V_{A\pm}$)

can be calculated knowing the variables $V_{IN,\,cm}$, β, and V_{OCM}, using the general Equation 19 for unequal β's, or the simplified Equation 20 for equal β's.

$$V_{acm}\ or\ V_{A\pm} = \frac{2\beta_1\beta_2 V_{ocm} + V_{ip}\beta_2(1-\beta_1) + V_{in}\beta_1(1-\beta_2)}{\beta_1+\beta_2} \quad (19)$$

$$V_{acm}\ or\ V_{A\pm} = V_{IN,cm} + \beta(Vocm - Vicm) \quad (20)$$

It may be useful to recall that V_A is always a scaled-down version of the input signal (as seen in Figure 4). The input common-mode voltage range differs among amplifier types. Analog Devices high-speed differential ADC drivers have two input stage configurations, *centered* and *shifted*. The centered ADC drivers have about 1 V of headroom from each supply rail (hence *centered*). The *shifted* input stages add two transistors to allow the inputs to swing closer to the $-V_S$ rail. Figure 10 shows a simplified input schematic of a typical differential amplifier (Q2 and Q3).

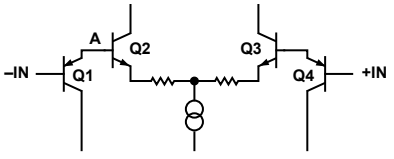


Figure 10. Simplified differential amplifier with shifted ICMVR.

The shifted input architecture allows the differential amplifier to process a bipolar input signal, even when the amplifier is powered from a single supply, making them well suited for single-supply applications with inputs at or below ground. The additional PNP transistor (Q1 and Q4) at the input shifts the input to the differential pair up by one transistor V_{be}. For example, with –0.3 V applied at –IN, point A would be 0.7 V, allowing the differential pair to operate properly. Without the PNPs (centered input stage), –0.3 V at point A would reverse bias the NPN differential pair and halt normal operation.

Table 1 provides a quick reference to many specifications of Analog Devices ADC drivers. A glance reveals the drivers that feature a shifted ICMVR and those that do not.

Input and Output Coupling: AC or DC

The need for ac or dc coupling can have a significant impact on the choice of a differential ADC driver. The considerations differ between input and output coupling.

An ac-coupled *input* stage is illustrated in Figure 11.

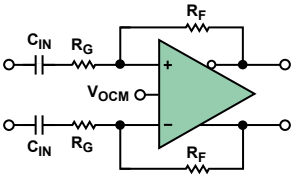


Figure 11. AC-coupled ADC driver.

For *differential-to-differential* applications with ac-coupled inputs, the dc common-mode voltage appearing at the amplifier input terminals is equal to the dc output common-mode voltage, since dc feedback current is blocked by the input capacitors. Also the feedback factors at dc are matched and exactly equal to unity. V_{OCM}—and consequently the dc input common-mode—is very often set near midsupply. An ADC driver with *centered* input common-mode range works well in these types of applications, with the input common-mode voltage near the center of its specified range.

AC-coupled *single-ended-to-differential* applications are similar to their differential-input counterparts but have common-mode ripple—a scaled-down replica of the input signal—at the amplifier input terminals. An ADC driver with centered input common-mode range places the average input common-mode voltage near the middle of its specified range, providing plenty of margin for the ripple in most applications.

When input coupling is optional, it is worth noting that ADC drivers with ac-coupled inputs dissipate less power than similar drivers with dc-coupled inputs, since no dc common-mode current flows in either feedback loop.

AC coupling the ADC driver *outputs* is useful when the ADC requires an input common-mode voltage that differs substantially from that available at the output of the driver. The drivers have

Table 1. High-Speed ADC Driver Specifications

ADC Drivers				ICMVR				V_{OCM}					
				Supply Voltage				Supply Voltage				Output Swing (V)	I_{SUPPLY} (mA)
Part Number	BW (MHz)	Slew Rate (V/µs)	Noise (nV)	±5 V	+5 V	+3.3 V	+3 V	±5 V	+5 V	+3.3 V	+3 V		
AD8132	360	1000	8	–4.7 to +3	0.3 to 3	0.3 to 1.3	0.3 to 1	±3.6	1 to 3.7	—	0.3 to 1	±1	12
AD8137	76	450	8.25	–4 to +4	1 to 4	1 to 2.3	1 to 2	±4	1 to 4	1 to 2.3	1 to 2	RR	3.2
AD8138	320	1150	5	–4.7 to +3.4	0.3 to 3.2	—	—	±3.8	1 to 3.8	—	—	±1.4	20
AD8139	410	800	2.25	–4 to +4	1 to 4	—	—	±3.8	1 to 3.8	—	—	RR	24.5
ADA4927-1/ ADA4927-2	2300	5000	1.4	–3.5 to +3.5	1.3 to 3.7	—	—	±3.5	1.5 to 3.5	—	—	±1.2	20
ADA49232-1/ ADA49232-2	1000	2800	3.6	–4.8 to +3.2	0.2 to 3.2	—	—	±3.8	1.2 to 3.2	—	—	±1	9
ADA4937-1/ ADA4937-2	1900	6000	2.2	—	0.3 to 3	0.3 to 1.2	—	—	1.2 to 3.8	1.2 to 2.1	—	±0.8	39.5
ADA4938-1/ ADA4938-2	1000	4700	2.6	–4.7 to +3.4	0.3 to 3.4	—	—	±3.7	1.3 to 3.7	—	—	±1.2	37
ADA4939-1/ ADA4939-2	1400	6800	2.6	—	1.1 to 3.9	0.9 to 2.4	—	—	1.3 to 3.5	1.3 to 1.9	—	±0.8	36.5

maximum output swing when V_{OCM} is set near midsupply; this presents a problem when driving low-voltage ADCs with very low input common-mode voltage requirements. A simple solution to this predicament (Figure 12) is to ac-couple the connection between the driver output and the ADC input, removing the ADC's dc common-mode voltage from the driver output, and allowing a common-mode level suitable for the ADC to be applied on its side of the ac-coupling. For example, the driver could be running on a single 5-V supply with V_{OCM} = 2.5 V, and the ADC could be running on a single 1.8-V supply with a required input common-mode voltage of 0.9 V applied at the point labeled *ADC CMV*.

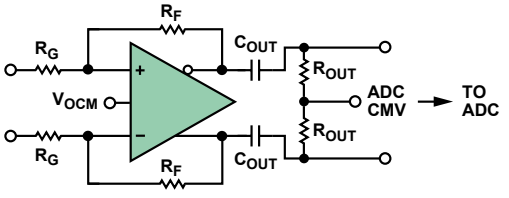


Figure 12. DC-coupled inputs with ac-coupled outputs.

Drivers with *shifted* input common-mode ranges generally work best in dc-coupled systems operating on single supplies. This is because the output common-mode voltage gets divided down through the feedback loops, and its variable components can get close to ground, which is the negative rail. With single-ended inputs, the input common-mode voltage gets even closer to the negative rail due to the input-related ripple.

Systems running on dual supplies, with single-ended or differential inputs and ac- or dc-coupling, are usually fine with either type of input stage because of the increased headroom.

Table 2 summarizes the most common ADC driver input-stage types used with various input-coupling and power-supply combinations. However, these choices may not always be the best; each system should be analyzed on a case-by-case basis.

Table 2. Coupling and Input-Stage Options

Input Coupling	Input Signal	Power Supplies	Input Type
Any	Any	Dual	Either
AC	Single-Ended	Single	Centered
DC	Single-Ended	Single	Shifted
AC	Differential	Single	Centered
DC	Differential	Single	Centered

Output Swing

To maximize the dynamic range of an ADC, it should be driven to its full input range. But care is needed: drive the ADC too hard and risk damaging the input, not hard enough and resolution is lost. Driving the ADC to its full *input* range does not mean that the amplifier *output* has to swing to its full range. A major benefit of differential outputs is that each output only has to swing half as much as a traditional single-ended output. The driver outputs can stay away from the supply rails, allowing decreased distortion. This is not the case for single-ended drivers, however. As the output voltage of the driver approaches the rail, the amplifier loses linearity and introduces distortion.

For applications where every last millivolt of output voltage is required, Table 1 shows that quite a few ADC drivers have rail-to-rail outputs, with typical headroom ranging from a few millivolts to a few hundred millivolts, depending on the load.

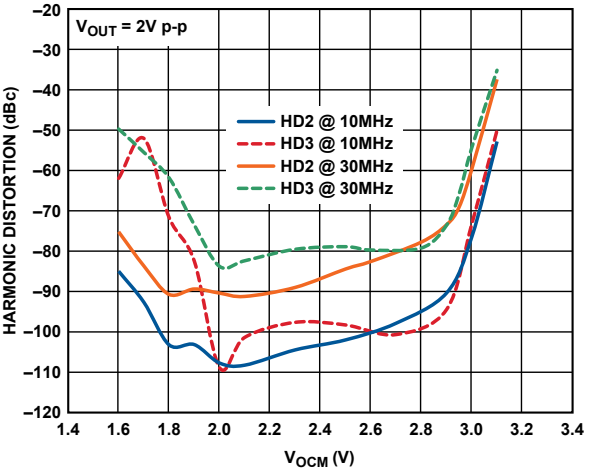


Figure 13. Harmonic distortion vs. V_{OCM} at various frequencies for the ADA4932 with a 5-V supply.

Figure 13 shows a plot of harmonic distortion vs. V_{OCM} at various frequencies for the ADA4932, which is specified with a typical output swing to within 1.2 V of each rail (headroom). The output swing is the sum of V_{OCM} and V_{PEAK} of the signal (1 V). Note that the distortion starts to take off above 2.8 V (3.8-V_{PEAK}, or 1.2 V below the 5-V rail). At the low end, distortion is still low at 2.2 V (–1 V_{PEAK}). The same type of behavior will appear in the discussions of bandwidth and slew rate.

Noise

ADC imperfections include quantization noise, electronic—or random—noise, and harmonic distortion. Important in most applications, noise is usually the most important performance metric in broadband systems.

All ADCs inherently have quantization noise, which depends on the number of bits, n, decreasing with increasing n. Because even "ideal" converters produce *quantization* noise, it will be used as a benchmark against which to compare random noise and harmonic distortion. The output noise from the ADC driver should be comparable to or lower than the ADC's random noise and distortion. Beginning with a review of the characterization of ADC noise and distortion, we will then show how to weigh ADC driver noise against the ADC's performance.

Quantization noise occurs because the ADC quantizes analog signals having infinite resolution into a finite number of discrete levels. An n-bit ADC has 2^n binary levels. The difference between one level and the next represents the finest difference that can be resolved; it is referred to as a *least significant bit* (LSB), or q, for quantum level. One quantum level is therefore $1/2^n$ of the converter's range. If a varying voltage is converted by a perfect n-bit ADC, then converted back to analog and subtracted from the ADC's input, the difference will look like noise. It will have an rms value of (Equation 21):

$$RMS\ Quantization\ Noise = \frac{q}{\sqrt{12}} = \frac{1}{2^n\sqrt{12}} \quad (21)$$

$$Signal\text{-}to\text{-}Quantization\text{-}Noise\ Ratio\ (\text{dB}) = 6.02n + 1.76\ \text{dB} \tag{22}$$

$$THD + Noise = \frac{\sqrt{[v_2(\text{rms})]^2 + [v_3(\text{rms})]^2 + [v_4(\text{rms})]^2 + [v_5(\text{rms})]^2 + [v_6(\text{rms})]^2 + {v_n}^2}}{[v_1(\text{rms})]^2} \tag{23}$$

From this, the logarithmic (dB) formula for the *signal-to-quantizing-noise ratio* of an n-bit ADC over its Nyquist bandwidth can be derived (Equation 22); it is the best achievable SNR for an *n*-bit converter.

Random noise in ADCs, a combination of thermal, shot, and flicker noise, is generally larger than the quantization noise. *Harmonic distortion*, resulting from nonlinearities in the ADC, produces unwanted signals in the output that are harmonically related to the input signals. *Total harmonic distortion and noise* (THD + N) is an important ADC performance metric that compares the electronic noise and harmonic distortion to an analog input that is close to the full-scale input range of the ADC. Electronic noise is integrated over a bandwidth that includes the frequency of the last harmonic to be considered. Here, the "total" in THD includes the first five harmonic-distortion components, which are *root-sum-squared* along with the noise (Equation 23).

The input signal is v_1; the first five harmonic-distortion products are v_2 through v_6; and the ADC electronic noise is v_n.

The reciprocal of THD + Noise, the *signal-to-noise-and-distortion ratio*, or SINAD, is usually expressed in dB (Equation 24).

$$SINAD(\text{dB}) = 20\log_{10}\left[\frac{1}{THD + N}\right] \tag{24}$$

If SINAD is substituted for the *signal-to-quantizing-noise ratio* (Equation 22), we can define an *effective number of bits* (ENOB) that a converter would have if its *signal-to-quantizing-noise ratio* were the same as its SINAD (Equation 25).

$$SINAD(\text{dB}) = 6.02\,(ENOB) + 1.76\ \text{dB} \tag{25}$$

ENOB can also be expressed in terms of SINAD as shown in Equation 26.

$$ENOB = \frac{SINAD(\text{dB}) - 1.76\ \text{dB}}{6.02} \tag{26}$$

ENOB can be used to compare noise performance of an ADC driver with that of the ADC to determine its suitability to drive that ADC. A differential ADC noise model is shown in Figure 14.

The contributions to the total output noise density of each of the eight sources are shown in Equation 27 for the general case, and when $\beta_1 = \beta_2 \equiv \beta$.

$$\begin{aligned}
v_{no,\,dm}\ \text{due to}\ v_{nIN} &= \frac{2v_{nIN}}{\beta_1 + \beta_2} = \frac{v_{nIN}}{\beta}\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ v_{nCM} &= \frac{2v_{nCM}(\beta_1 - \beta_2)}{\beta_1 + \beta_2} = 0\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ i_{nIN+} &= \frac{2i_{nIN+}(1 - \beta_1)R_{G1}}{\beta_1 + \beta_2} = (i_{nIN+})(R_{F1})\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ i_{nIN-} &= \frac{2i_{nIN-}(1 - \beta_2)R_{G2}}{\beta_1 + \beta_2} = (i_{nIN-})(R_{F2})\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ v_{nRG1} &= \frac{\left(2\sqrt{4kTR_{G1}}\right)(1 - \beta_1)}{\beta_1 + \beta_2} = \sqrt{4kTR_{G1}}\left(\frac{R_{F1}}{R_{G1}}\right)\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ v_{nRG2} &= \frac{\left(2\sqrt{4kTR_{G2}}\right)(1 - \beta_2)}{\beta_1 + \beta_2} = \sqrt{4kTR_{G2}}\left(\frac{R_{F2}}{R_{G2}}\right)\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ v_{nRF1} &= \frac{2\beta_1\sqrt{4kTR_{F1}}}{\beta_1 + \beta_2} = \sqrt{4kTR_{F1}}\ \text{for}\ \beta_1 = \beta_2 = \beta \\
v_{no,\,dm}\ \text{due to}\ v_{nRF2} &= \frac{2\beta_1\sqrt{4kTR_{F2}}}{\beta_1 + \beta_2} = \sqrt{4kTR_{F2}}\ \text{for}\ \beta_1 = \beta_2 = \beta
\end{aligned} \tag{27}$$

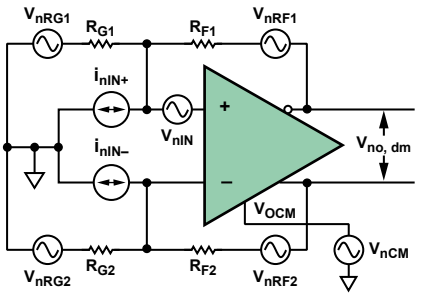


Figure 14. Noise model of differential ADC driver.

The total output noise voltage density, $v_{no,\,dm}$, is calculated by computing the root sum square of these components. Entering the equations into a spreadsheet is the best way to calculate the total output noise voltage density. The new ADI Diff Amp Calculator (Reference 3), which will quickly calculate noise, gain, and other differential ADC driver behavior, is also available on the Analog Devices website.

ADC driver noise performance can now be compared with the ENOB of an ADC. An example that illustrates this procedure is to select and evaluate a differential driver with a gain of 2 for an AD9445 ADC on a 5-V supply, with a 2-V full-scale input; it is processing a direct-coupled broadband signal occupying a 50 MHz (–3-dB) bandwidth, limited with a single-pole filter. From the data-sheet listing of ENOB specifications for various conditions: for a Nyquist bandwidth of 50 MHz, ENOB = 12 bits.

The ADA4939 is a high-performance broadband differential ADC driver that can be direct-coupled. Is it a good candidate to drive the AD9445 with respect to noise? The data sheet recommends R_F = 402 Ω and R_G = 200 Ω, for a differential gain of approximately 2. The data sheet gives a total output voltage noise density for this case as 9.7 nV/$\sqrt{\text{Hz}}$.

First, calculate the system noise bandwidth, B_N, which is the bandwidth of an equivalent rectangular low-pass filter that outputs the same noise power as the actual filter that determines the system bandwidth, for a given constant input noise power spectral density. For a one-pole filter, B_N is equal to π/2 times the 3-dB bandwidth, as shown here (Equation 28).

$$B_N = \left(\frac{\pi}{2}\right) 50\ \text{MHz} = 78.5\ \text{MHz} \quad (28)$$

Next, integrate the noise density over the square-root of the system bandwidth to obtain the output rms noise (Equation 29).

$$v_{no,\,dm}\,(\text{rms}) = \left(9.7\,\text{nV}/\sqrt{\text{Hz}}\right)\left(\sqrt{78.5\ \text{MHz}}\right) = 86\ \mu\text{V rms} \quad (29)$$

The amplitude of the noise is presumed to have a Gaussian distribution, so, using the common ±3σ limits for the peak-to-peak noise (noise voltage swings between these limits about 99.7% of the time), the peak-to-peak output noise is calculated in Equation 30.

$$v_{no,\,dm}\,(\text{p–p}) \approx 6\,(86\ \mu\text{V rms}) = 516\ \mu\text{V}_{\text{p-p}} \quad (30)$$

Now compare the driver's peak-to-peak output noise with 1 LSB voltage of the AD9445 LSB, based on an ENOB of 12 bits and full-scale input range of 2 V, as calculated in Equation 31.

$$One\ LSB = \frac{2\ \text{V}}{2^{12}} = 488\ \mu\text{V} \quad (31)$$

The peak-to-peak output noise from the driver is comparable to the ADC's LSB, with respect to 12 bits of ENOB; the driver is therefore a good choice to consider in this application from the standpoint of noise. The final determination must be made by building and testing the driver/ADC combination.

Supply Voltage

Considering supply voltage and current is a quick way to narrow the choice of ADC drivers. Table 1 provides a compact reference to ADC driver performance with respect to power supply. The supply voltage influences bandwidth and signal swing, as well as ICMVR. Weighing the specifications and reviewing the trade-offs are important to diff amp selection.

Power-supply rejection (PSR) is another important specification. The role of power-supply pins as inputs to the amplifier is often ignored. Any noise on the power-supply lines or coupled into them can potentially corrupt the output signal.

For example, consider the ADA4937-1 with 50 mV p-p at 60 MHz of noise on the power line. Its PSR at 50 MHz is –70 dB. This means the noise on the power supply line would be reduced to approximately 16 μV at the amplifier output. In a 16-bit system with a 1-V full-scale input, 1 LSB is 15.3 μV; the noise from the power supply line would therefore swamp the LSB.

This situation can be improved by adding series SMT ferrite beads, L1/L2, and shunt bypass capacitors, C1/C2 (Figure 15).

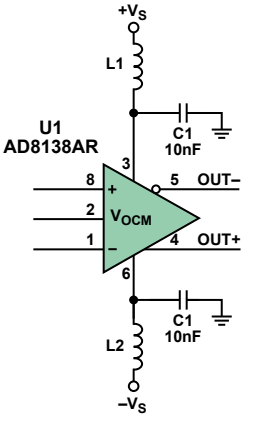


Figure 15. Power-supply bypassing.

At 50 MHz, the ferrite bead has an impedance of 60 Ω and the 10-nF (0.01-μF) capacitor has an impedance of 0.32 Ω. The attenuator formed by these two elements provides 45.5 dB of attenuation (Equation 32).

$$Divider\ Attenuation = 20\log\left(\frac{0.32}{0.32 + 60}\right) = -45.5\ \text{dB} \quad (32)$$

The divider attenuation combines with the PSR of –70 dB to provide about 115 dB of rejection. This reduces the noise to approximately 90 nV p-p, well below 1 LSB.

Harmonic Distortion

Low harmonic distortion in the frequency domain is important in both narrow-band and broadband systems. Nonlinearities in the drivers generate single-tone harmonic distortion and multitone intermodulation-distortion products at amplifier outputs.

The same approach used in the noise-analysis example can be applied to distortion analysis, comparing the ADA4939's harmonic distortion with 1 LSB of the AD9445's ENOB of 12 bits with 2-V full-scale output. One ENOB LSB was shown to be 488 μV in the noise analysis.

The distortion data in the ADA4939 specification table is given for a gain of 2, comparing 2nd and 3rd harmonics at various frequencies. Table 3 shows the harmonic distortion data for a gain of 2 and differential output swing of 2 V p-p.

Table 3. ADA4939 Second and Third Harmonic Distortion

Parameter	Harmonic Distortion
HD2 @ 10 MHz	–102 dBc
HD2 @ 70 MHz	–83 dBc
HD2 @ 70 MHz	–83 dBc
HD2 @ 100 MHz	–77 dBc
HD3 @ 10 MHz	–101 dBc
HD3 @ 70 MHz	–97 dBc
HD3 @ 100 MHz	–91 dBc

The data show that harmonic distortion increases with frequency and that HD2 is worse than HD3 in the bandwidth of interest (50 MHz). Harmonic distortion products are higher in frequency than the frequency of interest, so their amplitude may be reduced by system band-limiting. If the system had a brick-wall filter at 50 MHz, only the frequencies higher than 25 MHz would be of concern, since all harmonics of higher frequencies would be eliminated by the filter. Nevertheless, we will evaluate the system up to 50 MHz, since any filtering that is present may not sufficiently suppress the harmonics, and distortion products can alias back into the signal bandwidth. Figure 16 shows the ADA4939's harmonic distortion vs. frequency for various supply voltages with a 2 V p-p output.

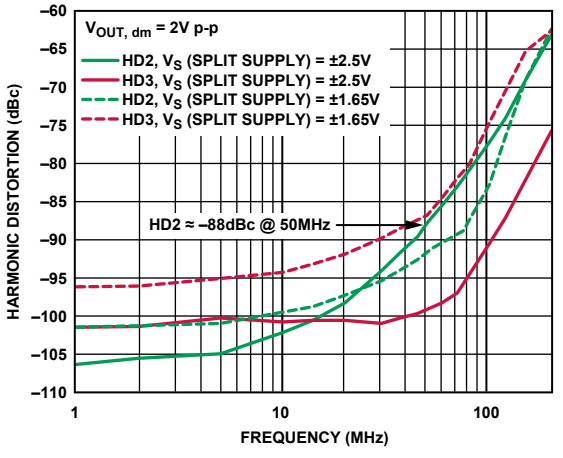


Figure 16. Harmonic distortion vs. frequency.

HD2 at 50 MHz is approximately –88 dBc, relative to a 2-V p-p input signal. In order to compare the harmonic distortion level to 1 ENOB LSB, this level must be converted to a voltage as shown in Equation 33.

$$HD2 = (2\text{ V p-p})\left(10^{\frac{-88}{20}}\right) \approx 80\ \mu\text{V p-p} \qquad (33)$$

This distortion product is only 80 µV p-p, or 16% of 1 ENOB LSB. Thus, from a distortion standpoint, the ADA4939 is a good choice to consider as a driver for the AD9445 ADC.

Since ADC drivers are negative feedback amplifiers, output distortion depends upon the amount of loop gain in the amplifier circuit. The inherent open-loop distortion of a negative feedback amplifier is reduced by a factor of 1/(1 + LG), where LG is the available loop gain.

The amplifier's input (error voltage) is multiplied by a large forward voltage gain, A(s), then passes though the feedback factor, β, to the input, where it adjusts the output to minimize the error. Thus, the loop gain of this type of amplifier is A(s) × β; as the loop gain (A(s), β, or both) decreases, harmonic distortion increases. Voltage-feedback amplifiers, like integrators, are designed to have large A(s) at dc and low frequencies, then roll off as 1/f toward unity at a specified high frequency. As A(s) rolls off, loop gain decreases and distortion increases. Thus, the harmonic distortion characteristic is the inverse of A(s).

Current-feedback amplifiers use an error *current* as the feedback signal. The error current is multiplied by a large forward transresistance, T(s), which converts it to the output voltage, then passes through the feedback factor, $1/R_F$, which converts the output voltage to a feedback current that tends to minimize the input error current. The loop gain of an ideal current feedback amplifier is therefore $T(s) \times (1/R_F) = T(s)/R_F$. Like A(s), T(s) has a large dc value and rolls off with increasing frequency, reducing loop gain and increasing the harmonic distortion.

Loop gain also depends directly upon the feedback factor, $1/R_F$. The loop gain of an ideal current-feedback amplifier does *not* depend upon a closed-loop voltage gain, so harmonic distortion performance does not degrade as closed-loop gain is increased. In a real current-feedback amplifier, loop gain does have some dependence on closed-loop gain, but not nearly to the extent that it does in a voltage-feedback amplifier. This makes a current-feedback amplifier, such as the ADA4927, a better choice than a voltage-feedback amplifier for applications requiring high closed-loop gain and low distortion. Figure 17 shows how well distortion performance holds up as closed-loop gain is increased.

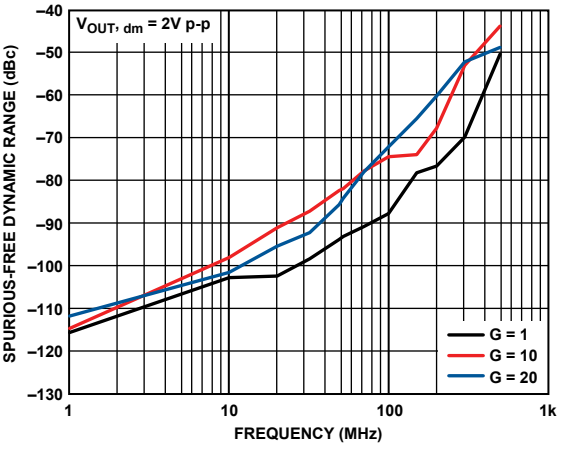


Figure 17. Distortion vs. frequency and gain.

Bandwidth and Slew Rate

Bandwidth and slew rate are especially important in ADC driver applications. Typically, *bandwidth* of a device is used to mean the small-signal bandwidth, while *slew rate* measures the maximum rate of change at the amplifier output for large signal swings.

Effective usable bandwidth (EUBW), a new acronym analogous to ENOB (effective number of bits), describes bandwidth. Many ADC drivers and op amps boast wide bandwidth specs, but not all that bandwidth is usable. For example,–3-dB bandwidth is a conventional way to measure bandwidth, but it doesn't mean that all the bandwidth is usable. The –3-dB bandwidth's amplitude and phase errors can be seen a decade earlier than the actual "break" frequency. So what is the EUBW of an amplifier and how is it determined? An excellent way to determine the usable bandwidth is to consult the distortion plots on the data sheet.

Figure 18 indicates that in order to maintain greater than –80 dBc for 2nd and 3rd harmonics, this ADC driver shouldn't be used for frequencies greater than 60 MHz. Since each application is different, the system requirements will be a guide to the appropriate driver with sufficient bandwidth and adequate distortion performance.

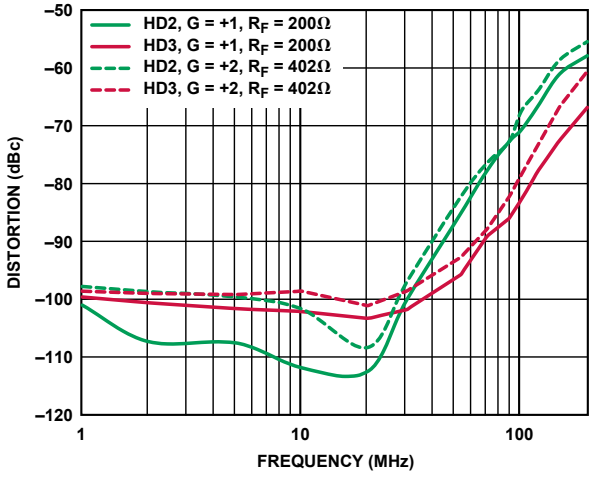


Figure 18. Distortion curves for ADA4937 current-feedback ADC driver.

Slew rate, a large signal parameter, refers to the max rate of change the amplifier output can track the input without excessive distortion. Consider the sine wave output at the slew rate.

$$vo = Vp \sin 2\pi ft \tag{34}$$

The derivative (rate of change) of Equation 34 at the zero crossing, the maximum rate, is

$$\left(\frac{dv}{dt}\right)_{\max} = 2\pi fVp \tag{35}$$

Where dv/dt max is the slew rate, Vp is the peak voltage, and f equals the *full-power bandwidth* (FPBW). Solving for FPBW,

$$FPBW = \frac{Slew\ Rate}{2\pi Vp} \tag{36}$$

Therefore, when selecting an ADC driver, it is important to consider the gain, bandwidth, and slew rate (FPBW) to determine if the amplifier is adequate for the application.

Stability

Stability considerations for differential ADC drivers are the same as for op amps. The key specification is *phase margin*. While the phase margin of a particular amplifier configuration can be determined from the data sheets, in a real system it can be significantly reduced by parasitic effects in the PC board layout.

Stability of a negative-voltage-feedback amplifier depends on the magnitude and sign of its loop gain, $A(s) \times \beta$. The differential ADC driver is a bit more complicated than a typical op-amp circuit, because it has two feedback factors. Loop gain is seen in the denominators of Equation 7 and Equation 8. Equation 37 describes the loop gain for the unmatched feedback factor case ($\beta_1 \neq \beta_2$).

$$Loop\ Gain = \frac{A(s)(\beta_1 + \beta_2)}{2} \tag{37}$$

With unmatched feedback factors, the effective feedback factor is simply the average of the two feedback factors. When they are matched and defined as β, the loop gain simplifies to $A(s) \times \beta$.

For a feedback amplifier to be stable, its loop gain must not be allowed to equal –1; or its equivalent, an amplitude of 1 with phase shift of –180°. For a voltage feedback amplifier, the point where the magnitude of loop gain equals 1 (that is, 0 dB) on its open-loop gain-frequency plot is where the magnitude of A(s) equals the reciprocal of the feedback factor. For basic amplifier applications, the feedback is purely resistive, introducing no phase shifts around the feedback loop. With matched feedback factors, the frequency independent reciprocal of the feedback factor, $1 + R_F/R_G$, is often referred to as the *noise gain*. If the constant noise gain in dB is plotted on the same graph as the open-loop gain, A(s), the frequency where the two curves intersect is where the loop gain is 1, or 0 dB. The difference between the phase of A(s) at that frequency and –180° is defined as the *phase margin*; for stable operation, it should be greater than or equal to 45°. Figure 19 illustrates the unity-loop-gain point and phase margin for the ADA4932 with $R_F/R_G = 1$ (noise gain = 2).

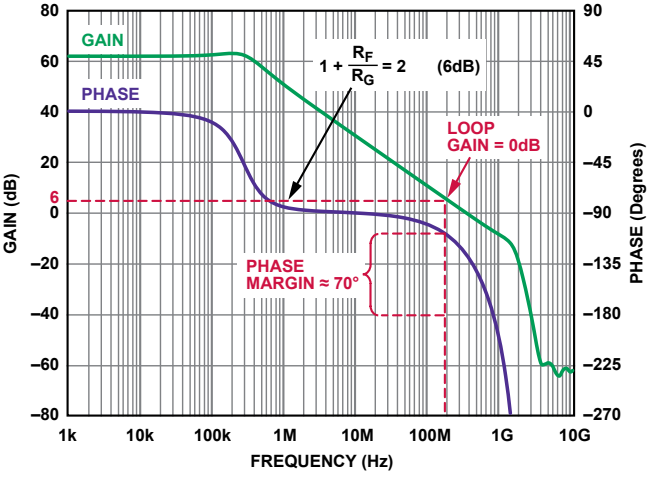


Figure 19. ADA4932 open-loop gain magnitude and phase vs. frequency.

Further examination of Figure 19 shows that the ADA4932 has approximately 50° of phase margin at a noise gain of 1 (100% feedback in each loop). While it is not practical to operate the ADC drivers at zero gain, this observation shows that the ADA4932 can operate stably at fractional differential gains ($R_F/R_G = 0.25$, noise gain = 1.25, for example). This is not true for all differential ADC drivers. Minimum stable gains can be seen in all ADC driver data sheets.

Phase margin for *current-feedback* ADC drivers can also be determined from open-loop responses. Instead of forward gain, A(s), current-feedback amplifiers use forward *transimpedance*, T(s), with an error current as the feedback signal. The loop gain of a current-feedback driver with matched feedback resistors is $T(s)/R_F$, so the magnitude of the current-feedback amplifier loop gain is equal to 1 (that is, 0 dB) when $T(s) = R_F$. This point can be easily located on the open-loop transimpedance and phase plot, in the same way as for the voltage-feedback amplifier. Note that plotting the ratio of a resistance to 1 kΩ allows resistances to be expressed on a log plot. Figure 20 illustrates the unity loop-gain point and phase margin of the ADA4927 current-feedback differential ADC driver with R_F = 300 Ω.

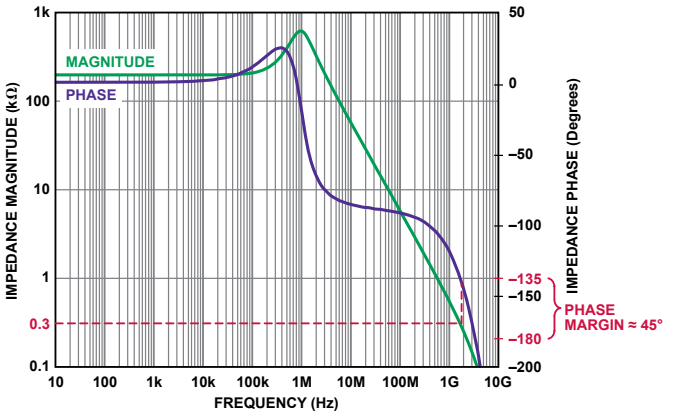


Figure 20. ADA4927 open-loop gain magnitude and phase vs. frequency.

The loop gain is 0 dB where the 300 Ω feedback resistance horizontal line intersects the transimpedance magnitude curve. At this frequency, the phase of T(s) is approximately –135°, resulting in phase margin of 45°. Phase margin and stability increase as R_F increases, and decrease as R_F decreases. Current-feedback amplifiers should always use purely resistive feedback with sufficient phase margin.

PCB Layout

Once a stable ADC driver is designed, it must be realized on a PC board. Some phase margin will always be lost because of the board's parasitic elements, which must be kept to a minimum. Of particular concern are load capacitance, feedback loop inductance, and summing-node capacitance. Each of these parasitic reactances adds lagging phase shift to the feedback loops, thereby reducing phase margin. A design may lose 20° or more of phase margin due to poor PC board layout.

With voltage-feedback amplifiers, it is best to use the smallest possible R_F in order to minimize the phase shift due to the pole formed by R_F and the summing-node capacitance. If large R_F is required, that capacitance can be compensated with small capacitors, C_F, across each feedback resistor with values such that R_FC_F equals R_G times the summing node capacitance.

PCB layout is necessarily one of the last steps in a design. Unfortunately, it is also one of the most often overlooked steps in a design, even though high-speed circuit performance is highly dependent on layout. A high-performance design can be compromised, or even rendered useless, by a sloppy or poor layout. Although all aspects of proper high-speed PCB design can't be covered here, a few key topics will be addressed.

Parasitic elements rob high-speed circuits of performance. Parasitic *capacitance* is formed by component pads and traces and ground or power planes. Long traces without ground plane will form parasitic inductances, which can lead to ringing in transient responses and other unstable behavior. Parasitic capacitance is especially dangerous at the summing nodes of an amplifier, by introducing a pole in the feedback response, causing peaking and instability. One solution is to make sure that the areas beneath the ADC driver mounting and feedback component pads are cleared of ground and power planes throughout all layers of the board.

Minimizing undesired parasitic reactances starts with keeping all traces as short as possible. Outer layer 50-Ω PC-board traces on FR-4 contribute roughly 2.8 pF/inch and 7 nH/inch. These parasitic reactances increase by about 30% for inner-layer 50 Ω traces. Also make sure there *is* ground plane under long traces to minimize trace inductance. Keeping traces short and small will help minimize both parasitic capacitance and inductance—and maintain the design's integrity.

Power-supply bypassing is another key area of concern for layout; make sure the power supply bypass capacitors, as well as the V_{OCM} bypass capacitor, are located as close to the amplifier pins as possible. Also, using multiple bypass capacitors on the power supplies will help ensure that a low impedance path is provided for broadband noise. Figure 21 shows a typical diff amp schematic with bypassing and output low-pass filters. The low-pass filter limits the bandwidth and noise entering the ADC. Ideally, the power supply bypass-capacitor returns are close to the load returns; this helps reduce circulating currents in the ground plane and improves ADC driver performance. (Figure 22a and Figure 22b).

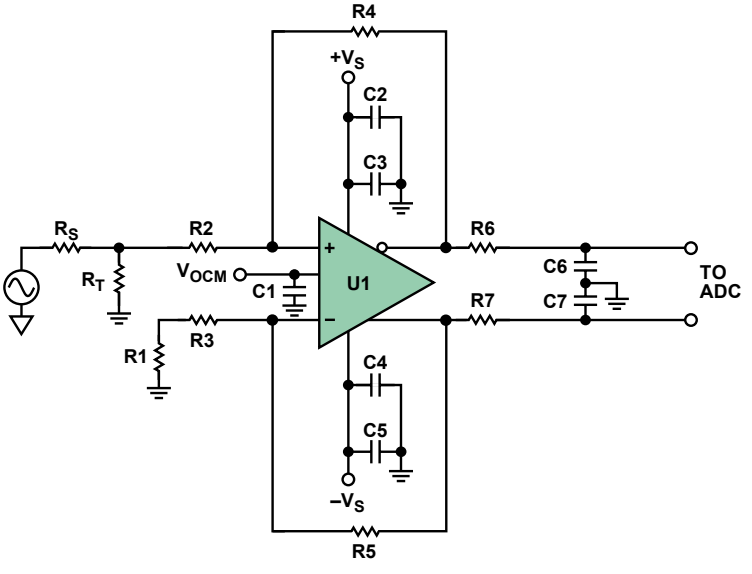


Figure 21. ADC driver with power supply bypassing and output low-pass filter.

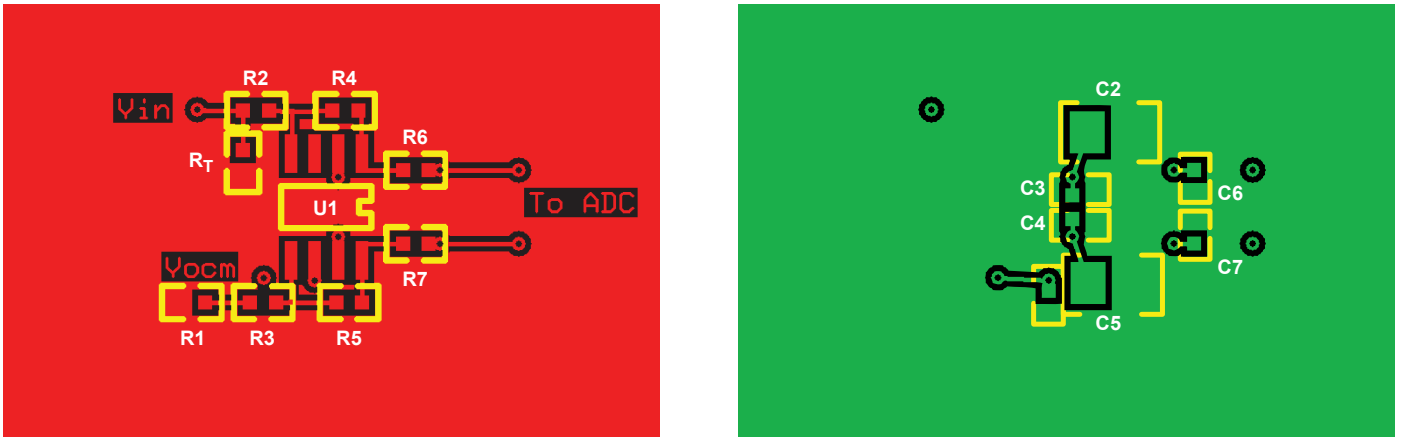


Figure 22 (a) Component side, (b) circuit side.

Use of ground plane, and grounding in general, is a detailed and complex subject and beyond the scope of this article. However, there are a few key points to make, which are illustrated in Figure 22a and Figure 22b. First, connect the analog and digital grounds together at only one point *and one point only*. This will minimize the interaction of analog and digital currents flowing in the ground plane, which would ultimately lead to "noise" in the system. Also, terminate the analog power supply into the analog power plane and the digital power supply into the digital power plane. For mixed-signal ICs, terminate the analog returns in the analog ground plane and the digital ground return in the digital ground plane.

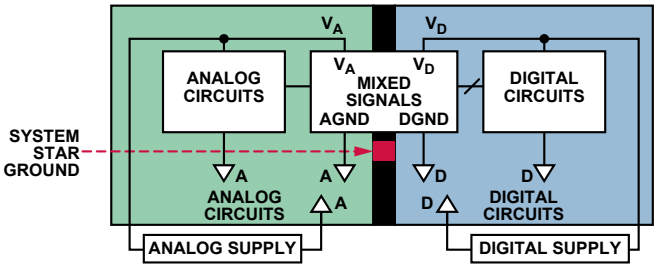
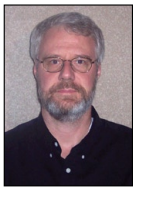


Figure 23. Mixed-signal grounding.

Refer to *A Practical Guide to High-Speed Printed-Circuit-Board Layout*[4] for a detailed discussion about high-speed PCB layout. We hope that the material presented here has helped you think about the many considerations that must be taken into account when you design with ADC drivers. Understanding differential amplifiers—and paying attention to the details of ADC driver design at the outset of a project—will minimize problems down the road, keeping you out of the ADC driver breakdown lane.

Authors

John Ardizzoni [john.ardizzoni@analog.com] is a senior applications engineer in ADI's High-Speed Linear Group. John joined Analog Devices in 2002 and has more than 28 years experience in the electronics industry. He has authored numerous articles and papers and is a coauthor of the popular RAQ series.



Jonathan Pearson [jonathan.pearson@analog.com] has been an applications engineer in the High-Speed Amplifier Group since August 2002. Prior to joining ADI, he worked as an analog circuit and systems designer in the telecom industry. He holds a BSEE from Northeastern University, an MSEE from WPI, and two patents. Besides spending time with his family, he enjoys playing a variety of guitars, recording music, and collecting vacuum-tube guitar amplifiers and antique radios.

References

[1]Information on all ADI components can be found at www.analog.com.

[2]http://designtools.analog.com/dtDiffAmpWeb/dtDiffAmpMain.aspx.

[3]www.analog.com/en/design-tools/dt-adisim-design-sim-tool/design-center/list.html.

[4]www.analog.com/library/analogdialogue/archives/39-09/layout.html.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

Printed in the U.S.A. M02000432-0-7/10

www.analog.com/analogdialogue

ANALOG DEVICES