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Analog Dialogue

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ANALOG DEVICES

Editors' Notes

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New High-Resolution Multiplying DACs Excel at Handling AC Signals

All digital-to-analog converters (DACs) provide an output proportional to the product of the digitally set gain and an applied reference voltage. A multiplying DAC differs from a fixed-reference DAC in that it can apply a high-resolution digitally set gain to a varying wideband analog signal. ADI's new resistance-ladder multiplying DACs are inherently suitable for ac signal-processing applications. Page 5.

Power Cycling 101: Optimizing Energy Use in Advanced Sensor Products

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Dual Difference Amplifier with On-Chip Resistors Implements Precision ADC Driver

Discrete difference amplifiers exhibit mediocre accuracy, significant drift over temperature, poor CMR, and a small input-voltage range. Monolithic diff amps have better CMR, but still suffer from gain drift due to the mismatch between on-chip devices and the external gain resistor. The AD8270 dual diff amp overcomes these limitations, providing a complete, inexpensive, high-performance solution. Page 13.

Quad, 16-Bit Voltage-/Current-Output DACs Save Space, Cost, and Power in Multichannel PLCs

Programmable logic controllers use deterministic functions to control machines and processes. As the number of sensor and control nodes continues to increase, some distributed control systems must handle thousands of nodes. A major challenge is to provide greater efficiency and reduced power consumption. The AD5755 4-channel, 16-bit DAC offers an integrated solution to resolve these issues. Page 14.

High-Speed, Current-Feedback Amplifier Drives and Equalizes Up to 100-m VGA Cables

In classrooms, lecture halls, and conference rooms, PCs transmit RGB video signals to projectors through VGA cables. The cable length depends on the room size and ceiling height, but most cables are shorter than 100 m. This article shows how the ADA4858-3 triple high-speed current-feedback op amp with integrated charge pump can drive and equalize up to 100 m of VGA cable. Page 19.

Dan Sheingold [dan.sheingold@analog.com]
Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 44, NUMBER 3

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

July

Controllers, synchronous buck, 20-V **ADP1882/ADP1883**
Detector, rms, 50-MHz to 9-GHz, 65-dB DR **ADL5902**
Detector, rms, 450-MHz to 6-GHz, 35-dB DR **ADL5505**
Driver, ADC/line, low-distortion, 5-GHz **ADA4960-1**
Driver, white LED **ADD5203**

August

Amplifier, CCD buffer **ADA4800**
Codec, audio, 28-/56-bit SigmaDSP **ADAU1461**
Converter, step-down, 3-MHz, 600-mA **ADP2140**
DAC, dual, 16-bit, 1-GSPS TxDAC+ **AD9125**
DAC, quad, 16-bit, 1-GSPS TxDAC+ **AD9148**
Generator, clock, low-jitter **AD9524**
Mixer, active, 2500-MHz to 2900-MHz **ADRF6604**
Prescaler, divide-by-8, 4-GHz to 18-GHz **ADF5002**
Processor, SHARC, fourth-generation **ADSP-21469**
Receivers, HDMI, dual/quad, 12-bit, 170-MHz ... **ADV7842/ADV7844**
References, voltage, micropower **ADR34xx**
Regulator, triple, low-dropout, 200-mA **ADP320**
Regulators, step-down, 1.2-MHz, 2-A/1.25-A **ADP2119/ADP2120**
Sensor, inertial, six-degrees-of-freedom **ADIS16385**
Sensor, vibration, 3-axis, digital **ADIS16223**
Transceiver, 2.4-GHz, GFSK/FSK **ADF7242**
Transistor Pair, matched NPN **SSM2212**

September

ADC, pipelined, dual 14-bit, 80-MSPS **AD9644**
ADC, pipelined, dual 16-bit, 105-MSPS **AD9650**
Amplifier, operational, JFET-input **ADA4637-1**
Amplifiers, operational, CMOS **ADA4891-3/ADA4891-4**
DAC, voltage-output, 16-bit, 1-µs **AD5541A**
DAC, voltage-output, 18-bit, ±0.5-LSB INL **AD5781**
DAS, 14-bit, 8-channel **AD7607**
Generator, clock, low-jitter **AD9523**
Isolator, digital, bidirectional USB **ADuM3160**
Microcontroller, precision analog, ARM7TDMI **ADuC7124**
Microphones, MEMS, analog output **ADMP404/ADMP405**
Monitor, current shunt, low drift, high CMR **AD8217**
MxFEs, 10-/12-bit, low-power, broadband **AD9961/AD9963**
Regulators, low-dropout, 150-mA **ADP160/ADP161**
Regulators, step-down, 2-A/3-A **ADP2302/ADP2303**
Sensor, inertial, four-degrees-of-freedom **ADIS16305**
Switch, CMOS, dual SPDT, latch-up proof **ADG5436**
Switches, CMOS, quad SPST, latch-up proof, ... **ADG5412/ADG5413**
Transceiver, RS-485, 2.5-kV isolation, 500-kbps **ADM2481**
Transistor Pair, matched NPN **MAT12**

Analog Dialogue

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Low-Voltage Current Sink Controls High-Voltage LED String

By Jon Kraft

Most portable products with displays that use white light emitting diode (WLED) backlights also need auxiliary LED lighting. Two ICs are generally needed: an inductive boost to obtain maximum efficiency (>80%) for the backlight LEDs; and a charge pump to allow independent control of each auxiliary LED. In addition, each IC requires a programmable current sink for brightness control or color blending, so the cost and complexity can increase quickly. This design tip shows how a single programmable LED driver can be combined with a low-cost boost converter to achieve a flexible, high-efficiency, easy-to-program solution. Figure 1 shows an implementation using the ADP1612 (see Figure 2) boost converter and the ADP8860 (see Figure 3) parallel LED driver.

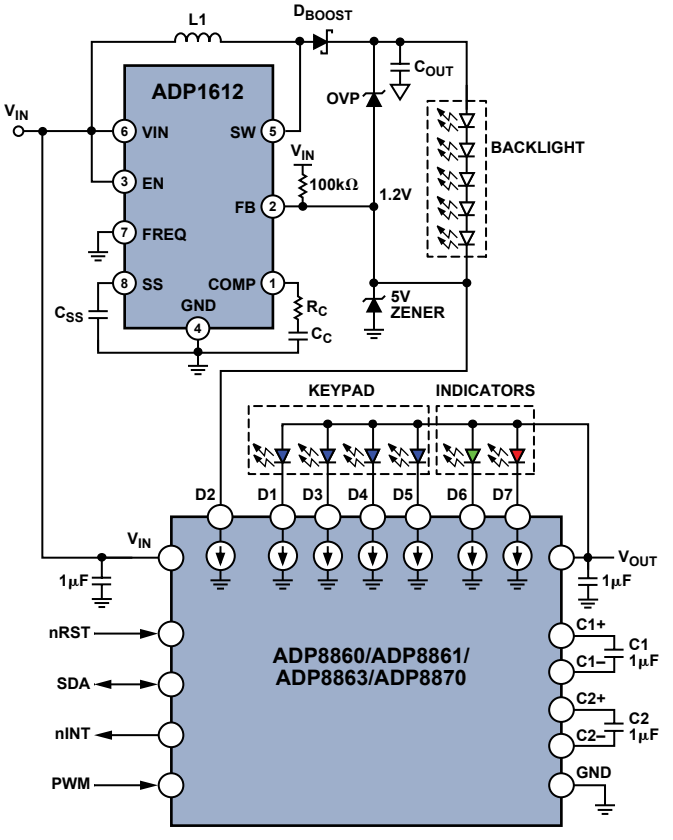

Figure 1. ADP1612 boost converter and ADP8860 LED driver implement programmable drive for backlight and auxiliary LEDs.

In this application, FB of the ADP1612 boost converter is connected to D2, one of the current sinks on the ADP8860 LED driver. The 5-V Zener diode protects that current sink in case of a fault or rapid shutdown. The OVP Zener diode protects the output capacitor, C_{OUT}, and the ADP1612 in case of an open-circuit fault in one of the backlight LEDs.

When current sink D2 is off, the voltage on FB is pulled to V_{IN}, shutting down the ADP1612. When D2 turns on, the voltage on FB is pulled low, and the boost starts switching. The ADP1612 regulates the output voltage to provide 1.2 V on FB and thus on D2. This is enough to allow accurate current regulation. As the current through D2's current sink changes, the ADP1612 automatically scales the output voltage to deliver exactly enough voltage to power the LEDs and the current sink. The ADP8860 has independent control of each sink, so the same programming used for the auxiliary LEDs can also be applied to the backlight LEDs.

Step-Up DC-to-DC Switching Converters Operate at 650 kHz/1300 kHz

The ADP1612 and ADP1613 step-up converters are capable of supplying over 150 mA at voltages as high as 20 V, while operating with a single 1.8-V to 5.5-V supply or single 2.5-V to 5.5-V supply, respectively. Integrating a 1.4-A/2.0-A, 0.13-Ω power switch with a current-mode, pulse-width modulated regulator, their output varies less than 1% with changes in input voltage, load current, and temperature. The operating frequency is pin-selectable and can be optimized for high efficiency or minimum external component size: at 650 kHz they provide 90% efficiency; at 1.3 MHz their circuit implementation occupies the smallest space, making them ideal for space-constrained environments in portable devices and liquid-crystal displays. The adjustable soft-start circuit prevents inrush currents—ensuring safe, predictable start-up conditions. The ADP1612/ADP1613 consume 2.2 mA in the switching state, 700 µA in the nonswitching state, and 10 nA in *shutdown* mode. Available in an 8-lead MSOP package, they are specified from –40°C to +85°C and priced at $1.50/$1.20 in 1000s.

7-Channel Smart LED Driver Includes Charge Pump, I²C Interface

The ADP8860 smart LED driver—which combines a programmable charge-pump driver with automatic phototransistor control—changes current density according to ambient light conditions, eliminating the need for a processor and allowing significant power savings in mobile displays. As many as six LEDs can be independently driven at up to 30 mA; a seventh LED can be driven at up to 60 mA. Light intensity thresholds, min/max LED current, and fade in/out times are all programmable via the I²C interface. The two-capacitor charge pump can source 240 mA. Automatic gain selection of 1×, 1.5×, or 2× maximizes its efficiency. Safety features include soft start, undervoltage lockout, and short-circuit-, overvoltage-, and overtemperature protection. Operating with a single 2.5-V to 5.5-V supply, the ADP8860 consumes 4.5 mA in switching mode and 0.3 µA in standby mode. Available in 20-lead LFCSP and 20-ball WLCSP packages, it is specified from –40°C to +85°C and priced from $1.36 in 1000s.

Author

Jon Kraft [jon.kraft@analog.com] joined Analog Devices in 2007 and works as an applications engineer at the Power Management Design Center in Longmont, Colorado. He holds a BSEE from Rose-Hulman Institute of Technology and an MSEE from Arizona State University; he has been awarded three patents.

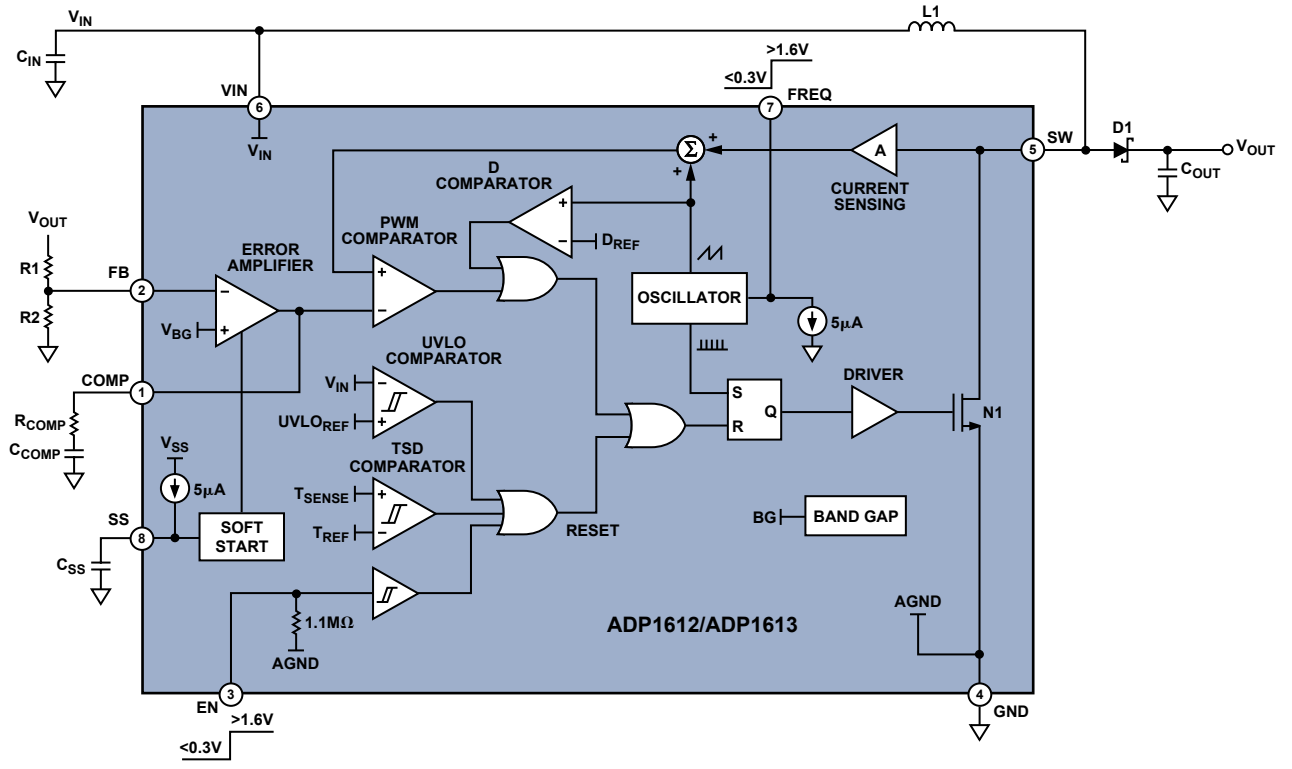

Figure 2. ADP1612/ADP1613 block diagram.

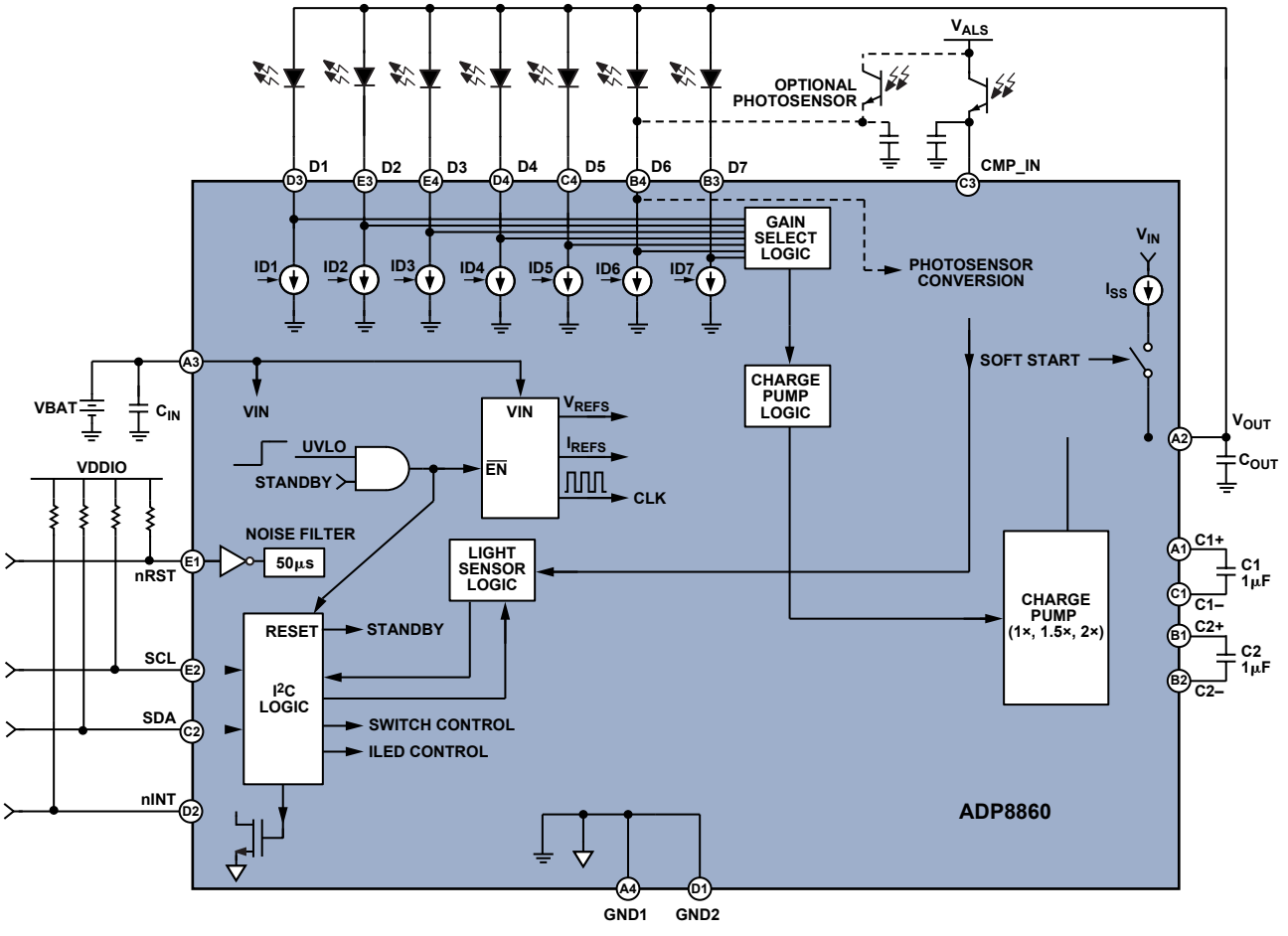

Figure 3. ADP8860 functional block diagram.

New High-Resolution Multiplying DACs Excel at Handling AC Signals

By Liam Riordan

Introduction

All digital-to-analog converters (DACs) provide an output proportional to the product of the digitally set gain and an applied reference voltage. A *multiplying* DAC differs from a *fixed-reference* DAC in that it can apply a high-resolution digitally set gain to a varying wideband analog signal. We discuss here resistance-ladder multiplying DACs and their inherent suitability for ac signal-processing applications.

Basics

Since 1974, when Analog Devices introduced the world's first (10-bit) CMOS IC multiplying DAC, Analog Devices has been a leader in designing and producing multiplying DACs. Used with an amplifier having appropriate bandwidth, they employ a switched R-2R ladder and an on-chip feedback resistor to embody a simple method of adjusting the gain of an ac or varying dc reference input signal, using the DAC to replace the input and feedback resistors of a classic inverting op-amp stage (Figure 1). The digitally adjusted resistive ladder, with the on-chip feedback resistor, provides a gain ($D/2^n$) proportional to the digital input, as if R_{DAC} were a variable input resistor.

$$V_{out} = -\frac{D}{2^n}V_{in} = -\frac{R_{FB}}{R_{DAC}}V_{in} = -\frac{R_{FB}}{(R_{FB}/D\times 2^{-n})}V_{in}$$

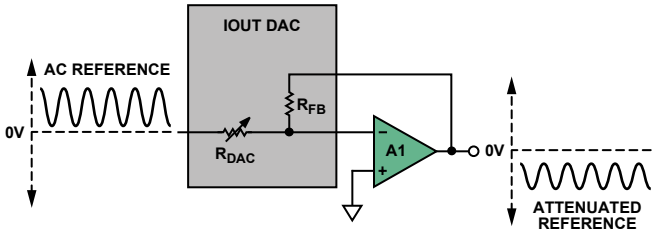

Figure 1. Inverting gain configuration.

A burgeoning market has seen several generations of multiplying DACs, with increased resolution, accuracy, and speed; various digital storage functions; serial-communication options; reduced size and cost; and additional DACs per chip. The latest generation of multiplying DACs offer ideal building blocks for controlling the gain of varying dc or fast ac voltage signals.

The resistance (R-2R) ladder, used in an op-amp feedback circuit, provides a digitally controlled current that is translated to an output voltage by R_{FB}. The amplifier provides this output at low impedance. The *reference* input has a constant resistance to ground, equal to R. Figure 2 shows the principle. In Figure 2a, one-half of the source current, V_{REF}/R, is steered by switch S1 to either I_{OUT1}, connected to the amplifier's negative input (at virtual ground), or to ground (often called I_{OUT2}). One-half the remaining current is steered similarly by switch S2 … and so on. If the switches are activated by a digital word, D (S1 is the MSB), the sum of the currents at I_{OUT1}, flowing through R_{FB} (=R), is $D \times 2^{-n} \times V_{REF}/R$. Important advantages of this configuration include minimization of transients, because the switches are switching between ground and virtual ground, and that R_{FB} is matched on-chip to the ladder resistance, with excellent tracking over temperature.

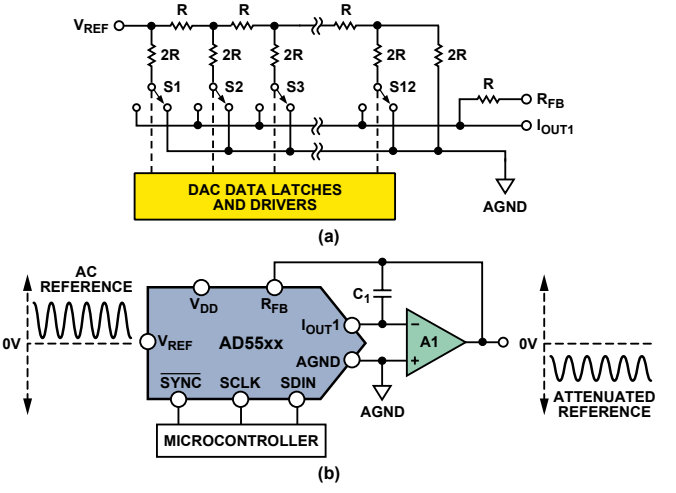

Figure 2. a) R-2R ladder principle. b) multiplying DAC, V_{OUT} = 0 to $-V_{REF}$.

The range of values given by the digital word, D, depends on the device used. Here are the ranges of D (first quadrant) for some Analog Devices multiplying DACs in the AD545x/AD554x families:

8-bit AD5450	0 to 255
10-bit AD5451	0 to 1023
12-bit AD5452	0 to 4095
14-bit AD5453	0 to 16,383
16-bit AD5543	0 to 65,535

Increasing the Gain

For applications in which the output voltage must be greater than V_{IN}, gain can be added by following the DAC stage with an additional external amplifier; or it can be achieved in a single stage, by simply attenuating the feedback voltage, as shown in Figure 3. The approximation shown is valid for $R_2||R_3 << R_{FB}$. R_2 and R_3 should have similar temperature coefficients, but if $R_2||R_3$ is small compared to R_{FB}, they need not match the temperature coefficient of the DAC.

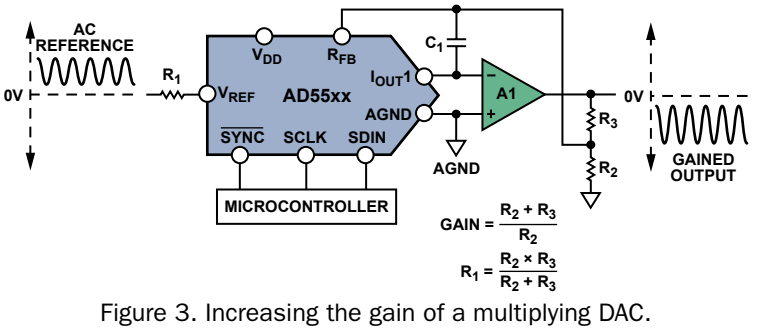

Figure 3. Increasing the gain of a multiplying DAC.

Positive Output

To generate a positive voltage output, an external inverting op amp circuit can be used to provide an additional inversion of either the input or the output. Because some multiplying DACs include uncommitted matched resistors (with tracking temperature coefficients), a positive output can be obtained simply by connecting an additional op amp (A2 in Figure 4)—which could be the companion op amp within a dual device.

If a differential output is required, two extra op amps are needed. Complete details can be found in Circuits from the Lab™ CN-0143, www.analog.com/CN-0143.

Stability Issues

An important component shown in Figure 2 and Figure 3 is the *compensation capacitor* (C_1). The output capacitance of the ladder, plus the amplifier's input capacitance and any strays, introduces a pole into the open-loop response—which can cause ringing or instability when the loop is closed. To compensate for this, an external feedback capacitor, C_1, is usually connected in parallel with the internal R_{FB} of the DAC. If the value of C_1 is too small, it can produce overshoot or ringing at the output, while too large a value can unduly reduce the system bandwidth. Since the internal output capacitance of the DAC varies with code, it is difficult to fix a precise value for C_1. The value is best approximated according to the equation:

$$C_1 = \sqrt{\frac{2C_O}{\pi \times R_{FB} \times GBW}}$$

where GBW is the small signal unity-gain bandwidth product of the op amp and C_O is the output capacitance of the DAC.

Key M-DAC Specifications for Signal Conditioning

Multiplying Bandwidth: the reference-input frequency at which the gain is –3 dB. For a given device, it is a function of amplitude and the choice of compensation capacitance. Figure 6 shows multiplying bandwidth plots for the AD5544, AD5554, or AD545x current-output DACs, which can multiply signals up to 12 MHz. The 350-MHz bandwidth of the accompanying low-power AD8038 op amp ensures that the op amp introduces insignificant dynamic errors on this scale.

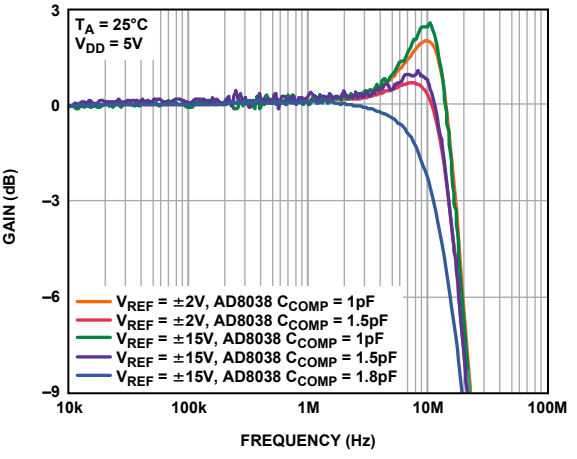

Figure 6. Multiplying bandwidth.

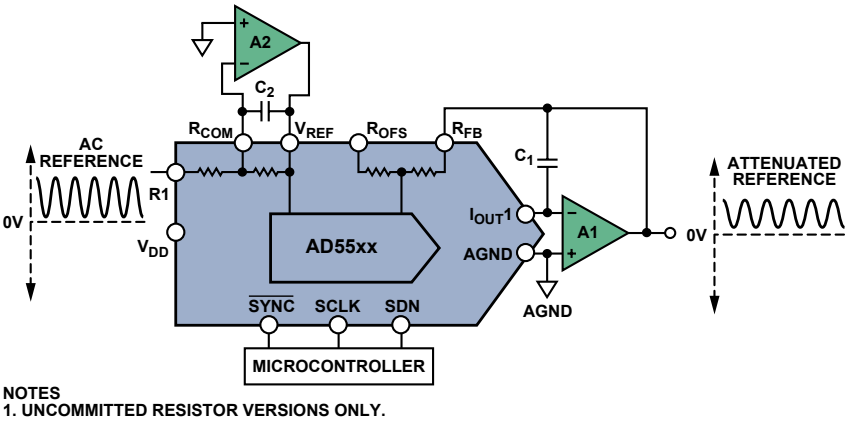

Figure 4. Multiplying DAC, V_{OUT} = 0 to V_{REF}. The AD5415, AD5405, AD5546/AD5556, AD5547/AD5557 include uncommitted resistors like those shown here.

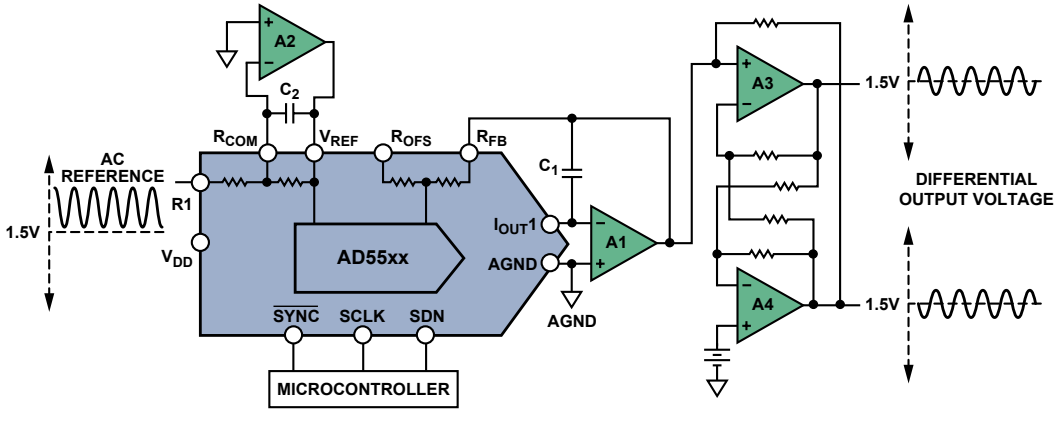

Figure 5. Single-ended to differential.

Table 1. Selection of Suitable Analog Devices High Speed Op Amps

Part Number	Supply Voltage (V)	BW (–3-dB) (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Package(s)
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23-5
AD8066	5 to 24	145	180	1500	0.006	SOIC-8, MSOP-8
AD8021	5 to 24	490	120	1000	10,500	SOIC-8, MSOP-8
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
ADA4899	5 to 12	600	310	35	100	LFCSP-8, SOIC-8
AD8057	3 to 12	325	1000	5000	500	SOT-23-5, SOIC-8
AD8058	3 to 12	325	850	5000	500	SOIC-8, MSOP-8
AD8061	2.7 to 8	320	650	6000	350	SOT-23-5, SOIC-8
AD8062	2.7 to 8	320	650	6000	350	SOIC-8, MSOP-8
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC-8, PDIP-8

Analog Total Harmonic Distortion (THD): a mathematical representation of the harmonic content in the multiplied waveform signal. It is approximated by the log ratio of the rms sum of the first four harmonics (V_2, V_3, V_4, and V_5) of the DAC output to the fundamental value, V_1, shown in Figure 7, and given by the equation:

$$THD\,(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}}}{V_1}$$

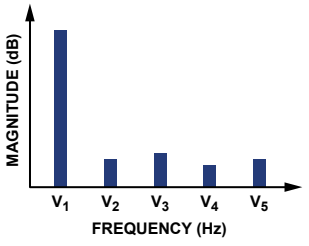

Figure 7. Harmonic distortion components.

Multiplying Feedthrough Error: the error due to capacitive feedthrough from the reference input to the DAC output, when the digital input to the DAC is all 0s. Ideally, with each bit that is dropped, the gain is reduced by 6 dB, all the way down to the least significant bit, DB0 (Figure 8). However, for the lower bits the capacitive feedthrough affects the gain at higher frequencies. This can be seen by the flat lines tailing upwards for the lower bits. For example, at DB2 for a 14-bit DAC, the ideal gain should be –72 dB at all frequencies, but because of feedthrough the actual gain is –66 dB at 1 MHz.

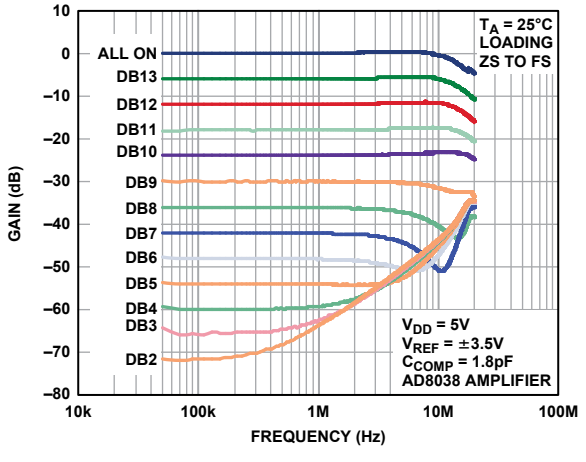

Figure 8. Multiplying feedthrough error.

Choosing the Correct Op Amp

Multiplying-DAC circuit performance is strongly dependent on the ability of the selected op amp to maintain the voltage null at the ladder output and perform the current-to-voltage conversion. For best dc accuracy, it is important to select an operational amplifier with low offset voltage and bias current so as to keep errors commensurate with the DAC's resolution. Detailed op amp specifications are included in device data sheets.

For applications where the reference input is a relatively high speed signal, a wide-bandwidth, high-slew-rate op amp is required to avoid degrading the signal. The gain-bandwidth of an op-amp circuit is limited by the impedance level of the feedback network and the gain configuration. To determine what GBW is required, a useful guideline is to select an op amp with a –3-dB bandwidth that is 10 times the frequency of the reference signal.

The slew-rate specification of the op amp must be considered in order to limit distortion of large high-frequency signals. For the AD54xx and AD55xx families, an op amp with a slew rate of 100 V/µs is generally sufficient.

Table 1 provides a selection of operational amplifiers that are useful for multiplying applications.

Finding the Right DAC

For a table of digital-to-analog converters, where M-DACs can be found, visit www.analog.com/en/digital-to-analog-converters/da-converters/products/index.html.

Conclusion

In the nearly 40 years of innovation since the introduction of the first CMOS M-DAC, a number of generations of devices have become available, with many new features, improved performance, and radical reductions in cost and size. Among the more recent improvements to our portfolio of high-resolution 14-bit/16-bit current-output AD55xx DACs are:

- Improved integral nonlinearity (INL), ±1 LSB
- Reduced analog THD and multiplying feedthrough—and wider multiplying bandwidths
- Reduced THD for digital signals; reduced midscale glitch and digital feedthrough for variable-reference (dc) applications.

Further Reading

1. Kester, Walt. *The Data Conversion Handbook* (2005). Newnes (Elsevier).

Author

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Power Cycling 101: Optimizing Energy Use in Advanced Sensor Products

By Mark Looney

Introduction

Highly integrated, fully specified sensor systems, such as the ADIS16209 tilt sensor (see Appendix), available in compact packages at attractive prices, allow system developers to readily use sensors that embrace technologies with which they may have little experience—with minimal investment and risk. Since accuracy is fully specified at a given power level, it might appear that the developer's ability to reduce power consumption is constrained. However, the use of power cycling provides an opening for reducing average power consumption in applications where energy use must be tightly managed. This article focuses on power cycling and its impact on overall power consumption.

Many of us grew up in homes with loving parents who would yell, "Turn off the lights when you leave the room! We don't own the power company!" In effect, they were teaching us an important energy management technique—*power cycling*—the process of removing power from a function when it is not needed, such as shutting off a sensor system when measurements are not required. This enables a reduction in average power dissipation, as quantified by the following equation:

$$P_{AVG} = [D \times P_{ON}] + [(1 - D) \times P_{OFF}]$$

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = duty\ cycle$$

$$P_{ON} = on \text{ power}, P_{OFF} = off \text{ power}$$

$$T_{ON} = on \text{ time}, T_{OFF} = off \text{ time}$$

P_{ON} is the system's power dissipation in its normal operating state. P_{OFF} is the system's overhead in its *off* state. Associated with residual currents, such as maintaining a power switch or a shutdown mode in a power regulator, it is typically on the order of 1 µA. The *on* time (T_{ON}) is the amount of time for the sensor system to turn on, produce a desired measurement, and turn back off. The *off* time (T_{OFF}) depends on how frequently the system requires sensor measurements. If the *off* power is much smaller than the *on* power, the average power dissipation is essentially proportional to the duty cycle. For example, if the *off* power is zero and the duty cycle is 10%, the average power dissipation is 10% of the normal operating power.

Sensor System Review

Transducers translate physical phenomena—such as temperature, acceleration, or strain—into electrical signals. To be used appropriately, transducer elements require support functions, such as excitation, signal conditioning, filtering, offset- and gain adjustment, and temperature compensation. Advanced sensor products also include analog-to-digital conversion and provide all these functions in a single package, delivering complete, calibrated sensor-to-bits functions. By eliminating the user's need to develop component-level designs or complex characterization and correction formulas, they enable faster design cycles with less investment. Although highly integrated sensor products reduce the burden of making circuit-level design decisions, it is helpful to understand their internal operation when considering power cycling to reduce average power.

Figure 1 shows many of the functions associated with a complete sensor system. Each transducer element requires an *interface circuit* to convert the physical change in the element into an electrical signal usable by standard signal processing components. For example, resistance strain gages—resistors that experience a change in resistance when subjected to a change in strain—are commonly used in the form of bridge circuits (with excitation) to convert the variable resistance into an electrical signal. Another example is *integrated microelectromechanical systems* (*i*MEMS®) inertial sensors, such as accelerometers and gyroscopes. Their tiny structures respond to inertial motion changes with displacement changes between plates, which results in capacitance changes between electrical nodes. The interface circuit for the variable capacitive element typically uses a combination of modulation and demodulation stages to translate the capacitance change into an electrical signal.

The *buffer* stage, which prepares the signal for the input stage of the *analog-to-digital converter* (ADC), can include level shifting, gain, offset correction, buffering, and filtering. Once the sensor signal has been digitized, digital processing functions help increase the value of the information. *Digital filtering*, $h(n)$, reduces noise and focuses on the frequency band of interest. For example, a machine-health system might use a band-pass filter to focus on the frequency signature associated with a common wear-out mechanism. Other sensors, which need a stable dc reference, may place more value on a low-pass filter.

Sensor accuracies may differ substantially across a population of parts. In order to tighten the error distribution and increase the measurement certainty, sensor systems often include a *calibration* process that characterizes each sensor under known stimuli and conditions and provides unit-specific formulas that correct the output over all expected operating conditions. The final processing stage, $f(n)$, represents specific processing—for example, the trigonometric relationship used to translate an accelerometer's static gravitational measurements into orientation angles.

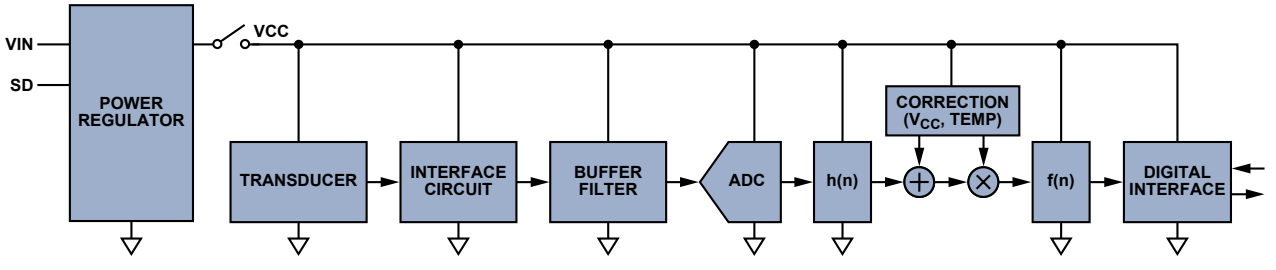

Figure 1. Example of a sensor system.

Power Cycling Considerations

When evaluating the effectiveness of power cycling in a sensor system, the designer must be sure to determine the time it takes to acquire useful data. Figure 2 shows how a typical sensor system responds when power is applied. T_M is the measurement time and T_C is the cycle time. The measurement time depends on the start-up time, T_1, the settling time, T_2, and the data-acquisition time, T_3.

The *start-up time* depends on the system processor and the initialization routines it must run to support sensor data sampling and signal-processing operations. When using a highly integrated sensor system, the start-up time is normally specified in the product documentation. Products of this type sometimes offer a *sleep* mode—which provides faster start-up times at the expense of higher power-off dissipation than *shutdown* mode.

Settling time can include electrical behavior of the transducer, interface circuit, filter, and physical components, as well as thermal and mechanical settling time. In some cases, these transient behaviors settle during the turn-on time, so they have little or no impact on the overall measurement time. The most conservative approach to analyzing the behaviors, however, is to consider that they happen in cascade, unless further analysis and research can support the more favorable assumption of simultaneous startup and settling.

The *data-acquisition time* depends on how many data samples are required, how fast the system processor can read data, and how soon the processor is available once accurate data is ready for acquisition.

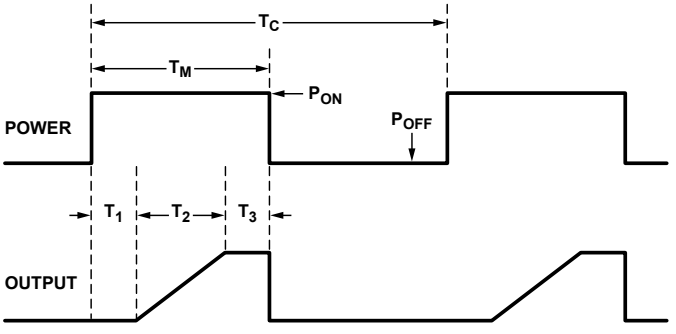

Figure 2. Sensor response during power cycling.

Analysis Example

This example evaluates a fully integrated MEMS tilt sensor to identify parameters that impact accuracy and measurement times in order to determine the important power vs. performance relationships. The following four steps provide a simple guideline for this process:

1. Learn how the sensor operates.
2. Capture relevant information from the product documentation.
3. Estimate important parameters that are not directly specified.
4. Develop power vs. performance relationships.

1. Operational Understanding

The example tilt sensor system is very similar to the generic system in Figure 1. The core MEMS accelerometer includes both the transducer element and the interface circuit. The accelerometer signal passes through a single-pole, low-pass filter, which limits the signal bandwidth to 50 Hz. The analog-to-digital converter runs at a sample rate of 200 SPS and feeds its output into the digital processing stage. The digital processing functions include an averaging filter, temperature-driver correction formulas, mathematical function for translating static accelerometer readings into inclination angles, user interface registers, and a serial interface.

When the accelerometer's measurement axis is perpendicular to gravity, its output will be zero, assuming zero bias error. It will produce an output of +1 *g* or –1 *g* when its measurement axis is parallel to gravity, with the polarity depending on its direction. The relationship between the static acceleration measurement and the inclination angle is a simple sine or tangent function, as shown in Figure 3. This analysis focuses on the *horizontal* mode (sine).

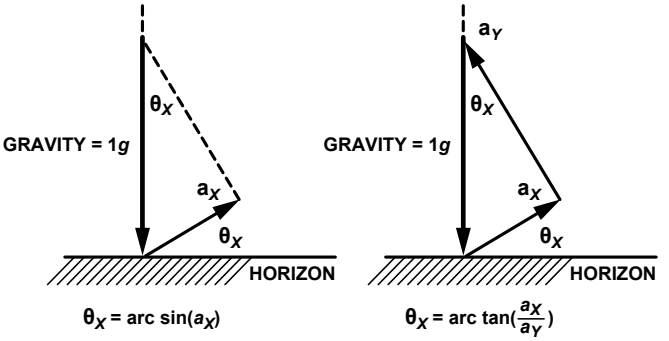

Figure 3. MEMS tilt sensor operation.

2. Capture Relevant Information from Product Literature

Table 1 provides an overview of the parameters that influence power cycling for an advanced sensor system. Some of these parameters are available in product data sheets, while others require analysis with respect to end-system performance goals. P_{ON} and T_1 are parameters from the data sheet. The remaining parameters can be used to estimate T_2 and T_3. The off-mode power comes from the shutdown current of the linear regulator.

Table 1. Sensor System Operating Specifications

Parameter	Value
Power supply	+3.3 V
Power, normal operation	46.2 mW (P_{ON})
Power, off-mode	3.3 μW (P_{OFF})
Power, sleep-mode	1.2 mW (P_{OFFS})
Turn-on time	190 ms (T_1)
Sleep-mode recovery	2.5 ms (T_{1S})
Accelerometer range	±1.7 *g*
Inclination angle range	±30°
Low-pass filter	–3 dB @ 50 Hz, single-pole
Sample rate	200 SPS
Digital filter	Running average, 256 max

3. Use Educated Assumptions to Quantify Remaining Influential Factors

The settling time influences the accuracy and measurement rate that a sensor system can support. Many different things can influence settling time, but this analysis focuses on the electrical factors. Estimating the settling time requires a performance objective, some key assumptions, and a model for analyzing the sensor's response to power application. The first key assumption is that the filter settling happens after the initial start-up period (turn-on time). While these two periods can be simultaneous,

analyzing them in cascade provides a more conservative approach as a starting point. Figure 4 provides a simplified model for analyzing the sensor's response to power application.

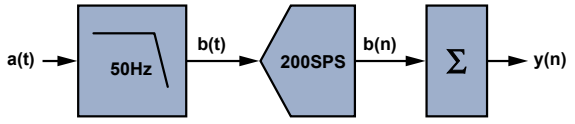

Figure 4. Electrical model for settling time analysis.

After power application, the accelerometer sensor's output, $a(t)$, exhibits a step response. Since the sensor runs off of a single supply, its output will likely start at zero and quickly transition to a level that establishes its orientation. For simplicity, assume that a zero output corresponds to the minimum acceleration level available. In this case, we use –2 *g*, in order to provide some margin over the specified minimum of –1.7 *g*. Also, the maximum incline range is +30°, which is equivalent to +0.5 *g*. Combining these two intervals, the maximum transition that the accelerometer signal will make at startup is +2.5 *g*. The step response of the single-pole, low-pass filter, $b(t)$, is captured in the following formula:

$$a(t) = 0, t < 0$$
$$a(t) = 2.5g, t \geq 0$$
$$b(t) = 2.5 \times \left(1 - e^{-100\pi t}\right)$$

A model that includes the digital filter requires a discrete version of $b(t)$, along with a summation model to simulate the filter.

$$b(n) = b(t), t = \frac{n}{f_S} = \frac{n}{200}$$

$$b(n) = 2.5 \times \left(1 - e^{-\frac{\pi}{2}}\right)$$

$$y(n) = \frac{1}{N}\sum_{n=1}^{N} b(n) = \frac{2.5}{N}\sum_{n=1}^{N}\left(1 - e^{-\frac{\pi}{2}}\right)$$

The settling time is the time required to settle to its final value within a specified accuracy, A_E. Figure 5 shows two transient response curves and indicates the settling time for each to an accuracy of 0.1 *g*.

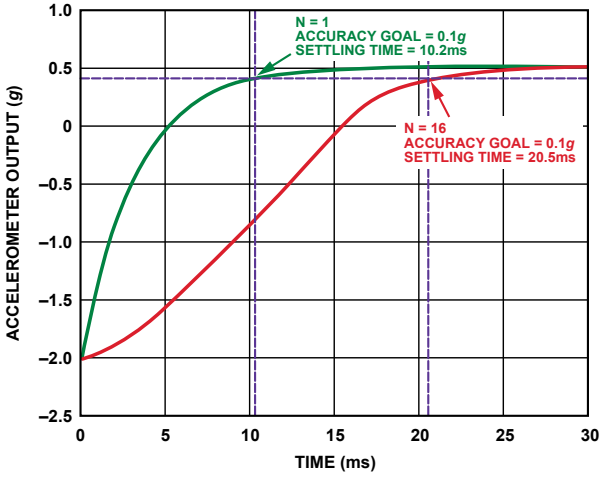

Figure 5. Power-on transient response.

For this example, the error budget allows 0.2° of settling accuracy. The sine formula provides a simple method for translating this goal into an acceleration metric.

$$a_{g\,\max} = \sin 0.2° \approx 3.5\ \text{mg}$$
$$a_{g\,\min} = \sin 30° - \sin 29.8° \approx 3.0\ \text{mg}$$

Modeling this formula is very simple with tools like Excel or MATLAB. When using Excel, the output reaches a level within 3 m*g* of 0.5 *g* on the 18th sample when N = 16—and on the 65th sample when N = 64. Dividing each of these numbers by the sample rate (200 SPS) provides settling time estimates for these settings of 21 ms for N = 1, 90 ms for N = 16, and 325 ms for N = 64. Assume (if reasonable) that the errors associated with thermal settling are negligible. Since the device being considered provides a temperature-calibrated response, this is probably an acceptable assumption. Validating this assumption offers a good opportunity to verify the accuracy as part of the final characterization process.

The data-acquisition time, T_3, for this type of system doesn't need to be longer than one sample cycle, since all of the necessary correction and filtering is handled inside the device. Here, the acquisition time will only contribute 5 ms to the overall measurement time.

4. Relate Power Dissipation to Cycle Time

The final part of this analysis relates the average power dissipation and the cycle time, which is, in effect, equal to the amount of time between individual measurement events. Table 2 summarizes key power cycling factors, either specified in the sensor's data sheet or produced through this simple analysis process, including numbers for both full start-up (power cycling) and sleep-mode recovery (sleep cycling).

Table 2. Summary of Critical Power Cycling Parameters

	Power Cycling	Sleep Cycling
P_{ON}	46.2 mW	
P_{OFF}	3.3 µW	1.15 mW
T_M, N = 1	190 + 21 + 5 = 216 ms	2.5 + 21 + 5 = 28.5 ms
T_M, N = 16	190 + 90 + 5 = 285 ms	2.5 + 90 + 5 = 97.5 ms
T_M, N = 64	190 + 325 + 5 = 520 ms	2.5 + 325 + 5 = 332.5 ms

The following calculation provides a quick example for using these parameters to analyze and compare power cycling and sleep cycling for a system that requires a measurement rate of 1 SPS.

Power cycling:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T_C} = \frac{0.216\ \text{s}}{1\ \text{s}} = 0.216$$
$$P_{AVG} = [D \times P_{ON}] + [(1 - D) \times P_{OFF}]$$
$$P_{AVG} = [0.216 \times 0.0462] + [0.784 \times 0.0000033] = 0.00998\ \text{W}$$
$$P_{AVG} \approx 10\ \text{mW}$$

Sleep cycling:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T_C} = \frac{0.0285\ \text{s}}{1\ \text{s}} = 0.0285$$
$$P_{AVG} = [D \times P_{ON}] + [(1 - D) \times P_{OFF}]$$
$$P_{AVG} = [0.0285 \times 0.0462] + [0.9715 \times 0.00115] = 0.00243\ \text{W}$$
$$P_{AVG} \approx 2.4\ \text{mW}$$

Here sleep cycling is advantageous. However, if the cycle time was increased to one sample per minute (T_C = 60 s), the average power dissipation would be 0.2 mW for the power cycling approach and 1.2 mW for the sleep cycling approach. A useful graphical relationship between cycle time and average power dissipation is shown in Figure 6.

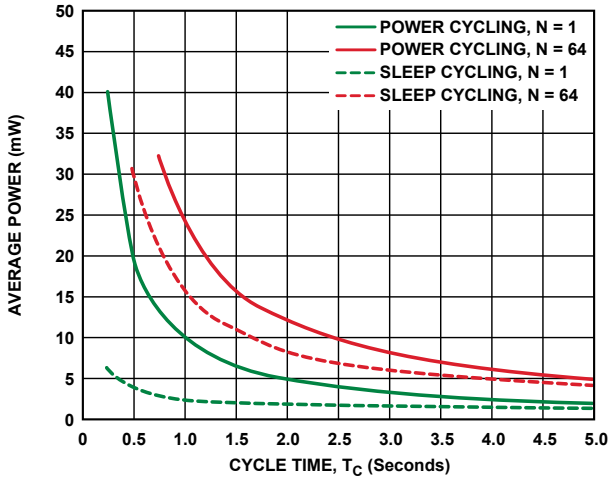

Figure 6. Cycle time vs. average power dissipation.

The *sleep* mode keeps all of the initialization values while shutting down the rest of the system. Although maintaining these settings requires some power, recovery times are faster than full start-up times. The ADIS16209 tilt sensor provides a programmable sleep time and automatic wake-up. This type of solution fits well with a master processor that can also wake up on a data-ready signal, take the data it needs, and command the sensor to go back to sleep for another fixed period. Another example of a MEMS product that uses *sleep* mode is the ADIS16223 vibration sensor, which collects and stores vibration data, automatically goes back into sleep mode, and then starts a countdown to another measurement event. This type of sensor works well for systems that require periodic monitoring, without the need to assign processor resources to manage the sleep and data collection modes.

This simple analysis provides some useful insights. In particular, there are some cases where, despite the power required in sleep mode, sleep-mode management can offer energy savings. In the above example, sleep mode offered a 4:1 improvement for systems that need tilt measurements at a rate of 1 SPS. Here, the sleep mode provides power saving for measurement cycle times up to 6 s. For systems that have longer measurement cycle times, the lower overhead associated with managing a shutdown feature enables lower average power levels.

Conclusion

Whether for economic or environmental reasons, the desire to reduce power consumption seems to be nearly universal. Reducing power consumption can reduce the size and cost of power sources, such as power converters, batteries, and solar cells. Other potential benefits include relaxed thermal and mechanical design requirements, lower EMI emissions, and more favorable environmental impact ratings.

The concepts and analysis techniques presented in this article provide a good starting point for engineers who value highly integrated sensor products but are also under pressure to reduce power consumption where possible. More importantly, the thought process associated with identifying and analyzing behaviors that can impact overall power goals will be even more important, as each system design offers new opportunities and risks. After completing the initial analysis, perhaps the Russian proverb, "Доверяй, но проверяй`" ("Trust, but verify!"), best summarizes how to assure success in the final implementation. Keep track of key assumptions, such as the settling accuracy (3 m*g*) and whether thermal settling will play a role. When appropriate hardware is available, test these solutions in conditions that match their intended use as closely as possible. In the end, testing these assumptions will add confidence and refine new assumptions for future analysis of power management techniques.

Appendix

The ADIS16209 *i*Sensor® dual-axis inclinometer (Figure A) provides a digital output proportional to the rotation in one plane parallel to the Earth's gravity (vertical mode) over a ±180° range, or two planes tangential to the Earth's gravity (horizontal mode) over a ±90° range. The on-chip ADC digitizes the output of the *i*MEMS® accelerometers, the internal temperature sensor, the power supply, and an auxiliary analog input, and provides the data via an SPI-compatible interface. Sensitivity, sample rate, bandwidth, and alarm thresholds are all digitally programmable. Functionally complete, the device also includes an auxiliary 12-bit DAC, precision 2.5-V reference, digital self-test function, and programmable power management. Operating with a single 3.0-V to 3.6-V supply, the ADIS16209 consumes 36 mA in fast mode, 11 mA in normal mode, and 140 µA in sleep mode. Available in a 16-terminal LGA package, it is specified from –40°C to +125°C.

The ADIS16223 *i*Sensor digital vibration sensor (Figure B) combines a ±70-*g* single-axis *i*MEMS accelerometer with a flexible, low-power signal processor. The 22-kHz sensor bandwidth and 72.9-kSPS sample rate are well-suited to machine-health applications; an averaging/decimating filter optimizes operation for lower bandwidth applications. The device can capture and store 1k samples from each of three axes using automatic, manual, or event-capture data collection modes. It also measures temperature and supply voltage, captures peaks, and provides a condition-based alarm function. Operating on a single 3.15-V to 3.6-V supply, the ADIS16223 consumes 38 mA in *capture* mode and 230 µA in *sleep* mode. Available in a 16-terminal LGA package, it is specified from –40°C to +125°C.

References

1. ADIS16209 Data Sheet. www.analog.com/ADIS16209.
2. ADIS16223 Data Sheet. www.analog.com/ADIS16223.

Author

Mark Looney [mark.looney@analog.com] is an *i*Sensor application engineer at Analog Devices in Greensboro, NC. Since joining ADI in 1998, he has accumulated experience in sensor signal processing, high-speed analog-to-digital converters, and dc-to-dc power conversion. He earned BS (1994) and MS (1995) degrees in electrical engineering from the University of Nevada, Reno, and has published several articles. Prior to joining ADI, he helped start IMATS, a vehicle electronics and traffic-solutions company, and worked as a design engineer for the Interpoint Corporation.

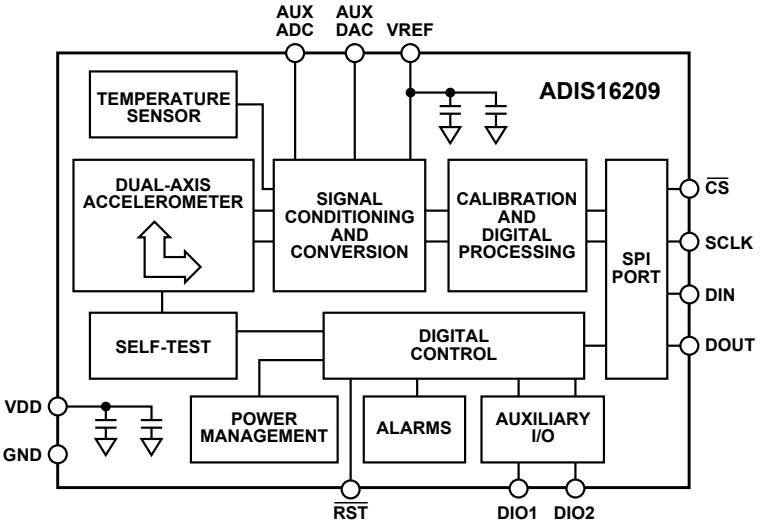

Figure A. ADIS16209 block diagram.

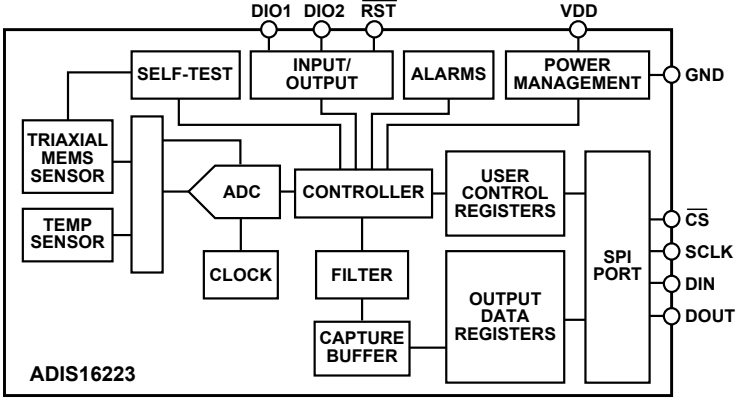

Figure B. ADIS16223 block diagram.

Dual Difference Amplifier with On-Chip Resistors Implements Precision ADC Driver

By Chau Tran

Introduction

Discrete difference amplifiers assembled from op amps and external gain-setting resistors exhibit mediocre accuracy and significant drift over temperature. With standard 1%, 100-ppm/°C resistors, the initial gain error of up to 2% can vary by up to 200 ppm/°C—and monolithic resistor networks, often used for precise gain setting, are bulky and expensive. Furthermore, most discrete op-amp circuits have poor common-mode rejection and an input voltage range smaller than the power supply voltage. While *monolithic differential amplifiers* have better common-mode rejection, they still suffer from gain drift due to the inherent mismatch between on-chip devices and the external gain resistor.

The versatile AD8270 dual difference amplifier, shown in Figure 1, overcomes these limitations, providing a complete, inexpensive, high-performance solution in the smallest available package. Each channel, which includes a low distortion amplifier and seven trimmed resistors, can be configured to implement a wide variety of high-performance amplifiers with various gains. All precision resistors are integrated on chip, so resistance matching and temperature tracking are excellent. Operating on a single 5-V to 36-V supply, or dual ±2.5-V to ±18-V supplies, and drawing a maximum supply current of only 2.5 mA per amplifier, the AD8270 is useful for driving high-performance ADCs.

This article shows two pin-strapped circuits that provide 0.1% gain accuracy with less than 10 ppm/°C gain drift—using *no external resistors*.

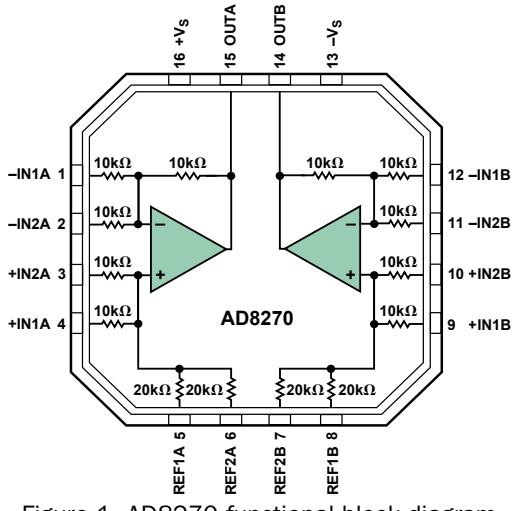

Figure 1. AD8270 functional block diagram.

Differential ADC Driver

The AD8270 can be configured to provide a differential output centered on a desired common-mode voltage, as shown in Figure 2. Amplifier A is configured for a gain of +½ and Amplifier B is configured for a gain of –½, so the combined gain is G = V_{OUT}/V_{IN} = ½ – (–½) = 1. The output common-mode voltage, (*OUT*+ + *OUT*–)/2, is equal to V_{OCM}.

When driving ADCs, the gain should be chosen such that the signal swing is close to the full-scale input range of the ADC. The impedance at the inverting and noninverting inputs of the amplifiers should be equal to eliminate the effect of bias currents and to maximize the common-mode rejection. The AD8603 unity-gain follower sets the common-mode output voltage of the differential amplifier to V_{OCM}, centering the signal in the middle of the ADC's input range. This pin can be tied to ground when the circuit is operated with dual supplies, to $V_S/2$ for single-supply operation, or—as shown—to the ADC's reference pin when driving single-supply ADCs, allowing ratiometric operation. The AD8603 can be eliminated if V_{OCM} is a low-impedance source.

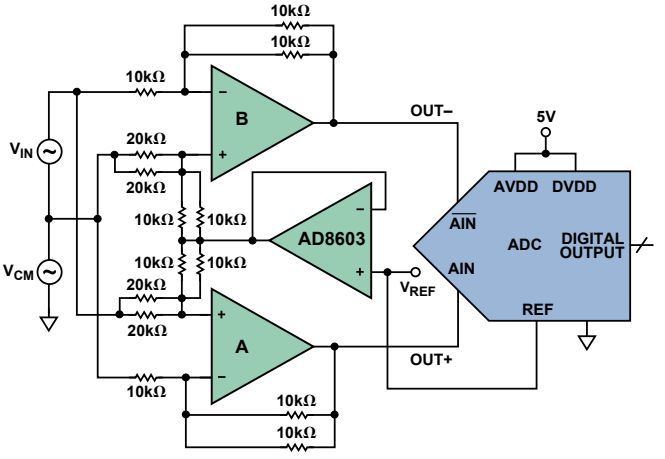

Figure 2. Differential amplifier drives ADC.

Operation at Gains Less Than 1 (Differential to Single-Ended)

To drive ADCs with low input ranges, the AD8270 gain block may be modified to provide gains of less than 1; an example is shown in Figure 3.

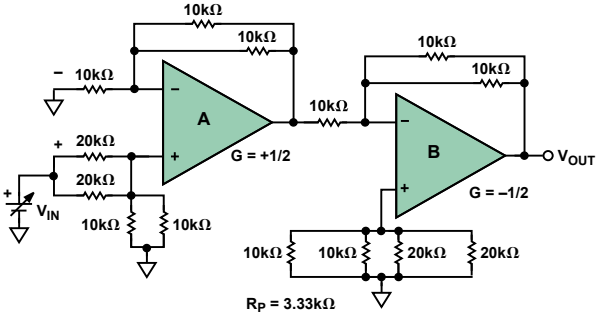

Figure 3. Connection for gains less than 1.

Pin strapping configures Amplifier A for a gain of +½. Amplifier B, configured for a gain of –½, attenuates the signal again, so the total gain for this connection is equal to –0.25.

$$G = \frac{V_{out}}{V_{in}} = \left(\frac{5\,\text{k}\Omega}{15\,\text{k}\Omega}\right)\left(1+\frac{5\,\text{k}\Omega}{10\,\text{k}\Omega}\right)\left(-\frac{5\,\text{k}\Omega}{10\,\text{k}\Omega}\right) = -0.25$$

Conclusion

The AD8270 dual difference amplifier—with its low offset voltage, low offset drift, low gain error, low gain drift, and 14 integrated precision resistors—can be used to implement accurate, stable amplifiers. Its wide power supply range allows it to accommodate a wide range of input voltage; and its space-saving package reduces PCB area, simplifies layout, decreases cost, and improves performance.

Author

Chau Tran [chau.tran@analog.com] joined Analog Devices in 1984 and works in the Instrumentation Amplifier Products (IAP) Group in Wilmington, MA. In 1990, he graduated with an MSEE degree from Tufts University. Chau holds more than 10 patents and has authored more than 10 technical articles.

Quad, 16-Bit Voltage-/Current-Output DACs Save Space, Cost, and Power in Multichannel PLCs

By Colm Slattery

Overview

Programmable logic controllers (PLCs) use fast, deterministic functions, such as logic, sequencing, timing, counting, and arithmetic algorithms, to control machines and processes. They use analog and digital signals to communicate with *end nodes* (reading sensors and controlling actuators, for example). Typical methods of communication include current/voltage loops, Fieldbus,[1] and industrial Ethernet[2] protocols.

The industry has a continuing tendency to increase the number of sensor and control nodes in the remote area, causing a corresponding increase in the number of I/O module nodes in the controller—and some *distributed control systems* (DCS) can handle thousands of nodes. This concentration of nodes brings increased temperature-related challenges, especially for systems that implement the 4-mA to 20-mA loop communications standard.

Perhaps the biggest and most relevant challenge to the system designer is the need for greater efficiency and reduced power consumption, as the inefficiency of existing systems results in wasted power and increased operating costs. This article explains the challenges of designing such systems for greater efficiency and introduces the AD5755, a versatile, 4-channel, 16-bit digital-to-analog converter (DAC) as a more integrated solution to help resolve these issues.

System

The levels of communication in a typical industrial control system are shown in Figure 1. Until recently, the distributed input/output (remote I/O and PLC) would typically be connected using such open or proprietary protocols as Modbus,[3] PROFIBUS[4] (process field bus), or Fieldbus. Nowadays, there is an increasing interest in using PROFINET,[5] a form of industrial Ethernet protocol that is designed for the fast exchange of data between Ethernet-based devices.

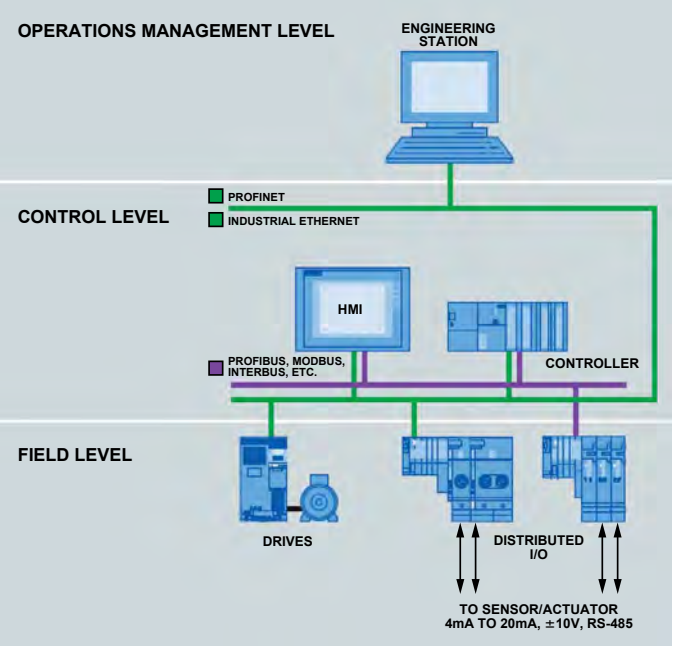

Figure 1. Hierarchy in a control system.

Some of the advantages of PROFINET are

- Increased speed, up from 9.6 kbps with RS-232 to 1 Gbps.
- Improved overall performance.
- Increased distance.
- Ability to use standard access points, routers, switches, hubs, cables, and optical fiber—which are immensely cheaper than the equivalent serial-port devices.
- Ability to have more than two nodes on link. This was possible with RS-485, but not with RS-232.

At the *field* level, field bus protocols, used to interconnect industrial drives, motors, actuators, and controllers to the PLC/DCS I/O systems, are numerous, including DeviceNet,™ CAN,[6] and InterBus,®[7] as well as the above-mentioned PROFIBUS and Fieldbus.

An input-output (I/O) controller connects to sensors and control actuators in a factory- or process environment; it communicates with multiple end nodes by analog and digital means, as noted above. Intrinsically safe systems connect via 4-mA to 20-mA current loops, and some use isolation. The control processor is typically an 8-bit to 32-bit processor with performance of up to 100 DMIPS (Dhrystone millions of instructions per second). Factory automation equipment is ruggedly constructed for fanless operation in a harsh industrial environment.

Examples of 8-channel analog I/O modules are featured in Figure 2. Because of their small size, they have limited power-dissipation capability, some even less than 5 W.

Figure 2. I/O modules.

Analog 4-mA to 20-mA current loops are commonly used for signaling in industrial process control, with 4 mA representing the low end of the range and 20 mA the high end. The key advantages of the current loop are that accuracy of the signal is not affected by voltage drops in the interconnecting wiring and the loop can supply up to 4 mA for powering the device. Even if the line has significant electrical resistance, the current loop transmitter will maintain the proper current, up to its maximum voltage capability.

The *live-zero* represented by 4 mA allows the receiving instrument to detect some failures of the loop (for example, 0 mA indicates an open loop, or 3 mA could indicate a fault condition on the sensor) and also allows *2-wire*-transmitter devices to be powered by the loop current. Such instruments are used to *measure* pressure, temperature, flow, pH, and other process variables and to *control* a valve positioner or other output *actuator*. The current in an analog current loop can be converted to a voltage input at any point in the loop with a series precision resistor. Since input terminals of instruments may have one side of the current loop tied to the chassis ground (earth), analog isolators may be required when connecting several instruments in series.

Power Dissipation Concerns

Figure 3 shows a system in which one channel is configured for 4-mA to 20-mA communications (in this case to drive an actuator load from a DAC). The termination resistance of the actuator determines the maximum compliance voltage needed across the loop. For example, a 100-Ω resistance would require at least 2 V at 20 mA. It is very common that today's systems must be able to drive loads of up to (and sometimes exceeding) 1 kΩ. With this load resistance, and a full-scale current of 20 mA, the supply would need to furnish at least 20 V. The power generated would be

$$P = V \times I = 20\ \text{V} \times 0.02\ \text{A} = 0.4\ \text{W}.$$

If the load resistance was changed to 100 Ω, using the same supply (a valid condition), the power dissipated would still be 0.4 W, even though only 0.04 W is needed. In this case there is a 90% loss of efficiency in the system, with 360 mW being wasted.

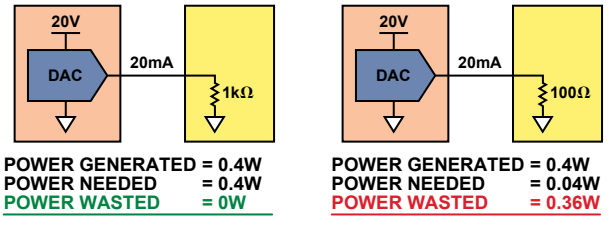

Figure 3. Power is wasted when full-scale output is much less than the power-supply voltage.

With an 8-channel module, the total power dissipation with a 20 V supply would be 3.2 W, of which as much as 2.88 W would be wasted in the module (if all loads are 100 Ω). In such cases, self heating, as well as the effect of the increased power budget, starts to become a consideration. Increased temperatures within the module can lead to increased system errors—the drift specs of the individual components need to be factored into the overall system error budget.

Designers may consider various ways to solve these problems:

- *Increasing the module size* allows more power dissipation, but the added cost makes this solution less competitive.
- *Heat sinking and/or fan control* can be used—an expensive solution that also increases space. Indeed, in some safety-critical applications, such temperature control devices are not allowed.
- *The maximum load resistance can be reduced* to limit the overall power dissipation in the circuit. This is a performance-limiting factor in some applications and is noncompetitive from a system marketing point of view.

In any event, the trend to provide an increased number of channels in a smaller space will cause further thermal power problems for many system designers.

One way to help solve this problem is to start with a 5-V supply. Monitor the output load voltage, then efficiently *boost* and regulate the output voltage as needed. The 5-V supply and an efficient dc-to-dc *boost converter* use *feedback control* to provide the appropriate output voltage, minimizing the on-chip power dissipation (Figure 4).

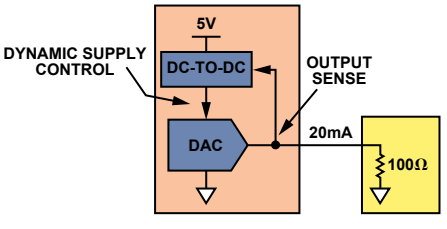

Figure 4. Dynamic supply control principle.

This kind of closed-loop dynamic power capability can be found in the AD5755 family of 4-channel, 16-bit, serial-input, voltage- and current-output DACs (see Appendix—Figure A). Because each of its four channels can individually furnish either current or voltage with 16-bit resolution, with output powered by an individual dc-to-dc converter under dynamic power control, the device provides the equivalent of four low-dissipation nodes in a very compact 9-mm × 9-mm × 0.8-mm package.

The simplified circuit of Figure 5 shows how the dynamic power control works, using an inductive boost circuit. Each channel is capable of providing a boosted output voltage greater than 30 V. The dynamic power control mechanism uses feedback to regulate the output voltage, which is divided down by a resistive voltage divider and compared to the reference voltage in an internal error amplifier to create an error current. At the beginning of the switching cycle, the MOSFET switch is turned on and the inductor current ramps up. The MOSFET current, converted to a voltage, is measured. When the current-sense voltage is greater than the error voltage, the MOSFET is turned off and the inductor current ramps down until the internal clock initiates the next switching cycle. A similar scheme is used to regulate the output compliance voltage in current mode. In this case a feedback error current is used.

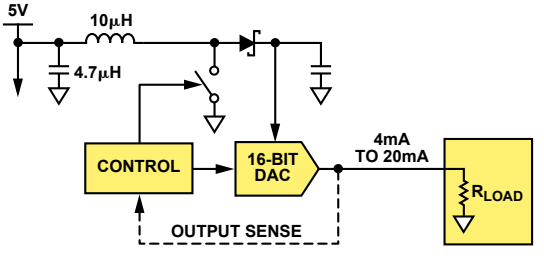

Figure 5. Voltage boost with power control.

The user has the option to switch the frequency and phase of each channel's dc-to-dc converter switching signals to allow for circuit and component optimization.

Programmable Switching Frequency: Offers the ability to change dc-to-dc switching frequencies, allowing for system optimization and more flexible choices of external components	**Programmable DC-to-DC Clock Phase:** Offers the ability to change the phase of the clock edges of individual dc-to-dc blocks, allowing for system optimization
• 333 kHz • 400 kHz • 500 kHz • 667 kHz	• All four channels clock on same edge • ChanA and ChanB clock on one edge, ChanC and ChanD clock on opposite edge • ChanA and ChanC clock on one edge, ChanB and ChanD on opposite edge • ChanA, ChanB, ChanC, and ChanD clock 90° out of phase from each other (0°, 90°, 180°, and 270°)

The dynamic power control on the output driver is designed to minimize package power dissipation. Typical ICs can operate at internal junction temperatures (T_{JMAX}) up to 125°C. Assume the ambient temperature, T_A, in the system is 85°C. The thermal impedance, θ_{JA}, for the LFCSP package is typically 28°C/W.

To calculate the allowable on-chip dissipation we can use the following analysis.

$$\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{125° - 85°}{28°C/W} = 1.42\ W$$

Without dynamic power control, assuming a 24-V supply, the worst-case power dissipation (per channel) can be calculated to be

$$\begin{aligned} \textit{Power Dissipation} &= \textit{Supply Voltage} \times \textit{Max Current} \\ &= 24\ V \times 20\ mA \\ &= 0.48\ W \end{aligned}$$

Four channels would dissipate nearly 2 W under similar conditions; this would cause problems for both the module and the semiconductor circuitry. By enabling the dynamic power feature, the AD5755 regulates the supply to minimize the on-chip power dissipation. Figure 6 shows a comparison of the power dissipated per channel with dynamic power enabled and disabled (fixed supply).

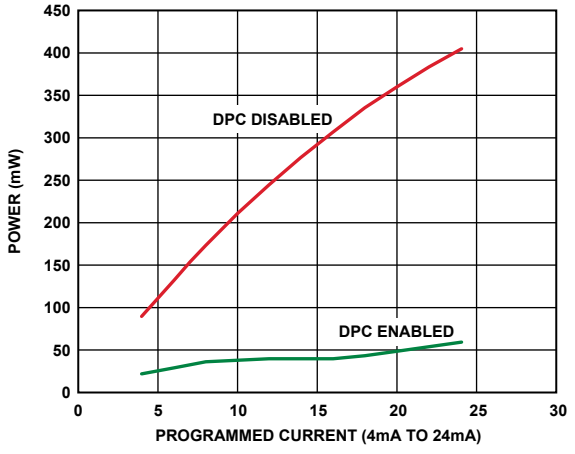

Figure 6. Dissipation comparison with and without dynamic power control.

When the dynamic power capability is enabled, the on-chip power dissipation is about 50 mW with output current of 24 mA vs. 400 mW with no regulation. This ability to control the on-chip power dissipation is of great value to the system designer because the number of channels in the system can be increased while minimizing module dissipation. It thus eliminates the need to consider extensive (and expensive) methods to control system temperatures.

System Error Checking and Diagnostics Under Fault Conditions:

For industrial applications, it is important to be able to monitor and report system-level faults and critical to have as much control as possible over the system under a fault condition. The AD5755 includes many on-chip diagnostic features that provide the user with system-level error checking.

One serious consideration is where the MCU/DSP that controls the DAC goes when a fault condition occurs. With no ability to control the output, the user would lose complete control of the system. The AD5755 has a watchdog timer (with programmable timeouts) that sets an alert flag (active *high*) if it has not received a command over the SPI interface within the timeout period. If desired, this alert pin can be directly connected to the CLEAR pin (also active high) to set the outputs into a known safe condition (Figure 7). Each channel on the AD5755 has a 16-bit programmable clear code register, giving the user flexibility to clear the output to any code.

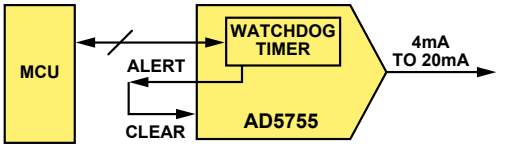

Figure 7. Watchdog timer flags loss of control signal and returns DAC to clear setting.

Even with the MCU operating normally, communications signals can become corrupted in noisy industrial environments. For dealing with this possibility, the AD5755 has an optional *packet error-checking* (PEC) function, which implements a CRC8 polynomial routine. This can be enabled or disabled through software to ensure that the output is never incorrectly updated.

Miswiring on the output can often lead to open- or short-circuit connections, potentially damaging the system. (Even if no damage occurs, the problem can often be difficult to diagnose. The AD5755 has open- and short-circuit detection, immediately setting a fault flag to alert a technician of the problem). In addition, short-circuit protection limits the output current in the event of a short circuit. All faults can be communicated via the SPI interface or through a hardware fault pin, allowing the user to take immediate action.

Flexible Output-Range Programmability

To deal with the required variety of voltages and currents, the AD5755 has many programmable ranges available for each channel, including: 4 mA to 20 mA, 0 mA to 24 mA, 0 mA to 20 mA, 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, and ±12 V. It is also possible for the user to digitally program the gain and offset of each range on individual channels. These gain- and offset registers have 16-bit resolution. For example, to set a 0-V to 10.5-V output range (as in Figure 8), first select the 0-V to 12-V range, then program the gain code to trim the gain to 10.5 V. Once the gain trim is complete, the output range will be 0 V to 10.5 V, with 16-bit resolution. The offset can be programmed in a similar manner.

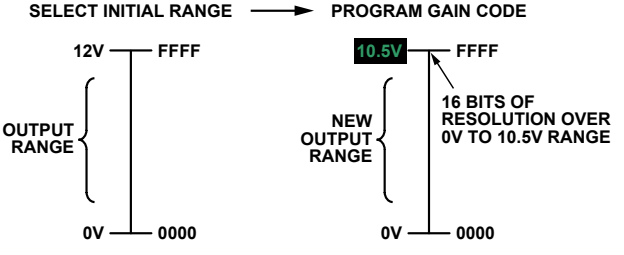

Figure 8. Arbitrary range scaling.

Communicating Additional Information Over the 4-mA to 20-mA Current Loop

The disadvantage of a pure 4-mA to 20-mA current loop is its unidirectional communication of a single process variable, an annoying limitation in modern industrial control systems. The development of the *highway-addressable remote transducer* (HART) standard opened up new possibilities for 4-mA to 20-mA communication lines.

HART provides for a digital two-way communication scheme that is compatible with 4-mA to 20 mA current loops. A 1-mA peak-to-peak *frequency-shift-keyed* (FSK) signal is superimposed on the 4-mA to 20-mA analog current signal. The two frequencies used are 1200 Hz (Logic 1) and 2200 Hz (Logic 0), based on the BELL 202 communications standard (Figure 9).

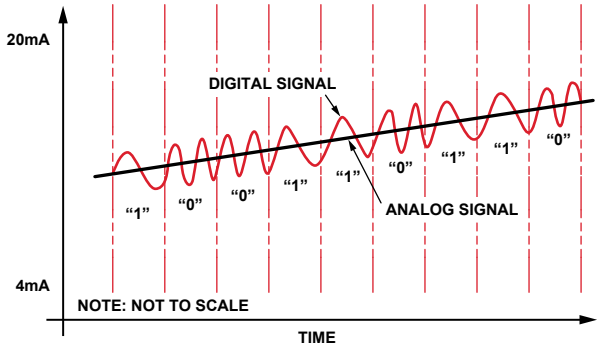

Figure 9. HART signal riding on an increasing loop current.

The AD5755 can be configured to transmit a HART signal with only two external components. The output of the HART modem is attenuated and ac-coupled at the CHART pin of the AD5755; this results in the modem output being modulated on top of the 4-mA to 20-mA analog current without affecting the "dc" level of the current. The circuit in Figure 10 shows how the AD5755 can interface to a HART modem to embody this dual form of communication.

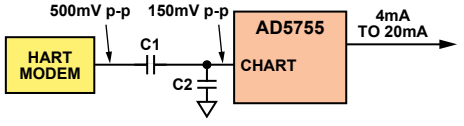

Figure 10. The AD5755 in HART communication.

The HART specification requires that the maximum rate of change of analog current not interfere with HART communications. Obviously, step changes in the current output can disrupt HART signaling. Fortunately, the AD5755 has controllable slew rate, which, when enabled, allows the user to digitally limit the slew rate of the current output.

AD5755 Complete Solution

Figure 11 shows a typical setup using the AD5755. (One HART modem channel is shown in the diagram, but four HART inputs are available—one per channel). When enabled, the dynamic power control feature requires four external components per channel: an inductor with a saturation current of the order of 1 A, a switching diode, and two capacitors having low *equivalent series resistance* (ESR). With a minimal number of external components, the AD5755 provides an integrated high-performance system capability on a single chip. The total unadjusted error (TUE), including all gain and offset errors at 25°C, is typically 0.01%.

Conclusion

As both the required number of channels and the density of channels per module increase, a number of problems present themselves to systems designers: How can I increase the number of channels while keeping the form factor of the module small? How can I increase the number of channels and design an energy-efficient system, while minimizing self-heating effects and drift errors within the system? How can I offer the most flexibility to my customer in terms of programmability of the outputs? What safety features and diagnostics can I provide to ensure robust systems in which problems can be easily tracked?

As a 4-channel device in a 9-mm × 9-mm CSP package, the AD5755 dramatically helps reduce board area while increasing channel density. With dynamic power control, the on-chip power dissipation is regulated and module power dissipation is minimized. The addition of on-chip diagnostics, including watchdog timers, PEC error checking, and open-/short-circuit detection and protection gives the end user higher confidence that the robust design is capable of working in harsh industrial environments. The AD5755 is a true system-on-a-chip solution.

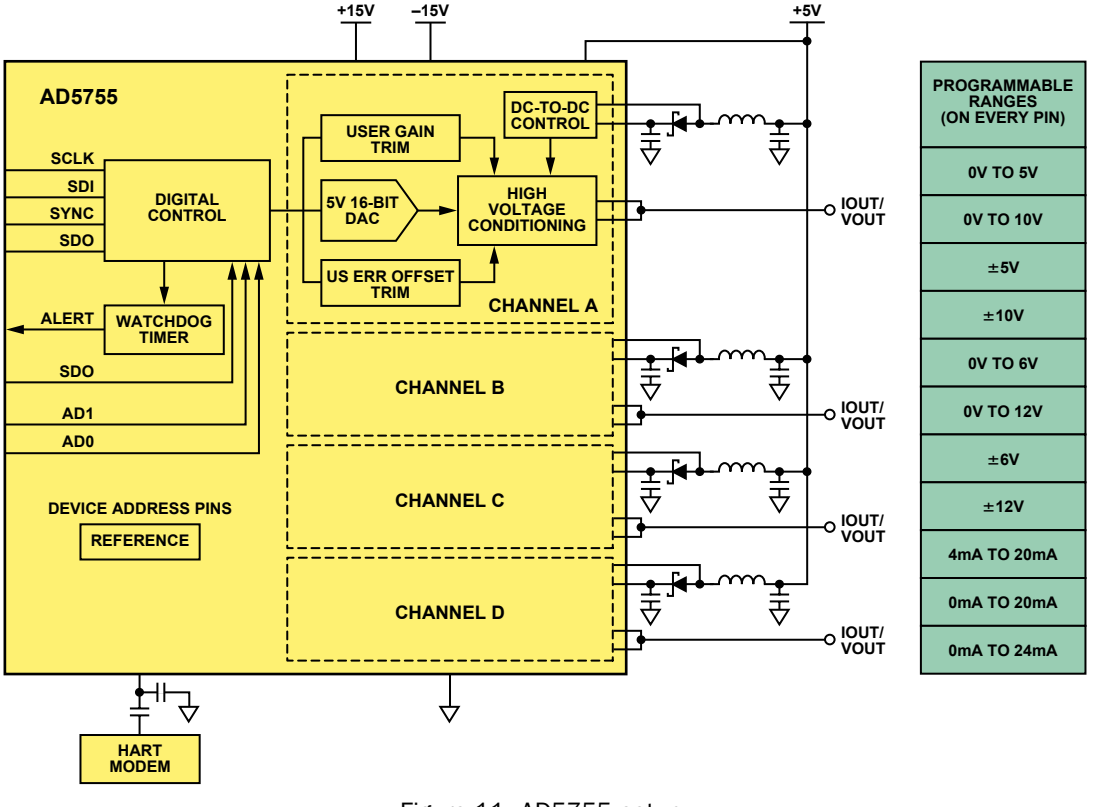

Figure 11. AD5755 setup.

APPENDIX

More About the AD5755 Quad DAC

The AD5755[8] quad voltage- and current-output DACs operate with a –26-V to +33-V power supply. On-chip dynamic power control minimizes package power dissipation in current mode by regulating the voltage on the output driver between 7 V and 30 V.

The AD5755 uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with standard SPI, QSPI,™ MICROWIRE,™ DSP, and microcontroller interface standards. The interface also features optional CRC-8 packet error checking, as well as a watchdog timer that monitors activity on the interface.

The AD5755 features 16-bit resolution and monotonicity, voltage or current output on the same pin, user-programmable offset and gain, on-chip diagnostics, an on-chip 5 ppm/°C max voltage reference, and a –40°C to +105°C operating temperature range. Available current-output ranges are 0 mA to 20 mA, 4 mA to 20 mA, and 0 mA to 24 mA ± 0.05%; available voltage ranges are 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, ±6 V, and ±12 V ± 0.05%.

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[8] www.analog.com/pr/AD5755.

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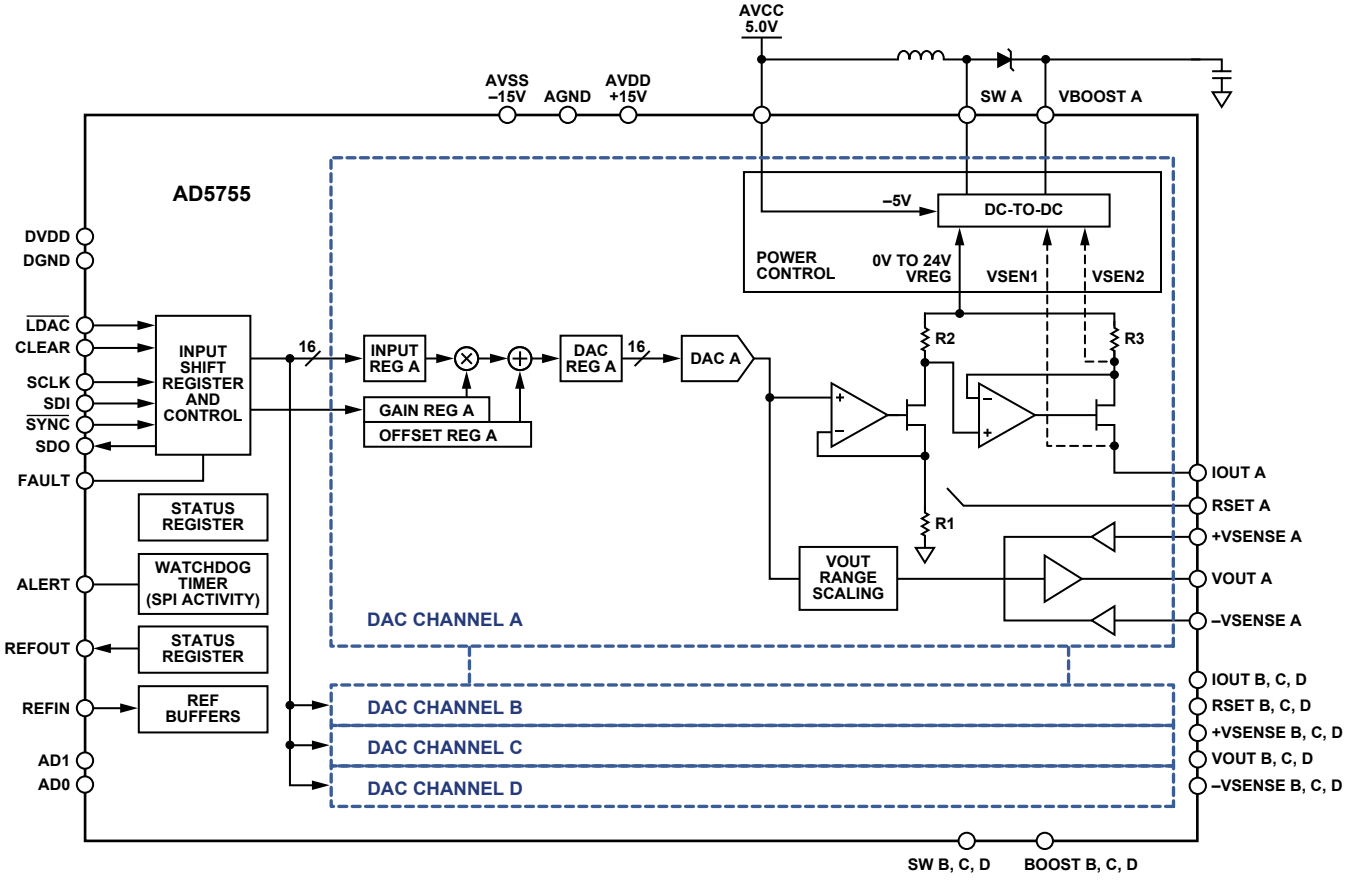

Figure A. Functional block diagram of the AD5755 quad DAC. All four channels are identical.

High-Speed, Current-Feedback Amplifier Drives and Equalizes Up to 100-m VGA Cables

By Charly El-Khoury

In classrooms, lecture halls, and conference rooms, PCs are connected to projectors through VGA cables to transmit red-green-blue (RGB) video signals. The average cable length depends on the room size and ceiling height, but most cables are shorter than 100 m. This article shows how the ADA4858-3[1] triple high-speed current-feedback op amp with integrated charge pump (see Appendix) can drive and equalize up to 100 m of VGA cable. This convenient, inexpensive, easy-to-implement solution—added between the PC and the cable—requires only a few passive components and a single 3.3-V to 5-V supply that can be generated from a USB port.

Driving and Equalizing a 45-m VGA Cable

Figure 1 shows one channel of a VGA cable equalizer based on the ADA4858-3 amplifier. Three channels are required for a complete RGB equalizer. The 150-Ω load resistor represents the 75-Ω terminated cable and its impedance-matching drive resistor.

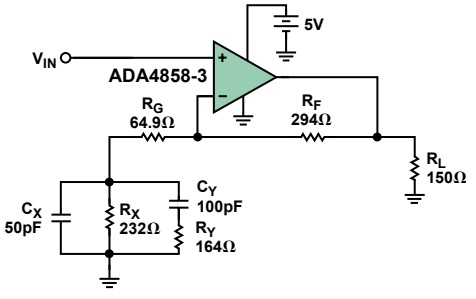

Figure 1. Schematic for 45-m VGA cable equalizer (single channel).

Figure 2 shows the large-signal frequency response of a 45-m VGA cable, the equalizer, and the equalizer/cable combination. In addition to the 6-dB attenuation inherent in the impedance-matched cable drive, the VGA cable has a 0.6-dB loss for frequencies lower than 1 MHz and an 8-dB loss at 100 MHz. To restore the signal strength, the equalizer must deliver 6.6-dB gain at low frequency and 14-dB gain at 100 MHz to boost the original signal by 6 dB for RGB video applications. The cable/equalizer combination shows a 100:1 improvement in 1-dB flatness, from 1.6 MHz unequalized to 160 MHz with equalization.

Equalization also improves the transient response, as shown in Figure 3. The high and low frequencies are restored, providing a sharper image without the smearing caused by the cable.

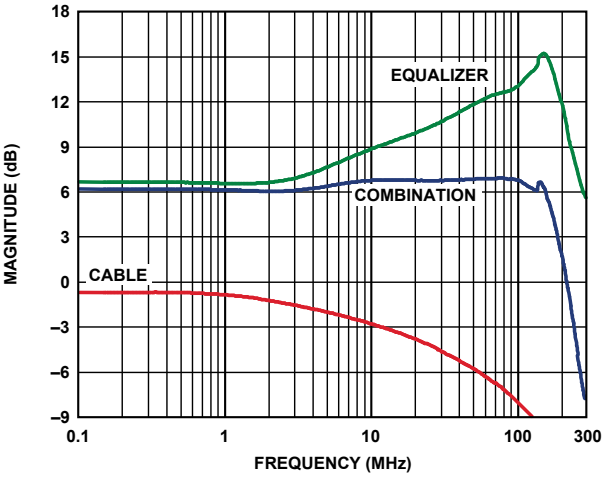

Figure 2. Large-signal frequency response (45-m VGA).

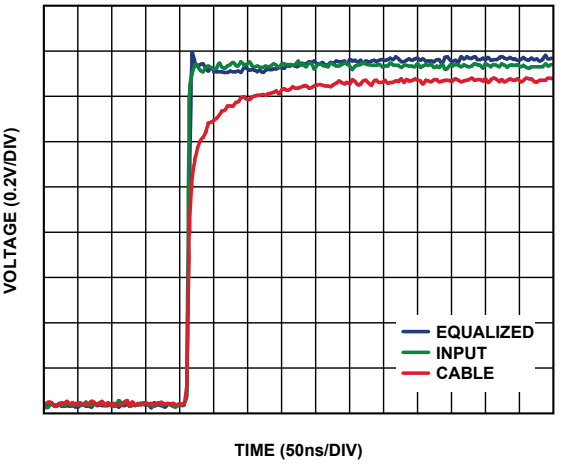

Figure 3. Transient response before and after equalization (45-m VGA).

The transfer function of this circuit is given by Equation 1. The magnitude is given by Equation 2.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_G + R_X \,||\, Z_{Cx} \,||\, (Z_{Cy} + R_Y)} \tag{1}$$

$$\left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{C_X C_Y (R_F + R_G) R_X R_Y \omega^2 + [C_X (R_F + R_G) R_X + C_Y (R_F (R_X + R_Y) + R_G (R_X + R_Y) + R_X R_Y] \omega + R_F + R_G + R_X}{C_X C_Y R_X R_Y R_G \omega^2 + [C_X R_X R_G + C_Y (R_G (R_X + R_Y) + R_X R_Y)] \omega + R_X + R_G} \tag{2}$$

Driving and Equalizing a 105-m VGA Cable

Figure 4 shows the schematic for driving a 105-m cable. This length was chosen because it is close to the maximum equalization of which the ADA4858-3 is capable. The schematic is similar to Figure 1, except for the addition of the R_ZC_Z feedback network that creates a pole to reduce the value of R_F at the higher frequencies.

Figure 5 shows the large-signal frequency response of the 105-m cable, the corresponding equalizer, and the combination of the two. The −3-dB bandwidth of the cable is about 2 MHz before equalization and 90 MHz after equalization; the −1-dB bandwidth has improved from 0.7 kHz to 75 MHz.

Figure 6 shows the transient response. Both high- and low frequencies have been restored. With more tweaking, better flatness between 1 MHz and 10 MHz could have been achieved for even better fidelity to the input signal.

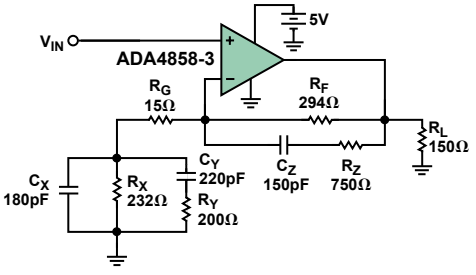

Figure 4. Schematic for 105-m VGA cable equalizer (single channel).

Figure 7 shows the schematic for all three channels (R, G, B), including all of the components required for a standalone solution. A mini USB port powers the overall system. R4, R5, and R6 are chosen to match the characteristic impedance of the cable.

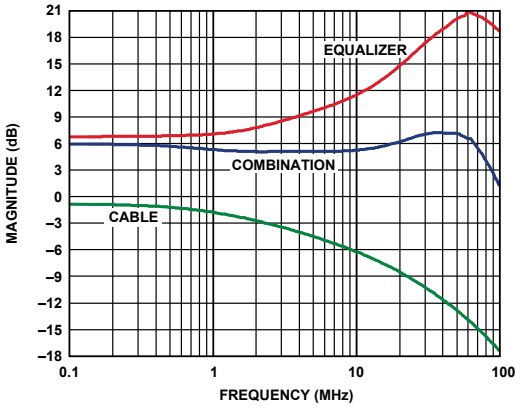

Figure 5. Large-signal frequency response (105-m VGA).

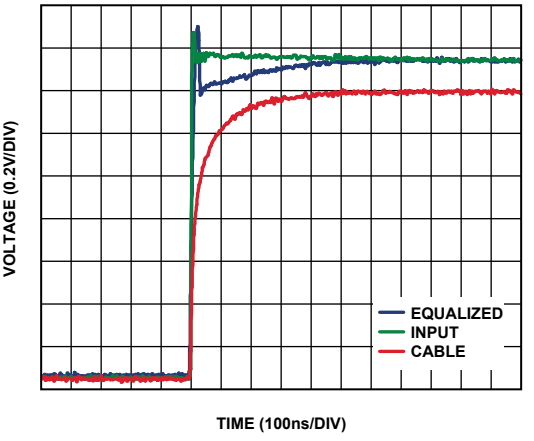

Figure 6. Transient response before and after equalization (105-m VGA).

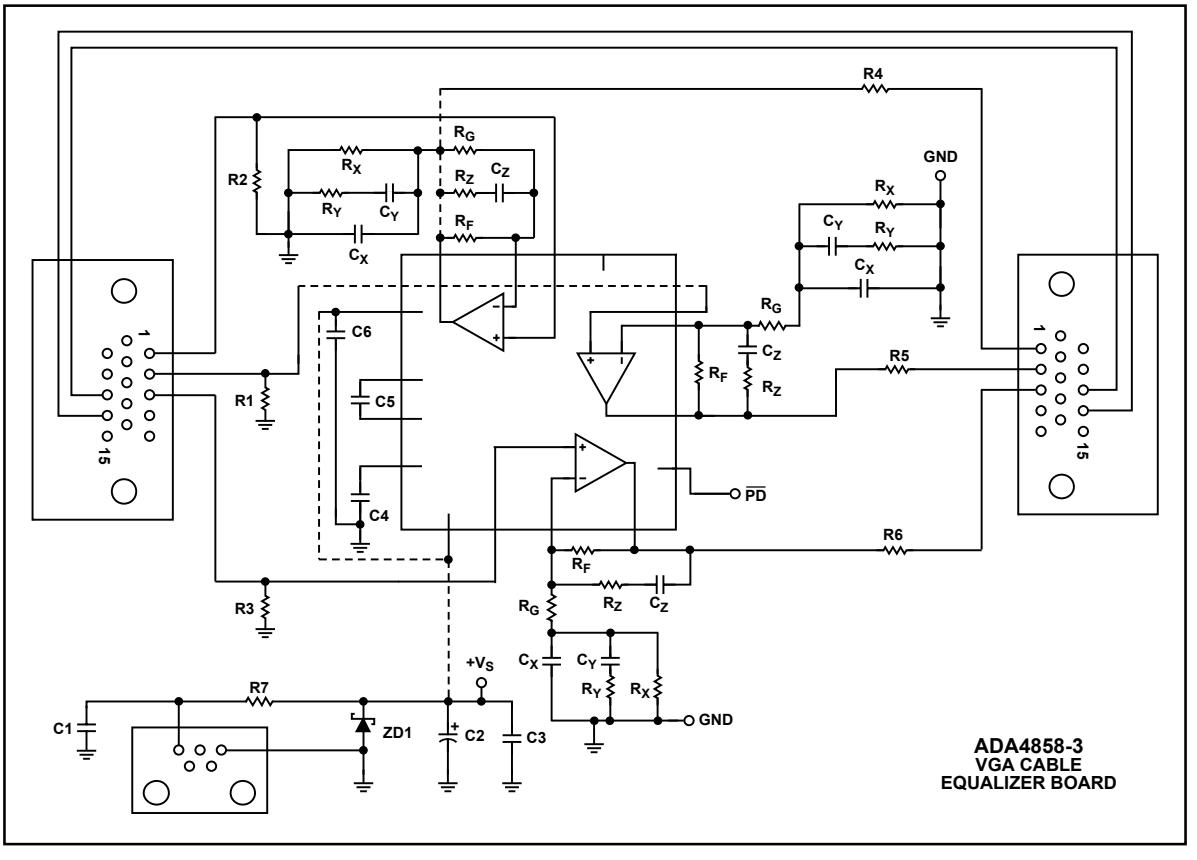

Figure 7. Complete board schematic showing all three equalization channels.

Conclusion

This article describes how to use the ADA4858-3 triple video driver to drive and equalize up to 100 m of VGA cable when transmitting RGB video. Two examples based on 45-m and 105-m cables are shown, but the solution can be scaled to accommodate various cable lengths. Convenient, inexpensive, and easy to implement, it combines the ADA4858-3, a few passive components, and a single 3.3-V to 5-V supply, which can be generated from a USB port.

Appendix

The ADA4858-3 triple current-feedback op amp draws only 42 mA of total quiescent current—including the charge pump. To further reduce the power consumption, a power-down feature lowers the total supply current to 2.5 mA when the amplifier is not being used; the charge pump, which eliminates the need for negative supplies, can still power external components in this mode. The ADA4858-3's wide input common-mode voltage range extends from 1.8 V below ground to 1.2 V below the positive rail (in 5-V operation). The 600 MHz bandwidth and 600 V/μs slew rate make it well suited for many high-speed applications, and the 0.1-dB flatness at frequencies up to 85 MHz (G = 2, 150-Ω load) make it well suited for professional- and consumer video. In addition, current-feedback amplifiers avoid the gain-bandwidth limitation of voltage-feedback amplifiers.

The on-chip charge pump creates a negative supply whose voltage depends on the positive supply voltage. With a 5-V positive supply, the charge pump generates a −3-V negative supply with 150 mA output current; with a 3.3-V supply, the charge pump generates a −2-V negative supply with 45 mA output current. External capacitors, C1 and C2, should have capacitance between 1 μF and 4 μF, with low ESR and low ESL, and should be placed as closely as possible to the ADA4858-3. C1 is connected between C1_a and C1_b; C2 is connected between CPO and ground.

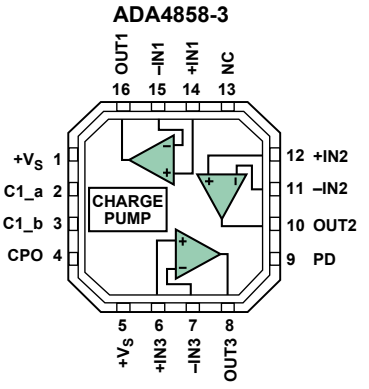

Figure A. Functional block diagram.

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