Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing • Volume 50, Number 1, 2016

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Editor's Notes

IN THIS ISSUE

Integrated Multiplexed Input ADC Solution Alleviates Power Dissipation and Increased Channel Density Challenges

Space- and power-constrained applications are driving the demand for integrated data acquisition solutions with high channel counts, low power, and a compact form factors. This article highlights the design considerations involved with multiplexed data acquisition systems and focuses on an integrated multiplexed input ADC solution that enables those critical applications that can be found in optical transceivers, wearable medical devices, the Internet of Things (IoT), and other portable instruments. (Page 3)

An Engineering Walk Through Virtual Eval, ADI's Online Data Converter Product Evaluation Tool

Do you need to develop a next-generation platform that meets cutting-edge requirements, on an implausible timeline, while remaining within an unjustly slim budget, and trying to do it all with a smile? ADI may have your answer with a comprehensive online product evaluation tool called Virtual Eval that employs detailed software models to simulate crucial part performance characteristics without the purchase of hardware. With this tool you can easily configure a variety of operating conditions and device features to establish your customized use case and get simulation results within minutes. This article explains it all. (Page 8)

Powering GSPS or RF Sampling ADCs: Switcher vs. LDO

The new breed of high performance GSPS data converters provides systems designers with the ability to sample wider and wider bandwidths at high levels of dynamic range. The traditional thinking was that in order to achieve its rated dynamic range, high speed converters must be powered by linear supplies. However, the constant market pressure to reduce overall system power, size, and costs has brought into question utilizing a more efficient, switching power supply solution. But will switchers work for GSPS ADC applications? In this article the author compares the two supply approaches in terms of system performance, power efficiency, operational costs, and BOM savings. (Page 11)

Ferrite Beads Demystified

A ferrite bead is a passive device that filters high frequency noise energy over a broad frequency range. It is frequently connected in series with the power supply rail and often combined with capacitors to ground on either side of the bead to form a low-pass filter to reduce supply noise. Sounds simple, but in this article the author details several critical design techniques involved with implementing ferrite beads that must be considered to avoid resonance that can induce noise and ripple in the supply. (Page 17)

Analog Front-End Design Considerations for RTD Ratiometric Temperature Measurements

Many system designers use Σ-Δ ADCs together with RTDs (resistance temperature detectors) for implementing a temperature measurement function, but have difficulties with achieving the level of performance as specified by the data sheet of the ADC they are using. For example, some designers may only be able to get 12- to 13- noise-free bits from a 16-bit to 18-bit ADC. The front-end RTD design techniques introduced in this article will enable designers to achieve 16+ noise-free bits in their system designs. (Page 23)

Phase Response in Active Filters

Part 3—The Band-Pass Response

While filters are designed primarily for their amplitude response, the phase response can be important in some applications—for instance, where a filter is utilized in a process control loop. Author Hank Zumbahlen has addressed many aspects of filter phase response in this article series. In the first article, he examined the relationship of the filter phase to the topology of the implementation of the filter. In the second article, he focused on the phase shift of the filter transfer function for low-pass and high-pass responses. In this third article in the series, he concentrates on the phase response of band-pass filters. (Page 26)

Jim Surber [jim.surber@analog.com]

Product Introductions: Volume 50, Number 1

Data sheets for all ADI products can be found by entering the part number in the search box at analog.com.

January

Low power, complete 3-axis accelerometer IC with signal conditioned voltage outputs **ADXL316**
Ultralow noise, low power current amplifier **ADPD2210**
Quad-channel, zero-drift op amp with low noise and power **ADA4522-4**
Operational amplifier with a femtoampere level input bias current **ADA4530-1**
High quality, low power, single-input HDMI® to LVDS display bridge **ADV7613**
Single-channel digital isolator supports data rates as high as 150 Mbps **ADuM110N**
Highly efficient, ultralow quiescent current step-down regulator **ADP5304**
High performance dc-to-dc inverting regulator **ADP5074**
1.2 A dc-to-dc switching inverting regulator **ADP5073**
11.07 GHz to 11.62 GHz MMIC VCO with half-frequency output **HMC1165**
GaAs, pHEMT, MMIC power amplifier provides 19 dB of gain **HMC1144**
6-bit digital phase shifter that is rated from 4 GHz to 7 GHz **HMC1133**
Broadband, nonreflective, single-pole, double-throw switch **HMC1118**
Triple SPDT with user-defined fault protection and detection **ADG5243F**

February

Family of ARM® Cortex®-M4 mixed-signal control processors **ADSP-CM40x**
5 kV rms, 600 Mbps, dual-channel LVDS isolator **ADN4651**
25 MHz to 3000 MHz fractional-N PLL with integrated VCO **HMC832A**
24 GHz VCO and PGA with 2-channel PA output **ADF5901**
24-output, 3-channel clock generator **AD9531**

March

Complete 6 degrees of freedom precision inertial system **ADIS16460**
Low cost, single-axis, PSI5-compatible satellite sensor **ADXL151**
Gallium nitride (GaN) 10 W broadband power amplifier **HMC1099**
8-channel, simultaneous sampling 24-bit Σ-Δ analog-to-digital converter **AD7768**
Robust 3.0 kV rms, dual-channel digital isolator and 0 reverse channel **ADuM120N**
Robust 3.0 kV rms, dual-channel digital isolator and 1 reverse channel **ADuM121N**
5 kV rms, 600 Mbps dual transmitter or receiver channel LVDS isolator **ADN4650**
20 V, 6 A, synchronous step-down, dc-to-dc regulator **ADP2387**
800 MHz to 4000 MHz, highly integrated intermediate frequency transmitter chip **HMC8200**
High performance, 3.2 GHz, 14-output fanout buffer **HMC7043**
11.41 GHz to 12.62 GHz MMIC VCO with half-frequency output **HMC1166**
12.17 GHz to 13.33 GHz MMIC VCO with half-frequency output **HMC1167**
300 MHz to 1100 MHz balanced mixer, LO buffer, and RF balun **ADL5369**
General-purpose, nonreflective, 0.1 GHz to 6.0 GHz, silicon SP4T switch **HMC7992**

Analog Dialogue

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Integrated Multiplexed Input ADC Solution Alleviates Power Dissipation and Increased Channel Density Challenges

By Maithil Pachchigar

Introduction

An increased number of applications in industrial, instrumentation, optical communication, and healthcare industries use multichannel data acquisition systems that result in increased printed circuit board (PCB) density and thermal power dissipation challenges. The need for increased channel density in these applications is driving the demand for a high channel count, low power, and compact form factor integrated data acquisition solution. These applications also demand precision measurements, reliability, affordability, and portability. System designers make trade-offs among performance, thermal stability, and PCB density to maintain optimum balance and they are continually pressed to find innovative ways to tackle these challenges while minimizing overall bill of material (BOM) cost. This article highlights the design considerations for multiplexed data acquisition systems and focuses on an integrated multiplexed input ADC solution to address these technical challenges for space constrained applications such as optical transceivers, wearable medical devices, the Internet of Things (IoT), and other portable instruments. The proposed low power solution using integrated, multiplexed input 4-channel/8-channel, 16-bit, 250 kSPS PulSAR® ADCs AD7682/AD7689 available in a miniature, 2.39 mm × 2.39 mm, wafer level chip scale package (WLCSP) footprint saves over 60% board space to address the challenges for increased channel density and battery-powered portable systems while offering a flexible configuration and precision performance.

Multiplexed Data Acquisition Systems

Multichannel data acquisition systems typically employ different types of discrete single-channel or integrated multiplexed and simultaneously sampled analog signal chains for interfacing with various sensor types such as temperature, pressure, optical, vibration, and many more based on application requirements. For example: multiplexing multiple input channels into a single ADC, using individual track and hold amplifiers, and multiplexing them into a single ADC, and using individual ADCs to allow the simultaneous sampling of each channel. The successive approximation register (SAR) analog-to-digital converter (ADC) is typically used in the first case, as shown in Figure 1. It offers significant power, space, and cost savings, where individual channels may need low-pass antialiasing filter at inputs, and their channel switching and sequencing are properly synchronized with the ADC conversion time. In the second case, as shown in Figure 2, the achievable throughput rate is divided by the number of channels simultaneously sampled, but the constant phase between the sampled channels can still be maintained. As shown in Figure 3, some applications require a dedicated amplifier and ADC on a per channel basis for simultaneously sampling the inputs to obtain an increased sampling rate per channel and to preserve the phase information at the expense of additional area and power. The simultaneous sampling ADCs are typically used in automated test equipment, power line monitoring, and multiphase motor controls that require continuous sampling at a higher throughput rate per channel to preserve the phase information between channels for accurate instantaneous measurements.

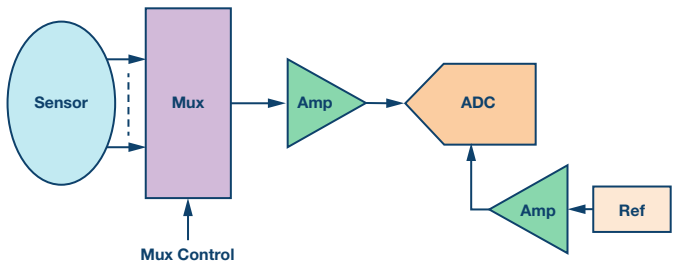

Figure 1. Simplified multichannel data acquisition signal chain case I.

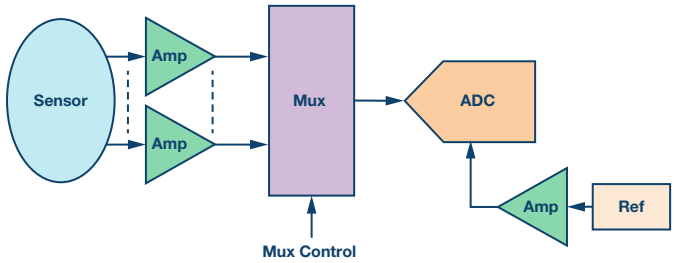

Figure 2. Simplified multichannel data acquisition signal chain case II.

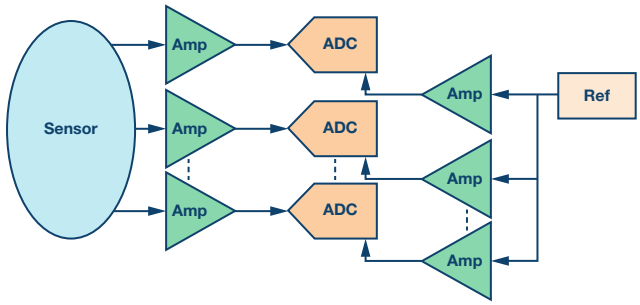

Figure 3. Simplified multichannel data acquisition signal chain case III.

The key benefit of multiplexing is that a fewer number of ADCs per channel are required, resulting in reduced space, power, and cost. However, the achievable throughput rate in a multiplexed system is the single ADC throughput rate divided by the number of channels being sampled. The SAR ADCs offer inherent merits of low latency and dynamic power scaling with throughput. They are often used in channel multiplexed architectures ideally suited for sensing and monitoring functions. Multiplexed data acquisition systems utilized in optical transceiver modules need high channel density and wearable medical devices require small form factors and low power, where the signals from multiple sensors need to be monitored and multiplex many input channels into a single or several ADCs. One of the main challenges with multiplexed data acquisition systems is that when the input is switched to the next channel, it requires a fast response to step input near full-scale amplitude to minimize any settling time or crosstalk issue. The following section presents a real-world use case of an SAR architecture-based multiplexed input ADC for optical transceivers and wearable electronic devices. It explains why the AD7689 is ideally suited for these types of applications.

Optical Transceivers

The market for 100 Gbps optical transceivers is uniquely positioned to grow in the next decade for high speed coherent optical transmission. The key challenge for optical transceivers is to acquire and process wider bandwidth signals or multiplex a number of input channels at lower power in a smaller footprint. The size, power, and cost structure of today's transceivers originally designed for long haul applications limit their utilization in more cost-sensitive metro networks. The metro networks include: metro regional 500 km to 1000 km, metro core 100 km to 500 km, and metro access <100 km applications. Due to fierce competition in metro networks, the space comes at a high premium, making line-card density extremely crucial and, consequently, a path to lower cost optical line cards or pluggable modules in a smaller footprint has become increasingly important for coherent applications.

In optical networks, as the bit rates per channel increases from 10 Gbps toward 100 Gbps and higher, the optical fiber nonidealities severely degrade signal quality and affect its transmission performance. Technical challenges also arise in long haul optical networks when the penalties occur in terms of optical noise, nonlinear effects, and dispersion due to optical fiber impairment. To address these significant challenges, various manufacturers of 40 Gbps and 100 Gbps optical transceivers use coherent technology that allow higher data rate connectivity with maximum reach at longer distances for metro long haul, long haul, and ultralong haul networks. The coherent technology generally combines multilevel signal formats and coherent detection using dual polarization, quadrature, phase-shift keying (DP-QPSK) for optimized signal modulation, allowing immunity to fiber impairments at higher data rates, and making 100 Gbps transmission economically and technically feasible. The next generation of 100 Gbps (and above) data rate optical transceivers will require lower power consumption and a miniature form factor to allow increased channel density for significant space, power, and cost savings. Depending on the requirements, the channel count typically varies anywhere from eight to 64 in an optical system. The component placement and trace routing become prominent for the PCB designers, especially for high channel density system.

A simplified block diagram of generic optical module is shown in Figure 4, which includes transmitter, receiver, micro-ITLA (integrated tunable laser assembly), and data acquisition components. Figure 5 shows the simplified block diagram of a micro-ITLA, which is a wideband electronically tunable laser device that controls rapid wavelength switching. The transmitter includes a Mach-Zehnder driver and modulator to control the amplitude or intensity of the exiting laser light. The multiplexed input ADC is typically used in control and monitoring functions to digitize the data from the multiple channels in optical module and micro-ITLA.

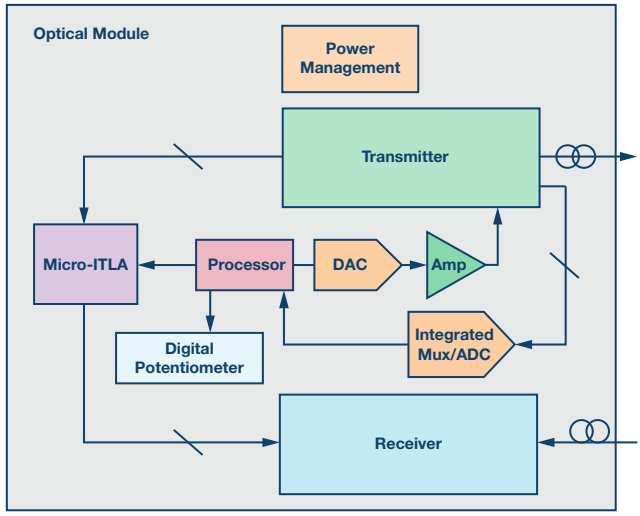

Figure 4. Simplified block diagram of an optical module.

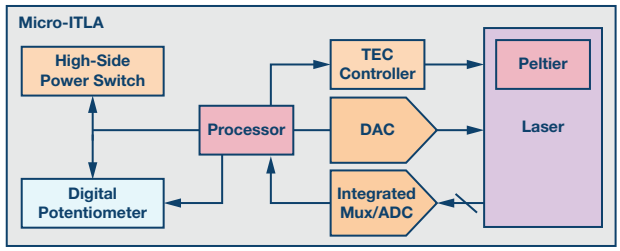

Figure 5. Simplified block diagram of a microintegrated tunable laser assembly.

Vital Sign Monitoring Using Wearable Electronic Devices

A high level block diagram of a typical wearable electronic device is shown in Figure 6. Modern wearable electronic devices integrate various sensors to accurately monitor multiple human biometrics in real time. They offer a flexible user interface for data storage and data transmission through Wi-Fi to a personal smartphone, tablet, or laptop. They use biopotential, bioimpedance, or optical sensors to derive information about multiple vital signs such as the heart rate, respiration rate, and oxygen saturation level in blood (SpO2). The acoustical sensor is used to extract information about blood pressure and dietary activities, and the temperature sensor is used to measure body temperature. The MEMS-based inertial motion sensor (accelerometer) is used to track daily physical activity. The signals from different sensors require analog signal conditioning, which are then multiplexed into an ADC. Some of the signals might need to get sampled simultaneously as well, depending on the system. The ADC then digitizes these signals and the processor or microcontroller finally postprocess them to extract information about numerous physiological measures.

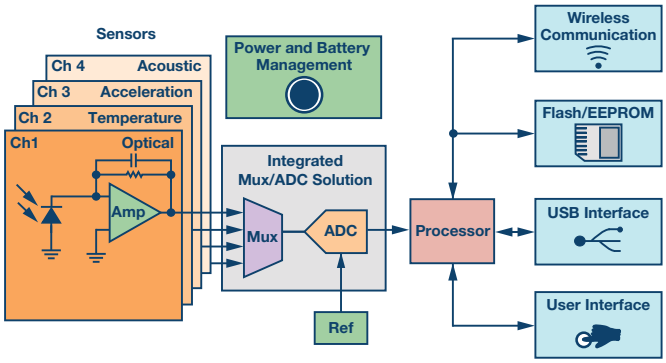

Figure 6. A simplified block diagram of wearable electronic device.

An electrocardiogram (ECG) has traditionally been used to monitor heart activity, which is critical for physiological monitoring and cardiac diagnosis. However, smart wearable systems use optical and bioimpedance sensors that allow integration of heart rate monitors in wearable electronic devices such as wrist-worn watches, bands, or activity trackers.

In optical systems, rapidly flashing infrared light is transmitted through the skin surface and a photodetector measures the light absorbed by the red blood cells. The analog front end conditions and digitizes this tiny signal, which is then post-processed to extract information about multiple physiological variables such as the heart rate, respiration rate, and SpO2 using a photoplethysmographic (PPG) technique.

The bioimpedance sensors consume much less power compared to other technology such as optical, extending battery life. Bioimpedance sensors can be used to measure the respiration rate or skin impedance. A sinusoidal signal is injected into the skin (body tissue) through electrodes and a tiny current flow through is measured, digitized, and postprocessed to accurately interpret various physiological signals like the respiration rate, skin conductance, or water in the lungs.

These devices demand highly integrated and very sensitive, cost-effective, power efficient battery-powered solution that can fit into a miniaturized module. They must reliably and accurately monitor multiple physiological variables while offering increased immunity to motion generated artifacts and external environmental conditions, otherwise they can obscure the true signal with noise, leading to inaccurate readings. Therefore, it is important to have good noise performance of the ADC and oversampling or averaging is often used to improve the overall dynamic range. The input frequency band of interest is from dc to 250 Hz, so ADC sampling rates are close to a few kilosamples per second (kSPS).

Integrated Multiplexed Input 4-Channel/8-Channel, 16-Bit, 250 kSPS ADCs

The AD7682/AD7689 is the industry's leading integrated, multiplexed input 4-channel/8-channel, 16-bit, 250 kSPS SAR-based ADC manufactured on Analog Devices' proprietary 0.5 µm CMOS process. The integrated 4-channel/8-channel low crosstalk multiplexer introduces minimal mismatch from between adjacent channels and allows sequential sampling. These ADCs allow the choice of a very low temperature drift internal 2.5 V or 4.096 V precision voltage reference, an external reference, or an external buffered reference and on-board temperature sensor monitors the typical internal temperature of the ADC. This eliminates the need for external components, significantly saving PCB area and BOM cost. They include a channel sequencer useful for scanning channels as singles or pairs, with the internal temperature sensor enabled or disabled in a repeated fashion. It offers a flexible serial digital interface compatible with SPI, MICROWIRE, QSPI, and other digital hosts. Its 14-bit internal configuration register allows the user to select various options including a number of channels to be sampled, a reference, a temperature sensor, and a channel sequencer. The interface allows a 4-wire read during conversion, read after conversion, and read spanning conversion modes with and without a busy indication. The AD7682/AD7689 is ideally suited for high channel density applications such as optical transceivers, wearable medical devices, and other portable instruments for precision sensing and monitoring.

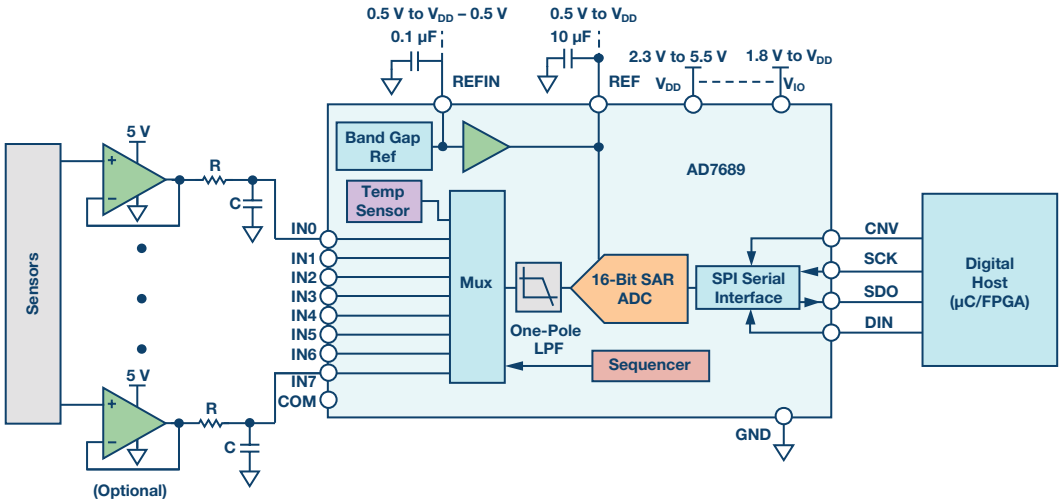

Figure 7. AD7689 typical application diagram (all connections and decoupling not shown).

Figure 7 shows a simplified AD7689 block diagram for a multichannel data acquisition system, which offers easy to use flexible configuration options and precision performance. It solves the complex design issues related to the channel switching, sequencing, and settling time and it saves design time.

For multichannel, multiplexed applications, some designers use a low output impedance buffer to handle the kickback from the multiplexer inputs depending on the throughput rate used. The input bandwidths of the SAR ADC (tens of MHz) and ADC driver (tens to hundreds of MHz) are higher than the sampling frequency, whereas the desired input signal bandwidth is typically in the tens of Hz to hundreds of kHz range. Therefore, depending on the system requirements, a single-pole, low-pass RC antialiasing filter may be required at the input of the multiplexer to eliminate unwanted signals (aliases) from folding back into the bandwidth of interest, to limit the noise, and to reduce settling time issues. The value of the RC filter used at each input channel should be carefully selected based on the following trade-off because too much band limiting can affect settling time and increase distortion; if the capacitance is large, it will help attenuate the kickback from the multiplexer, but it can also make the previous amplifier stage unstable by degrading its phase margin. C0G or NP0 type capacitors are recommended for an RC filter that has a high Q, low temperature coefficient, and stable electrical characteristics under varying voltages. A reasonable value of series resistance should be chosen to keep the amplifier stable and limit its output current. The resistance cannot be too large or the ADC driver will not be able to recharge the capacitor after the multiplexer kickback.

Small Form Factor

The AD7682/AD7689 is now available in a 2.39 mm × 2.39 mm, pin-compatible, wafer level chip scale package (WLCSP), which is an over 60% smaller form factor compared to its existing 4 mm × 4 mm lead frame chip scale package (LFCSP) or other competitive device of its class, allowing increased circuit density in a small system footprint. Figure 8 compares the miniaturized size of its WLSCP with the size of a standard 6 mm pencil.

Figure 8. Size comparison of AD7682/AD7689 wafer level, chip scale package with a standard pencil.

The active side of the of AD7682/AD7689 WLCSP die is inverted and can be connected to the PCB using solder balls and its dimensions after PCB assembly are, as shown in Figure 11. The actual separation between the surface of the die and the substrate (standoff) after PCB assembly varies with the amount of solder screen printed on to the substrate and pad diameter.

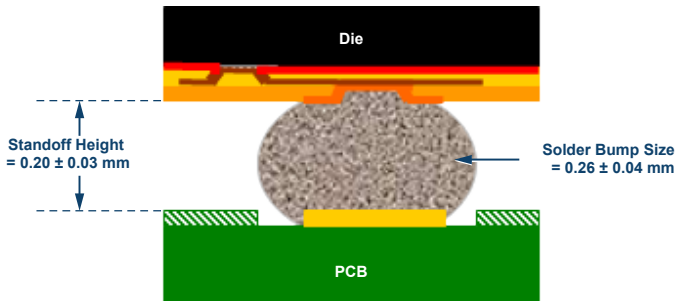

Figure 9. AD7682/AD7689 WLCSP dimensions after PCB assembly.

Low Power Dissipation

The AD7682/AD7689 requires an analog and digital core supply (V_{DD}) and a digital input/output interface supply (V_{IO}) for a direct interface with any logic between 1.8 V and V_{DD}. The V_{DD} and V_{IO} pins can also be tied together to save on the number of supplies required in the system, and they are independent of power supply sequencing. Powered from 5 V (V_{DD}) and 1.8 V (V_{IO}) supplies, its power scales linearly with throughput rate, enabling very low power consumption—

typically around 1.7 µW typ at 100 SPS and 12.5 mW at 250 kSPS with a 5 V external reference, as shown in Figure 10. This makes the ADC power efficient and well-suited for both high and low sampling rates even as low as a few Hz and for portable and battery-powered systems. One of the key features of this part is that it powers down automatically at the end of each conversion phase and consumes a very low standby current of typically only 50 nA, allowing conservation of the battery when the device is not utilized, thus extending battery life.

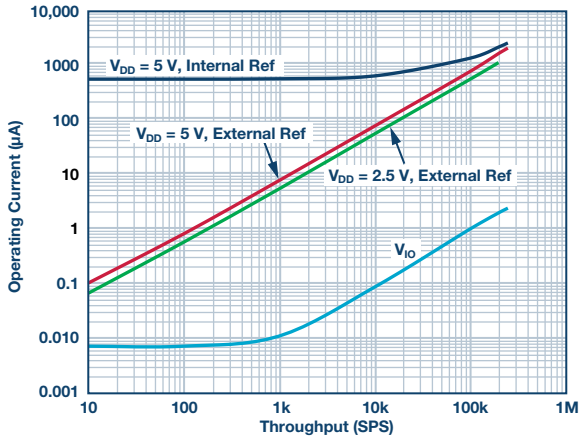

Figure 10. AD7682/7689 operating current vs. throughput.

Precision Performance

For applications that require multiple AD7682/AD7689 devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk. The best SNR is achieved with a 5 V external reference since the internal reference is limited to 4.096 V. It offers excellent ac and dc performance in terms of INL of ±1.5 LSB, signal-to-noise plus distortion ratio (SINAD) of ~93 dB and an effective number of bits (ENOB) of ~15.2 bits using a 5 V external reference for a 2 kHz input tone while running at the full speed of 250 kSPS. Figure 11 shows the typical performance of SNR, SINAD, and ENOB for a given external reference voltage utilized.

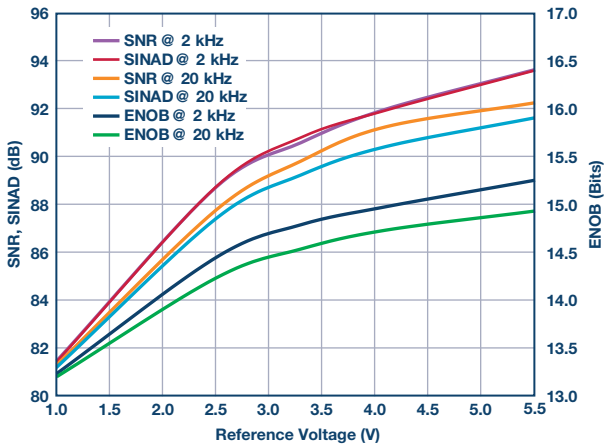

Figure 11. AD7682/7689 SNR, SINAD, and ENOB vs. reference voltage.

Conclusion

The next generation of pluggable optical transceiver modules and other portable systems demand power efficient data acquisition system in a small, low cost form factor. The AD7682/AD7689, with industry-leading integration and precision performance, supports a wide range of sensor interfaces and enables designers to differentiate their systems while meeting stringent user requirements. This power efficient integrated ADC solution addresses the increased circuit density and thermal power dissipation challenges for space constrained applications by saving over 60% space compared to its existing LFCSP and competitive offerings, which is well-suited for both high and low sampling rates applications.

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Maithil Pachchigar

Also by this Author:

A Low Power Data Acquisition Solution for High Temperature Electronics Applications

Volume 49, Number 3

An Engineering Walk Through Virtual Eval, ADI's Online Data Converter Product Evaluation Tool

By Tom MacLeod and Jason Cockrell

Overview

Setting down your third cup of coffee, you pick up a pile of specifications with a sigh. Today you face a familiar challenge: Develop a next-generation platform that meets cutting-edge requirements on an implausible timeline while remaining within an unjustly slim budget, and do it all with a smile. You must choose the right vendors for the project, and to meet these ever more strenuous goals, you need vendors that provide quality support alongside their core products.

Analog Devices rises to meet these expectations with such support software as the Analog Filter Wizard and ADC modeling tools. Now Analog Devices is taking the next step with a comprehensive online product evaluation tool called Virtual Eval. Virtual Eval employs detailed software models to simulate crucial part performance characteristics without the purchase of hardware. The overworked engineer can configure a variety of operating conditions and device features to establish custom use cases. The configuration settings are dispatched to Analog Devices servers to kick off a simulation job. Within seconds, the completed simulation results display as graphs and performance metrics in the browser window.

Virtual Eval can solve a wide variety of design problems to accelerate the product development cycle. The remainder of this article covers two such problems out of many. In the first, a data acquisition scenario, you must balance throughput rate and noise performance to choose the right precision converter. In the second, while working on a radio receiver, you need to digitize some spectra with a minimum dynamic range requirement, while keeping overall system power low. In both cases, Virtual Eval facilitates faster design decisions with greater confidence through the use of online simulation.

Problem #1

Wading through the specification tome, the key requirements slowly start to emerge:

- 4-channel signal acquisition, ±75 mV
- 18-bit performance or higher
- 50 Hz rejection below –40 dB
- Settling time of 50 ms, but faster is better

Spoiler alert! The Analog Devices AD7193 is the right part for this job. The traditional method for making the correct part selection is by utilizing the specifications in the product's data sheet to analyze the component's performance under various filtering and application conditions. There is a lot of manual labor involved in this method and data sheets cannot provide performance specifications for every possible combination of frequency selection and use case conditions of interest to a wide variety of customers. What you really need is an interactive tool like Virtual Eval to understand product performance through custom simulations tailored to your particular use case.

The first screen you see is the product chooser.

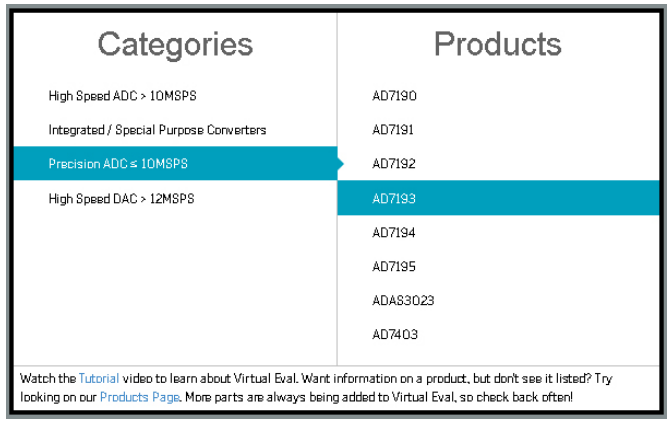


Figure 1. Product chooser.

Under **Precision ADC ≤ 10 MSPS**, find the AD7193. One click loads the evaluation session.

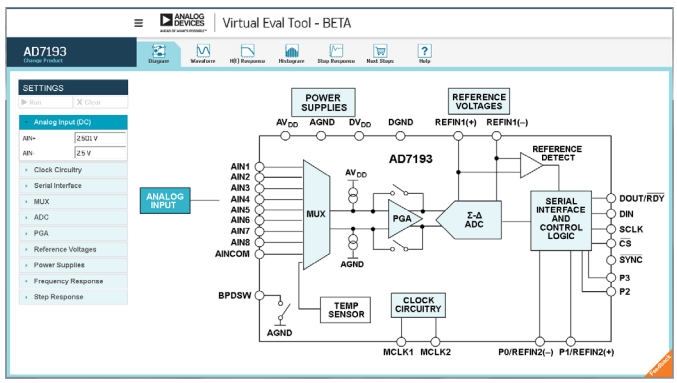


Figure 2. AD7193 functional block diagram.

The **Functional Block Diagram** view illustrates the layout of the AD7193. Clickable components of the diagram reveal the associated configurable settings in the accordion on the left-hand side of the screen. Select the reference voltages and observe a V_{REF} of 2.5 V. Then, select the PGA component, and change the PGA gain from 128 to 32, allowing for an analog input range of ±2.5 V/32 = ±78.125 mV. This satisfies the amplitude specification. Finally, click the **Run** button at the top of the **Settings** column. Remote servers run a collection of simulations, and deliver the performance results back to the Virtual Eval client.

To interpret the results, switch to the **Waveform** view using the tabs near the top of the screen.

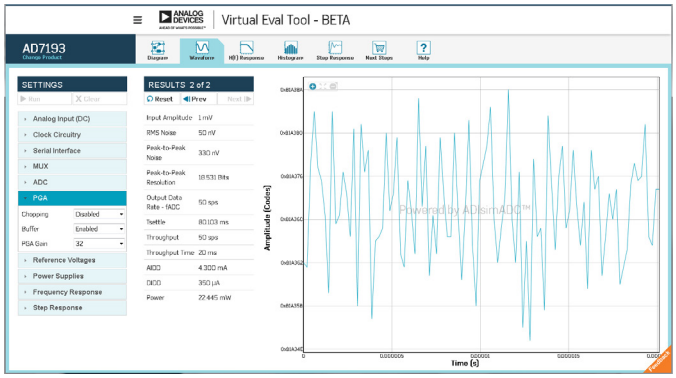


Figure 3. Waveform view.

The **Results** column contains dependent variables computed in the simulation, such as noise and power characteristics. The peak-to-peak resolution is 18.531 bits, which satisfies the specifications; however, the settling time of 80.103 ms does not.

In precision converters, this settling time is a function of the filter configuration. Switching to the **H(f) Response** view gives insight into the filtering performance of the product.

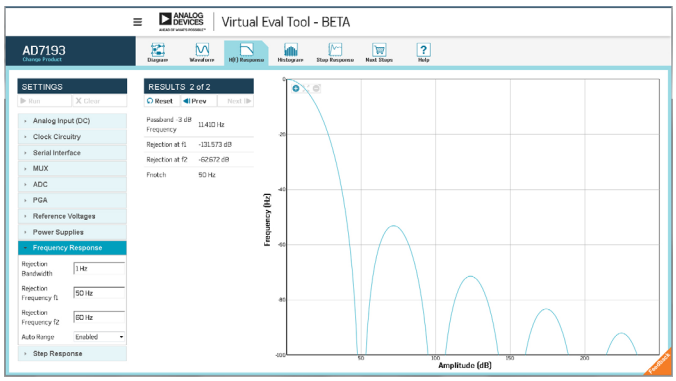


Figure 4. H(f) response view.

The specifications require –40 dB of rejection at 50 Hz, but the actual rejection power is –131 dB! That surplus of rejection can be sacrificed to improve settling time. To dial back the filtering, select the **ADC** element in the **Settings** column, and change FS from 96 to 48. To ensure there is still a zero in the filter response at 50 Hz, increase the **Averaging** from 1 to 2. Lastly, change the **Sinc Order** from 4 to 3 to save a little more settling time. Then run the simulation again.

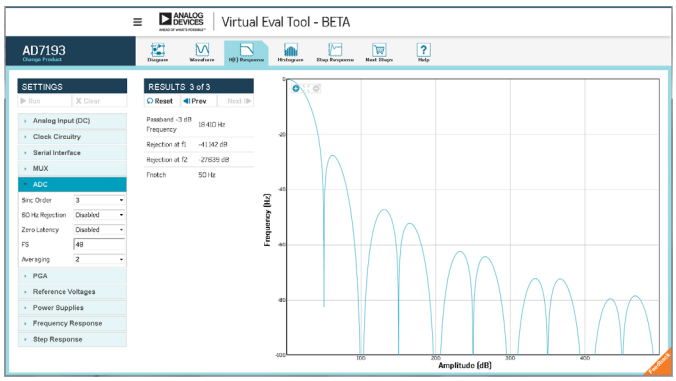


Figure 5. H(f) response modified.

The rejection at 50 Hz is now about –41 dB, which satisfies the specification. There is no way to determine this from the data sheet, since Analog Devices does not publish the formulas used to compute frequency rejection. Only an interactive simulation allows the engineer to directly verify product performance in particular scenarios such as this.

Switching back to the **Waveform** view reveals that the settling time is just 40.103 ms due to the reduction in filtering, easily meeting the specifications.

Problem #2

Your company's new platform must digitize approximately 50 MHz worth of spectrum located at 354 MHz with 72 dB of signal-to-noise ratio. Fast forward to a design choice to use an RF ADC, the AD9680. It has a sampling rate of 1 GSPS, an on-chip digital downconverter, and a flexible JESD204B serial interface. Its data sheet is very detailed and thorough, but as mentioned previously, it just cannot possibly address every potential use case. Virtual Eval can, so you open it from the AD9680 product page.

Select the **High Speed ADC** category and click on the AD9680.

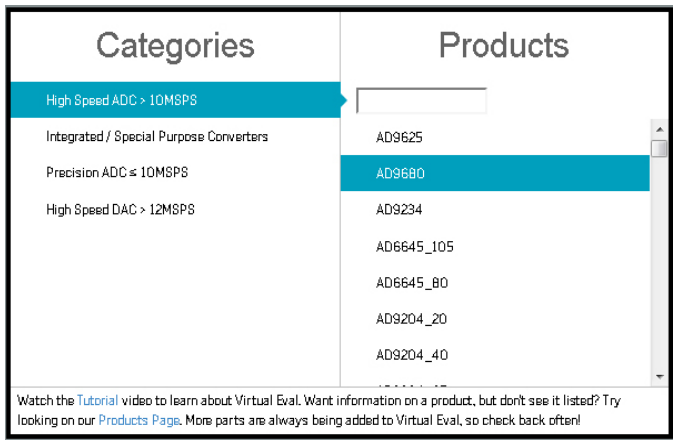


Figure 6. Product chooser.

You are presented with the default Virtual Eval session starting with the **Functional Block Diagram** view.

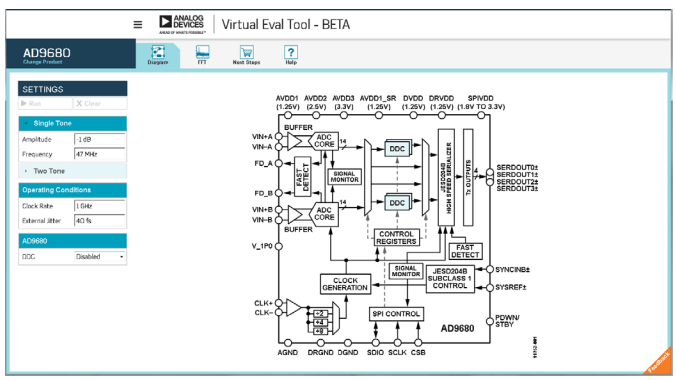


Figure 7. AD9680 functional block diagram.

Visible are DDCs and JESD204B, both a good sign based on the requirements. Set the **Single Tone Input Frequency** to 354 MHz to represent the use case and press **Run**.

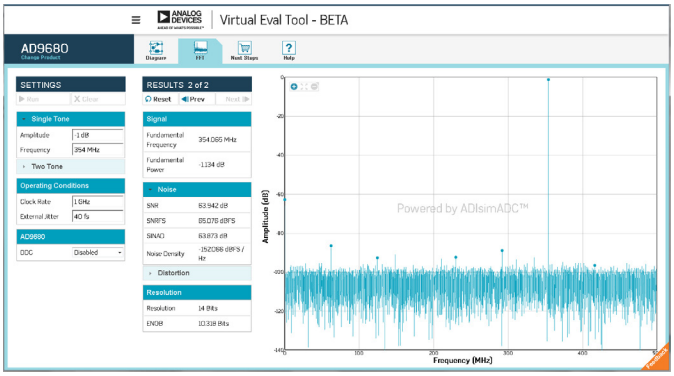


Figure 8. Spectrum analysis with 354 MHz input tone, DDC disabled.

Virtual Eval performs a simulation and a full spectral analysis. The figure of merit in this case is the SNR. 63.9 dB is certainly insufficient, but that can be remedied. Switch the DDC from **Disabled** to **Enabled**. This presents several new options for digital signal processing to improve performance.

Set the NCO Frequency to 354 MHz so that the spectrum is centered appropriately. Additionally, switch the C2R (complex-to-real) to **Enabled**. Switching to real values halves the amount of data transmitted, reducing I/O power between the ADC and FPGA. Press **Run** again to see the new simulation results.

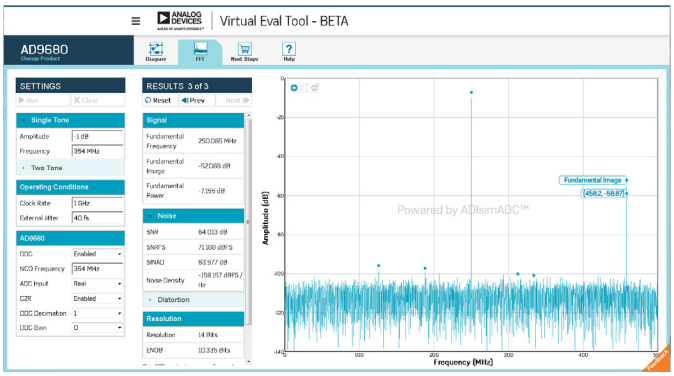


Figure 9. Spectrum analysis with 354 MHz input tone, DDC enabled.

The input tone is centered as expected. However, there is a large Fundamental Image near the right side of the graph. Fortunately, the specification requires just 50 MHz of bandwidth, much less than the 500 MHz currently digitized. The solution here is to reduce the spectrum under consideration, simultaneously improving SNR and filtering out the image. In the **Settings** column, change the DDC decimation from 1 to 8, and **Run** again. This reduces the spectrum to 500 MHz/8 = 62.5 MHz.

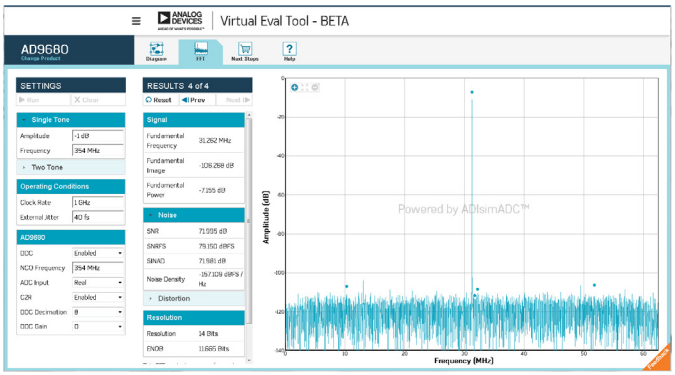


Figure 10. Spectrum analysis with 354 MHz input tone, DDC with decimation enabled.

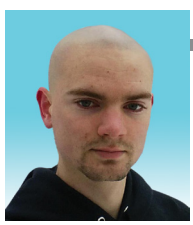
The fundamental image is digitally filtered out, and the SNR is better than 72 dB. Since the converter is only digitizing 62.5 MHz of spectrum, the data link between the ADC and FPGA is nearly optimal.

Conclusion

Virtual Eval provides a fast, convenient, low risk way to virtually interact with products through online simulation. It illustrates complex product features, and allows engineers to discern whether a product can satisfy their requirements under custom operating conditions. No other form of product evaluation experience enables the same level of detail and interactivity through the convenience of the Web browser.

This walkthrough demonstrates only a small slice of the features available on Virtual Eval. More features and more products are often added to the Beta site. Please take this opportunity to be a part of the on-going development process by trying Virtual Eval yourself. We welcome any and all feedback via the **Feedback** tab in the lower right. As Virtual Eval continues to develop and grow, we hope to bring online simulation to the center stage of the product evaluation and design process.

Jason Cockrell



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Powering GSPS or RF Sampling ADCs: Switcher vs. LDO

By Umesh Jayamohan

Introduction

The analog-to-digital converter (ADC) is an integral component in any system that depends on gathering information from the outside (analog) world for (digital) processing. These systems vary in applications from communications receivers to electronic test and measurement, to military and aerospace, to name a few. Advancements in silicon processing technology (such as 65 nm CMOS and 28 nm CMOS) have enabled the high speed ADC to cross the GSPS (gigasample per second) barrier. What this provides the systems designer with is the ability to sample wider and wider bandwidths for digital processing. Systems designers are constantly trying to reduce overall power for environmental and cost reasons. Traditionally, low noise LDO (low dropout) regulators have been recommended by ADC manufacturers for powering GSPS (or RF sampling) ADCs in order to extract maximum performance. However, this is not an efficient power delivery network (PDN) implementation. Systems designers are increasingly demanding to use switching power regulators to power the GSPS ADC directly without a significant drop in ADC performance.

The solution lies in careful PDN implementation and layout to ensure that the ADC performance is not compromised. This article discusses the difference between linear and switching supplies and demonstrates that combining a GSPS ADC with a dc-to-dc converter can significantly improve system power efficiency without any penalty in ADC performance. This article discusses the performance of the GSPS ADC using a combination of power delivery networks and makes comparative analyses on cost and performance.

Traditionally Recommended PDN for GSPS ADCs

A high bandwidth, high sample rate ADC (or GSPS ADC) can have multiple power domains (such as AVDD or DVDD). With the shrinking geometries, not only have the power domains increased in number, but the number of different voltages required to power the ADC have increased as well. For example, the AD9250,[1] a 14-bit,170 MSPS/250 MSPS, JESD204B, dual analog-to-digital converter, is built using the 180 nm CMOS process and has three domains: AVDD, DVDD, and DRVDD. However, all three domains are the same voltage: 1.8 V.

Now consider the AD9680,[2] a 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS JESD204B, dual analog-to-digital converter, which is built on a 65 nm CMOS process. This GSPS ADC has seven different domains (AVDD1, AVDD1_SR, AVDD2, AVDD3, DVDD, DRVDD, and SPIVDD) and three different voltages: 1.25 V, 2.5 V, and 3.3 V.

The proliferation of these supply domains and the various voltages is somewhat of a necessity for operation at these sample rates. They are required to ensure proper isolation between the various circuit domains (such as sampling, clock, digital, and serializer) while providing optimal performance. It is for this very reason that the ADC manufacturers design the evaluation

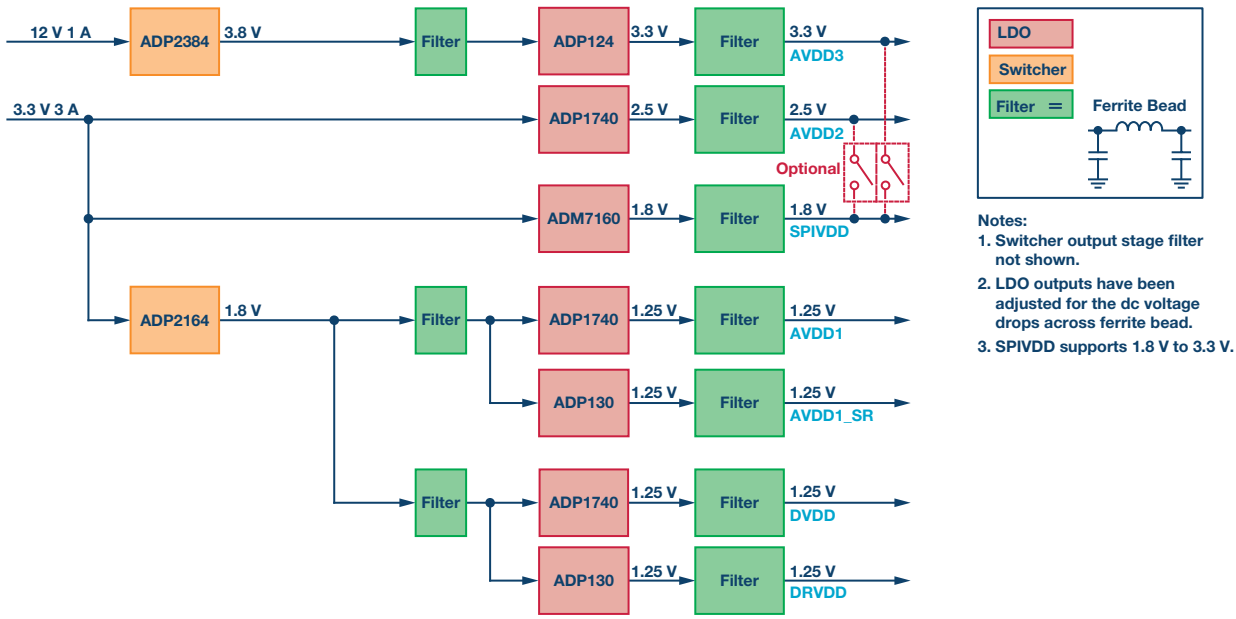

Figure 1. Default PDN for the AD9680 evaluation board.

boards and recommend an elaborate power supply design to ensure minimal risk and maximum performance. For example, Figure 1 shows the block diagram representation of the default PDN used in the AD9680 evaluation board. The power input is derived from the 12 V/1 A and 3.3 V/3 A supplies offered by the FMC (FPGA mezzanine card) connector using the Vita57.1 specification. The ADP2384[3] and ADP2164[4] dc-to-dc converters were used to step down the voltages to a manageable level so the LDOs can regulate without having to go into thermal shutdown.

It does not take much to realize that this is an expensive implementation, with seven LDO regulators—one for each domain. This PDN may be the most optimal in terms of performance, but it certainly is not the most cost effective or efficient in terms of cost of operation. Systems designers find it challenging to implement a system with multiple ADCs. For example, a phased array radar implementation will contain hundreds of AD9680s all working synchronously. It is unreasonable to ask the systems designer to have one LDO regulator per voltage domain across hundreds of ADCs.

A Simpler PDN for GSPS ADCs

A more cost-effective approach to the PDN design would be to combine the domains that have the same voltage value (such as all having 1.25 V analog domains) and drive them from the same LDO. This reduces the component count (and bill of material—BOM—cost) and may be suitable for some designs. The simplified PDN is shown in Figure 2 as implemented on the AD9680 evaluation board. In this implementation, the entire AD9680 can be powered using a single 3.3 V input.

A DC-to-DC Converter Driving the AD9680

A further simplification to the PDN can be implemented by removing the LDO that supplies the 1.25 V domains altogether. This would be the most efficient and cost-effective solution. The challenge here is to ensure stable operation to the dc-to-dc converter so as to not affect the ADC's performance. The PDN where the ADP2164 drives all the 1.25 V domains (AVDD1, AVDD1_SR, DVDD, and DRVDD) of the AD9680 is shown in Figure 3.

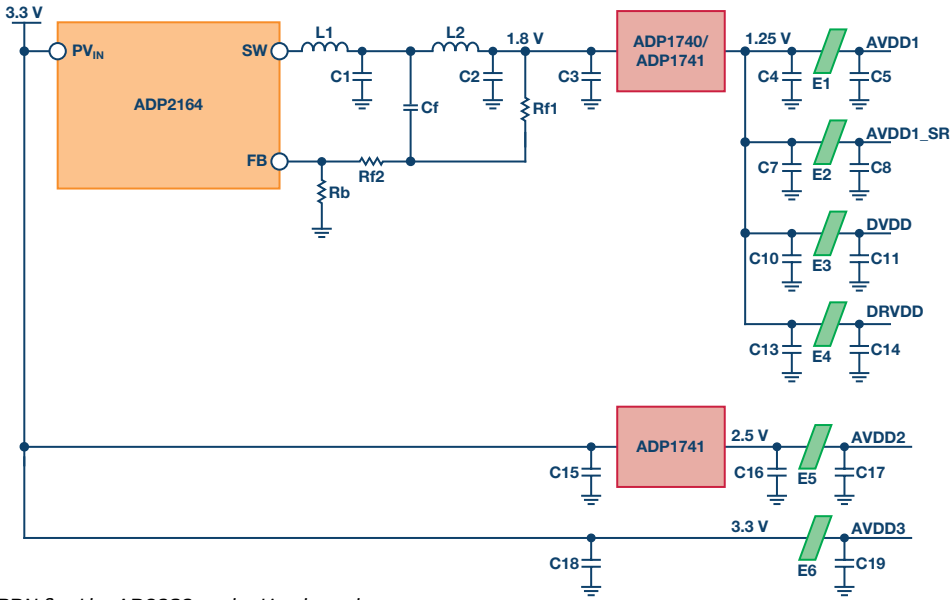

Figure 2: Simplified PDN for the AD9680 evaluation board.

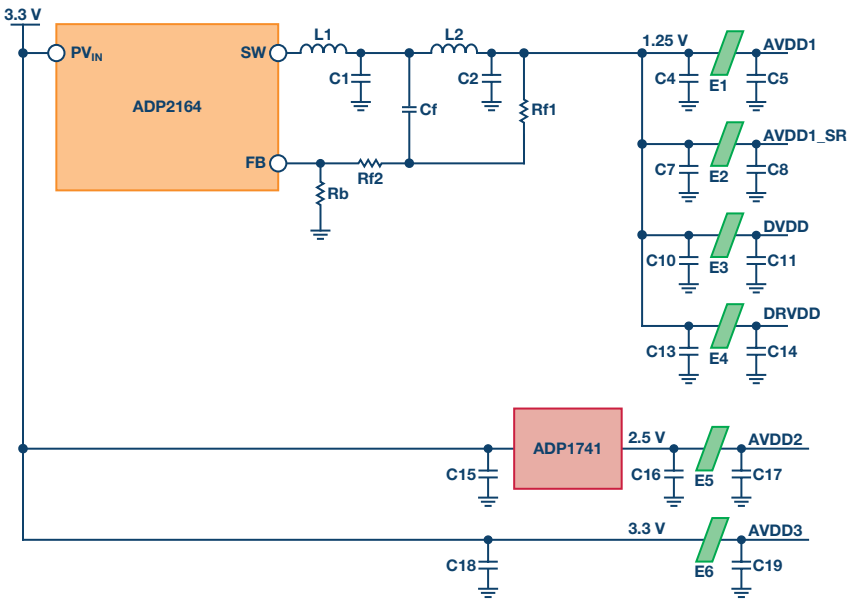

Figure 3: Using a dc-to-dc converter to power the AD9680.

Comparing the Various PDNs

The three PDNs discussed above were put to test along with a fourth network where the AD9680 evaluation board was powered from the bench supplies. Table 1 lists the various power delivery networks implemented on the AD9680 evaluation board.

Table 1. List of Power Delivery Networks

PDN Setup	Description
Bench	AD9680 run using bench supply
PDN #1	Default PDN on evaluation board (shown in Figure 1)
PDN #2	All 1.25 V domains driven from one LDO (shown in Figure 2)
PDN #3	All 1.25 V domains driven from a dc-to-dc converter (shown in Figure 3)

Since SPIVDD could support 1.8 V to 3.3 V and was considered a noncritical node, it was powered using a 1.8 V LDO output. In a regular system implementation, the SPIVDD can be connected to the 2.5 V or 3.3 V domain. That said, the SPIVDD connection should still be monitored in systems where the SPI bus is shared between many ADCs and DACs. If this is the case, care must be taken to ensure that the normal SPI operation does not cause supply transients on the SPIVDD domain. Their supply transients might trigger a power-on reset (POR) situation if the SPIVDD goes lower than the threshold level.

Table 2. SNR Performance Comparison (dBFS)

Frequency (MHz)	Bench	Default (PDN #1)	Simplified (PDN #2)	Switcher (PDN #3)
63	66.5	66.5	66.6	66.7
170	66.4	66.1	65.9	66.2
340	64.8	64.5	64.5	64.7
450	64.0	63.7	63.6	63.8
765	62.5	62.2	62.2	62.3
985	61.3	61.0	61.0	61.1
1283	59.8	59.5	59.5	59.5
1725	57.7	57.4	57.4	57.5
1983	56.7	56.4	56.5	56.6

Table 3. SFDR Performance Comparison (dBFS)

Frequency (MHz)	Bench	Default (PDN #1)	Simplified (PDN #2)	Switcher (PDN #3)
63	83	82	88	83
170	86	85	85	84
340	77	76	76	76
450	72	72	71	71
765	77	76	76	82
985	77	76	76	83
1283	74	74	74	75
1725	67	67	68	67
1983	60	60	60	60

Table 2 and Table 3 show the SNR and SFDR performance, respectively, of the AD9680 when using the various PDNs. The recommendations for front-end network and register settings for various Nyquist zones were followed as per the AD9680 data sheet.[2]

The PDN using just the dc-to-dc converter to power the AD9680's 1.25 V domains (PDN #3) shows good performance over the input frequencies. This proves that it is possible to combine domains and power them efficiently and cost effectively without paying a huge penalty in ADC performance. The PDN supplied from the bench provides the best noise performance as it is the lowest noise power source. However, it is worth noting that PDN #3 consistently shows better SNR performance than the default network (PDN #1). This could be attributed to the fact that LDOs are good for low frequency cleanup but do not do much above a few 100 kHz even when they are in the circuit. This could explain the 0.2 dB advantage in SNR when using the PDN #3.

FFT Plots

Figure 4 and Figure 5 show the single-tone FFTs at 170 MHz and 785 MHz input, respectively. The FFT shows no spectral degradation due to the fact that the 1.25 V domains have been powered from a single dc-to-dc converter.

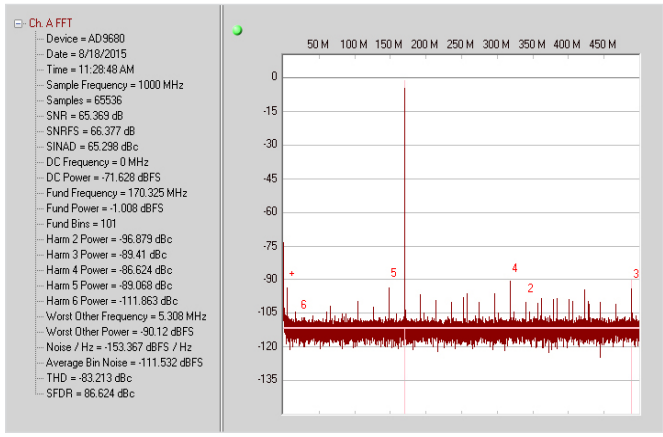

Figure 4. Single-tone FFT at 170 MHz input, with PDN #3.

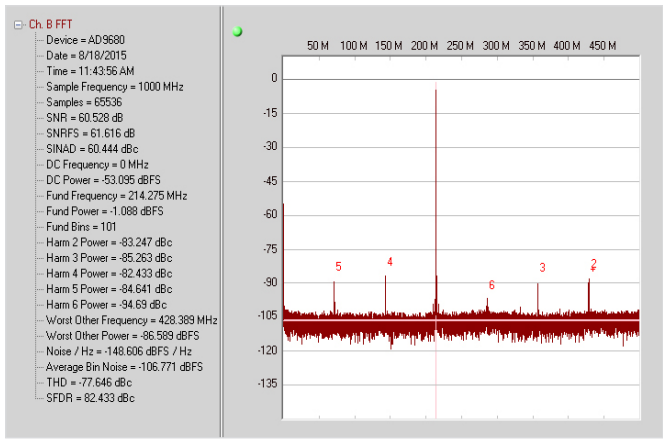

Figure 5. Single-tone FFT at 785 MHz input, with PDN #3.

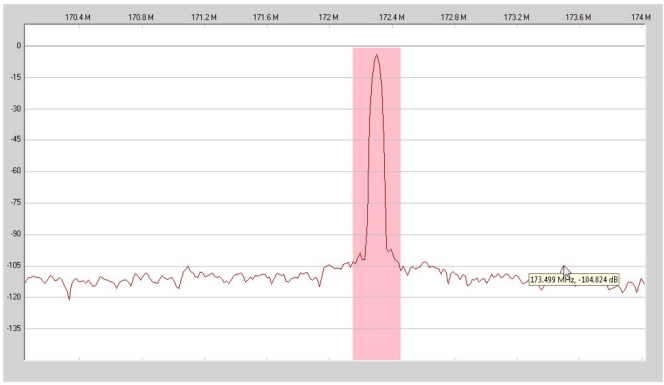

Figure 6. 1.2 MHz sideband switching spur at 170 MHz input. Spur level = –105 dBFS.

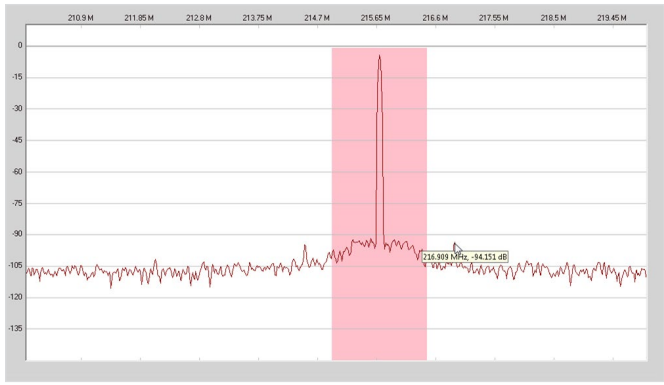

Figure 7. 1.2 MHz sideband switching spur at 785 MHz input. Spur level = –94 dBFS.

Switching Spurs

In addition to the noise performance, the dc-to-dc converter implementation should also be checked for spurious content due to the switching elements and the magnetics involved. This is where careful layout techniques to reduce ground loops and ground bounce will be beneficial. There are many resources that can help with measurement of the switching supply noise.[5,6] The sideband spurs appear on either side of the fundamental offset by the switching frequency (in this example, 1.2 MHz). It must be noted that the output filter stage shown in Figure 2 or Figure 3 is a two-stage filter. This two-stage filter is a main contributor in reducing the switching noise (ripple) that helps improve the ADC noise (SNR) performance. In the same token, the two-stage filter also helps in reducing the switching spurs that manifest itself in the output FFT. These are shown in Figure 6 and Figure 7 for 170 MHz and 785 MHz, respectively.

The level of the sideband spur can be estimated by understanding the PSRR (power supply rejection ratio) or the ADC's power supply domain.[7]

Simulating DC-to-DC Converter Switching Circuits

The two-stage filter at the output of the dc-to-dc converter can be simulated using a tool such as ADIsimPE.[8] Figure 8 shows the ADIsimPE schematic generated to simulate the output noise and stability characteristics of the PDN. ADIsimPE is a convenient and powerful tool that helps the systems engineer design, optimize, and analyze power supply networks.

Figure 9 shows the output ripple at the output of the first stage and the filtered output after the second stage of the circuit, simulated in ADIsimPE. The ripple, as shown here, is around 3 mV p-p.

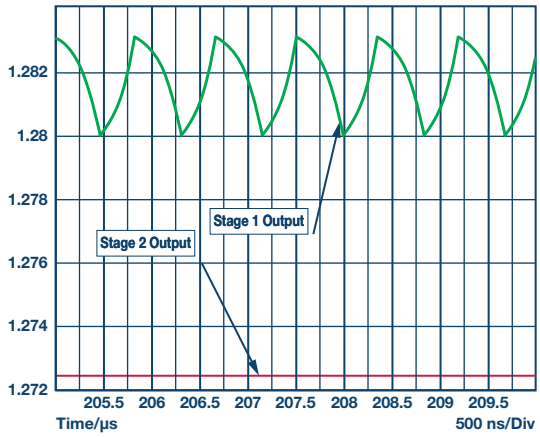

Figure 9. Stage 1 and Stage 2 outputs of the ADIsimPE simulation.

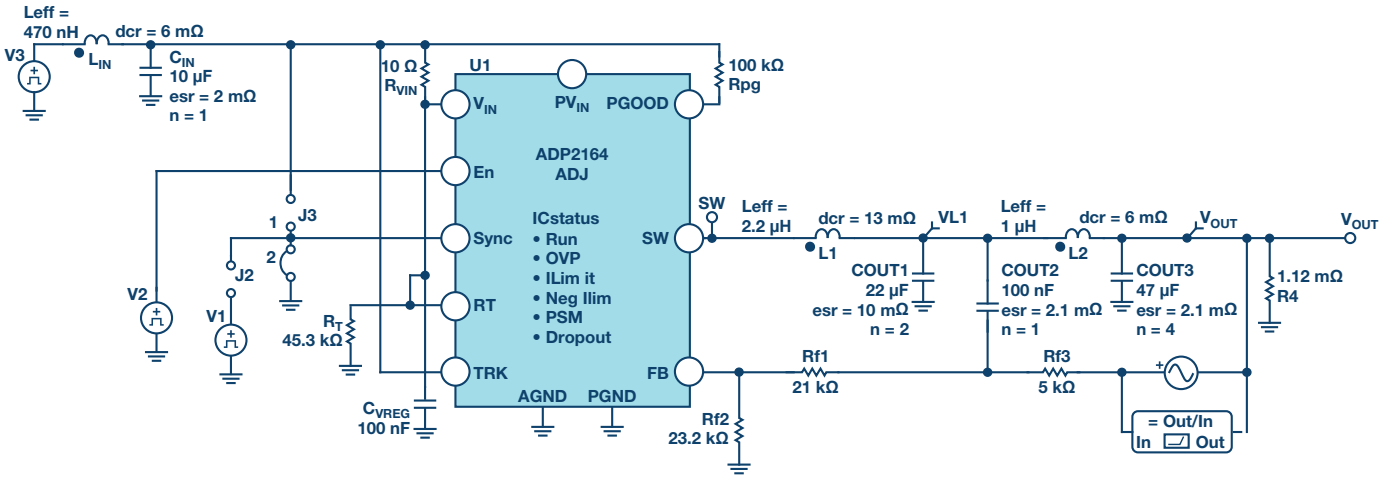

Figure 8. ADIsimPE schematic of ADP2164 driving the 1.25 V domains.

Table 4. Bill of Material of PDN Shown in Figure 2

REFDES	Qty	Description	MFG	Part Number	Value
C1	1	22 µF, 6.3 V, X5R 0805 capacitor	Murata	GRM21BR60J226ME39L	22 µF
C2	4	22 µF, 6.3 V, X5R 0805 capacitor	Murata	GRM21BR60J226ME39L	22 µF
Cf	1	0.1 µF, 10 V, X5R 0402 capacitor	Murata	GRM155R61A104KA01D	0.1 µF
C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	17	4.7 µF, 6.3 V, X5R 0402 capacitor	Murata	GRM155R60J475ME47D	4.7 µF
E1, E2, E3, E4, E5, E6	6	Ferrite chip 10 Ω 0402	Murata	BLM15AX100SN1D	10 Ω
L1	1	1.0 µH shielded power inductor, 10 mΩ	Coilcraft	XAL5030-102ME	1.0 µH
L2	1	2.2 µH shielded power inductor, 0.1 Ω	Coilcraft	ME3220-222ML	2.2 µH
Rf1	1	4.99 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF4991X	4.99 kΩ
Rf2	1	41.2 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF4122X	41.2 kΩ
Rb	1	23.2 kΩ, 1% 1, W/10 W 0402 resistor	Panasonic	ERJ-2RKF2322X	23.2 kΩ
ADP2164	1	IC, REG, buck ADJ, 4 A, sync, 16-lead LFCSP	Analog Devices	ADP2164ACPZ-R7	
ADP1741	3	IC, REG, LDO, ADJ, 2 A, 16-lead LFCSP	Analog Devices	ADP1741ACPZ-R7	
ADP171	2	IC, REG, LDO, ADJ, 0.3 A, 5-lead TSOT-23	Analog Devices	ADP171AUJZ-R7	

Bill of Material

Table 4 shows the bill of material used for the simplified PDN of the AD9680 evaluation board, which is shown in Figure 2. By using the network shown in Figure 3, a systems designer can realize savings of up to 40% to 45% in BOM cost. The BOM cost is estimated by calculating the 1k unit prices of the components on a popular electronic component vendor website.

Component Selection and Layout

The performance of the ADC when running on the various PDNs depends on not only careful design, but also the selection of components and their layout on the PCB. The high currents produced in a switching power supply often lead to strong magnetic fields that can couple into other magnetic components on the board, including inductors found in matching networks and transformers used to couple analog and clock signals. Careful board layout techniques must be utilized to prevent these fields from coupling into critical signals.

Inductor Selection

Since the inductor and the capacitor that form the output filter stage perform the bulk of the power delivery, they need to be selected carefully. In this example, a mix of shielded and unshielded inductors were used. The first filter stage used a shielded inductor. The second stage could do with an unshielded inductor in this case. However, it is recommended to use shielded inductors in both stages to minimize possible EMI emissions. The inductors also were chosen to have enough headroom in terms of saturation current (ISAT) and dc resistance (DCR) to make sure they didn't go into saturation or cause too much voltage drop across themselves.

Capacitor Selection

X5R or X7R capacitors are recommended for use as output filter capacitors. The capacitors also have to have low ESR (equivalent series resistance). The low ESR helps in reducing switching ripple at the output. Another trick that is employed to minimize the total ESR and ESI (equivalent series inductance) is to combine capacitors in parallel. As shown in Figure 3 and Table 4, the first filter stage uses 2× 22 µF capacitors, whereas the second filter stage uses 4× 22 µF capacitors. The voltage rating of the capacitors is also an important factor in its selection. This is because the dielectric of the ceramic capacitor degrades as the dc bias increases. This means that a 6.3 V rated 22 µF capacitor could degrade by up to 50% at a 4 V dc bias.[9,10] In this example, the 6.3 V rated capacitor is used for the 1.25 V supplies. Adding more capacitors at the output does increase the BOM cost and board space slightly but this is a good insurance against switching noise and ripple that could interfere with ADC performance.

Ferrite Bead Selection

As shown in Figure 3, ferrite beads are used to isolate the various domains. The selection of the ferrite bead is also critical, as a higher than desired DCR (dc resistance) of the ferrite bead will cause lower than optimal voltage at the domains. This low voltage results in less than optimal ADC performance (SNR and SFDR). Sufficient attention must be paid to the impedance characteristics, maximum dc carrying capability, and the DCR of the ferrite bead.[11]

PCB Layout Considerations

In order to minimize the interactions between the switching regulator and the ADC, the dc-to-dc converter and its switching elements should be placed far away from any magnetics that interact with the ADC (such as the front-end matching network or clock network). Within the dc-to-dc converter layout, the two stage filter should be placed as close to the dc-to-dc converter as possible so as to minimize loop currents.

Acknowledgement

The author would like to acknowledge Justin Correll for help with the measurement and data collection.

Conclusion

RF sampling (or GSPS) ADCs offer a unique advantage in systems design by allowing the digitization of wide swaths of bandwidth. The industry is keen on reducing the complexity, size, and cost of power supply designs for these GSPS ADCs. It is possible to have a low noise and cost-effective PDN that can power a GSPS ADC by paying adequate attention to the design, component selection, and PCN layout. Thus implemented, switching regulators also help improve power system efficiency and provide operational cost and BOM savings, without any penalty in performance.

References

[1] AD9250. Analog Devices, Inc.

[2] AD9680. Analog Devices, Inc.

[3] ADP2384. Analog Devices, Inc.

[4] ADP2164. Analog Devices, Inc.

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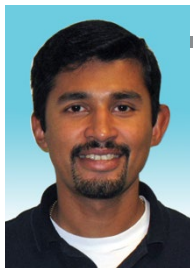


Umesh Jayamohan

Also by this Author:

RF Sampling ADC Input Protection: Not Black Magic After All

Volume 49, Number 4

Ferrite Beads Demystified

By Jefferson Eco and Aldrick Limjoco

Introduction

An effective method for filtering high frequency power supply noise and cleanly sharing similar voltage supply rails (that is, analog and digital rails for mixed-signal ICs) while preserving high frequency isolation between the shared rails is the use of ferrite beads. A ferrite bead is a passive device that filters high frequency noise energy over a broad frequency range. It becomes resistive over its intended frequency range and dissipates the noise energy in the form of heat. The ferrite bead is connected in series with the power supply rail and is often combined with capacitors to ground on either side of the bead. This forms a low-pass filter network, further reducing the high frequency power supply noise.

However, improper use of ferrite beads in system design can lead to some detrimental issues. Some examples are unwanted resonance due to combining the bead with a decoupling capacitor for low-pass filtering and the effect of dc bias current dependency that degrades the EMI suppression capability of the bead. With proper understanding and consideration of the ferrite bead's behavior, these issues can be avoided.

This article discusses the important considerations that system designers need to be aware of when using ferrite beads in power supply systems such as impedance vs. frequency characteristics with varying dc bias current and unwanted LC resonance effects. Ultimately, to address the issue on the unwanted resonance, damping techniques will be introduced and a comparison of the effectiveness of each damping method will be presented.

The device used to demonstrate the effects of ferrite beads as an output filter is a 2 A/1.2 A dc-to-dc switching regulator with independent positive and negative outputs (ADP5071). The ferrite beads used in the article are mainly chip type surface-mount packages.

Ferrite Bead Simplified Model and Simulation

A ferrite bead can be modeled as a simplified circuit consisting of resistors, an inductor, and a capacitor, as shown in Figure 1a. R_{DC} corresponds to the dc resistance of the bead. C_{PAR}, L_{BEAD}, and R_{AC} are (respectively) the parasitic capacitance, the bead inductance, and the ac resistance (ac core losses) associated with the bead.

Ferrite beads are categorized by three response regions: inductive, resistive, and capacitive. These regions can be determined by looking at a ZRX plot (shown in Figure 1b), where Z is the impedance, R is the resistance, and X is the reactance of the bead. To reduce high frequency noise, the bead must be in the resistive region; this is especially desirable for electromagnetic interference (EMI) filtering applications. The component acts like a resistor, which impedes the high frequency noise and dissipates it as heat. The resistive region occurs after the bead crossover frequency (X = R) and up to the point where the bead becomes capacitive. This capacitive point occurs at the frequency where the absolute value of capacitive reactance (–X) is equivalent to R.

In some cases, the simplified circuit model can be used to approximate the ferrite bead impedance characteristic up to the sub-GHz range.

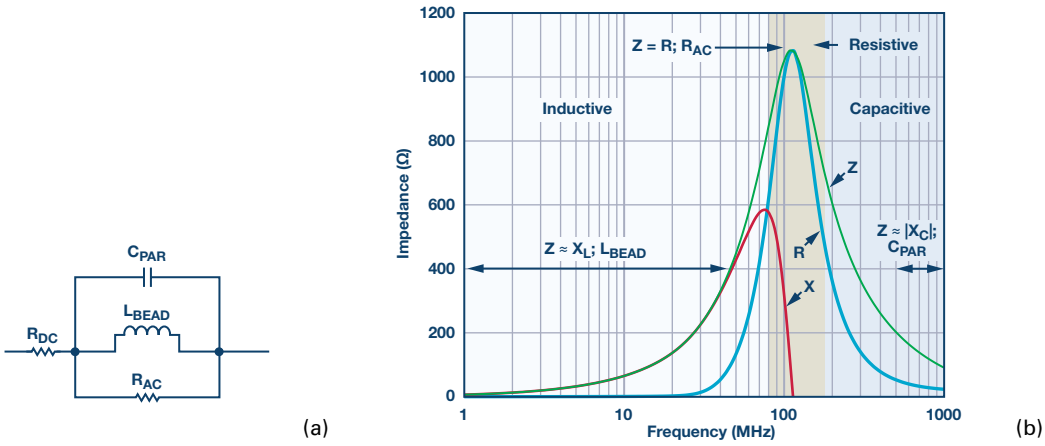


Figure 1. (a) Simplified circuit model and (b) Tyco Electronics BMB2A1000LN2 measured ZRX plot.

The Tyco Electronics BMB2A1000LN2 multilayer ferrite bead is used as an example. Figure 1b shows the measured ZRX response of the BMB2A1000LN2 for a zero dc bias current using an impedance analyzer.

For the region on the measured ZRX plot where the bead appears most inductive ($Z \approx XL$; L_{BEAD}), the bead inductance is calculated by the following equation:

$$L_{BEAD} = \frac{X_L}{2 \times \pi \times f} \quad (1)$$

where:

f is the frequency point anywhere in the region the bead appears inductive. In this example, f = 30.7 MHz. X_L is the reactance at 30.7 MHz, which is 233 Ω.

Equation 1 yields an inductance value (L_{BEAD}) of 1.208 µH.

For the region where the bead appears most capacitive ($Z \approx |X_C|$; C_{PAR}), the parasitic capacitance is calculated by the following equation:

$$C_{PAR} = \frac{1}{2 \times \pi \times f \times |X_C|} \quad (2)$$

where:

f is the frequency point anywhere in the region the bead appears capacitive. In this example, f = 803 MHz $|X_C|$ is the reactance at 803 MHz, which is 118.1 Ω.

Equation 2 yields a parasitic capacitance value (C_{PAR}) of 1.678 pF.

The dc resistance (R_{DC}), which is 300 mΩ, is acquired from the manufacturer's data sheet. The ac resistance (R_{AC}) is the peak impedance where the bead appears to be purely resistive. Calculate R_{AC} by subtracting R_{DC} from Z. Because R_{DC} is very small compared to the peak impedance, it can be neglected. Therefore, in this case R_{AC} is 1.082 kΩ. The ADIsimPE circuit simulator tool powered by SIMetrix/SIMPLIS was used to generate the impedance vs. the frequency response. Figure 2a shows the circuit simulation model with the calculated values and Figure 2b shows both the actual measurement and simulated result. In this example, the impedance curve from the circuit simulation model closely matches the measured one.

The ferrite bead model can be useful in noise filtering circuit design and analysis. For example, approximating the inductance of the bead can be helpful in determining the resonant frequency cutoff when combined with a decoupling capacitor in a low-pass filter network. However, the circuit model specified in this article is an approximation with a zero dc bias current. This model may change with respect to dc bias current and, in other cases, a more complex model is required.

DC Bias Current Considerations

Selecting the right ferrite bead for power applications requires careful consideration not only of the filter bandwidth, but also of the impedance characteristics of the bead with respect to dc bias current. In most cases, manufacturers only specify the impedance of the bead at 100 MHz and publish data sheets with frequency response curves at zero dc bias current. However, when using ferrite beads for power supply filtering, the load current going through the ferrite bead is never zero, and as dc bias current increases from zero, all of these parameters change significantly.

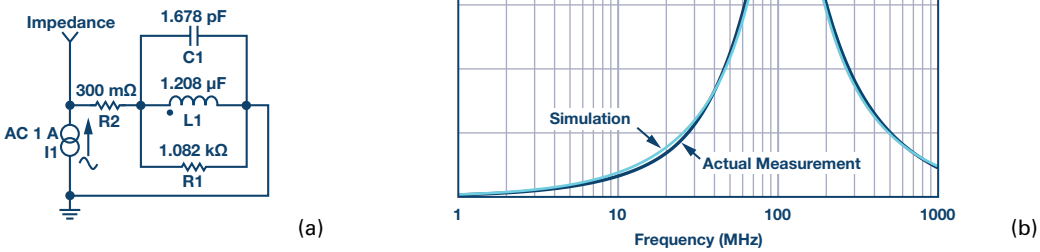
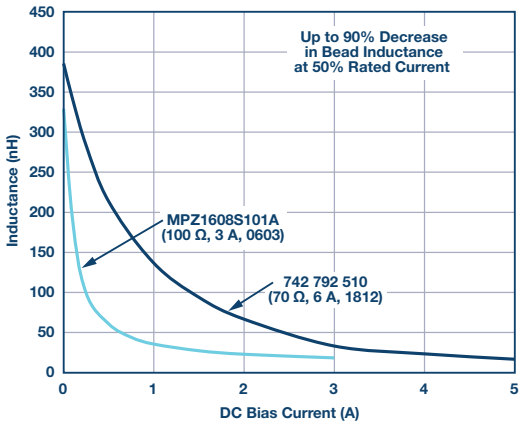


Figure 2. (a) Circuit simulation model and (b) Actual measurement vs. simulation.

As the dc bias current increases, the core material begins to saturate, which significantly reduces the inductance of the ferrite bead. The degree of inductance saturation differs depending on the material used for the core of the component. Figure 3a shows the typical dc bias dependency of the inductance for two ferrite beads. With 50% of the rated currents, the inductance decreases by up to 90%.



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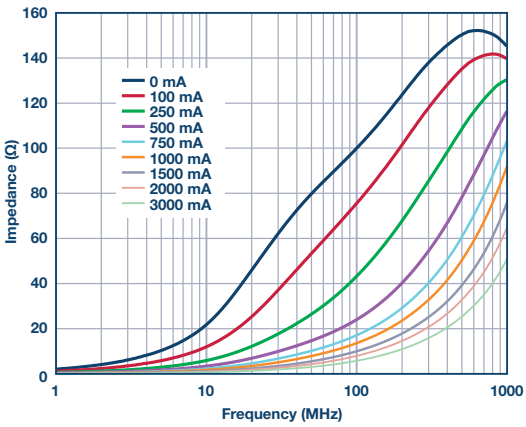

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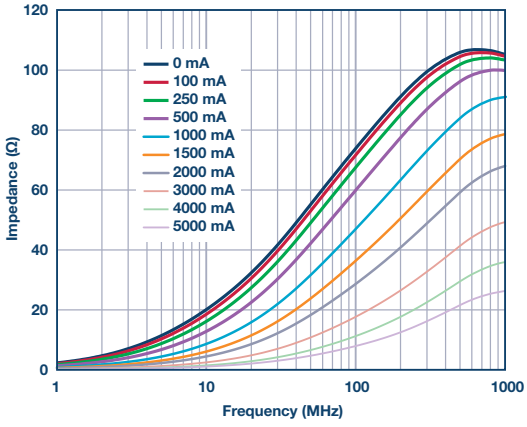


(c)

Figure 3. (a) The effect of dc bias current on bead inductance and impedance curves with respect to dc bias current for: (b) a TDK MPZ1608S101A bead, and (c) a Würth Elektronik 742 792 510 bead.

For effective power supply noise filtering, a design guideline is to use ferrite beads at about 20% of their rated dc current. As shown in these two examples, the inductance at 20% of the rated current drops to about 30% for the 6 A bead and to about 15% for the 3 A bead. The current rating of ferrite beads is an indication of the maximum current the device can take for a specified temperature rise and it is not a real operating point for filtering purposes.

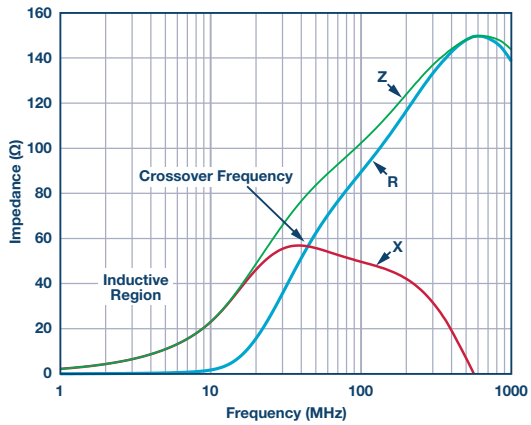
In addition, the effect of dc bias current can be observed in the reduction of impedance values over frequency, which in turn reduces the effectiveness of the ferrite bead and its ability to remove EMI. Figure 3b and Figure 3c show how the impedance of the ferrite bead varies with dc bias current. By applying just 50% of the rated current, the effective impedance at 100 MHz dramatically drops from 100 Ω to 10 Ω for the TDK MPZ1608S101A (100 Ω, 3 A, 0603) and from 70 Ω to 15 Ω for the Würth Elektronik 742 792 510 (70 Ω, 6 A, 1812).

System designers must be fully aware of the effect of dc bias current on bead inductance and effective impedance, as this can be critical in applications that demand high supply current.

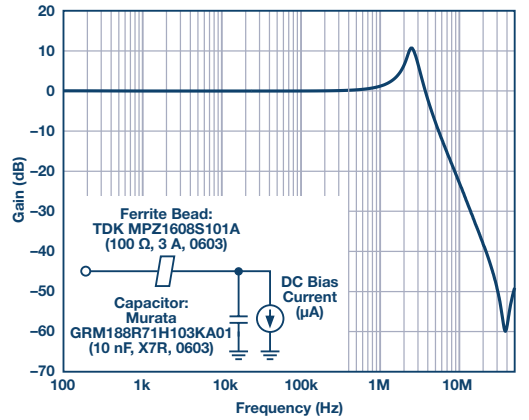
LC Resonance Effect

Resonance peaking is possible when implementing a ferrite bead together with a decoupling capacitor. This commonly overlooked effect can be detrimental because it may amplify ripple and noise in a given system instead of attenuating it. In many cases, this peaking occurs around the popular switching frequencies of dc-to-dc converters.

Peaking occurs when the resonant frequency of a low-pass filter network, formed by the ferrite bead inductance and the high Q decoupling capacitance, is below the crossover frequency of the bead. The resulting filter is underdamped. Figure 4a shows the measured impedance vs. frequency plot of the TDK MPZ1608S101A. The resistive component, which is depended upon to dissipate unwanted energy, does not become significant until reaching about the 20 MHz to 30 MHz range. Below this frequency, the ferrite bead still has a very high Q and acts like an ideal inductor. LC resonant frequencies for typical bead filters are generally in the 0.1 MHz to 10 MHz range. For typical switching frequencies in the 300 kHz to 5 MHz range, additional damping is required to reduce the filter Q.



(a)



(b)

Figure 4. (a) A TDK MPZ1608S101A ZRX plot and (b) a S21 response for a ferrite bead and capacitor low-pass filter.

As an example of this effect, Figure 4b shows the S21 frequency response of the bead and capacitor low-pass filter, which displays a peaking effect. The ferrite bead used is a TDK MPZ1608S101A (100 Ω, 3 A, 0603) and the decoupling capacitor used is a Murata GRM188R71H103KA01 low ESR ceramic capacitor (10 nF, X7R, 0603). Load current is in the microampere range.

An undamped ferrite bead filter can exhibit peaks from approximately 10 dB to approximately 15 dB depending on the Q of the filter circuit. In Figure 4b, peaking occurs at around 2.5 MHz with as much as 10 dB gain.

In addition, signal gain can be seen from 1 MHz to 3.5 MHz. This peaking is problematic if it occurs in the frequency band in which the switching regulator operates. This amplifies the unwanted switching artifacts, which can wreak havoc on the performance of sensitive loads such as the phase-locked loop (PLL), voltage-controlled oscillators (VCOs), and high resolution analog-to-digital converters (ADCs). The result shown in Figure 4b has been taken with a very light load (in the microampere range), but this is a realistic application in sections of circuits that need just a few microamperes to 1 mA of load current or sections that are turned off to save power in some operating modes. This potential peaking creates additional noise in the system that can create unwanted crosstalk.

As an example, Figure 5 shows an ADP5071 application circuit with an implemented bead filter and Figure 6 shows the spectral plot at the positive output. The switching frequency is set at 2.4 MHz, the input voltage is 9 V, the output voltage is set at 16 V, and the load current of 5 mA.

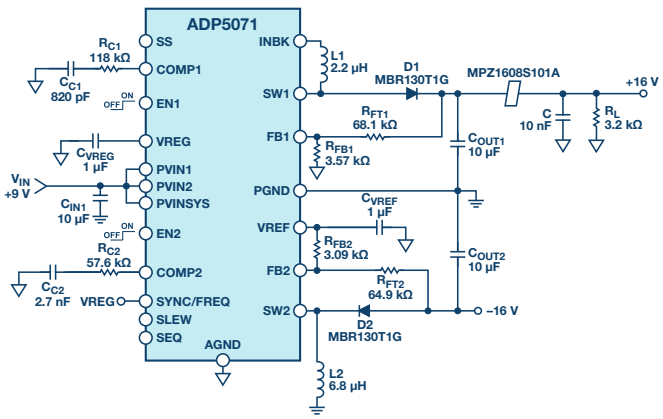


Figure 5. ADP5071 application circuit with a bead and capacitor low-pass filter implementation on positive output.

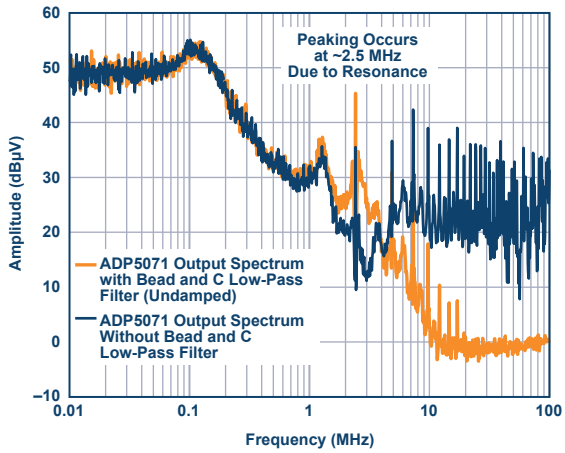


Figure 6. ADP5071 spectral output at 5 mA load.

Resonant peaking occurs at around 2.5 MHz due to the inductance of the bead and the 10 nF ceramic capacitor. Instead of attenuating the fundamental ripple frequency at 2.4 MHz, a gain of 10 dB occurs.

Other factors that have an effect on the resonant peaks are the series and load impedances of the ferrite bead filter. Peaking is significantly reduced and damped for higher source resistance. However, the load regulation degrades with this approach, making it unrealistic in practice. The output voltage droops with load current due to the drop from the series resistance. Load impedance also affects the peaking response. Peaking is worse for light load conditions.

Damping Methods

This section describes three damping methods that a system engineer can use to reduce the level of resonant peaking significantly (see Figure 7).

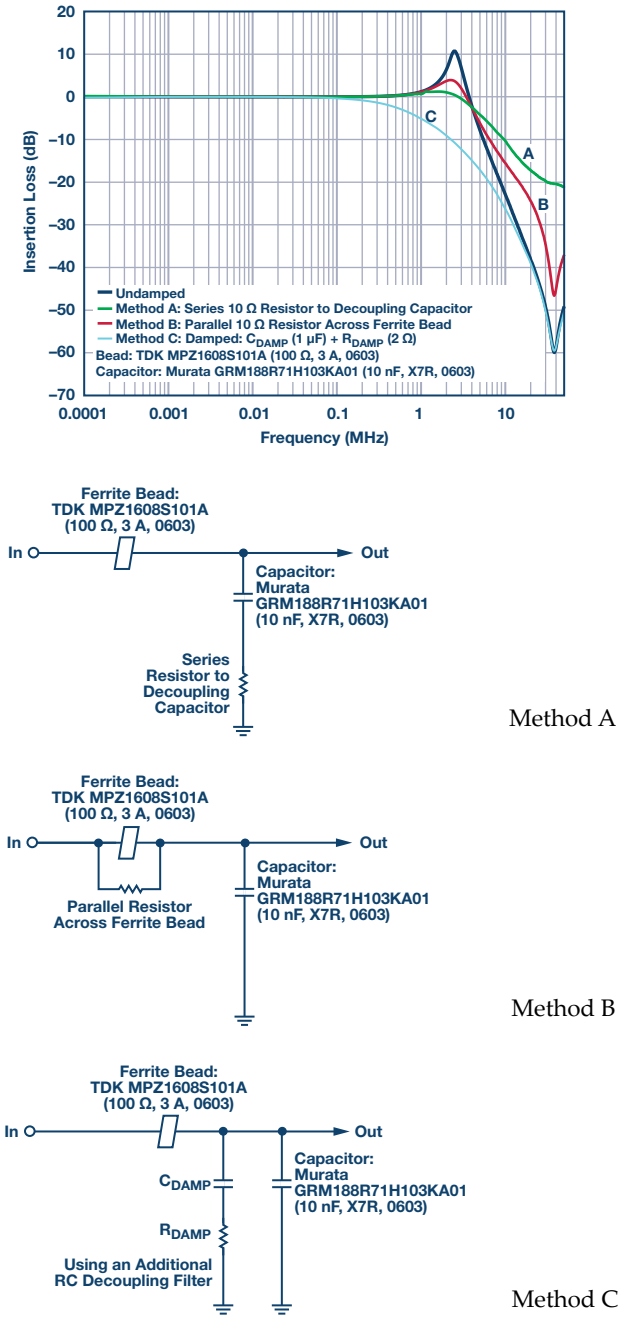


Figure 7. Actual frequency response for various damping methods.

Method A consists of adding a series resistor to the decoupling capacitor path that dampens the resonance of the system but degrades the bypass effectiveness at high frequencies. Method B consists of adding a small parallel resistor across the ferrite bead that also dampens the resonance of the system. However, the attenuation characteristic of the filter is reduced at high frequencies. Figure 8 shows the impedance vs. frequency curve of the MPZ1608S101A with and without a 10 Ω parallel resistor. The light green dashed curve is the overall impedance of the bead with a 10 Ω resistor in parallel. The impedance of the bead and resistor combination is significantly reduced and is dominated by the 10 Ω resistor. However, the 3.8 MHz crossover frequency for the bead with the 10 Ω parallel resistor is much lower than the crossover frequency of the bead on its own at 40.3 MHz. The bead appears resistive at a much lower frequency range, lowering the Q for improved damped performance.

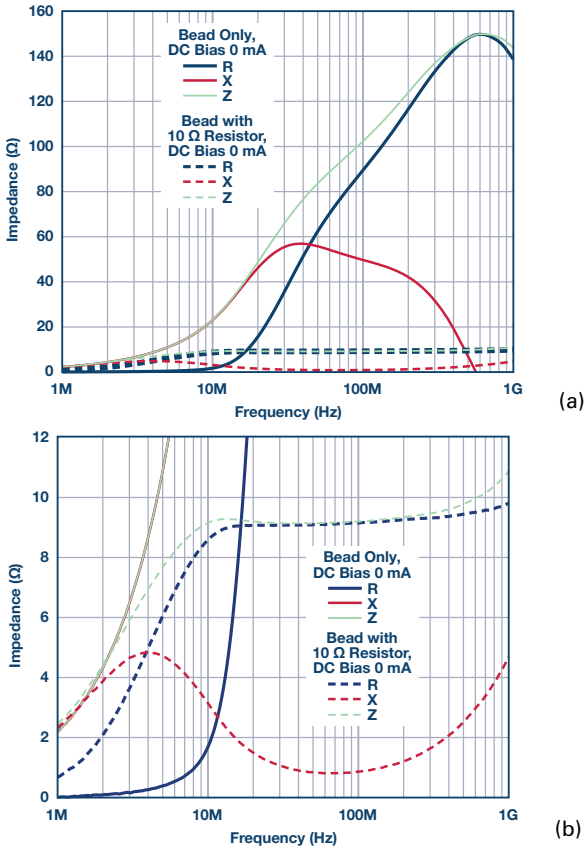


Figure 8. (a) MPZ1608S101A ZRX plot and (b) MPZ1608S101A ZRX plot, zoom view.

Method C consists of adding a large capacitor (C_{DAMP}) with a series damping resistor (R_{DAMP}), which is often an optimal solution.

Adding the capacitor and resistor damps the resonance of the system and does not degrade the bypass effectiveness at high frequencies. Implementing this method avoids excessive power dissipation on the resistor due to a large dc blocking capacitor. The capacitor must be much larger than the sum of all decoupling capacitors, which reduces the required damping resistor value. The capacitor impedance must be sufficiently smaller than the damping resistance at the resonant frequency to reduce the peaking.

Figure 9 shows the ADP5071 positive output spectral plot with Method C damping implemented on the application circuit shown in Figure 5. The C_{DAMP} and R_{DAMP} used are a 1 µF ceramic capacitor and a 2 Ω SMD resistor, respectively. The fundamental ripple at 2.4 MHz is reduced by 5 dB as opposed to the 10 dB gain shown in Figure 9.

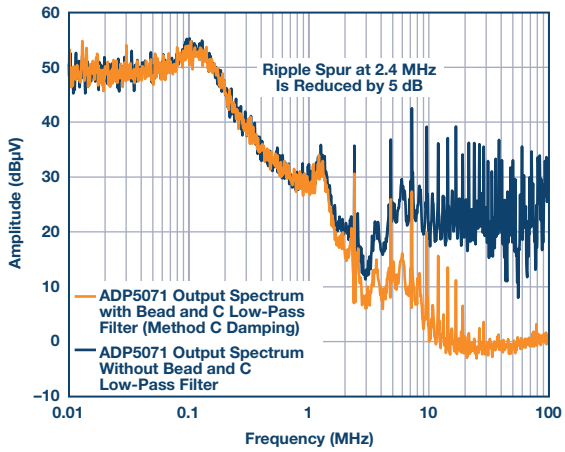


Figure 9. ADP5071's spectral output plus a bead and capacitor low-pass filter with Method C damping.

Generally, Method C is the most elegant and is implemented by adding a resistor in series with a ceramic capacitor rather than buying an expensive dedicated damping capacitor. The safest designs always include a resistor that can be tweaked during prototyping and that can be eliminated if not necessary. The only drawbacks are the additional component cost and greater required board space.

Conclusion

This article shows key considerations that must be taken into account when using ferrite beads. It also details a simple circuit model representing the bead. The simulation results show good correlation with the actual measured impedance vs. the frequency response at zero dc bias current.

This article also discusses the effect of the dc bias current on the ferrite bead characteristics. It shows that a dc bias current greater than 20% of the rated current can cause a significant drop in the bead inductance. Such a current can also reduce the effective impedance of the bead and degrade its EMI filtering capability. When using ferrite beads in supply rail with dc bias current, ensure that the current does not cause saturation of the ferrite material and produce significant change of inductance.

Because the ferrite bead is inductive, do not use it with high Q decoupling capacitors without careful attention. Doing so can do more harm than good by producing unwanted resonance in a circuit. However, the damping methods proposed in this article offer an easy solution by using a large decoupling capacitor in series with a damping resistor across the load, thus avoiding unwanted resonance. Applying ferrite beads correctly can be an effective and inexpensive way to reduce high frequency noise and switching transients.

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Acknowledgements

The authors would like to acknowledge Jeff Weaver, Donal O'Sullivan, Luca Vassalli, and Pat Meehan (University of Limerick, Ireland) for sharing their technical expertise and inputs.

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Also by this Author:

Understanding Switching Regulator Output Artifacts Expedites Power Supply Design

Volume 48, Number 3

Analog Front-End Design Considerations for RTD Ratiometric Temperature Measurements

By Barry Zhang and Alex Buda

Introduction

Many system designers use Σ-Δ ADCs together with RTDs (resistance temperature detectors) for temperature measurements, but have difficulties achieving the high performance as specified by the data sheet of the ADC they are using. For example, some designers may only be able to get 12 to 13 noise-free bits from a 16-bit to 18-bit ADC. The front-end techniques introduced in this article will enable designers to achieve 16+ noise-free bits in their system designs.

Using RTDs in a ratiometric measurement has the advantage in that it eliminates sources of error such as the accuracy and drift of the excitation current source. Below is a typical circuit for a 4-wire RTD ratiometric measurement circuit. The 4-wire configuration has the advantage that the error due to lead resistance can be canceled.

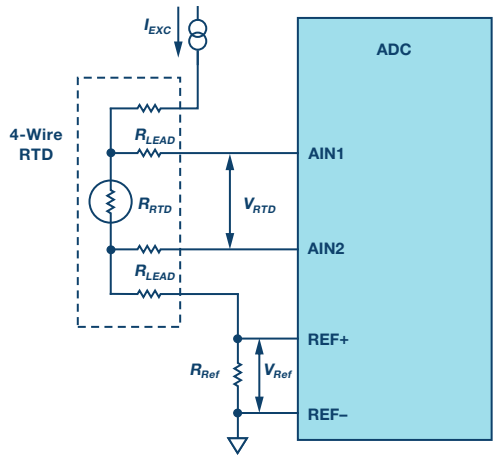

Figure 1. 4-wire RTD ratiometric measurement circuit.

From the circuit above, we can derive the following two equations:

$$V_{RTD} = R_{RTD} \times I_{EXC}$$
$$V_{Ref} = R_{Ref} \times I_{EXC}$$

The general expression used to calculate the RTD resistance (R_{RTD}) when the ADC is operating in bipolar differential mode is given by:

$$R_{RTD} = \frac{Code_{RTD} \times R_{Ref}}{Code_{ADC\_Fullscale}}$$

where:

$Code_{RTD}$ is the ADC code.

$Code_{ADC\_Fullscale}$ is the ADC full-scale code.

The measured resistance value of the RTD is theoretically only related to the precision and drift of the reference resistor. Normally R_{REF} is an accurate and low drift resistor with 0.1% precision.

When engineers design their products using this type of circuit, they will add some resistors and capacitors before the analog input, external reference pins for low-pass filtering, and overvoltage protection, as shown in Figure 2. In this article, we will show what should be considered in choosing suitable resistors and capacitors for better noise performance.

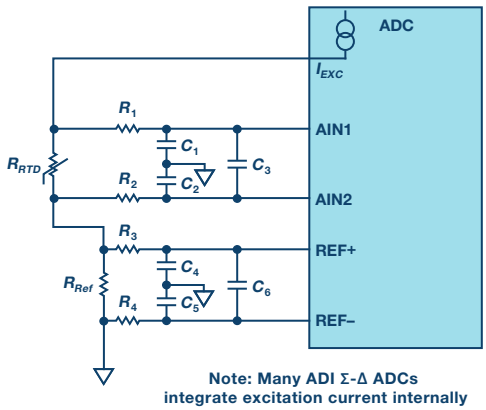

Figure 2. Typical 4-wire RTD ratiometric measurement circuit.

From Figure 2 we can see that R_1, R_2, C_1, C_2, and C_3 are used as a first-order, low-pass RC filter that provides attenuation for both differential and common-mode voltage signals. The values of R_1 and R_2 should be the same and similarly for the values of C_1 and C_2. Similarly, R_3, R_4, C_4, C_5, and C_6 are used as a low-pass filter for the reference path.

Common-Mode Low-Pass RC Filter

Figure 3 shows the common-mode, low-pass filter equivalent circuit.

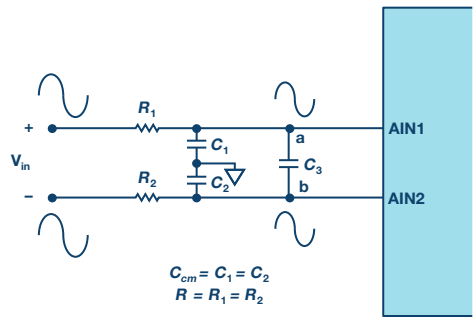

Figure 3. Common-mode low-pass filter.

Because the common-mode voltage at Point a is equal to the voltage at Point b, there is no current flowing through C_3. Therefore, the common-mode cutoff frequency can be expressed as

$$f = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \mathrm{R} C_{cm}}$$

Differential Mode Low-Pass RC Filter

To better understand the low-pass RC filter cutoff frequency for differential signals, the C_3 capacitor in Figure 4 can be thought of as two separate capacitors C_a and C_b in Figure 5.

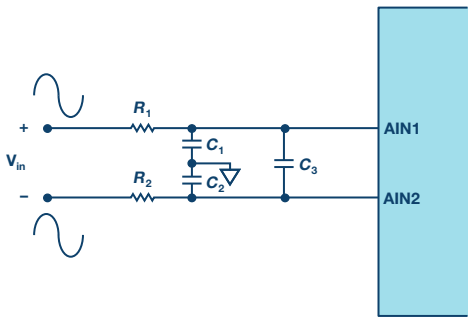

Figure 4. Differential mode low-pass filter.

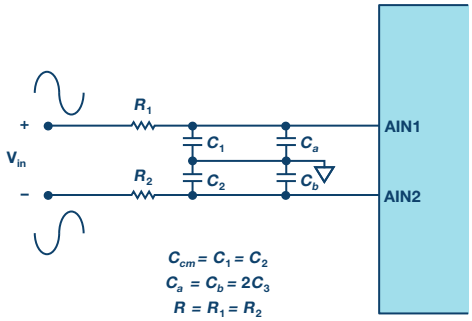

Figure 5. Differential mode low-pass filter equivalent circuit.

From Figure 5, the differential mode cutoff frequency is:

$$f = \frac{1}{2\pi R_1 (C_1 + C_a)} = \frac{1}{2\pi R (C_{cm} + 2C_3)}$$

Normally the value of C_3 is 10× larger than the value of C_{cm}. The purpose of this is to decrease the effects that are introduced by the mismatch of C_1 and C_2. For example, with an analog front-end design used in the Analog Devices circuit note CN-0381 as seen in Figure 6, the cutoff frequency for differential signals is around 800 Hz and the cutoff frequency for common-mode signals is 16 kHz.

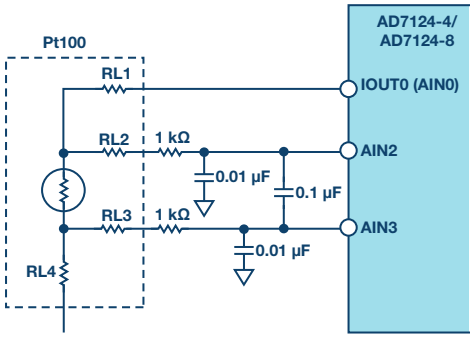

Figure 6. Analog input configuration for RTD measurement using AD7124.

Resistor and Capacitor Considerations

Other than being part of the low-pass filter, R_1 and R_2 can also provide overvoltage protection. If 3 kΩ resistors are used before the AD7124-4 A_{IN} pins in Figure 6, these can protect against up to 30 V miswiring. It's not recommended to use larger resistors before the A_{IN} pins for the following two reasons. First of all, they will generate more thermal noise. Secondly, the A_{IN} pins will have input currents that will flow across these resistors and introduce errors. These input currents do not have a constant value and when combined with a mismatch between them they will generate noise that will increase with the size of the resistors.

The resistor and capacitor values play a vital role in determining the performance of the final circuit. Designers need to understand their field requirements and calculate the resistor and capacitor values according to the equations above. For ADI Σ-Δ ADC parts and precision analog microcontrollers with an integrated excitation current source, it is recommended to use the same resistor and capacitor values before the A_{IN} and reference pins. This design ensures that the analog input voltage remains ratiometric to the reference voltage and any errors in the analog input voltage due to the temperature drift and noise of the excitation current are compensated by the variation of the reference voltage.

Measured Noise Performance on ADuCM360 with Ratiometric Measurement

The ADuCM360 is a fully integrated, 3.9 kSPS, 24-bit data acquisition system that incorporates dual high performance, multichannel Σ-Δ ADCs, a 32-bit ARM® Cortex®-M3 processor, and Flash/EE memory on a single chip. It also integrates programmable gain instrumentation amplifiers, a precision band gap reference, programmable excitation current sources, a flexible multiplexer, and many other features. It allows a direct interface to resistive temperature sensors.

When using the ADuCM360 for RTD measurements, the REF– pin is normally connected to ground so R_4 and C_5 from Figure 2 can be removed as there is no current flowing across them. C_4 and C_6 are in parallel so these two can be added together. However, because C_4 is much smaller than C_6, it can be ignored. This results in the simplified analog front-end circuit as shown in Figure 7.

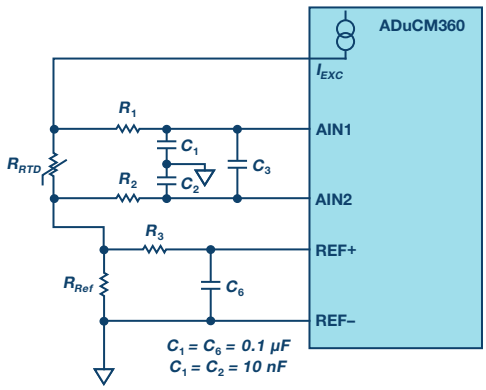

Figure 7. ADuCM360 analog front-end circuit for RTDs measurement.

Table 1 shows the noise level with matched and unmatched filters in front of the analog and reference input paths. A 100 Ω precision resistor is used instead of R_{RTD} to measure the noise voltage on the ADC input pins. The value of R_{Ref} is 5.62 kΩ.

Table 1. Noise Test Results

ADC Gain	I_{SOURCE} (μA)	Noise Voltage on 100 Ω Resistor (μV)	
		$R_1 = R_2 = R_3 = 1k$	$R_1 = R_2 = 10k$, $R_3 = 1k$
16	100	1.6084	1.8395
16	200	1.6311	1.7594
16	300	1.6117	1.9181
16	400	1.6279	1.9292

From Table 1 we can see that using a matched analog front-end circuit where the values of R_1 and R_2 are the same as R_3, the noise decreases by around 0.1 μV to 0.3 μV as compared to the unmatched circuit, which means that the number of ADC noise-free bits increases by about 0.25 bit to 16.2 bits with an ADC PGA gain of 16.

Conclusion

Using matched RC filter circuits and choosing the right resistor and capacitor values based on field requirements according to the considerations introduced in this article, the RTDs in ratiometric measurement applications can achieve optimum results.

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CN-0267 Circuit Note. "Complete 4 mA to 20 mA Loop-Powered Field Instrument with HART Interface." Analog Devices, Inc.

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Phase Response in Active Filters

Part 3—The Band-Pass Response

By Hank Zumbahlen

Introduction

In the first article of this series,[1] I examined the relationship of the filter phase to the topology of the implementation of the filter. In the second article,[2] I examined the phase shift of the filter transfer function for the low-pass and high-pass responses. This article will concentrate on the band-pass response. While filters are designed primarily for their amplitude response, the phase response can be important in some applications.

For purposes of review, the transfer function of an active filter is actually the cascade of the filter transfer function and the amplifier transfer function (see Figure 1).

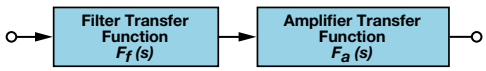

Figure 1. Filter as cascade of two transfer functions.

The Band-Pass Transfer Function

Changing the numerator of the low-pass prototype to $H_0 \frac{\omega_0}{Q} s$ will convert the filter to a band-pass function. This will put a zero in the transfer function. An s term in the numerator gives us a zero and an s term in the numerator gives us a pole. A zero will give a rising response with frequency while a pole will give a falling response with frequency.

The transfer function of a second-order band-pass filter is then:

$$H(s) = \frac{H_0 \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (1)$$

ω_0 here is the frequency ($F_0 = 2\pi\omega_0$) at which the gain of the filter peaks.

H_0 is the circuit gain (Q peaking) and is defined as:

$$H_0 = H/Q \quad (2)$$

where H is the gain of the filter implementation.

Q has a particular meaning for the band-pass response. It is the selectivity of the filter. It is defined as:

$$Q = \frac{F_0}{F_H - F_L} \quad (3)$$

where F_L and F_H are the frequencies where the response is –3 dB from the maximum.

The bandwidth (BW) of the filter is described as:

$$BW = F_H - F_L \quad (4)$$

It can be shown that the resonant frequency (F_0) is the geometric mean of F_L and F_H, which means that F_0 will appear half way between F_L and F_H on a logarithmic scale.

$$F_0 = \sqrt{F_H F_L} \quad (5)$$

Also, note that the skirts of the band-pass response will always be symmetrical around F_0 on a logarithmic scale.

The amplitude response of a band-pass filter to various values of Q is shown in Figure 2. In this figure, the gain at the center frequency is normalized to 1 (0 dB).

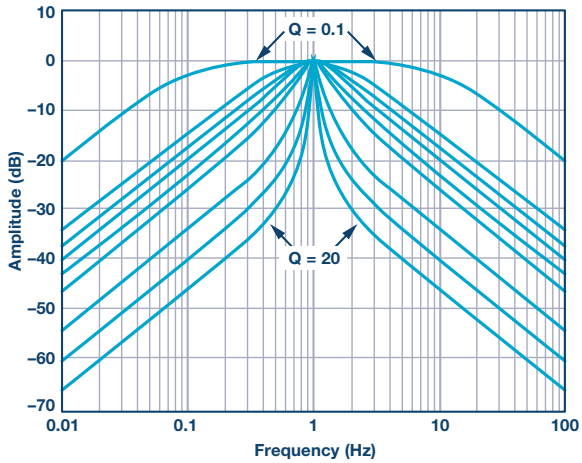

Figure 2. Normalized band-pass filter amplitude response.

Again, this article is primarily concerned with the phase response, but it is useful to have an idea of the amplitude response of the filter.

A word of caution is appropriate here. Band-pass filters can be defined two different ways. The narrow-band case is the classic definition that we have shown above. In some cases, however, if the high and low cutoff frequencies are widely separated, the band-pass filter is constructed out of separate high-pass and low-pass sections. Widely separated, in this context, means separated by at least two octaves (×4 in frequency). This is the wideband case. We are primarily concerned with the narrow-band case for this article. For the wideband case, evaluate the filter as separate high-pass and low-pass sections.

While a band-pass filter can be defined in terms of standard responses, such as Butterworth, Bessel, or Chebyshev, they are also commonly defined by their Q and F_0.

The phase response of a band-pass filter is:

$$\phi(\omega) = \frac{\pi}{2} - \arctan\left(\frac{2Q\omega}{\omega_0} + \sqrt{4Q^2-1}\right) - \arctan\left(\frac{2Q\omega}{\omega_0} - \sqrt{4Q^2-1}\right) \quad (6)$$

Note that there is no such thing as a single-pole band-pass filter.

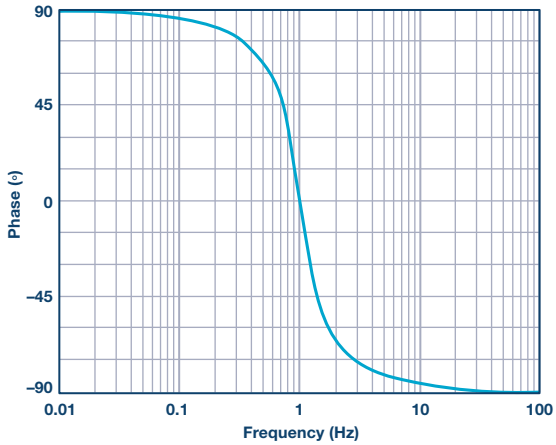

Figure 3. Normalized band-pass filter phase response.

Figure 3 evaluates Equation 6 from two decades below the center frequency to two decades above the center frequency. The center frequency has a phase shift of 0°. The center frequency is 1 and the Q is 0.707. This is the same Q used in the previous article, although in that article we used α. Remember α = 1/Q.

Inspection shows the shape of this curve is basically the same as that of the low-pass (and the high-pass for that matter). In this case, however, the phase shift is from 90°, below the center frequency going to 0° at the center frequency to –90° above the center frequency.

In Figure 4 we examine the phase response of the band-pass filter with varying Q. If we take a look at the transfer function, we can see that the phase change can take place over a relatively large frequency range, and that the range of the change is inversely proportional to the Q of the circuit. Again, inspection shows that the curves have the same shape as those for the low-pass (and high-pass) responses, just with a different range.

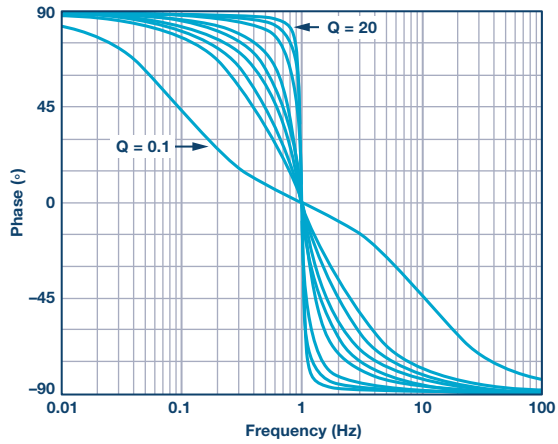

Figure 4. Normalized band-pass filter phase response with varying Q.

The Amplifier Transfer Function

It has been shown in previous installments that the transfer function is basically that of a single-pole filter. While the phase shift of the amplifier is generally ignored, it can affect the overall transfer of the composite filter. The AD822 was arbitrarily chosen to use in the simulations of the filters in this article. It was chosen partially to minimize the effect on the filter transfer function. This is because the phase shift of the amplifier is considerably higher in frequency than the corner frequency of the filter itself. The transfer function of the AD822 is shown in Figure 5, which is information taken directly from the data sheet.

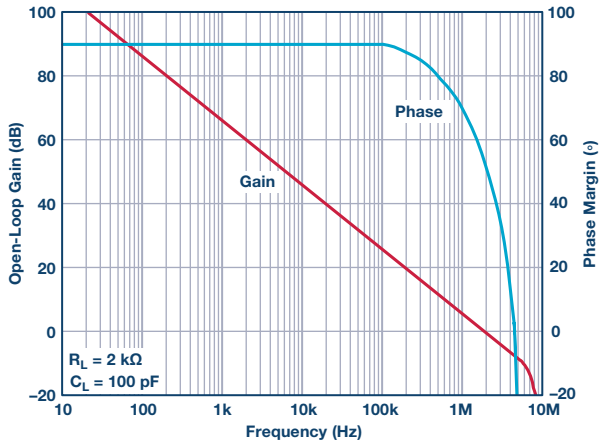

Figure 5. AD822 bode plot gain and phase.

Example 1: A 1 kHz, 2-Pole Band-Pass Filter with a Q = 20

The first example will be a filter designed as a band-pass from the start. We arbitrarily choose a center frequency of 1 kHz and a Q of 20. Since the Q is on the higher side, we will use the dual amplifier band-pass (DABP) configuration. Again, this is an arbitrary choice.

We use the design equations from Reference 1. The resultant circuit is shown in Figure 6:

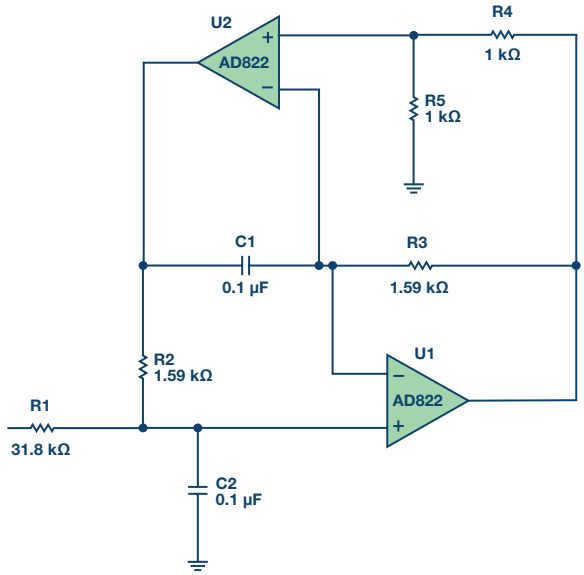

Figure 6. 1 kHz, Q = 20 DABP band-pass filter.

We are primarily concerned with phase in this article, but I think it is useful to examine the amplitude response.

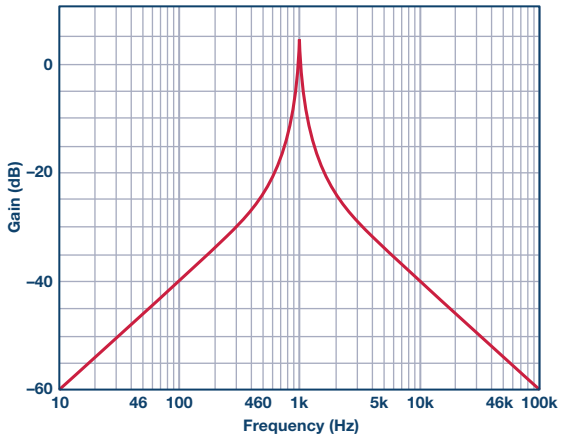

Figure 7. 1 kHz, Q = 20 DABP band-pass filter amplitude response.

We see the phase response in Figure 8:

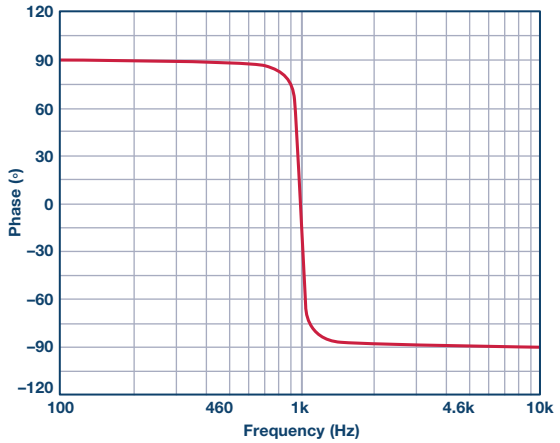

Figure 8. 1 kHz, Q = 20 DABP band-pass filter phase response.

Note that the DABP configuration is noninverting. Figure 8 matches Figure 3.

Example 2: A 1 kHz, 3-Pole 0.5 dB Chebyshev Low-Pass to Band-Pass Filter Transformation

Filter theory is based on a low-pass prototype that can then be manipulated into the other forms. In this example, the prototype that will be used is a 1 kHz, 3-pole, 0.5 dB Chebyshev filter. A Chebyshev filter was chosen because it would show more clearly if the responses were not correct. The ripples in the pass band, for instance, would not line up. A Butterworth filter would probably be too forgiving in this instance. A 3-pole filter was chosen so that a pole pair and a single pole would be transformed.

The pole locations for the LP prototype (from Reference 1) are:

Stage	α	β	F_0	α
1	0.2683	0.8753	1.0688	0.5861
2	0.5366		0.6265	

The first stage is the pole pair and the second stage is the single pole. Note the unfortunate convention of using α for two entirely separate parameters. The α and β on the left are the pole locations in the s plane. These are the values that are used in the transformation algorithms. The α on the right is 1/Q, which is what the design equations for the physical filters want to see.

The low-pass prototype is now converted to a band-pass filter. The equation string outlined in Reference 1 is used for the transformation. Each pole of the prototype filter will transform into a pole pair. Therefore, the 3-pole prototype, when transformed, will have six poles (3-pole pairs). In addition, there will be six zeros at the origin. There is no such thing as a single-pole band-pass.

Part of the transformation process is to specify the 3 dB bandwidth of the resultant filter. In this case this bandwidth will be set to 500 Hz. The results of the transformation yield:

Stage	F_0	Q	A_0
1	804.5	7.63	3.49
2	1243	7.63	3.49
3	1000	3.73	1

In practice, it might be useful to put the lower gain, lower Q section first in the string, to maximize signal level handling. The reason for the gain requirement for the first two stages is that their center frequencies will be attenuated relative to the center frequency of the total filter (that is, they will be on the skirt of other sections).

Since the resultant Qs are moderate (less than 20), the multiple feedback topology will be chosen. The design equations for the multiple feedback band-pass filter from Reference 1 are used to design the filter. Figure 9 shows the schematic of the filter itself.

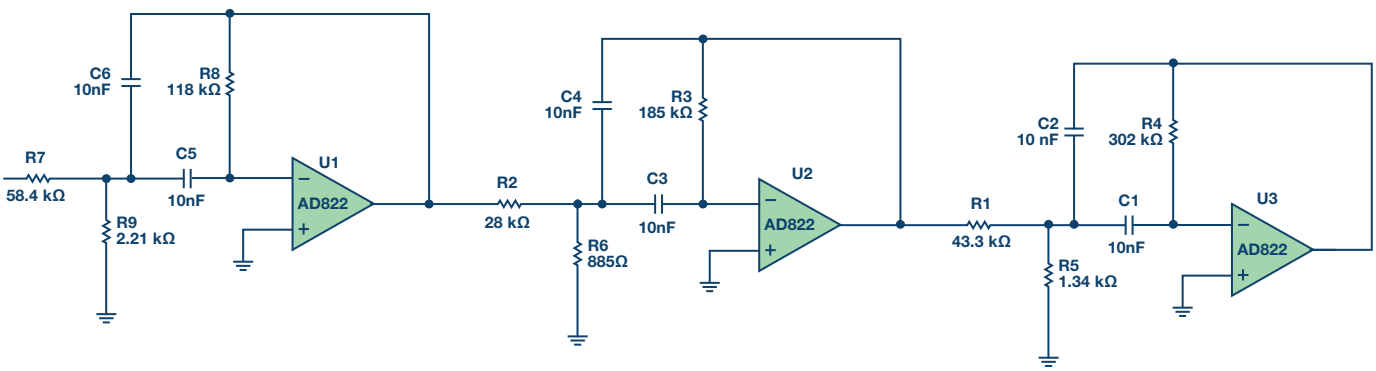

Figure 9. 1 kHz, 6-pole, 0.5 dB Chebyshev band-pass filter.

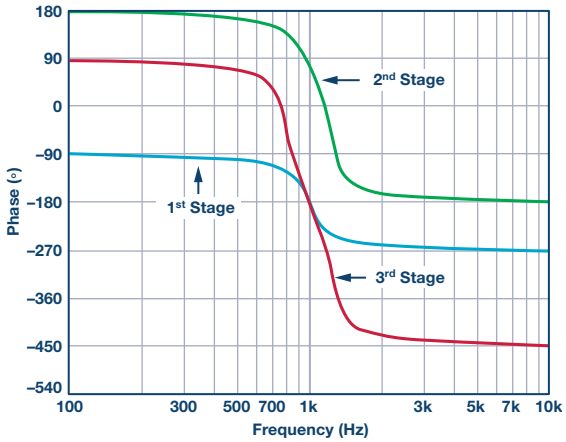

Figure 10. Phase response of a 1 kHz, 6-pole, 0.5 dB Chebyshev band-pass filter.

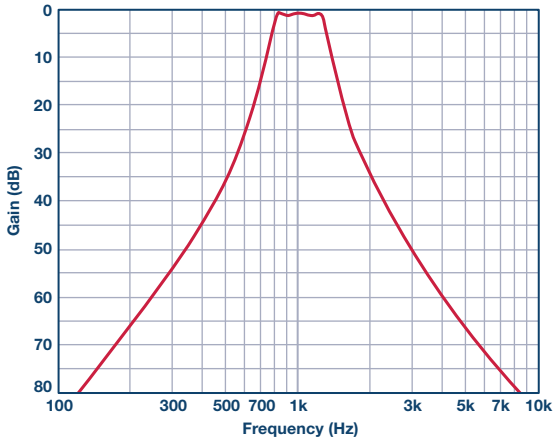

Figure 11. Amplitude response of a 1 kHz, 6-pole, 0.5 dB Chebyshev band-pass filter.

In Figure 10 we look at the phase shift of the complete filter. The graph shows the phase shift of the first section alone (Section 1), of the first two sections together (Section 2), and of the complete filter (Section 3). These show the phase shift of the "real" filter sections, including the phase shift of the amplifier and the inversion of the filter topology.

There are a couple of details to note on Figure 10. First, the phase response is cumulative. The first section shows a change in phase of 180° (the phase shift of the filter function, disregarding the phase shift of the filter topology). The second section shows a phase change of 360° due to having two sections, 180° from each of the two sections. Remember that 360° = 0°. And the third section shows 540° of phase shift, 180° from each of the sections. Also note that at the frequencies above 10 kHz we are starting to see the phase roll-off slightly due to the amplifier response. We can see that the roll-off is again cumulative, increasing for each section.

In Figure 11 we see the amplitude response of the complete filter.

Conclusion

This article considers the phase shift of band-pass filters. In previous articles in this series, we examined the phase shift in relation to filter topology and for high-pass and low-pass topologies. In future articles, we will look at notch and all-pass filters. In the final installment, we will tie it all together and examine how the phase shift affects the transient response of the filter, looking at the group delay, impulse response, and step response, and what that means to the signal.

Endnotes:

[1] Hank Zumbahlen. "Phase Relations in Active Filters." *Analog Dialogue*, Volume 41, Number 4, 2007.

[2] Hank Zumbahlen. "Phase Response in Active Filters Part 2, the Low-Pass and High-Pass Responses." *Analog Dialogue*, Volume 43, Number 3, 2009.

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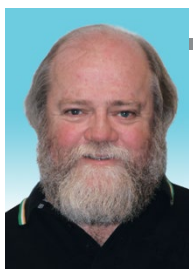

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Volume 46, Number 6

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