**ANALOG DEVICES**

## Interfacing AD7276 High-Speed Data Converters to ADSP-BF535 Blackfin® Processors

*Contributed by Aseem Vasudev Prabhugaonkar*                                    *Rev 1 – October 4, 2004*

## Introduction

This application note explains how to interface AD7276 high-speed data converters to Blackfin® processors. This application note also provides example code to demonstrate how the Blackfin processor's serial ports (SPI and SPORTs) can be programmed to receive data from AD7276 devices in core and DMA modes. The power-down scheme for AD7276 ADCs between conversions in DMA mode is also described. The interface is achieved using an ADSP-BF535 EZ-KIT Lite™ board.

## About AD7276/7277/7278 ADCs

The AD7276/AD7277/AD7278 devices are 12-, 10-, and 8-bit, high-speed, low-power, successive-approximation ADCs, respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates up to 3 million samples per second (MSPS).

The conversion process and data acquisition are controlled using the /CS signal and the serial clock, allowing the devices to interface with variety of microprocessors or DSPs. The input signal is sampled on the falling edge of /CS, and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7276/AD7277/AD7278 ADCs use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from VDD. This allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is from 0 V to VDD. The conversion rate is determined by the serial clock SCLK.

### AD7276/7277/7278 Product Highlights

- 3 MSPS ADCs in a 6-lead TSOT package

- Pin compatible to AD7476/7477/7478 and AD7476A/7477A/7478A parts

- High throughput with low power consumption

- Flexible power / serial clock speed management

  The conversion rate is determined by the serial clock. Increasing the serial clock speed reduces the conversion time. This reduces average power consumption while in power-down mode (i.e., while not converting). The part also features a power-down mode to maximize power efficiency at lower throughput rates. Current consumption is 1 µA max in power-down mode.

- Reference derived from the power supply

- No pipeline delay

  The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a /CS input and once-off conversion control.

### AD7276/7277/7278 A/D Applications

AD7276/7277/7278 applications include:

- Battery-Powered Systems

- Personal Digital Assistants

- Medical Instruments

- Mobile Communications

- Instrumentation and Control Systems

- Data Acquisition Systems

- High-Speed Modems

- Optical Sensors

## About ADSP-BF535 Processors

The ADSP-BF535 processor is the first member of the Blackfin family—ADI's newest family of high-performance processors based on the Micro Signal Architecture (MSA). ADSP-BF535 parts feature dual-MACs, high clock rates, and dynamic power management, allowing for optimization of system performance and power consumption. Additionally, through the advantages of a clean, orthogonal RISC instruction set, ADSP-BF535 processors are optimized for programming in high-level languages such as C/C++, resulting in extremely dense code.

### Blackfin Processor Applications

Target applications of Blackfin processor include:

- Automotive

- Broadband Home Gateways

- Central Office/Network Switches

- Digital Imaging and Printing

- Global Positioning Systems

- Home Networking

- Internet Appliances

- Modem Solutions

- Personal Digital Assistants

- Video Conferencing

- VoIP Phone Solutions

- PDAs and other portable/hand-held devices

## AD7276-to-ADSP-BF535 Interface

This application note focuses on the interface to an AD7276 high-speed data converter. AD7277 and AD8278 converters interface the same way. The ADCs have a serial interface for DSPs and micro-controllers for transferring 12-bit digitized data. The ADCs support SPI (Serial Peripheral Interface) and SPORT (DSP Serial Port) interface protocols. Blackfin processors can connect to an AD7276 over their SPI or SPORT interfaces.

The serial interface of AD7276 comprises three signals.

- `/CS` Chip Select is an active low input. This signal initiates A-to-D conversion and frames the serial data transfer.

- `SDATA` The AD7276 drives conversion results onto this pin. The data bits are clocked out on the falling edge of the serial clock.

- `SCLK` Serial clock is an input to the ADC. The converter clocks the data bits out on the falling serial clock edges.

The falling edge of `/CS` puts track-and-hold into hold mode and initiates conversion. For compatibility with the 16-bit word length supported by SPI, the ADC outputs 16-bits. The first two bits (zeros) are followed by 12 valid data bits and two zero bits at the end of the serial data stream. Though the ADC data is 12 bits, each word is transferred as a 16-bit word. This ensures compatibility with the SPI standard, configurable to word lengths of 8 or 16 bits on Blackfin devices. When interfaced to SPORT modules, the serial word length can be configured to 14 bits; hence, the last two bits can be ignored. On the 14th SCLK rising edge, the converter logic changes back to track mode.
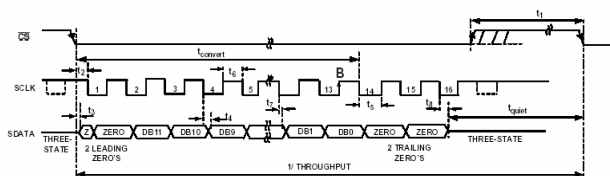
Figure 1. AD7276 Serial Interface Timing Diagram

Refer to the AD7276 data sheet for detailed information about the timing specifications.

## SPI Interface Details

This section discusses the AD7276 interface with SPI port using an ADSP-BF535 EZ-KIT Lite board.

ADSP-BF535 Blackfin processors feature two independent Serial Peripheral Interface (SPI) ports (SPI0 and SPI1) that provide an I/O interface to a wide variety of SPI-compatible peripheral devices including codecs, data converters, and sample rate converters. Each SPI port has a set of control registers and data buffers.

The ADSP-BF535 processor's SPI module is an industry-standard synchronous serial link that supports communication with multiple SPI-compatible devices. The SPI peripheral is a synchronous, 4-wire interface consisting of two data pins (MOSI and MISO), one device select pin (/SPISS), and a gated clock pin (SCK). The ADSP-BF535 SPI supports the following features:

- Full duplex operation
- Master-slave mode multi-master environment
- Open drain outputs
- Programmable bit rates, clock polarities, and phases
- Slave operations with another master SPI device

The ADSP-BF535 processor is an SPI master for this interface, supplying a serial bit clock and the chip select /CS to the AD7276 ADC. The processor receives data on its MISO pin. Refer to Figure 2 for interface details.
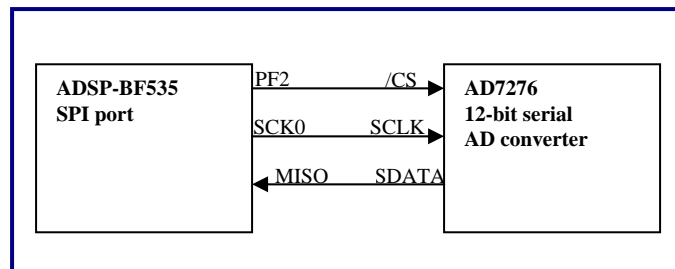


Figure 2. ADSP-BF535 SPI Interface with AD7276

The ADSP-BF535 SPI and AD7276 interface can be accomplished using CPHASE=0, CPOL=1 mode as well as the CPHASE=1, CPOL=1 mode. These modes have been tested with serial clock frequency of about 6 MHz. The advantage of CPHASE=0 mode over CPHASE=1 mode is that CPHASE=0 mode can be used with the DMA mode of operation. For CPHASE=1 mode, the slave device select (PFx) must be asserted and de-asserted manually. For CPHASE=0 mode, the slave device select (/CS for AD7276) is controlled by the Blackfin processor's SPI hardware, and hence, it is automated. The code supplied along with this application note includes core as well DMA SPI modes of operation.

In core and DMA mode of SPI operation, the SPI is configured for a 16-bit word length by setting the SIZE bit in the SPI0_CTL register.

### CPHASE=0, CPOL=1 SPI Modes

Core as well as DMA SPI modes of operation are possible with CPHASE=0. Refer to Figure 3 for timing details.

In CPHASE=0, CPOL=1 mode, the received word must be right-shifted by 2 bits before being stored in internal memory. This is done because the last 2 bits are zero. The data is driven on the falling edge of the serial clock. The ADSP-BF535 SPI samples the data on the serial clock's falling edges. The AD7276 converter's data hold time specification enables this scheme. Refer to Figure 4 for timing information regarding hold time.
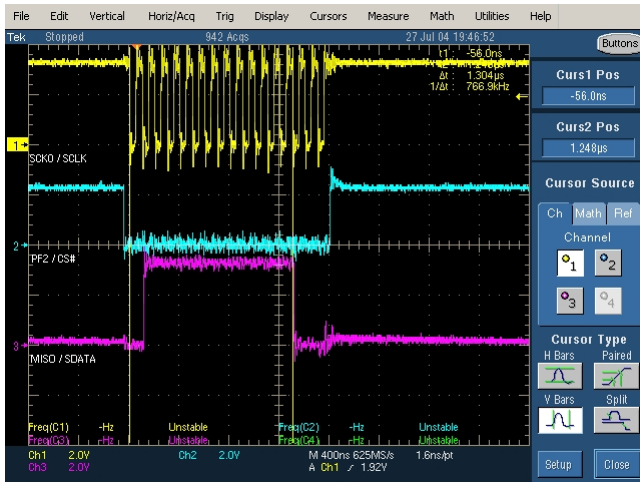
*Figure 3. CPHASE=0, CPOL=1 in Core Mode.*



*Figure 4. CPHASE=0, CPOL=1 in Core Mode – AD7276 Hold Time*

### CPHASE=1, CPOL=1 SPI Modes

When CPHASE=1, only core mode is possible as the device chip select must be controlled manually. Refer to Figure 5 for timing information.

In CPHASE=1, CPOL=1 mode, the received word must be right-shifted by 3 bits before being storing in internal memory. Since the SPI samples the serial data on the serial clock's rising edge, the second bit latched is *not* the *second* zero bit driven by the ADC. It is the first valid MSB driven by the converter.
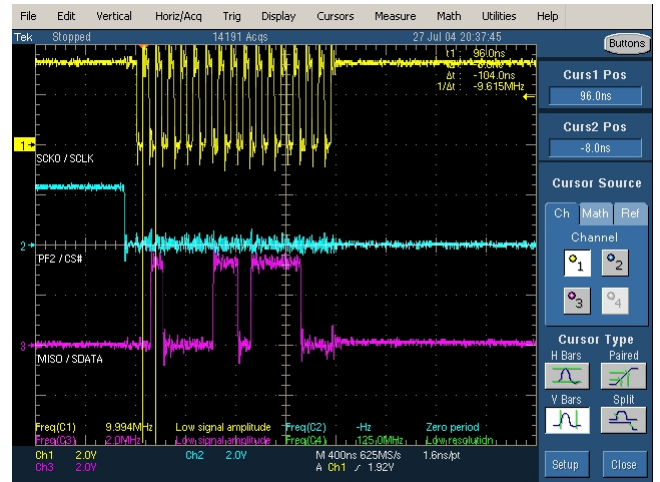


*Figure 5. CPHASE=1, CPOL=1 in Core Mode*

## AD7276 Power-Down Mode

AD7276/7277/7278 converters feature a power-down mode for power-sensitive designs. This allows power savings between conversions. To enter the power-down mode, the conversion process must be interrupted by deasserting /CS between the second falling edge of SCLK and the 10th falling edge of SCLK. This feature is demonstrated in the accompanying code, showing the DMA mode of operation. Inside the DMA completion interrupt, the SPI is configured for an 8-bit data word length. A dummy write is performed, ensuring that the /CS is brought high before the 10th SCLK. This drives the ADC into power-down mode.



*Figure 6. AD7276 Power-Down Mode*

# SPORT Interface Details

The ADSP-BF535 processor has two identical synchronous serial ports (SPORTs) which support a variety of serial data communications protocols and can provide a direct connection between processors in a multiprocessor system.

Each SPORT is a full-duplex device, capable of simultaneous data transfer in two directions. Each SPORT has one group of pins (data, clock, and frame sync) for transmit operation and a second set of pins for receive operation. The receive and transmit functions are programmed separately. The SPORTs can be programmed for bit rate, frame sync, and bits per word, by writing to memory-mapped registers.

AD7276 ADCs can be interfaced to the ADSP-BF53x processor's serial port. The interface works with both early and late frame sync modes. The serial port is configured for internal frame sync and internal serial port clock. Configure the serial port for 14-bit word length. Potentially, this increases the A/D converter's throughput by not having to pad two trailing zero bits at the end of the 12-bit word. Since the SPORT is configured for a 14-bit word length, bit shifting is *not* required, unlike the case of SPI.
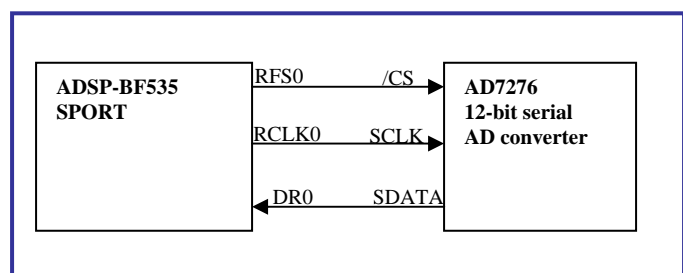
Refer to for interface details.



Figure 7. SPORT Interface with AD7276 ADC

The code supplied with this application note includes both early and late frame sync options.

## Early Frame Sync Option

When programmed for an early frame sync, configure the frame sync as an active high frame

sync. Data can be sampled at the serial clock's rising or falling edges.

Refer to for timing details.



Figure 8. SPORT Early Frame Sync Option, Rising Clock Edge Sampling - Core Mode

## Late Frame Sync Option

When programmed for a late frame sync, configure the frame sync as an active low frame sync. Data can be sampled at the serial clock's rising or falling edges.

Refer to for the timing details.



Figure 9. SPORT Late Frame Sync Option, Rising Clock Edge Sampling – Core Mode

## Summary

As seen in this application note, one can interface AD7276/7277/7278 ADCs to ADSP-BF535 Blackfin processors gluelessly and use a variety of interface methods and modes.

## Appendix

Refer to the code in the attached ZIP file for various modes of operation.

## References

[1]  *ADSP-BF535 Blackfin® Processor Hardware Reference Manual.* Rev 2.0, April 2003. Analog Devices, Inc.

[2]  *AD7276 Preliminary Technical Data Sheet.* Rev PrF, June 2004. Analog Devices, Inc.

[3]  *ADSP-BF535 EZ-KIT Lite Evaluation System Manual.* Rev 2.1, April 2003. Analog Devices, Inc.

## Document History

| Revision | Description |
|---|---|
| *Rev 1 – October 04, 2004 by Aseem Vasudev Prabhugaonkar* | Initial Release |