



DS26303

3.3V, T1/E1/J1, Short-Haul, Octal Line Interface Unit

www.maxim-ic.com

REVISION A1 ERRATA

The errata listed below describe situations where DS26303 revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS26303 revision A1 components. Revision A1 components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS26303 die revision, visit our website at www.maxim-ic.com/errata.

NOTE: THE FOLLOWING ARE FEATURE ENHANCEMENTS IMPLEMENTED IN REV A2 THAT WILL NOT WORK FOR REV A1:

- 1) Programmable corner frequency for the jitter attenuator in E1 mode.
- 2) Fully internal impedance matching option for RTIP/RRING.
- 3) Option for system-side deployment of BERT.

1. HARDWARE MODE

Description:

Hardware mode does not work. Putting the device in hardware mode resets the part.

Work Around:

None.

2. ALL-ONES INSERTION IN DIGITAL LOOPBACK

Description:

The transmit all-ones logic is inside the digital loopback path. The data looped back to RPOS/RNEG will be overwritten by any transmit all-ones condition.

Work Around:

TPOS/TNEG can be looped back to RPOS/RNEG while simultaneously sending all ones on TTIP/TRING. However all-ones will be sent on all 8 TTIP/TRING outputs. Use the settings in Table 1 to enable this feature. Use these settings instead of the TAOE register.

Table 1. Addresses and Register Settings to Transmit All Ones in Digital Loopback

ADDRESS TO THE ADDP REGISTER	HEX VALUE TO ENTER IN ADDP REGISTER	WILL ACCESS THE FOLLOWING LIUs	WRITE TO THE FOLLOWING ADDRESS WITHIN THE TEST BANK	HEX VALUE TO WRITE IN ADDRESS TO TRANSMIT ALL ONES IN DIGITAL LOOPBACK
1Fh	03h	LIU 1–8	07h	07h

3. CLKA PIN**Description:**

CLKA pin does not provide the programmable output clock when enabled.

Work Around:

None.

4. RECEIVE IMPEDANCE MODE SELECT (RIMPMS) BIT**Description:**

The RIMPMS bit (GC.7) selects between internal and external impedance-matching mode. When this bit is set, RTIP and RING require no external resistance component. When reset, RTIP and RING require external resistance. In the internal impedance-matching mode, the receiver does not function properly with the maximum 12dB cable attenuation.

Work Around:

None.