DALLAS SEMICONDUCTOR MAXIM

# DS3141/DS3142/DS3143/DS3144 Single/Dual/Triple/Quad DS3/E3 Framers



## REVISION A1 ERRATA

The errata listed below describe situations where the DS3141/DS3142/DS3143/DS3144 (DS314_) revision A1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3141/DS3142/DS3143/DS3144 revision A1 components. Revision A1components are branded on the top side of the package with a six-digit code in the form yywwA1, where yy and ww are two-digit numbers representing the year and work-week of manufacture, respectively. To obtain an errata sheet on another DS3141/DS3142/DS3143/DS3144 die revision, visit the website at www.maxim-ic.com/errata.

### 1. IMPROPER TCLK OUTPUT DURING LINE LOOPBACK

**Description:**
The TCLK output pin is not properly sourced from the RCLK input pin during line loopback (MC2:LLB = 1).

**Work Around:**
When using line loopback, also enable payload loopback (MC2:LLB = 1 and MC2:PLB = 1) to get proper TCLK operation.

Many systems have a requirement to support line loopback requests (Rx to Tx) from the far end and local loopback requests (Tx to Rx) simultaneously. Without this errata, the DS314_ framers can support this requirement using simultaneous line loopback and diagnostic loopback. With this errata, DS314_ line loopback and diagnostic loopback cannot be enabled simultaneously because proper line loopback operation requires payload loopback to be enabled as well. To support simultaneous line loopback and local loopback requests, use the line loopback (sometimes called remote loopback) of the neighboring DS3/E3 LIU and the diagnostic loopback of the DS314_ framers.

### 2. FRESYNC BIT IS LEVEL-SENSITIVE RATHER THAN EDGE-SENSITIVE

**Description**:
The data sheet indicates that a 0-to-1 transition (edge-sensitive) on T3E3CR2:FRESYNC causes the receive framer to resynchronize. On rev A1 parts, FRESYNC = 1 (level-sensitive) holds the receive framer in the resynchronize state. Thus, FRESYNC must be set back to 0 before the framer is allowed to complete the resynchronization.

**Work Around:**
To resynchronize the receive framer, software should set FRESYNC high and then immediately set it low. For most reliable operation, this pair of writes to FRESYNC can be executed with interrupt servicing disabled in the microprocessor to prevent an interrupt while the framer is held in the resynchronize state.

### 3. TRANSMIT FEAC CAN SEND ADDITIONAL COPIES OF CODEWORD A

**Description:**
If TFS[1:0] transitions from 01 to 00 after the FEAC transmitter is done sending codeword A 10 times, then the FEAC transmitter erroneously sends codeword A 10 more times before sending all ones. Similarly, if TFS[1:0]

transitions from 10 to 00 after the FEAC transmitter is done sending codeword A 10 times and codeword B 10 times, then the FEAC transmitter erroneously sends codeword A 10 more times before sending all ones.

**Work Around:**
For TFS = 01 mode (send codeword A 10 times), immediately after writing TFS to 01, write TFS back to 00. When this is done the FEAC transmitter behaves properly and only sends codeword A 10 times.

For TFS = 10 mode (send codeword A 10 times, then send codeword B 10 times), TFS must be written back to 00 during the transmission of codeword B 10 times. This must be timed by the host processor and should occur 20ms to 30ms after TFS is set to 10. An alternate work around for TFS = 10 mode is to use TFS = 01 mode to send the first codeword, wait for transmit FEAC idle (status bit TFIL = 1), and then use TFS = 01 mode again to send the second codeword.

## 4. DS3 AIS ANOMALIES

**Description:**
When transmit AIS is activated (T3E3CR1:TAIS set to 1) in DS3 mode, the transmitted DS3 AIS pattern is not frame aligned with the previous traffic (i.e., the frame alignment indicated by the TSOF pin). This results in a change-of-frame alignment when DS3 AIS is activated (TAIS = 1) and a change-of-frame alignment when DS3 AIS is deactivated (TAIS = 0). In addition, activating and deactivating AIS in DS3 mode can cause the insertion of a bipolar violation and may cause the generation of erroneous P-bits in one or both of the next two M-frames.

All these anomalies are caused by transitions into and out of DS3 AIS. The framer transmits DS3 AIS with no errors, starting two M-frames after AIS activation, and transmits normal traffic with no errors, starting two M-frames after AIS deactivation.

**Work Around:**
None

## 5. RECEIVER AIS, RAI, AND T3IDLE STATUS BITS DO NOT CLEAR DURING LOF

**Description:**
Any of the T3E3SR:AIS, T3E3SR:RAI, or T3E3SR:T3IDLE real-time status bits that are already set to 1 when the framer declares out-of-frame (and sets the T3E3SR:OOF status bit) remain set throughout the OOF interval. After the DS3 framer resynchronizes to the framing information in the incoming data stream, the status bits are allowed to clear. This erratum only occurs in DS3 mode, not in E3 mode.

**Work Around:**
If the OOF status bit is set, ignore the AIS, RAI, and T3IDLE status bits.