DS3151/DS3152/DS3153/DS3154 Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs

DALLAS SEMICONDUCTOR **MAXIM**

www.maxim-ic.com

REVISION A2 ERRATA

The errata listed below describe situations where DS3151/DS3152/DS3153/DS3154 revision A2 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS3151/DS3152/DS3153/DS3154 revision A2 components. Revision A2 components are branded on the topside of the package with a six-digit code in the form yywwA2, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS3151/DS3152/DS3153/DS3154 die revision, visit the website at **www.maxim-ic.com/errata**.

1. **TEST REGISTERS SHOULD BE WRITTEN TO MINIMIZE THE JITTER ATTENUATOR'S GENERATED JITTER**

   Description:
   LIU ports that have the jitter attenuator enabled can have excessive generated jitter unless some test register bits are set. When the test register bits are set, generated jitter is in compliance with all applicable telecom standards.

   Work Around:
   CPU bus mode: As part of the initialization routine for each LIU port, write 40h to the test register at address 09h and write 01h to the test register at address 0Ch.

   Hardware mode: None

2. **JTAG OPERATION**

   Description:
   The implementation of the JTAG logic creates some additional requirements for driving device output pins from the boundary scan register (BSR).

   Work Around:
   - When JTAG is used to drive outputs, the $\overline{TEST}$ pin must be held high. $\overline{TEST}$ can still be 0, 1, or high-impedance when JTAG is capturing the state of input pins.
   - To drive the outputs D[7:0], load the normal control cell (BSR cell 104) with 0 and also load BSR cell 87 (which enables $\overline{TDM1}$, PRBS1, and $\overline{RLOS1}$) with 0.
   - To drive the outputs RCLK1, RPOS1, and RNEG1, load the normal control cell (BSR cell 83) with 0 and also load BSR cell 87 (which enables $\overline{TDM1}$, PRBS1, and $\overline{RLOS1}$) with 0.
   - To drive the outputs RCLK2, RPOS2, and RNEG2, load the normal control cell (BSR cell 60) with 0 and also load BSR cell 64 (which enables $\overline{TDM2}$, PRBS2, and $\overline{RLOS2}$) with 0.
   - To drive the outputs RCLK3, RPOS3, and RNEG3, load the normal control cell (BSR cell 37) with 0 and also load BSR cell 41 (which enables $\overline{TDM3}$, PRBS3, and $\overline{RLOS3}$) with 0.

REV: 030807

3. POWER-ON RESET TIMING ISSUE

Description:
If during power-up V_{DD} is ramped too fast or the $\overline{RST}$ pin is asserted at the wrong time, an internal timing problem can cause some LIU ports on some devices to remain stuck in reset. When a port is stuck in reset, the RCLK, RPOS/RDAT and RNEG/RLCV pins do not toggle, and the TXP/TXN pins either drive no signal or a low-amplitude signal (< 600mV). This condition persists until V_{DD} is ramped down and back up again.

Work Around:
This timing issue can be avoided if two conditions are met:

1) V_{DD} must ramp up with a slew rate of 40μs/V or slower.

2) During power-up $\overline{RST}$ must not be asserted while V_{DD} < 3.135V.

During power-up the DS3151/2/3/4 devices are completely reset by their internal power-on reset circuits and do not need to be reset by asserting the $\overline{RST}$ pin. Since $\overline{RST}$ has an internal pull-up resistor, one easy way to meet Condition #2 above is to leave $\overline{RST}$ floating.