DS80C390
Dual CAN High-Speed Microprocessor

REVISION B1 ERRATA

The errata listed below describe situations where DS80C390 revision B1 components perform differently than expected or differently than described in the data sheet. Dallas Semiconductor intends to correct these errata in subsequent die revisions.

This errata sheet only applies to DS80C390 revision B1 components. Revision B1 components are branded on the top side of the package with a six-digit code in the form yywwB1, where yy and ww are two-digit numbers representing the year and workweek of manufacture, respectively. To obtain an errata sheet on another DS80C390 die revision, visit our website at www.maxim-ic.com/errata.

1. MOVX AND MOVC INSTRUCTIONS WILL NOT OPERATE PROPERLY WHEN V_{CC} > 4.7V

Description:
MOVX and MOVC instructions will not operate properly when V_{CC} > 4.7V.

Work Around:
Operate the device with V_{CC} between 4.0V and 4.7V.

2. THE DIV INSTRUCTION RETURNS INCORRECT RESULTS

Description:
The DIV instruction returns incorrect results.

Work Around:
Use the Arithmetic Accelerator to perform division operations instead of the DIV instruction. This erratum will be corrected in the next revision of the device.

3. THE $\overline{MUX}$ PIN REMAINS LOW IN HOOKS MODE

Description:
The $\overline{MUX}$ pin remains low in Hooks mode. This gives the appearance that all MOVX operations in Hooks mode operate on internal data memory.

Work Around:
Use external hardware/software to monitor the MOVX instructions to determine which instructions operate on internal or external memory.

4. USE OF THE WATCHDOG RESET FUNCTION WHILE THE CTM BIT IS SET WILL CAUSE UNPREDICTABLE DEVICE OPERATION

Description:
Use of the watchdog reset function while the CTM bit is set will cause unpredictable device operation.

Work Around:
Do not use the watchdog reset function in conjunction with the crystal clock multiplier. This erratum will be corrected in the next revision of the device.

5. SERIAL PORT 0 WILL NOT OPERATE CORRECTLY UNDER CERTAIN CONDITIONS

Description:
Serial port 0 will not operate correctly under the following conditions:
1) Timer 2 is used as the time base (RCLK = TCLK = 1), and
2) The SMOD bit for serial port 0 is cleared, and
3) Timer 1 is running (TR1 = 1).

Work Around:
Ensure that these conditions never occur simultaneously while using serial port 0. The easiest way is to use the serial port with the serial port doubler bit set (SMOD = 1).

6. WHILE OPERATING IN THE 24-BIT CONTIGUOUS ADDRESSING MODE, THE EXECUTION OF AN LCALL INSTRUCTION WHEN THE RETURN ADDRESS IS LOCATED WITHIN 4 BYTES OF A 64kB ADDRESS BOUNDARY CAN RESULT IN INCORRECT DATA BEING PUSHED ONTO THE STACK

Description:
While operating in the 24-bit contiguous addressing mode, the execution of an LCALL instruction when the return address is located within 4 bytes of a 64kB address boundary can result in incorrect data being pushed onto the stack.

Work Around:
Ensure that the return addresses are not located within 4 bytes of a 64kB page boundary.

7. WHEN EITHER SERIAL PORT 0 OR PORT 1 IS OPERATED IN MODE 3, THE RI BIT OF THAT SERIAL PORT MAY BE UNINTENTIONALLY SET UNDER CERTAIN CONDITIONS

Description:
When either serial port 0 or port 1 is operated in mode 3, the RI bit of that serial port may be unintentionally set under the following conditions:
a) multiprocessor communication mode is enabled (SM2 = 1), and
b) a byte is received by that serial port with the RB8 bit set, and
c) the SADEN register associated with that serial port is non-zero, and
d) the received byte, masked by the SADEN register, does not match the associated SADDR register.

Work Around:
Make sure that RB8 = 0 any time a byte is received. If using the serial port in Mode 3 with SM2 = 1, clear RB8 when initializing the serial port and after every byte is received. If the RI bit is set and RB8 = 0, then the received byte did not match and can be ignored.

8. EXTERNAL INTERRUPTS 2–5 CANNOT BE USED TO CAUSE THE DEVICE TO EXIT STOP MODE

Description:
External interrupts 2–5 cannot be used to cause the device to exit Stop mode.

Work Around:
Use external interrupts 0 and 1 if an external interrupt must be used to exit Stop Mode. It may also be possible to use the Idle mode of operation in place of Stop mode. This erratum does not affect DS80C390 revision C devices.

9. CAN AUTOBAUD MODE RXS BIT FUNCTION CLARIFIED

Description:
When either CAN is operating in autobaud mode, the RXS bit in the CxS SFR will only be set upon reception of a valid (i.e., no bus errors) identifier that matches one or more of the message IDs programmed into the CAN module. The documentation implies that the RXS bit should be set if a valid identifier is received, even if the identifier did not match any of the message IDs programmed into the CAN module.

Work Around:
If it is desired to use the autobaud mode to monitor bus activity and set RXS when any message is successfully received, the user should enable a message center to receive messages with any ID. Upon exit from autobaud mode, this message center can be reconfigured for other uses.