Rev: 110107

DS26900 Demo Kit

General Description

The DS26900 design kit provides a convenient platform to evaluate the DS26900. Connectors are provided to access all of the master and secondary JTAG ports. Jumpers allow configuration of all the DS26900 operating modes, and LEDs provide visual indication of device states.

This document is intended to be used along with the DS26900 data sheet, available online at www.maxim-ic.com/DS26900.

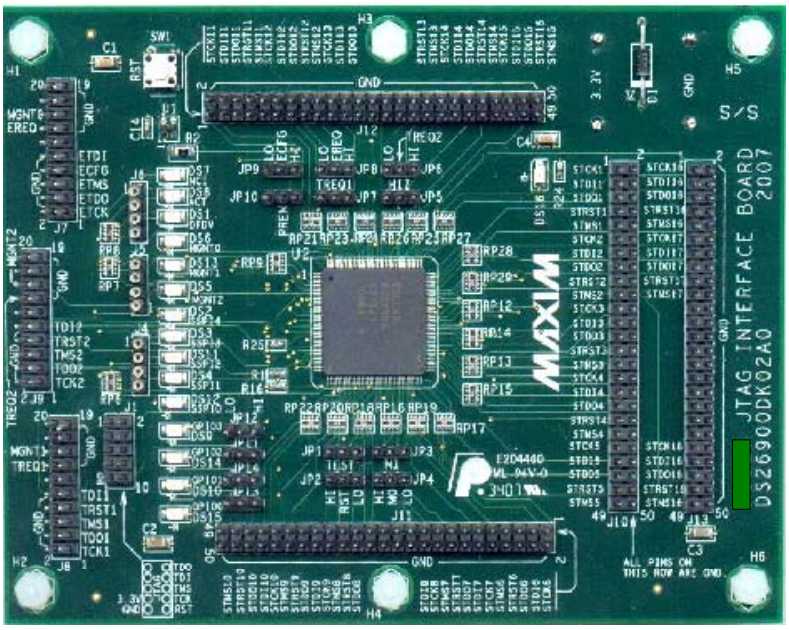
Features

- **Ribbon Cable Connectors for Master and Secondary JTAG Port Connections**
- **Jumpers for Device Configuration**
- **LEDs for Device State Outputs**
- **Simple Power Connections**

Ordering Information

PART	DESCRIPTION
DS26900DK	Demo kit for DS26900

DS26900 Demo Kit Layout



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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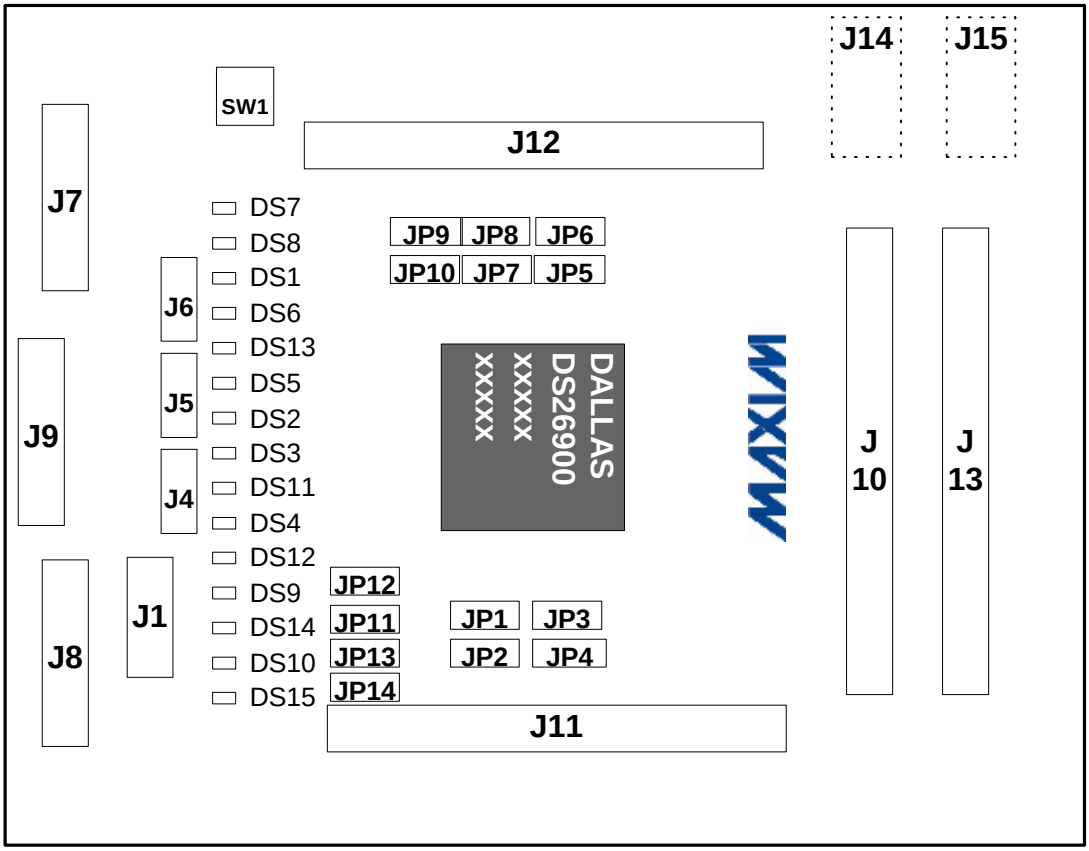
1. DS26900 Demo Kit PCB Layout

Figure 1-1 shows the location of the master and secondary JTAG ports, jumpers, power connectors, and reset switch.

Figure 1-1. DS26900 Demo Kit Board Floorplan



2. Operation

The simplest configuration to test for communication with the DS26900 demo kit is to connect a JTAG source to master port 1, connect power, and, using JTAG sequences, manipulate some of the device state output LEDs on the board. The SSPIx LEDs can be used to verify that the desired secondary port is being selected. The GPIOx LEDs can be observed to verify that the GPIO pins are being correctly selected. See Section 4 for the basic setup.

3. DS26900DK Connectors, Jumpers, and Indicators

See Figure 1-1 for location of connectors, switches, jumpers, and LED indicators described in this section. Refer to the DS26900 data sheet for a complete explanation of these device functions.

3.1 Power

The DS26900 demo kit is powered from a 3.3V supply. Two banana-type connectors are provided on the backside of the board, one for +3.3V and one for ground. See Table 3-3.

Table 3-1. Power Connections

CONNECTOR	FUNCTION
J14	+3.3V
J15	Ground

3.2 Reset

The reset pushbutton (SW1) controls the DS26900's $\overline{\text{RST}}$ input. Pushing this button provides an asynchronous reset for all the global registers and logic in the DS26900.

3.3 Device Status Outputs

The status of the following signals can be observed through LEDs on the board. Additionally, connectors J4, J5, and J6 are provided to make electrical connection for driving off-board circuitry.

3.3.1 Selected Secondary Port Indication

$\overline{\text{SSPI4}}$–$\overline{\text{SSPI0}}$ provide a binary indication as to which secondary port is currently selected in the manner described below.

4 3 2 1 0
1 1 1 1 1 = No secondary port selected
1 1 1 1 0 = Secondary port 1 selected
.
.
.
0 1 1 0 1 = Secondary port 18 selected

Table 3-2. $\overline{SSPI4}$–$\overline{SSPI0}$ Connections

CONNECTOR	FUNCTION
J6 - 4	$\overline{SSPI4}$
J4 - 1	$\overline{SSPI3}$
J4 - 2	$\overline{SSPI2}$
J4 - 3	$\overline{SSPI1}$
J4 - 4	$\overline{SSPI0}$

3.3.2 MGNT2–MGNT0

The MGNT2–MGNT0 outputs provide an indication as to which master port currently has control of the device as shown in Table 3-3.

Table 3-3. MGNT0–MGNT2 Connections

CONNECTOR	FUNCTION
J5 - 3	MGNT2
J5 - 2	MGNT1
J5 - 1	MGNT0

3.3.3 DPDV, $\overline{MCI}$, and $\overline{ACT}$

The signals DPDV, $\overline{MCI}$, and $\overline{ACT}$ provide indications of various device states as shown in Table 3-4.

Table 3-4. DPDV, $\overline{MCI}$, and $\overline{ACT}$ Connections

CONNECTOR	FUNCTION
J6 - 1	$\overline{MCI}$: LED ON when more than one of the $\overline{EREQ}$, $\overline{TMREQ1}$, or $\overline{TMREQ2}$ signals is asserted low.
J6 - 2	$\overline{ACT}$: LED ON when active. Active state is determined by the MSB of the instruction code and the state of the mode input pins M0 and M1, and the presence of an active master.
J6 - 3	**DPDV:** LED ON when the DPDV bit in the Device Configuration register is set = 1.

3.4 JTAG Port Connections

Table 3-5. JTAG Master Port Connectors

CONNECTOR	FUNCTION (MicroTCA™ JSM NOMENCLATURE)
J7	MASTER 3 (Extended Test Master)
J8	MASTER 1 (Test Master 1)
J9	MASTER 2 (Test Master 2)
J10	SECONDARY PORTS 1–5
J11	SECONDARY PORTS 6–10
J12	SECONDARY PORTS 11–15
J13	SECONDARY PORTS 16–18

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3.4.1 JTAG Master Connectors Pinouts

Connectors J7, J8, and J9 interface to the DS26900's three master ports. Some signals available at these connectors can be controlled dynamically from the connector or from jumpers. Table 3-6 indicates which signals have alternate jumpers. When driving a signal from the master port connectors the jumper can be removed or placed in a pullup or pulldown position determined by the method of driving the signal.

Table 3-6. J7, J8, and J9 Master Port Connector Pinouts

PIN	J7 EXTENDED TEST MASTER		J8 TEST MASTER 1		J9 TEST MASTER 2	
	SIGNAL	I/O	SIGNAL	I/O	SIGNAL	I/O
1	ETCK	I	TCK1	I	TCK2	I
2	GND	—	GND	—	GND	—
3	ETDO	0	TDO1	0	TDO2	0
4	GND	—	GND	—	GND	—
5	ETMS	I	TMS1	I	TMS2	I
6	GND	—	GND	—	GND	—
7	$\overline{\text{ECFG}}$ *	I	$\overline{\text{TRST1}}$	I	$\overline{\text{TRST2}}$	I
8	GND	—	GND	—	GND	—
9	ETDI	I	TDI1	I	TDI2	I
10	GND	—	GND	—	GND	—
11	N.C.	—	N.C.	—	N.C.	—
12	N.C.	—	N.C.	—	N.C.	—
13	GND	—	GND	—	GND	—
14	$\overline{\text{EREQ}}$ *	I	$\overline{\text{TMREQ1}}$*	I	$\overline{\text{TMREQ2}}$*	I
15	GND	—	GND	—	GND	—
16	$\overline{\text{MGNT0}}$	O	$\overline{\text{MGNT1}}$	O	$\overline{\text{MGNT2}}$	O
17	GND	—	GND	—	GND	—
18	N.C.	—	N.C.	—	N.C.	—
19	GND	—	GND	—	GND	—
20	N.C.	—	N.C.	—	N.C.	—

** Indicates that a jumper option is available for this signal.*

3.4.2 JTAG Secondary Port Connections

Table 3-7. Secondary Port Connections

PORT	CONNECTOR	SIGNALS	PIN
1	J10	STCK1	1
		STDI1	3
		STDO1	5
		$\overline{\text{STRST1}}$	7
		STMS1	9
2	J10	STCK2	11
		STDI2	13
		STDO2	15
		$\overline{\text{STRST2}}$	17
		STMS2	19
3	J10	STCK3	21
		STDI3	23
		STDO3	25
		$\overline{\text{STRST3}}$	27
		STMS3	29
4	J10	STCK4	31
		STDI4	33
		STDO4	35
		$\overline{\text{STRST4}}$	37
		STMS4	39
5	J10	STCK5	41
		STDI5	43
		STDO5	45
		$\overline{\text{STRST5}}$	47
		STMS5	49
6	J11	STCK6	1
		STDI6	3
		STDO6	5
		$\overline{\text{STRST6}}$	7
		STMS6	9
7	J11	STCK7	11
		STDI7	13
		STDO7	15
		$\overline{\text{STRST7}}$	17
		STMS7	19
8	J11	STCK8	21
		STDI8	23
		STDO8	25
		$\overline{\text{STRST8}}$	27
		STMS8	29
9	J11	STCK9	31
		STDI9	33
		STDO9	35
		$\overline{\text{STRST9}}$	37
		STMS9	39
10	J11	STCK10	41
		STDI10	43
		STDO10	45
		$\overline{\text{STRST10}}$	47
		STMS10	49
11	J12	STCK11	1
		STDI11	3
		STDO11	5
		$\overline{\text{STRST11}}$	7
		STMS11	9
12	J12	STCK12	11
		STDI12	13
		STDO12	15
		$\overline{\text{STRST12}}$	17
		STMS12	19
13	J12	STCK13	21
		STDI13	23
		STDO13	25
		$\overline{\text{STRST13}}$	27
		STMS13	29
14	J12	STCK14	31
		STDI14	33
		STDO14	35
		$\overline{\text{STRST14}}$	37
		STMS14	39
15	J12	STCK15	41
		STDI15	43
		STDO15	45
		$\overline{\text{STRST15}}$	47
		STMS15	49
16	J13	STCK16	1
		STDI16	3
		STDO16	5
		$\overline{\text{STRST16}}$	7
		STMS16	9
17	J13	STCK17	11
		STDI17	13
		STDO17	15
		$\overline{\text{STRST17}}$	17
		STMS17	19
18	J13	STCK18	41
		STDI18	43
		STDO18	45
		$\overline{\text{STRST18}}$	47
		STMS18	49

3.5 Jumpers and Indicators

Table 3-8. Jumpers

JUMPER	DEVICE PIN
JP1	TEST
JP2	$\overline{\text{RST}}$
JP3	M[1]
JP4	M[0]
JP5	$\overline{\text{HIZ}}$
JP6	$\overline{\text{TMREQ2}}$
JP7	$\overline{\text{TMREQ1}}$
JP8	$\overline{\text{EREQ}}$
JP9	PREN
JP10	$\overline{\text{ECFG}}$
JP11	GPIO[2]
JP12	GPIO[3]
JP13	GPIO[0]
JP14	GPIO[1]

Table 3-9. LED Indicators

LED	FUNCTION
DS1	DPDV
DS2	$\overline{\text{SSPI4}}$
DS3	$\overline{\text{SSPI3}}$
DS4	$\overline{\text{SSPI1}}$
DS5	$\overline{\text{MGNT2}}$
DS6	$\overline{\text{MGNT0}}$
DS7	$\overline{\text{MCI}}$
DS8	$\overline{\text{ACT}}$
DS9	GPIO[3]
DS10	GPIO[1]
DS11	$\overline{\text{SSPI2}}$
DS12	$\overline{\text{SSPI0}}$
DS13	$\overline{\text{MGNT1}}$
DS14	GPIO[2]
DS15	GPIO[0]
DS16	POWER

4. Sample Setup

4.1 Configure Device

Jumpers are used to configure the basic settings of the device.

Table 4-1. Jumper Settings for Single Package Mode of Operation

JUMPER	SETTING/FUNCTION
JP3, JP4	M[1:0] = 00: Configures device to single package mode
JP10	PREN = 1: Enables internal pull resistors
JP2	$\overline{RST}$ = 1: Enables switch SW1 to perform reset function
JP1	$\overline{TEST}$ = 1: Disable factory test mode
JP5	$\overline{HIZ}$ = 1: Disable output high-impedance mode

4.2 Select Master Port

The following signals can be controlled through jumper settings or from the J7, J8, and J9 master port connectors. If using the signals from the connectors, the jumpers may be removed or configured as pullup or pulldown resistors as needed.

Table 4-2. Using External Test Master as the Master Port

JUMPER	CONNECTOR PIN	SETTING/FUNCTION
JP8	J7 - 14	EREQ = 0: Selects external test master as the master port
JP10	J7 - 7	ECFG = 0: Enables Configuration Mode ECFG = 1: Enables Transparent (normal) Mode

Table 4-3. Using Test Master 1 as the master port

JUMPER	CONNECTOR PIN	SETTING/FUNCTION
JP8	J7 - 14	EREQ = 1: Deselects external test master as the master port
JP7	J8 - 14	TREQ1 = 0: Selects test master 1 as the master port
—	J8 - 7	TRST1 = 0: Enables Configuration Mode TRST1 = 1: Enables Transparent (normal) Mode

Table 4-4. Using Test Master 2 as the Master Port

JUMPER	CONNECTOR PIN	SETTING/FUNCTION
JP8	J7 - 14	EREQ = 1: Deselects external test master as the master port
JP7	J8 - 14	TREQ1 = 1: Deselects test master 1 as the master port
JP6	J9 - 14	TREQ2 = 0: Selects test master 2 as the master port
—	J9 - 7	TRST2 = 0: Enables Configuration Mode TRST2 = 1: Enables Transparent (normal) Mode

5. Additional Information/Resources

5.1 DS26900 Information

For more information about the DS26900, refer to the DS26900 data sheet at www.maxim-ic.com/DS26900.

5.2 DS26900DK Information

For more information about the DS26900DK including software downloads, refer to the DS26900DK Quick View page at www.maxim-ic.com/DS26900DK.

5.3 Technical Support

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

6. Schematics

The schematics are featured in the following 11 pages.

7. Document Revision History

REVISION DATE	DESCRIPTION
110107	Initial release.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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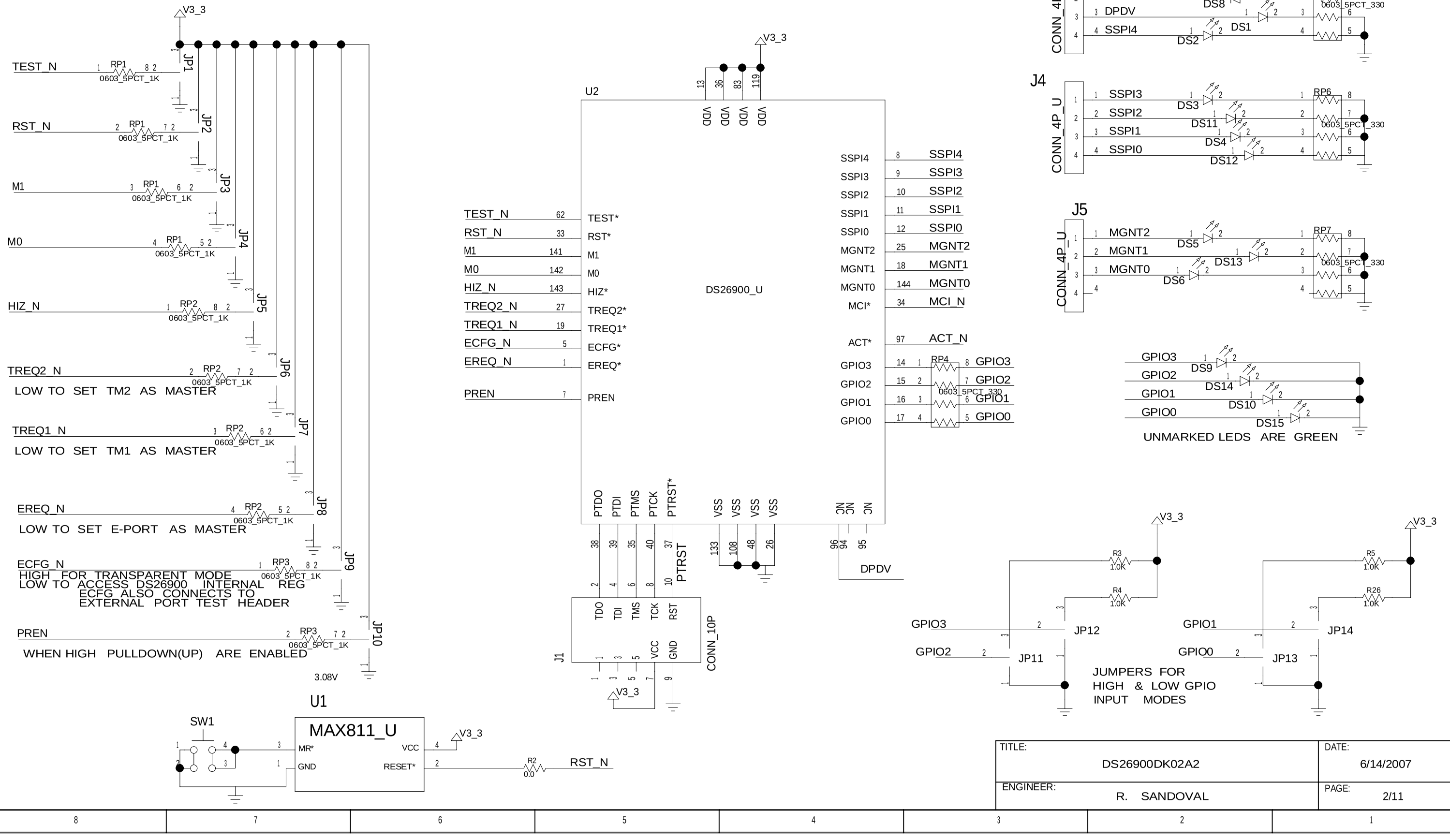
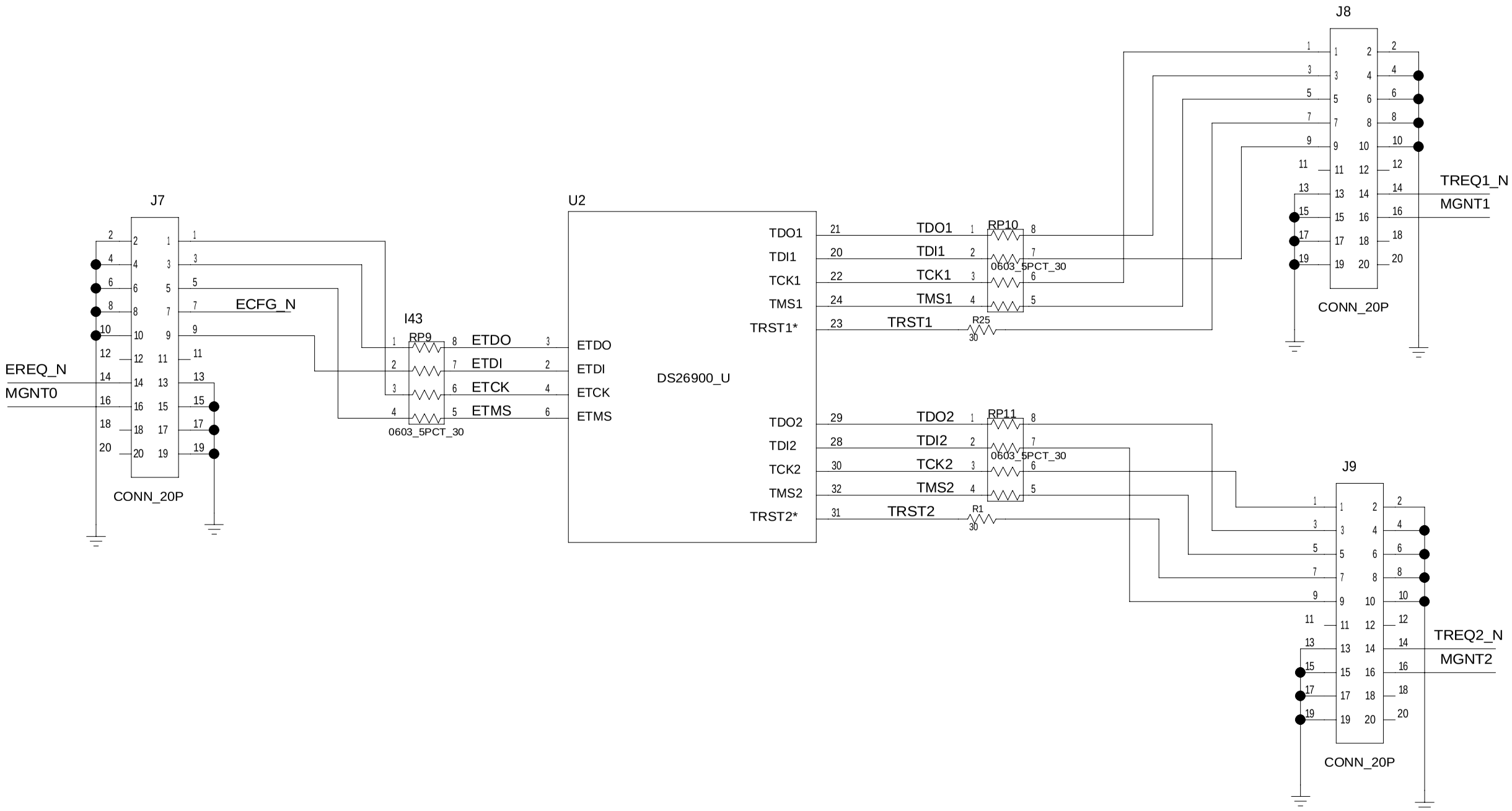
DS26900DK02A0

DS26900 JTAG INTERFACE BOARD

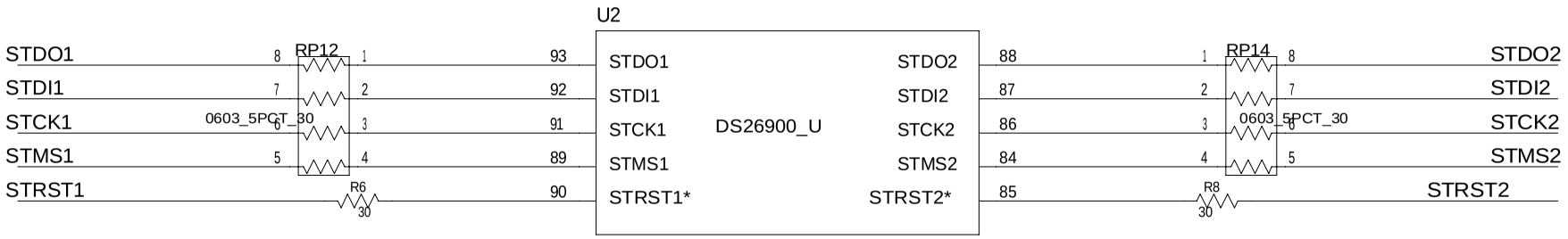
TITLE: DS26900DK02A2	DATE: 6/14/2007
ENGINEER: R. SANDOVAL	PAGE: 1/11

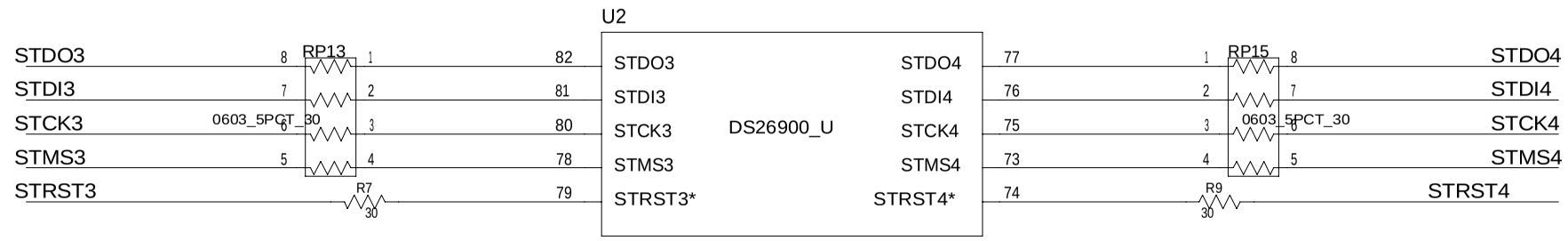


TITLE: DS26900DK02A2	DATE: 6/14/2007
ENGINEER: R. SANDOVAL	PAGE: 2/11

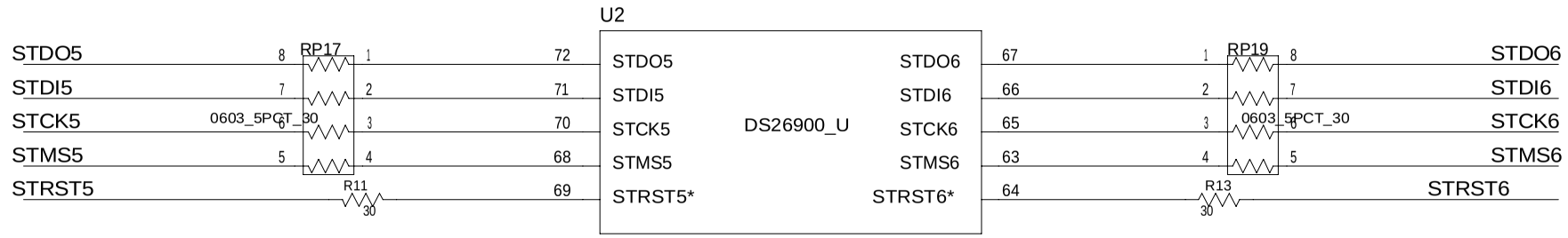


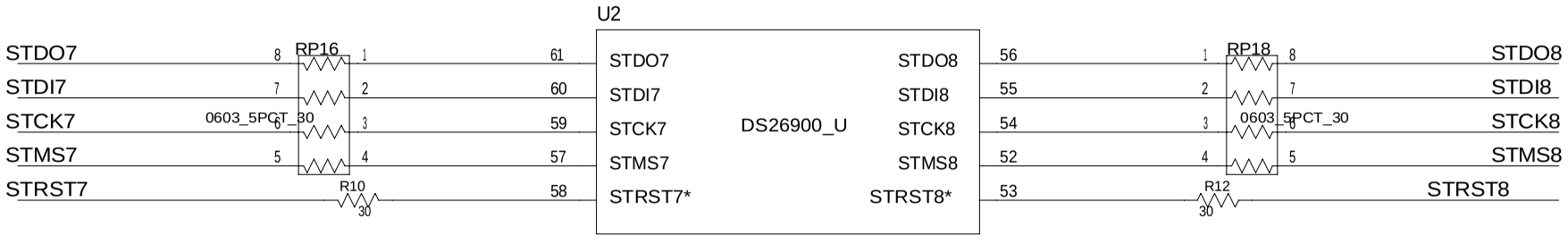
TITLE:	DATE:
DS26900DK02A2	06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 3/11



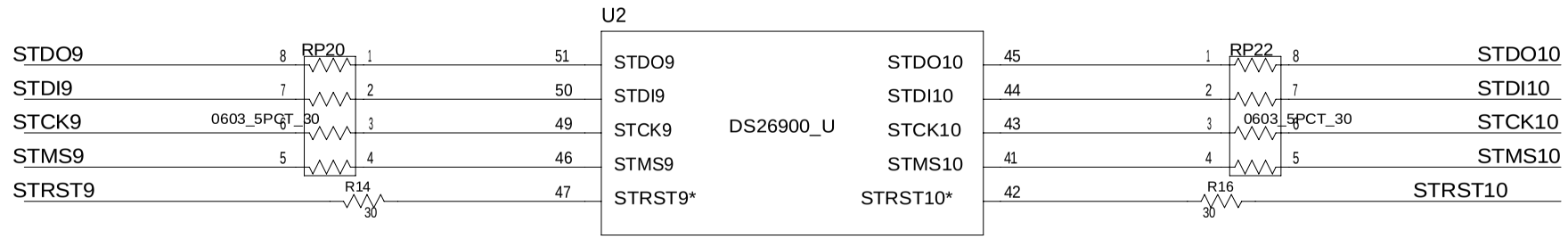


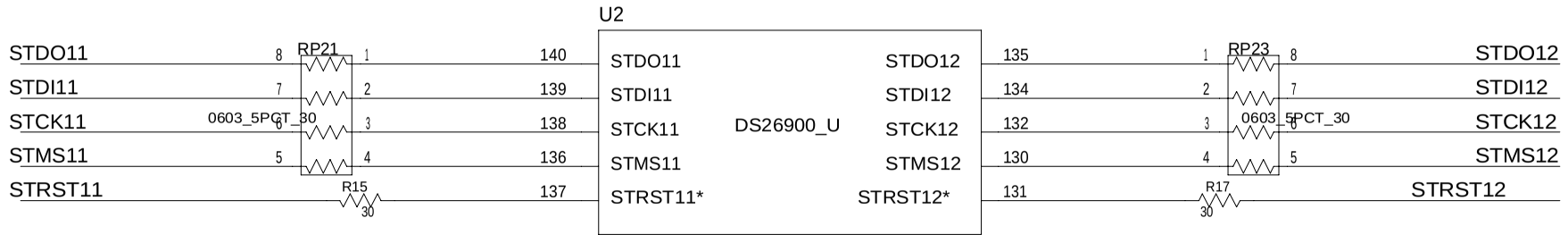
TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 4/11



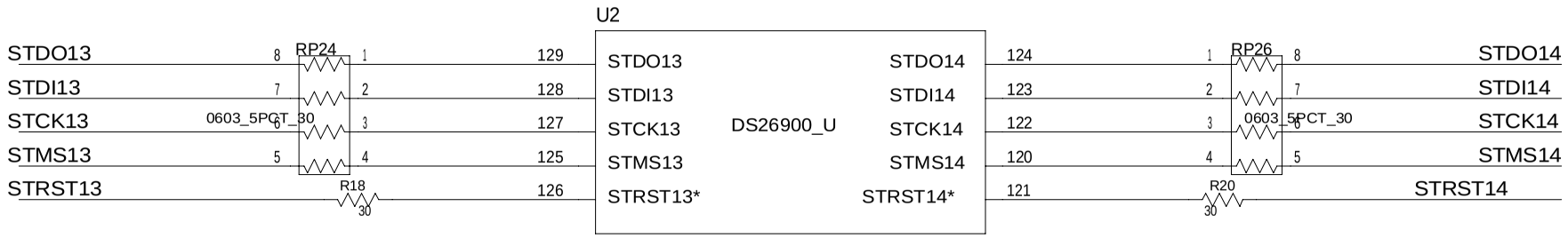


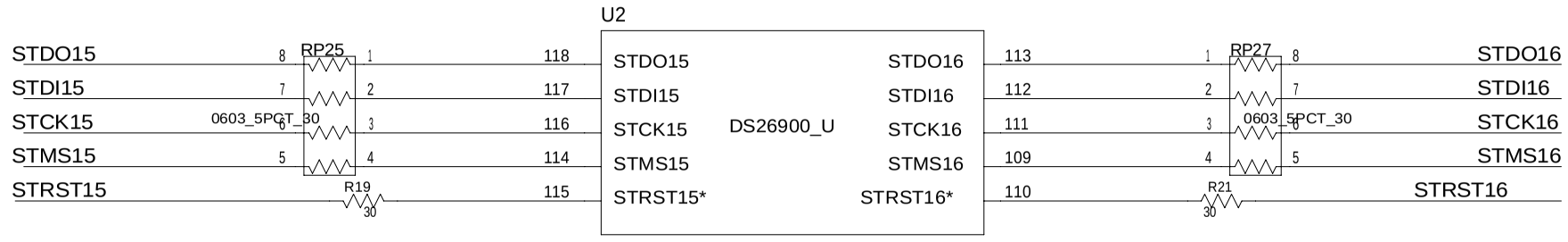
TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 5/11



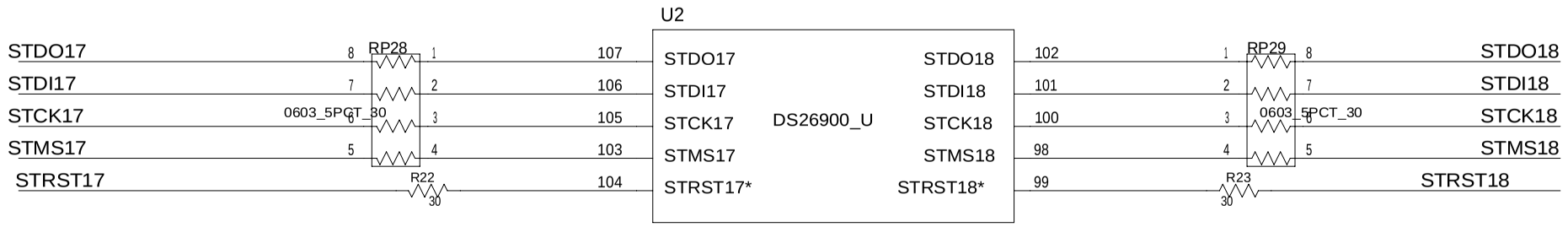


TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 6/11





TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 7/11



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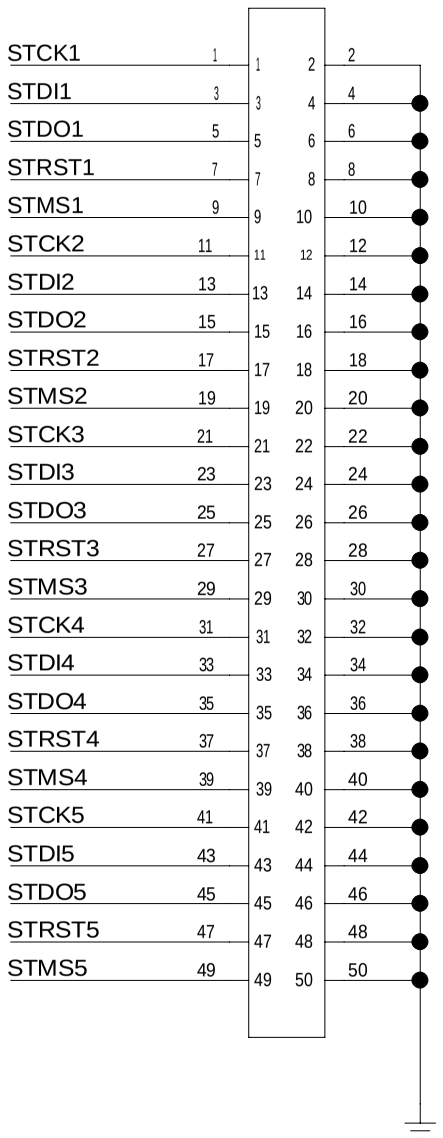
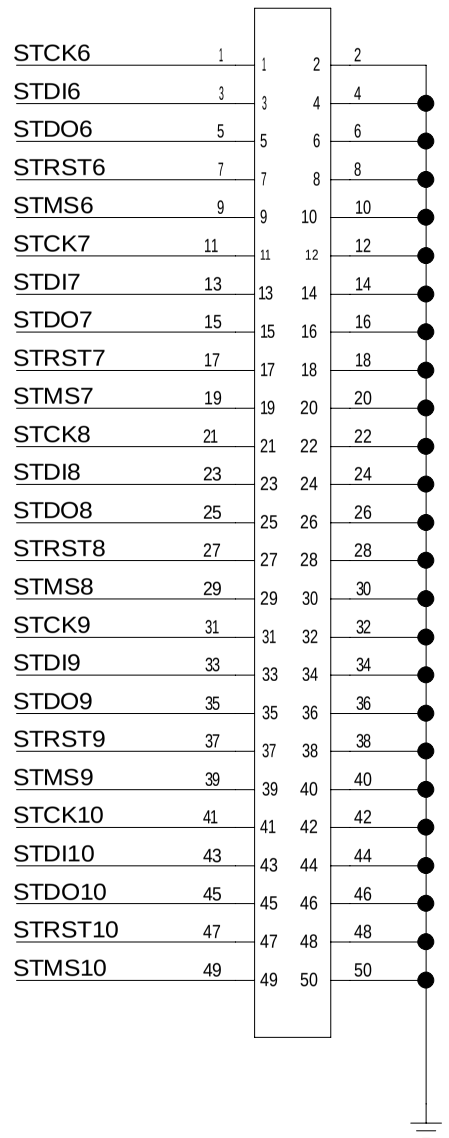
ENGINEER: ROGER SANDOVAL	PAGE: 8/11

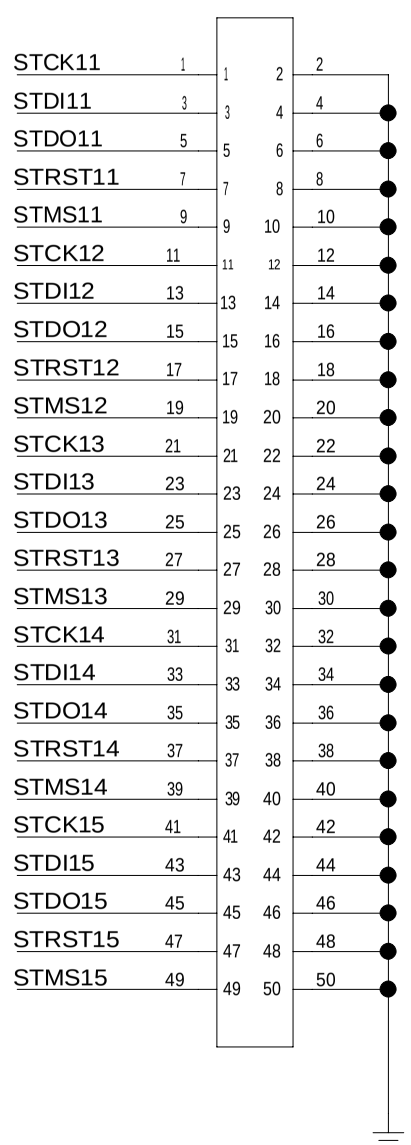
J10



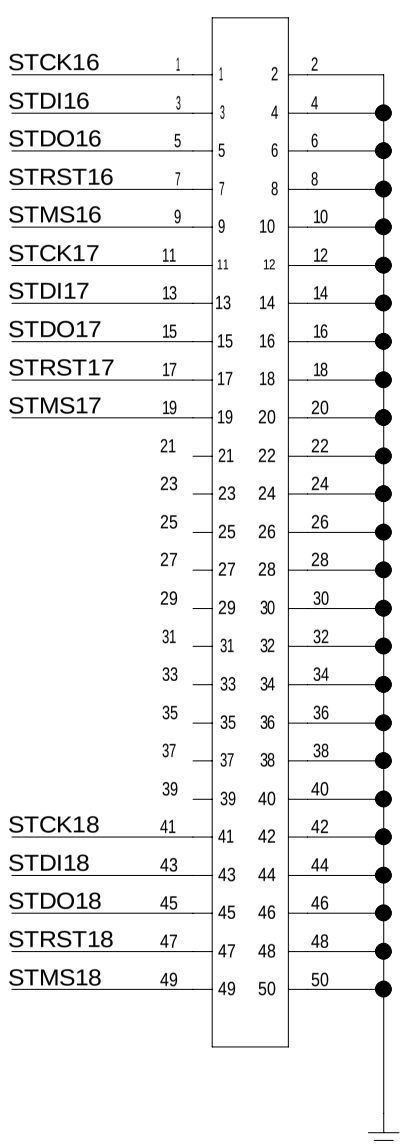
J11



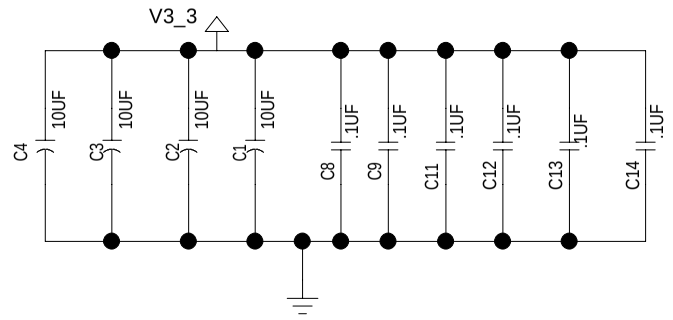
J12

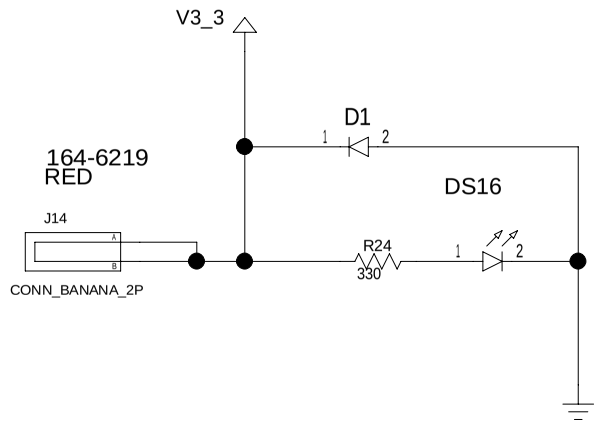


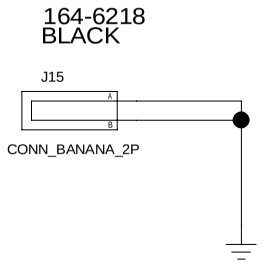
J13



TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 9/11







I94 H1
I92 H4
I90 H5
I95 H2
I93 H3
I91 H6

.50STANDOFF__NUT

TITLE: DS26900DK02A2	DATE: 06/14/2007
ENGINEER: ROGER SANDOVAL	PAGE: 10/11

REVISION HISTORY:

6/18/2007 - DISTRIBUTED 'A0' VERSION FOR REVIEW.

8/8/2007 - 'A1' - CORRECTED CONNECTION OF DS1 & DS2 - CATHODE TO GROUND.
FIXED THE 'TREQ1' & 'TREQ2' NETS, WHICH WERE INCORRECT IN INITIAL SKETCH.
ADDED HI/LO JUMPERS TO THE GPIO NETS SO THAT THE LED'S WILL LIGHT WHEN THE GPIO SIGNALS ARE HIGH IN BOTH THE INPUT AND THE OUTPUT MODES.

10/31/2007 - 'A2' - ADDED THE REVISION HISTORY PAGE. UPDATED PAGE NUMBERING.

TITLE: DS26900DK02A2		DATE: 06/14/2007	
ENGINEER: ROGER SANDOVAL		PAGE: 11/11	