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Evaluates: MAX14720/MAX14750

MAX14750 Evaluation System

General Description

The MAX14750 evaluation system (EV system) is a fully assembled and tested circuit for evaluating the MAX14720/MAX14750 power-management solutions with I²C capability for space-constrained, battery-powered applications. Both the MAX14720 and MAX14750 integrate a synchronous buck converter, a buck-boost converter, a linear regulator, and a power switch. The MAX14750 provides individual pin enables for each function, while the MAX14720 includes a push-button monitor and sequencing controller. Refer to the MAX14720/MAX14750 IC data sheet for detailed information regarding the operation and features of the devices.

The EV kit comes standard with the MAX14750A installed but can also be used to evaluate the MAX14720 by replacing the MAX14750A (U1) with the MAX14720. Request a free sample of the MAX14720 when ordering the EV kit.

Features

- USB-Power Option
- Flexible Configuration
- On-Board Battery Simulation
- Sense Test Point for Output-Voltage Measurement
- Windows 8[®]/Windows 10[®]-Compatible Graphical User Interface (GUI) Software
- Fully Assembled and Tested

EV Kit Contents

- MAXX14750_SYS_EVKIT_A system
- MAXPICO2PMB# board
- Two USB A to USB micro-B cables

Ordering Information appears at end of data sheet.



Figure 1. MAX14750 EV System Photo

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MAX14750 EV System Photo

MAX14750 EV Kit Files

FILE	DESCRIPTION
MAXPICO2PMBSetupVXXX.exe	PC GUI Program

Quick Start

Required Equipment

Note: In the following sections, software-related items are identified by **bold** text. Text in **bold** refers to items directly from the install of adapter board software. Text which is **bold and underlined** refers to items from the Windows operating system.

- MAX14750 EV system
- Windows PC with USB ports
- One USB A-to-USB micro-B cable and PICO2PMB adapter board with the latest firmware
- One USB A-to-USB micro-B cable or power supply (for battery simulation or battery voltage)
- One voltmeter

Procedure

The EV system is fully assembled and tested. Follow the steps below to verify board operation.

- Visit <u>https://www.maximintegrated.com</u> to download the latest version of the EV system software, MAXPICO2PMBSetupVXXX.exe located on the MAX14750 EV system web page. Download the EV system software to a temporary folder and unzip the zip file.
- Install the EV system software on the computer by running the MAXPICO2PMBSetupVXXX.exe program inside the temporary folder.

- 3) Verify that all jumpers are in their default positions, as shown in Table 1.
- 4) Make sure JP2 and JP14 are not installed until all connections have been verified.
- 5) Connect the type-A end of a cable to the PC and micro-USB end of a cable to the MAXPICO2PMB# board, and connect the MAXPICO2PMB# to J1 located on the lower left of the EV kit board.
- 6) Connect a USB A to micro-B cable from the computer to J2 on the upper right corner of the EV kit board to use VBUS to power the battery simulation circuits on the board, or power the battery simulation circuits from the VHC test point.
- Use a voltmeter to check VHC is approximately 5V; BATSIM test point is approximately 3.7V. To adjust the BATSIM voltage, turn the R58 BATSIM potentiometer.
- On the computer, open the MAXPICO2PMB Register Map Tool. The status bar on the bottom of the MAX-PICO2PMB Register Map Tool software shows Not Connected as shown in Figure 2.
- 9) Drag the MAX14720-50_Regmap.regmap to the MAXPICO2PMB Register Map Tool.
- 10) Alternative method to load the Regmap file:
- Click on the File menu, then Open Register File and select the appropriate directory by choosing Browse to load the MAX14720-50_Regmap.regmap.
- 12) Once the Regmap has been loaded, the device name and slave address appear on the window (See Figure 3).
- 13) Click **OK** and Regmap will be populated.
- 14) Reinstall JP2 and JP16 on the MAX14750_SYS_ EVKIT_A and the status of the EV kit tool now show **Connected**. Upon successful connection, the device info populates in the EV kit software (See Figure 4).

The Device	Options H	lelp									
Open Reg	ister File										
Exit										Deed All	
Register I	Лар									Read All	
Slave Address	Register Address	Register	Value	^	Field	Name			Descript	ion	
0x50	0x00	Register 0x00	0xFF		Bit[7:0]	REG_00		No descrip	tion.		_
0x50	0x01	Register 0x01	0x00								
0x50	0x02	Register 0x02	0x00								
0x50	0x03	Register 0x03	0x00								
0x50	0x04	Register 0x04	0x00								
0x50	0x05	Register 0x05	0x00								
0x50	0x06	Register 0x06	0x00								
0x50	0x07	Register 0x07	0x00								
0x50	0x08	Register 0x08	0x00								
0x50	0x09	Register 0x09	0x00								
0x50	0x0A	Register 0x0A	0x00								
0x50	0x0B	Register 0x0B	0x00								
0x50	0x0C	Register 0x0C	0x00								
0x50	0x0D	Register 0x0D	0x00	~							
7		6	5		4	3	2		1	0	
REG_00	[7] RE	G_00[6] REC	6_00[5]	R	EG_00[4]	REG_00[3]	REG_	00[2] F	EG_00[1]	REG_00[0]	
Nata: Olial	text to set a	or clear bit and "M	ite" to com	mit t	o device. Bo	ld text is logic 1	Degular	levt is logic (Rea	Mrite	
NOTO: L'IICI	lext to set t	i cieai bitaliu vvi	ite to com	i i iii c	o device. Do	iu text is logic 1.	Regular	lext is logic t	. Near	a wine	
Note: Clici											
Note: Clici										Not Conne	cted .
Mote: Clici	nister File					×				Not Conne	cted
Open Reg	gister File				-	×				Not Conne	cted .
Open Reg	gister File	1. D. (æ	×				Not Conne	cted .
Open Reg	gister File Register Fi	ile: Default			. Ip	×				Not Conne	cted
Open Reg Current Device 1	gister File Register Fi Name: I²C S	ile: Default Slave			œ	×				Not Conne	cted
Current Device I Slave Ac	jister File Register Fi Varne: I ² C \$ Idress: 0b0	ile: Default Slave 1101000 (0x50 V	Vrite / 0x5	1 Re	IP ead)	×				Not Conne	cted
Current Device I Slave Ac Select F	gister File Register Fi Vame: IPC S Idress: 0b0 Register File	ile: Default Slave 1101000 (0x50 V	Vrite / 0x5	1 Re	la ead) Browse	×				Not Conne	cted
Current Current Device I Slave Ac Select F Note: Sk	gister File Register Fil Name: I²C \$ Idress: 0b0 Register File ave addres	ile: Default Slave 1101000 (0x50 V e ses are shown a	Vrite / 0x5	1 Re	ead) Browse	×				Not Conne	cted .

Figure 2. Configuring the EV Kit Tool with MAXPICO2PMB Adapter Board

😡 Open Register File		×
Current Register File: MAX14720- Device Name: MAX14720/MAX147 Slave Address: 0b0101010 (0x55	50_Regmap.regmap 750 Write / 0x55 Read)	
Select Register File	Browse	
Note: Slave addresses are shown	as the 8-bit write address.	
	OK Cance	!

Figure 3. Click OK to Load the Register Map

Evaluates: MAX14720/MAX14750

le Device	Options H	elp							
egister Map									
Register M	lap							Read All	
Slave Address	Register Address	Register	Value	^ Field	Nam	e	Descrip	tion	
0x56	0x00	Chipld	0x01	Bit[7:0]	Chipld	abo	p_Id[7:0] bits show ut the version of the	Information	
0x56	0x01	ChipRev	0x00	Diffici	ompid	MAX	x14720/MAX14750.		
0x56	0x03	BoostCDiv	0x00						_
0x56	0x04	BoostlSet	0x00						
0x56	0x05	BoostVSet	0x00						
0x56	0x06	BoostCfg	0x00						
0x56	0x07	BuckVSet	0x00						
0x56	0x08	BuckCfg	0x00						
0x56	0x09	BucklSet	0x00						
0x56	0x0A	LDOVSet	0x00						
0x56	0x0B	LDOCfg	0x00						
0x56	0x0C	SwitchCfg	0x00						
0x56	0x0D	BatTime	0x00						
0x56	0x0E	BatCfg	0x00	~					
7		6	5	4	3	2	1	0	
Chipld[7] C	hipld[6] (Chipld[5]	Chipld[4]	Chipld[3]	Chipld[2]	Chipld[1]	Chipld[0]	
Note: Click	text to set o	r clear bit and "V	Vrite" to com	mit to device	Bold text is logic 1	Regular text is	logic 0 Rea	d Write	
NOLE. CILL	TEAT TO SET O		white to com	The to device.	Doid text is logic 1.	regular text is	Nea	u wille	

Figure 4. Regmap Populated and Status Shows Connected

Detailed Description of Software

Software Startup

After opening the application, make sure that **Connected** is shown in the status bar at the bottom of the window. If any other message is displayed, check all connections, and verify that the steps in the procedure section were followed in the correct order.

Buck Regulator

MAX14720

- 1) Register can be read and written by clicking the **Read** and **Write** button.
- 2) Click Read All button to refresh the register map.
- Connect DMM positive lead to TP12 (BIN) and negative lead to any GND test point.

- 4) Click on register address 0x08, BuckCfg.
- 5) To enable the Buck output, write 1 into bit 3 of register 0x08, BuckEn[0].
- Ensure that DMM is reading voltage 1.2V-1.8V (depending on MAX14750/14720 OTP) after the previous step and 0x08 register value changed from 0xE0 to 0xE8.

MAX14750

- 1) For MAX14750, the regulator must be enabled using JP4 jumper to pull BEN high.
- 2) Use a shunt to connect BEN_MPC to HI in JP4.
- The same procedure applies to LEN, HVEN, and SWEN.

gister Map	Options He	ip											
Register N	Лар									C	Rea	ad All	
Slave Address	Register Address	Register	Value	^	Field	1	lame	0.15.11.0	Descrip	tion			^
0x56	0x00	Chipld	0x01					000 = Disabled					
0x56	0x01	ChipRev	0x01					001 = Reserved					
0x56	0x03	BoostCDiv	0x00					010 = Enabled	010 = Enabled at 0% of Boot/POR Process Delay				
0x56	0x04	BoostlSet	0x02					Control 011 = Enabled at 25% of Reat/ROB Process Delay					
0x56	0x05	BoostVSet	0x07		Bit[7:5]	BuckSeg		Control	Control				
0x56	0x06	BoostCfg	0x40					100 = Enabled at 50% of Boot/POR Process Delay					
0x56	0x07	BuckVSet	0x20					Control	d				
0x56	0x08	BuckCfg	0xE0					101 = Reserved 110 = Controlled by BEN (MAX14750) 111 = Controlled by BuckEn [1:0] after 100% of					
0x56	0x09	BucklSet	0xA7										
0x56	0x0A	LDOVSet	0x09					Boot/POR Pro	cess Delay Cor	ntrol			
0x56	0x0B	LDOCfg	0xE1					Buck Enable Configuration (effective only when					
0x56	0x0C	SwitchCfg	0xE1					BUCKSeq[2:0] == 111) 00 = Disabled Active discharge behavior depends on					
0x56	0x0D	BatTime	0x00		Bit[4:3]	3] BuckEn		BuckActDsc.					
0x56	0x0E	BatCfg	0x00					01 = Enabled 10 = Enabled when MPC is high					
0x56	0x0F	BatV	0x00										
0x56	0x10	BatOCV	0x00			_		Ruck Mode Se	lact				1
0x56	0x11	BatLCV	0x00					00 = Burst mo	de				
0x56	0x19	MONCfg	0x00	~	Bit[2:1]	BuckMd		01 = Forced P	WM mode				~
	7	6		5	4	1	3	2	1		0		
	BuckSeq[2]	BuckSeq[1]	Buck	Seq[0	Buck	En[1]	BuckEn[0]	BuckMd[1]	BuckMd[0]	Buc	ckFst		
N	lote: Click tex	t to set or clear bit	and "Wri	ite" to	commit to d	evice. Bold	text is logic 1	. Regular text is I	ogic 0. Re	ead \	Write		

Figure 5. Enabling Buck Regulator

egister Map	options He	φ.									
Register M	lap						Read A	1			
Slave	Register Address	Register	Value	Field	Name	Description					
0x56	0x00	Chipld	0x01			Buck Enable Configuration (Read-Only)					
0x56	0x01	ChipRev	0x01			001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control					
0x56	0x03	BoostCDiv	0x00								
0x56	0x04	BoostlSet	0x02								
0x56	0x05	BoostVSet	0x07	Bit[7:5]	BuckSeg						
0x56	0x06	BoostCfg	0x40	Sufr.o)	Duchecq	100 = Enabled at 50% of B	oot/POR Process Delay				
0x56	0x07	BuckVSet	0x20			Control					
0x56	0x08	BuckCfg	0xE8			101 = Reserved 110 = Controlled by BEN (I	(AX14750)				
0x56	0x09	BucklSet	0xA7			111 = Controlled by BuckEn [1:0] after 100% of					
0x56	0x0A	LDOVSet	0x09			Boot/POR Process Delay Control					
0x56	0x0B	LDOCfg	0xE1			Buck Enable Configuration (effective only when BuckSeq[2:0] == 111) 00 = Disabled Active discharge behavior depends on					
0x56	0x0C	SwitchCfg	0xE1								
0x56	0x0D	BatTime	0x00	Bit[4:3]	BuckEn	BuckActDsc.					
0x56	0x0E	BatCfg	0x00			01 = Enabled					
0x56	0x0F	BatV	0x00			10 = Enabled when MPC is	MPC is high				
0x56	0x10	BatOCV	0x00	-		11 - Reserved		-			
0x56	0x11	BatLCV	0x00			Buck Mode Select					
0x56	0x19	MONCfg	0x00 v	Bit[2:1]	BuckMd	01 = Forced PWM mode		~			
	7	6	5		4 3	2 1	0				
	BuckSeq[2]	BuckSeq[1]	BuckSec	[0] Buc	kEn[1] BuckEn[0]	BuckMd[1] BuckMd	[0] BuckFst				
N	lote: Click tex	t to set or clear bit	and "Write"	to commit to	device. Bold text is logic	1. Regular text is logic 0.	Read Write				

Figure 6. Verifying Buck Regulator is Enabled

Evaluates: MAX14720/MAX14750

Detailed Description of Hardware

To use the EV kit with the EV kit software, connect the MAXPICO2PMB# to the PMOD connector in the bottom left corner of the board. The MAXPICO2PMB# also provides 3.3V to the logic voltage VIO of the EV kit when shunting JP2. Use the JP14 and JP1 USB VBUS to power the battery simulation circuits on the EV kit to supply BAT of the IC. Turning the R58 (BATSIM) potentiometer can change the BATSIM voltage. Connect BATSIM to VCC of the IC with shunt on JP1.

PFNs and MPCs States

The PFNs and MPCs can be pulled up to VIO through a 100 k Ω resistor or connected to ground through a 100 k Ω resistor.

The MAX14750 provides direct pin control of each function and allows greater flexibility for controlling sequencing. BEN, LEN, HVEN, and SWEN pins can be pulled up using the JP4-JP7 jumpers on the board. The MAX14720 includes a button monitor to power on the part and exit seal mode.

Regulators and Peripherals

All regulator outputs are made available on test points. The inputs to the HVIN, BIN, LIN, and SWIN must be supplied through JP9, JP10, JP11, and JP12, respectively.



Figure 7. MAX14750_SYS_EVKIT_A

Evaluates: MAX14720/MAX14750

Table 1. Jumper Table

JUMPER	SHUNT POSITION	MAX14750 DESCRIPTION	MAX14720 DESCRIPTION		
	1-2	Supplies VCC through VBUS			
JPT	2-3*	Supplies VCC through BATSIM			
JP2	1-2*	VIO connect to 3.3V from PMOD			
201	1-2	SDA connects to ground. Used to probe I ² C			
JF3	2-3	SCL connects to ground. Used to probe I ² C			
	1-2	BEN pulldown to ground	MPC pulldown to ground		
JP4	1-3	BEN connect to GPIO3	MPC connect to GPIO3		
	1-4	BEN pullup to VIO	MPC pullup to VIO		
	1-2	LEN pulldown to ground	RSTB pulldown to ground		
JP <u>5</u>	1-3	LEN connect to GPIO4	RSTB connect to GPIO4		
	1-4	LEN pullup to VIO	RSTB pullup to VIO		
	1-2	HVEN pulldown to ground	KOUT pulldown to ground		
JP6	1-3	HVEN connect to GPIO2	KOUT connect to GPIO2		
	1-4	HVEN pullup to VIO	KOUT pullup to VIO		
	1-2	SWEN pulldown to ground	KIN (PFN1) pulldown to ground		
JP7	1-3	SWEN connect to GPIO1	KIN (PFN1) connect to GPIO1		
	1-4	SWEN pullup to VIO	KIN (PFN1) pullup to VIO		
JP8	1-2**	Connects LEN to LED reset indicator	Connects RSTB to LED reset indicator		
JP9	1-2*	Supplies HVIN through VSYS			
JP10	1-2*	Supplies BIN through VSYS			
1011	1-2*	Supplies LIN through VSYS			
JEII	2-3	Supplies LIN through BOUT			
	1-2	Supplies SWIN through BOUT			
JP12	1-3	Supplies SWIN through VCC			
	1-4*	Supplies SWIN through VSYS			
1042	1-2*	Connects VSYS to VCC			
JF 1 <u>3</u>	2-3	Connects VSYS to SWOUT			
JP14	1-2*	VHC connect to USB VBUS			

*Default position.

**MAX14720 default position.

Table 2. Connectors Description

CONNECTOR	DESCRIPTION
J1	Connect to MAXPICO2PMB#
J2	Connect to the USB cable for battery simulation

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MAXPICO2PMB Firmware Update

This section covers the procedure to update the PICO2PMB adapter board with the latest firmware by programming a firmware image file (.bin) onto the on-board MAX32625PICO microcontroller.

- Put the board in maintenance mode by holding the button while the board is being connected to the computer. It may be easier to hold the button while inserting the USB cable at the computer end rather than the micro USB connector end (see Figure 8).
- 2) If the board enters bootloader mode successfully, the LED on the board turns red and the board appears to the computer as a USB drive named MAINTE-NANCE.
- 3) Drag and drop the firmware image file (.bin) into the MAINTENANCE drive and the board will install the new firmware.



Figure 8. Enter Maintenance Mode on the MAX32625PICO.

Ordering Information

FILE	DESCRIPTION
MAX14750EVSYS#	EV Kit

#Denotes RoHS compliance.

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MAX14750 EV System Bill of Materials

ITEM	REF_DES	DNI/DNP	QTY	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
	DATCINA TRA TRA 1440		-	5010	VENETONIE		TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN;
1	BATSIM, TP1-TP3, VHC	-	5	5010	KEYSTONE	N/A	BOARD HOLE=0.063IN; RED; PHOSPHOR BRONZE WIRE SIL;
	BIN S. BOUT S. HVIN S.		-				TEST POINT: PIN DIA=0.1IN: TOTAL LENGTH=0.3IN:
2	HVOUT S. TP4. TP5	-	6	5002	KEYSTONE	N/A	BOARD HOLE=0.04IN: WHITE: PHOSPHOR BRONZE WIRE SILVER:
				C1608X5R0J226M080AC:			
3	C1, C2, C6, C10	-	4	GRM188R60J226ME15	TDK;MURATA	22UF	CAP; SMT (0603); 22UF; 20%; 6.3V; X5R; CERAMIC
				ZRB15XR61A475ME01:			
				CL05A475MP5NRN:	MURATA:SAMSUNG:		
4	C3, C4, C7	-	3	GRM155R61A475MFAA	MURATA	4.7UF	CAP; SMT (0402); 4.7UF; 20%; 10V; X5R; CERAMIC
				C1005X5R1A475M050BC			
				C1005X7R1H104K050BB			
				GPM155R71H104K630BB,			
5	C5, C9	-	2	C100EV7D1U104KE14,		0.1UF	CAP; SMT (0402); 0.1UF; 10%; 50V; X7R; CERAMIC
					TAITO TODEN		
c	<u></u>		1	C2216VED104KV-FR	TDK	100115	CAD, SMT (1206), 100UE, 20%, 10V/, YED, CEDAMIC
0	634	-	1	C3210X5R1A10/W100AC		1000F	CAP, SIVIT (1200); 1000F; 20%; 10V; XSR; CERAIVIC
/	C24	-	1	C1608X5R1H104K080AA	IDR	0.10F	CAP; SMT (0603); 0.10F; 10%; 50V; X5R; CERAMIC
				C0603C225K9PAC;			
8	C26	-	1	GRM188R60J225KE01;	KEMET;MURATA;TDK	2.20F	CAP; SMT (0603); 2.2UF; 10%; 6.3V; X5R; CERAMIC;
				C1608X5R0J225K080AB			
				GRM31CR71H475KA12;			
				GRJ31CR71H475KE11;	MURATA;MURATA;		
9	C27	-	1	GXM31CR71H475KA10;	MURATA;TAIYO	4.7UF	CAP; SMT (1206); 4.7UF; 10%; 50V; X7R; CERAMIC
				UMK316AB7475KL;	YUDEN;MURATA		
				GRM31CR71H475KA12L			
10	C28	-	1	C0603C475K9PAC	KEMET	4.7UF	CAP; SMT (0603); 4.7UF; 10%; 6.3V; X5R; CERAMIC;
				C0402X7R500-222KNE;			
11	C29	-	1	GRM155R71H222KA01;	VENKEL LID.;	2200PF	CAP; SMT (0402); 2200PF; 10%; 50V; X7R; CERAMIC
				C1005X7R1H222K050BA	MURATA;TDK		
12	C30	-	1	C0603C104K8RAC	KEMET	0.1UF	CAP; SMT (0603); 0.1UF; 10%; 10V; X7R; CERAMIC
				C3216X5R1C476M160AB:			
13	C31	-	1	GRM31CR61C476ME44	IDK;MURATA	470F	CAP; SMT (1206); 47UF; 20%; 16V; X5R; CERAMIC
				C3216X5R1H106K160AB:			
14	C32	-	1	GRM31CR61H106KA12	TDK;MURATA	10UF	CAP; SMT (1206); 10UF; 10%; 50V; X5R; CERAMIC
15	C34	-	1	GRM188R60J105KA01	MURATA	1UF	CAP: SMT (0603): 1UF: 10%: 6.3V: X5R: CERAMIC:
						-	DIODE: LED: SMT (0603): Vf=1.7V: If(test)=0.002A:
16	DS3, DS10	-	2	LG L29K-G2J1-24	OSRAM	LG L29K-G2J1-24	-40 DEGC TO +100 DEGC
							CONNECTOR: MALE: THROUGH HOLE: BREAKAWAY:
17	J1	-	1	PBC06DBAN	SULLINS ELECTRONICS CORP.	PBC06DBAN	RIGHT ANGLE: 12PINS: 12PINS - ALTERNATE PIN NUMBERING
							CONNECTOR: MALE: SMT: MICRO UNIVERSAL
18	J2	-	1	ZX62D-B-5P8	HIROSE ELECTRIC CO LTD.	ZX62D-B-5P8	
19	JP1, JP3, JP11, JP13	-	4	PBC03SAAN	SULLINS	PBC03SAAN	STRAIGHT SPINS -65 DECC TO +125 DECC
┣───				ł			
20	JP2, JP8-JP10, JP14	-	5	PBC02SAAN	SULLINS ELECTRONICS CORP.	PBC02SAAN	CONNECTOR, WALE; THROUGH HULE; BREAKAWAT;
21	JP4-JP7, JP12	-	5	TSW-104-07-L-S	SAMTEC	TSW-104-07-L-S	EVKIT PART-CONNECTOR; MALE; THROUGH HOLE;
							ISW SERIES; SINGLE ROW; STRAIGHT; 4PINS
22	11	-	1	VLS201610E1-4R/M	IDK	4.7UH	INDUCTOR; SMT; WIREWOUND CHIP; 4.70H; TOL=+7-20%; 0.72A
23	LZ	-	1	5KP2010-2K2M	BOOKINS	2.2UH	INDUCTOR; SMT; POWDERED IRON CORE; 2.20H; TOL=+/-20%; 1.7A
24	MISC3	-	1	MAXPICO2PMB#	MAXIM	MAXPICO2PMB#	ACCESSORY; BRD; PACKOUT; MAXPICO2PMB ADAPTER BOARD
25	PB1	-	1	1825910-6	TE CONNECTIVITY	1825910-6	SWITCH; SPST; THROUGH HOLE; 24V; 0.05A; TACTILE SWITCH;
L		L	<u> </u>				RCOIL=0 OHM; RINSULATION=100M OHM; TE CONNECTIVITY
26	R1, R13, R15, R16	-	4	ERJ-2RKF1001	PANASONIC	1K	RES; SMT (0402); 1K; 1%; +/-100PPM/DEGC; 0.1000W
27	R2, R5, R10, R11,	-	7	CRCW040210K0FK;	VISHAY DALE;	10K	RES: SMT (0402): 10K: 1%: +/-100PPM/DEGC: 0.0630W
	R39, R49, R53		Ĺ	RC0402FR-0710KL	YAGEO PHICOMP		
28	R12, R42	-	2	CRCW0402499RFK	VISHAY DALE	499	RES; SMT (0402); 499; 1%; +/-100PPM/DEGC; 0.0630W
	R17, R18, R20, R23-R25,						
29	R34, R35, R45, R46,	-	13	ERJ-2GEJ104	PANASONIC	100K	RES; SMT (0402); 100K; 5%; +/-200PPM/DEGC; 0.1000W
	R48, R50, R57			<u> </u>			
30	R51	-	1	ERJ-2GE0R00	PANASONIC	0	RES; SMT (0402); 0; JUMPER; JUMPER; 0.1000W

Evaluates: MAX14720/MAX14750

MAX14750 EV System Bill of Materials (continued)

ITEM	REF_DES	DNI/DNP	QTY	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
31	R52	-	1	ERJ-2RKF5100	PANASONIC	510	RES; SMT (0402); 510; 1%; +/-100PPM/DEGC; 0.1000W
32	R54, R56	-	2	WSL0805R1000FEA18	VISHAY DALE	0.1	RES; SMT (0805); 0.1; 1%; +/-75PPM/DEGC; 0.1250W
							RESISTOR; THROUGH-HOLE-RADIAL LEAD; 3296 SERIES; 25K OHM;
33	R58	-	1	3296Y-1-253LF	BOURNS	25K	10%; 100PPM; 0.5W; SQUARE TRIMMING POTENTIOMETER;
							25 TURNS; MOLDER CERAMIC OVER METAL FILM
34	R59	-	1	ERJ-2RKF1152	PANASONIC	11.5K	RES; SMT (0402); 11.5K; 1%; +/-100PPM/DEGC; 0.1000W
25			4	0022	KEVETONE	0033	MACHINE FABRICATED; ROUND-THRU HOLE SPACER;
35	SPACERI-SPACER4	-	4	9052	RETSTONE	9052	NO THREAD; M3.5; 5/8IN; NYLON
26			14	S1100-B;SX1100-B;	KYCON;KYCON;	CV(1100 D	TEST POINT; JUMPER; STR; TOTAL LENGTH=0.24IN; BLACK;
30	501-5014	-	14	STC02SYAN	SULLINS ELECTRONICS CORP.	SX1100-B	INSULATION=PBT;PHOSPHOR BRONZE CONTACT=GOLD PLATED
							TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN;
37	TP6-TP13	-	8	5003	KEYSTONE	N/A	BOARD HOLE=0.04IN; ORANGE; PHOSPHOR BRONZE WIRE
							SILVER PLATE FINISH;
							TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN;
38	TP14	-	1	5000	KEYSTONE	N/A	BOARD HOLE=0.04IN; RED; PHOSPHOR BRONZE WIRE
							SILVER PLATE FINISH;
							TEST POINT; PIN DIA=0.125IN; TOTAL LENGTH=0.445IN;
39	TP20-TP24	-	5	5011	KEYSTONE	N/A	BOARD HOLE=0.063IN; BLACK; PHOSPHOR BRONZE WIRE
							SILVER PLATE FINISH;
							TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN;
40	TP25-TP30	-	6	5001	KEYSTONE	N/A	BOARD HOLE=0.04IN; BLACK; PHOSPHOR BRONZE
							WIRE SILVER PLATE FINISH;
41	U1	-	1	MAX14750AEWA+	MAXIM	MAX14750AEWA+	IC; PWRM; POWER-MANAGEMENT SOLUTION; WLP25
42	112		1				IC; AMP; RAIL-TO-RAIL I/O; POWER AMPLIFIER;
42	02	-	1	OFAJOJAIDWER	TEXAS INSTRUMENTS	OFA309AID WFK	WSOIC20-EP 300MIL
12	112		1				IC; VREG; ULTRA-LOW-IQ LOW-DROPOUT LINEAR
45	03	-	Т	WIAX000UEUT+		WIAX8880E01+	REGULATOR WITH POK; SOT23-6
44	U4	-	1	NC7WZ07P6X	FAIRCHILD SEMICONDUCTOR	NC7WZ07P6X	IC; BUF; TINY LOGIC ULTRA-HIGH SPEED DUAL BUFFER; SC70-6
45	PCB	-	1	MAX14750SYS	MAXIM	PCB	PCB:MAX14750SYS
46	MISC1, MISC2	DNI	2	AK67421-0.5	ASSMANN	AK67421-0.5	CONNECTOR; USB CABLE; MALE-MALE; USB_2.0; 5PINS-4PINS; 500MM
TOTAL			129				

Evaluates: MAX14720/MAX14750

MAX14750 EV System Schematics



Evaluates: MAX14720/MAX14750

MAX14750 EV System Schematics (continued)



Evaluates: MAX14720/MAX14750



MAX14750 EV System Schematics (continued)



MAX14750 EV System Schematics (continued)

Evaluates: MAX14720/MAX14750



MAX14750 EV System PCB Layouts

MAX14750 EV System Component Placement Guide—Top Silkscreen



MAX14750 EV System PCB Layout—Top



MAX14750 EV System PCB Layout—Internal2

Evaluates: MAX14720/MAX14750



MAX14750 EV System PCB Layouts (continued)

MAX14750 EV System PCB Layout—Internal3



MAX14750 EV System PCB Layout—Bottom

Evaluates: MAX14720/MAX14750

Revision History

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	12/21	Initial release	_



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