Click here to ask an associate for production status of specific part numbers.

Ultra-Small, High Accuracy, Adjustable Sequencing/Supervisory Circuits

MAX16895—MAX16899

General Description

The MAX16895—MAX16899 is a family of small, low power, voltage-monitoring circuits with sequencing capability. These miniature devices offer tremendous flexibility with an adjustable threshold capable of monitoring down to 0.5V and an external capacitor-adjustable time delay. These devices are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

A high-impedance input with a 0.5V threshold allows an external resistive divider to set the monitored threshold. The output asserts (OUT = high or OUT = low) when the input voltage rises above the 0.5V threshold and the enable input is asserted (ENABLE = high or ENABLE = low). When the voltage at the input falls below 0.5V or when the enable input is deasserted (ENABLE = low or ENABLE = high), the output deasserts (OUT = low or OUT = high). All devices provide a capacitor-programmable delay time from when the input rises above 0.5V to when the output is asserted. The MAX1689_A versions provide the same capacitor-adjustable delay from when enable is asserted to when the output asserts. The MAX1689_P devices have a 150ns propagation delay from when enable is asserted to when the output asserts.

The MAX16895A/P offers an active-high enable input and an active-high push-pull output. The MAX16896A/P offers an active-low enable input and an active-low push-pull output. The MAX16897A/P offers an active high enable input and an active-high open-drain output. Finally, the MAX16898A/P offers an active-low enable input and an active-low open-drain output. The MAX16899A/P offers an active-low enable with an active high push-pull output.

All devices operate from a 1.5V to 5.5V supply voltage and are fully specified over the -40°C to +125°C operating temperature range. These devices are available in ultra-small 6-pin µDFN (1.0mm x 1.5mm) and thin SOT23 (1.60mm x 2.90mm) packages.

Features

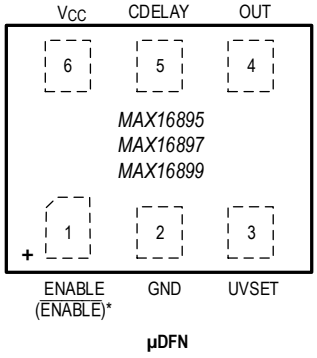
- 1% Accurate Adjustable Threshold Over Temperature
- Operate from V_{CC} of 1.5V to 5.5V
- Capacitor-Adjustable Delay
- Active-High/Low Enable Input Options
- Active-High/Low Output Options
- Open-Drain (28V Tolerant)/Push-Pull Output Options
- Low Supply Current (10µA, typ)
- Fully Specified from -40°C to +125°C
- Ultra-Small 6-Pin µDFN Package or Thin SOT23 Package

Applications

- Medical Equipment
- Intelligent Instruments
- Portable Equipment
- Computers/Servers
- Critical µP Monitoring
- Set-Top Boxes
- Telecom

***Ordering Information*, Typical Operating Circuit, and Selector Guide appear at end of data sheet.**

Pin Configurations



µDFN

( ) Only for MAX16899

19-101215; Rev 1; 1/22

Absolute Maximum Ratings

V_{CC}, ENABLE, ENABLE, UVSET .....-0.3V to +6V

OUT, OUT (Push-pull) .....-0.3V to V_{CC} + 0.3V

OUT, OUT (Open-drain).....-0.3V to +30V

CDELAY.....-0.3V to V_{CC} + 0.3V

Output Current (all pins) ..... ±20mA

Continuous Power Dissipation (T_A = +70°C, 6-Pin µDFN, (derate 2.1mW/°C above +70°C)..... 167.7mW

Continuous Power Dissipation (T_A = +70°C, 6-Pin Thin SOT23, (derate 9.1mW/°C above +70°C)..... 727.3mW

Operating Temperature Range .....-40°C to +125°C

Storage Temperature Range.....-65°C to +150°C

Junction Temperature .....+150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 µDFN

Package Code	L611+1C
Outline Number	*21-0147*
Land Pattern Number	*90-0080*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	477°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	122°C/W

6 Thin SOT23

Package Code	Z6+1
Outline Number	*21-0114*
Land Pattern Number	*90-0242*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	110°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	50°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.*

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial*.*

Electrical Characteristics

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted (*Note 1*).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Operating Voltage Range	V_{CC}		1.5		5.5	V
Undervoltage Lockout (*Note 2*)	UVLO	V_{CC} falling	1.05		1.39	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 3.3V, no load		10	20	µA
UVSET						
Threshold Voltage	V_{TH}	V_{UVSET} rising, 1.5V < V_{CC} < 5.5V	0.495	0.5	0.505	V
Hysteresis	V_{HYST}	V_{UVSET} falling		5		mV
Input Current (*Note 3*)	I_{IN}	V_{UVSET} = 0V or 600mV	-15		+15	nA
CDELAY						
Delay Charge Current	I_{CD}		200	250	300	nA
Delay Threshold	V_{TCD}	CDELAY rising	0.95	1.00	1.05	V
CDELAY Pulldown Resistance	R_{CDELAY}			130	500	Ω
ENABLE/ENABLE						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		1.4			V
Input Leakage Current	I_{LEAK}	ENABLE, ENABLE = V_{CC} or GND	-100		+100	nA
OUT/OUT						
Output Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90µA, MAX16895/MAX16897/MAX16899 only			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA			0.4	
Output High Voltage (Push-Pull)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA	0.8 x V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			
Output Open-Drain Leakage Current (Open-Drain)	I_{LKG}	Output high impedance, V_{OUT} = 28V			1	µA
TIMING						
UVSET to OUT/ OUT Propagation Delay	t_{DELAY}	V_{UVSET} rising, C_{CDELAY} = 0µF		40		µs
		V_{UVSET} rising, C_{CDELAY} = 0.047µF		190		ms
UVSET to OUT/ OUT Propagation Delay	t_{DL}	V_{UVSET} falling overdrive = 20mV		16		µs
Startup Delay (*Note 4*)				2		ms
ENABLE/ENABLE Minimum Input Pulse Width	t_{PW}		1			µs
ENABLE/ ENABLE Glitch Rejection				100		ns
ENABLE/ ENABLE to OUT/ OUT Delay	t_{OFF}	From device enabled to device disabled		150		ns

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted (*Note 1*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE/ ENABLE to OUT/ OUT Delay	t_{PROPP}	From device disabled to device enabled (P version)			150		ns
	t_{PROPA}	From device disabled to device enabled (A version)	C_{CDELAY} = 0µF		16		µs
			C_{CDELAY} = 0.047µF		190		ms

Note 1: All devices are production tested at T_A = +25°C. Limits over temperature are guaranteed by design

Note 2: When V_{CC} falls below the $UVLO_{MAX}$ (1.39V), the outputs deassert (OUT goes low, OUT goes high); when V_{CC} falls below $UVLO_{MIN}$ (1.05V), the outputs cannot be determined

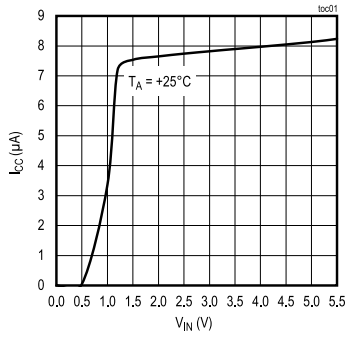
Note 3: Guaranteed by design

Note 4: During the initial power-up, V_{CC} must exceed 1.5V for at least 2ms before the output is guaranteed to be in the correct state

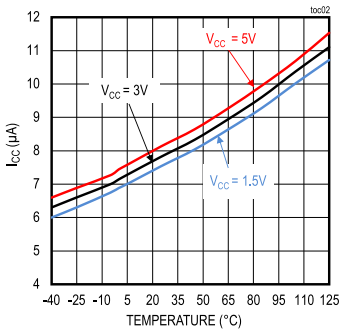
Typical Operating Characteristics

(V_{CC} = 3.3V and T_A = +25°C, unless otherwise noted.)

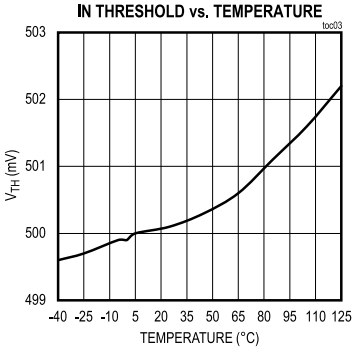
SUPPLY CURRENT vs. SUPPLY VOLTAGE



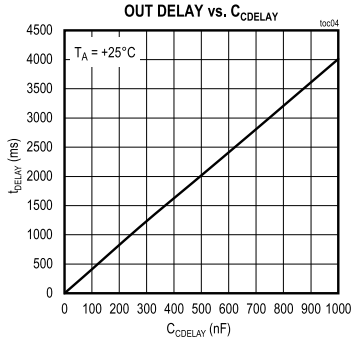
SUPPLY CURRENT vs. TEMPERATURE



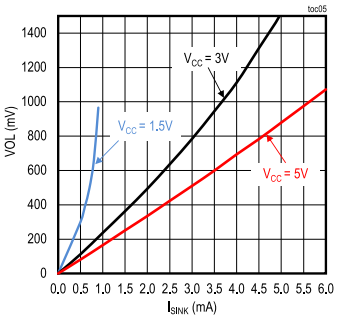
IN THRESHOLD vs. TEMPERATURE



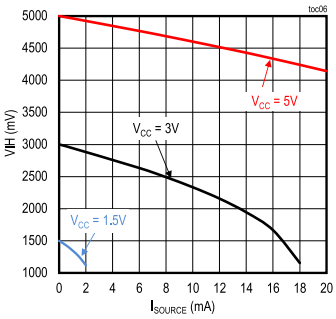
OUT DELAY vs. C_{CDELAY}



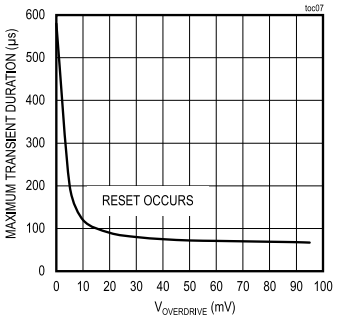
OUTPUT LOW VOLTAGE vs. SINK CURRENT



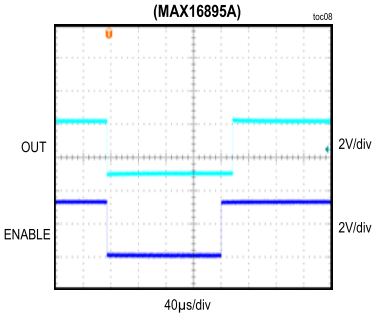
OUTPUT LOW VOLTAGE vs. SINK CURRENT



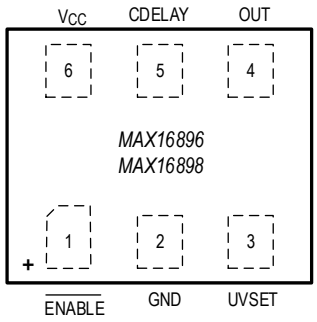
MAXIMUM TRANSIENT DURATION vs. INPUT OVERDRIVE



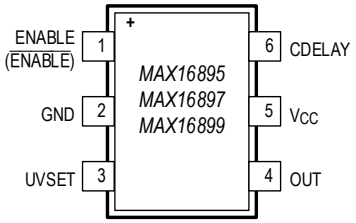
ENABLE TURN-ON/OFF DELAY (MAX16895A)



Pin Configurations

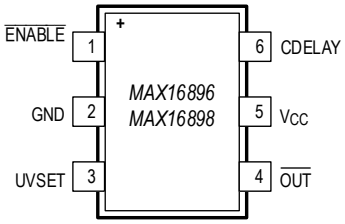


µDFN



THIN SOT23

( ) Only for MAX16899



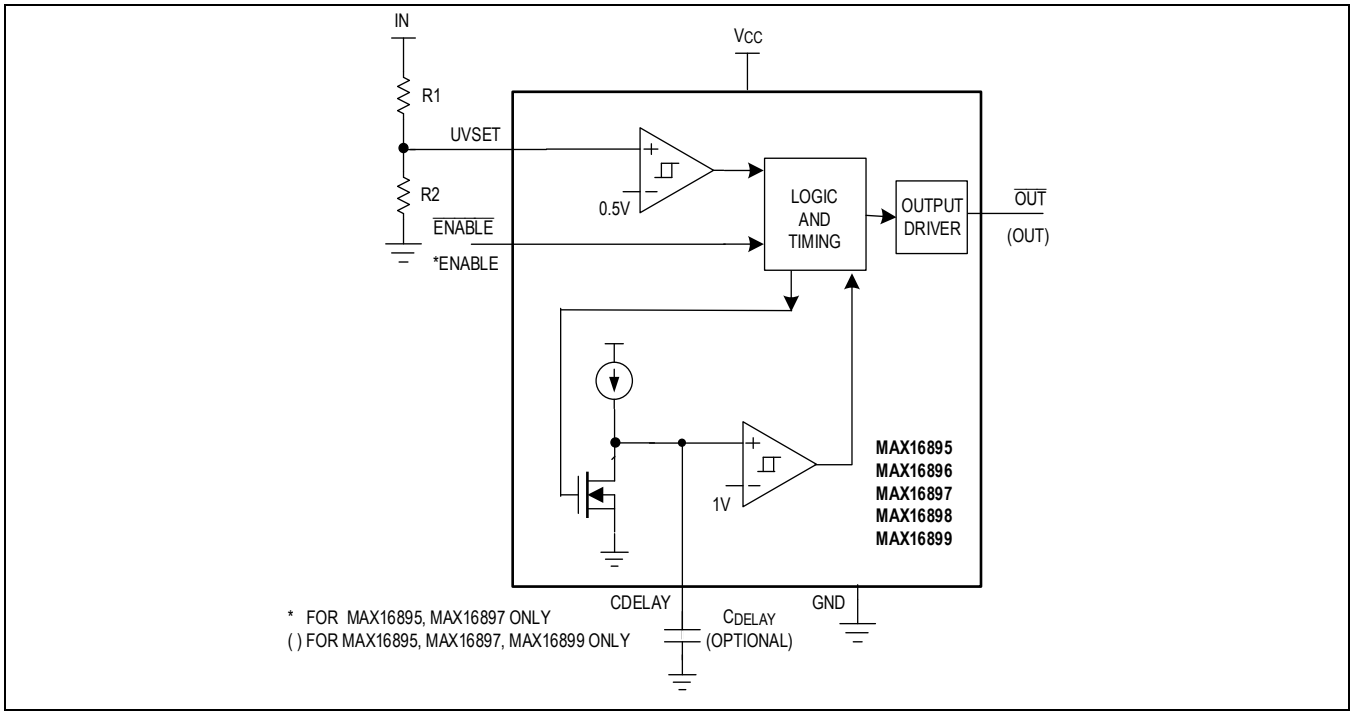
THIN SOT23

Pin Descriptions

PIN						NAME	FUNCTION
MAX16895/ MAX16897 µDFN	MAX16895/ MAX16897 THIN SOT23	MAX16896/ MAX16898 µDFN	MAX16896/ MAX16898 THIN SOT23	MAX16899 µDFN	MAX16899 THIN SOT23		
1	1	—	—	—	—	ENABLE	Active-High Logic-Enable Input. Drive ENABLE low to immediately deassert the output to its false state (OUT = low or OUT = high) independent of V_{UVSET}. With V_{UVSET} above V_{TH}, drive ENABLE high to assert the output to its true state (OUT = high or OUT = low) after the adjustable delay period (MAX1689_A) or a 150ns propagation delay (MAX1689_P).
—	—	1	1	1	1	ENABLE	Active-Low Logic-Enable Input. Drive ENABLE high to immediately deassert the output to its false state (OUT = low or OUT = high) independent of V_{UVSET}. With V_{UVSET} above V_{TH}, drive ENABLE low to assert the output to its true state (OUT = high or OUT = low) after the adjustable delay period (MAX1689_A) or a 150ns propagation delay (MAX1689_P).
2	2	2	2	2	2	GND	Ground
3	3	3	3	3	3	UVSET	High-Impedance Monitor Input. Connect UVSET to an external resistive divider to set the desired monitored threshold. The output changes state when V_{UVSET} rises above 0.5V and when V_{UVSET} falls below 0.495V.
4	4	—	—	4	4	OUT	Active-High Sequencer/Monitor Output, Push-Pull (MAX16895/MAX16899) or Open-Drain (MAX16897). OUT is asserted to its true state (OUT = high) when V_{UVSET} is above V_{TH} and the enable input is in its true state (ENABLE = high or ENABLE = low) for the capacitor- adjusted delay period. OUT is deasserted to its false state (OUT = low) immediately after V_{UVSET} drops below V_{TH} - 5mV or the enable input is in its false state (ENABLE = low or ENABLE = high). The open-drain version requires an external pullup resistor.
—	—	4	4	—	—	OUT	Active-Low Sequencer/Monitor Output, Push-Pull (MAX16896) or Open-Drain (MAX16898). OUT is asserted to its true state (OUT = low) when V_{UVSET} is above V_{TH}

							and the enable input is in its true state (ENABLE = high or ENABLE = low) after the CDELAY adjusted timeout period. OUT is deasserted to its false state (OUT = high) immediately after V_{UVSET} drops below V_{TH} - 5mV or the enable input is in its false state (ENABLE = low or ENABLE = high). The open-drain version requires an external pullup resistor.
5	6	5	6	5	6	CDELAY	Capacitor-Adjustable Delay. Connect an external capacitor (C_{CDELAY}) from CDELAY to GND to set the UVSET to OUT (and ENABLE to OUT or ENABLE to OUT for A version devices) delay period. t_{DELAY} = (C_{CDELAY} x 4.0 x 10^6) + 40µs. There is a fixed short delay (16µs, typ) for the output deasserting when V_{UVSET} falls below V_{TH}.
6	5	6	5	6	5	V_{CC}	Supply Voltage Input. Connect a 1.5V to 5.5V supply to V_{CC} to power the device. For noisy systems, bypass with a 0.1µF ceramic capacitor to GND.

Functional Diagrams



Detailed Description

The MAX16895–MAX16899 is a family of ultra-small, low- power, sequencing/supervisory circuits. These devices provide adjustable voltage monitoring for inputs down to 0.5V. They are ideal for use in power-supply sequencing, reset sequencing, and power-switching applications. Multiple devices can be cascaded for complex sequencing applications.

Voltage monitoring is performed through a high-impedance input (UVSET) with an internally fixed 0.5V threshold. When the voltage at UVSET falls below 0.495V (include hysteresis) or when the enable input is deasserted (ENABLE = low or ENABLE = high), the output deasserts (OUT goes low or OUT goes high). When V_{UVSET} rises above 0.5V and the enable input is asserted (ENABLE = high or ENABLE = low), the output asserts (OUT goes high or OUT goes low) after a capacitor-programmable time delay.

With V_{UVSET} above 0.5V, the enable input can be used to turn the output on or off. After the enable input is asserted, the output turns on with a capacitor-programmable delay period (A version) or with a 150ns propagation delay (P version). Tables 1, 2, and 3 detail the output state depending on the various input and enable conditions.

Table 1. MAX16895/MAX16897 Output

UVSET	ENABLE	OUT
$V_{UVSET} < V_{TH}$	Low	Low
$V_{UVSET} < V_{TH}$	High	Low
$V_{UVSET} > V_{TH}$	Low	Low
$V_{UVSET} > V_{TH}$	High	OUT = VCC (MAX16895)
		OUT = high Impedance (MAX16897)

Table 2. MAX16896/MAX16898 Output

UVSET	ENABLE	OUT
$V_{UVSET} < V_{TH}$	Low	OUT = VCC (MAX16896)
		OUT = high impedance (MAX16898)
$V_{UVSET} < V_{TH}$	High	OUT = VCC (MAX16896)
		OUT = high impedance (MAX16898)
$V_{UVSET} > V_{TH}$	Low	Low
$V_{UVSET} > V_{TH}$	High	OUT = VCC (MAX16896)
		OUT = high impedance (MAX168956898)

Table 3. MAX16899 Output

UVSET	ENABLE	OUT
$V_{UVSET} < V_{TH}$	Low	Low
$V_{UVSET} < V_{TH}$	High	Low
$V_{UVSET} > V_{TH}$	Low	High
$V_{UVSET} > V_{TH}$	High	Low

Supply Input (V_{CC})

The device operates with a V_{CC} supply voltage from 1.5V to 5.5V. To maintain a 1% accurate threshold, V_{CC} must be above 1.5V. When V_{CC} falls below the UVLO threshold, the output deasserts. When V_{CC} falls below 1.05V, the output state cannot be determined. For noisy systems, connect a 0.1µF ceramic capacitor from V_{CC} to GND as close to the device as possible. For the push-pull active-high output option, a 100kΩ external pulldown resistor to ground ensures the correct logic state for V_{CC} down to 0.

Monitor Input (UVSET)

Connect the center point of a resistive divider to UVSET to monitor external voltages (see R1 and R2 of the Typical Operating Circuit). UVSET has a rising threshold of V_{TH} = 0.5V and a falling threshold of 0.495V (5mV hysteresis). When V_{UVSET} rises above V_{TH} and ENABLE is high (or ENABLE is low), OUT goes high (OUT goes low) after the programmed t_{DELAY} period. When V_{UVSET} falls below 0.495V, OUT goes low (OUT goes high) after a 16µs delay. UVSET has a maximum input current of 15nA, so large-value resistors are permitted without adding significant error to the resistive divider.

Adjustable Delay (CDELAY)

When V_{UVSET} rises above V_{TH} with ENABLE high (ENABLE low), the internal 250nA current source begins charging an external capacitor connected from CDELAY to GND. When the voltage at CDELAY reaches 1V, the output asserts (OUT goes high or OUT goes low). When the output asserts, C_{CDELAY} is immediately discharged. Adjust the delay (t_{DELAY}) from when V_{UVSET} rises above V_{TH} (with ENABLE high or ENABLE low) to OUT going high (OUT going low) according to the equation:

$$t_{DELAY} = C_{CDELAY} \times 4.0 \times 10^6 + 40\mu s$$

where C_{CDELAY} is the external capacitor from C_{DELAY} to GND.

For adjustable delay devices (A version), when V_{UVSET} > 0.5V and ENABLE goes from low to high (ENABLE goes from high to low), the output asserts after a t_{DELAY} period. For nonadjustable delay devices (P version), there is a 150ns propagation delay from when the enable input is asserted to when the output asserts. Figures 1 through 4 show the timing diagrams for the adjustable and fixed delay versions, respectively.

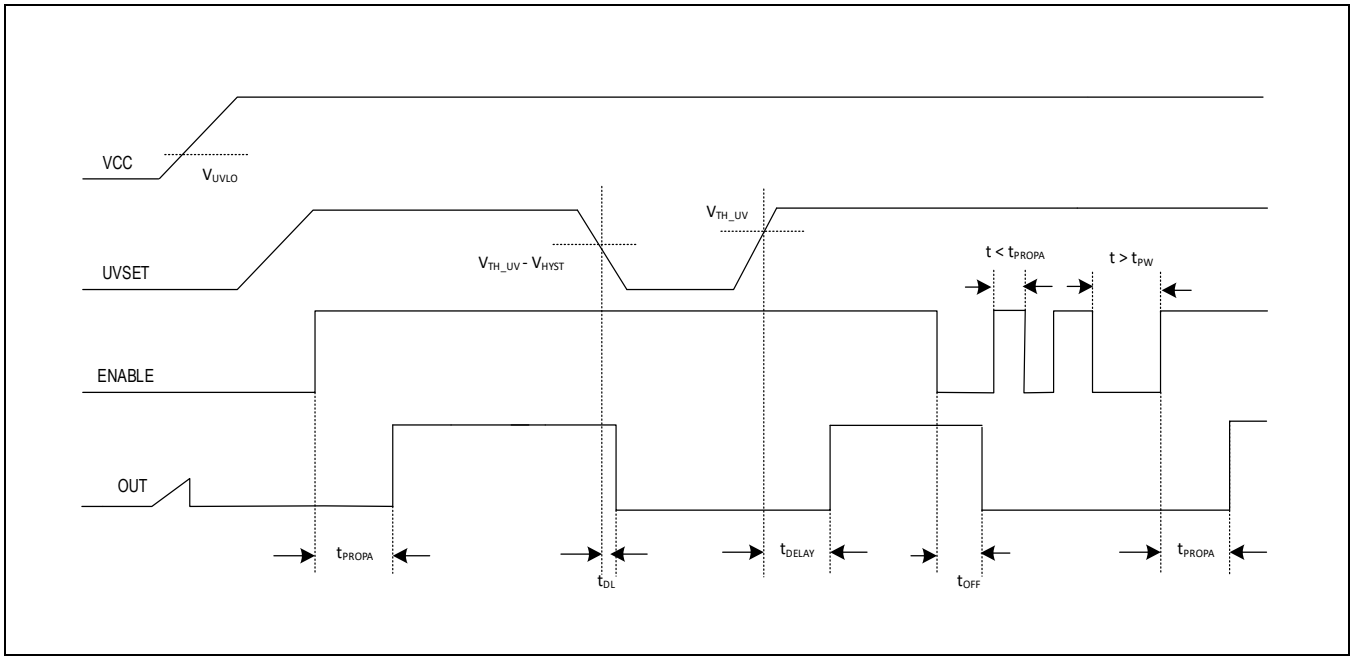


Figure 1. MAX16895A/MAX16897A Timing Diagram

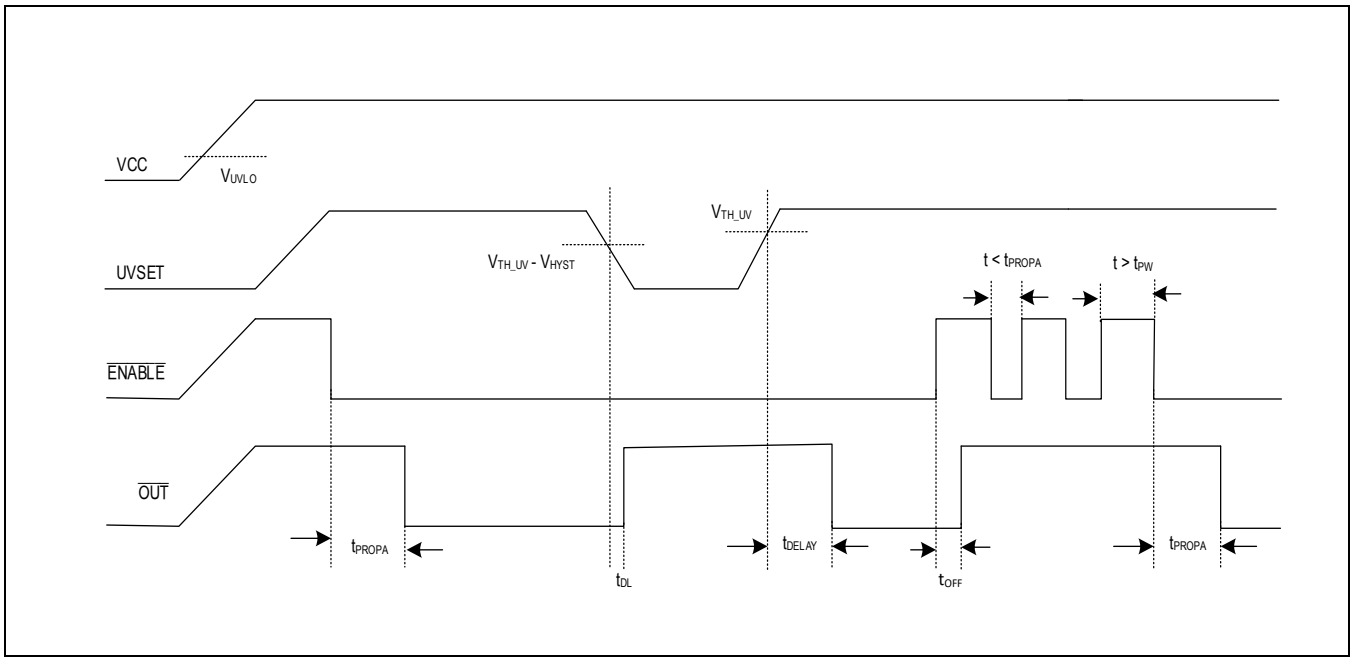


Figure 2. MAX16896A/MAX16898A Timing Diagram

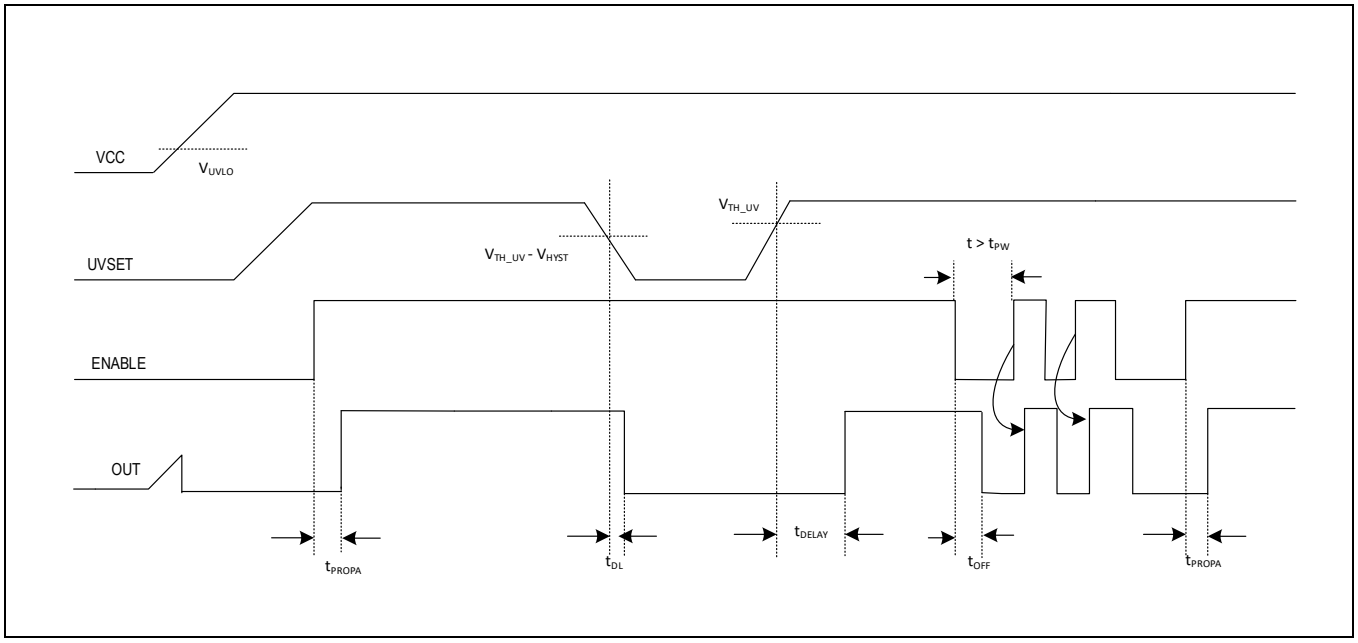


Figure 3. MAX16895P/MAX16897P Timing Diagram

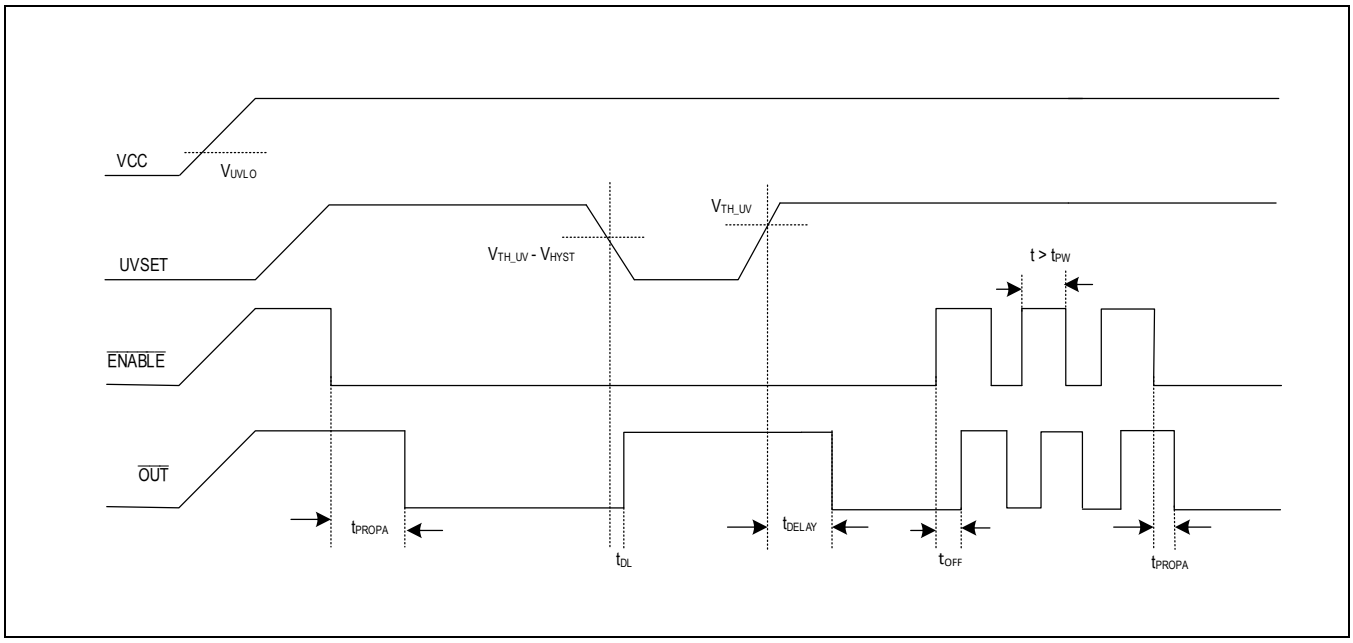


Figure 4. MAX16896P/MAX16898P Timing Diagram

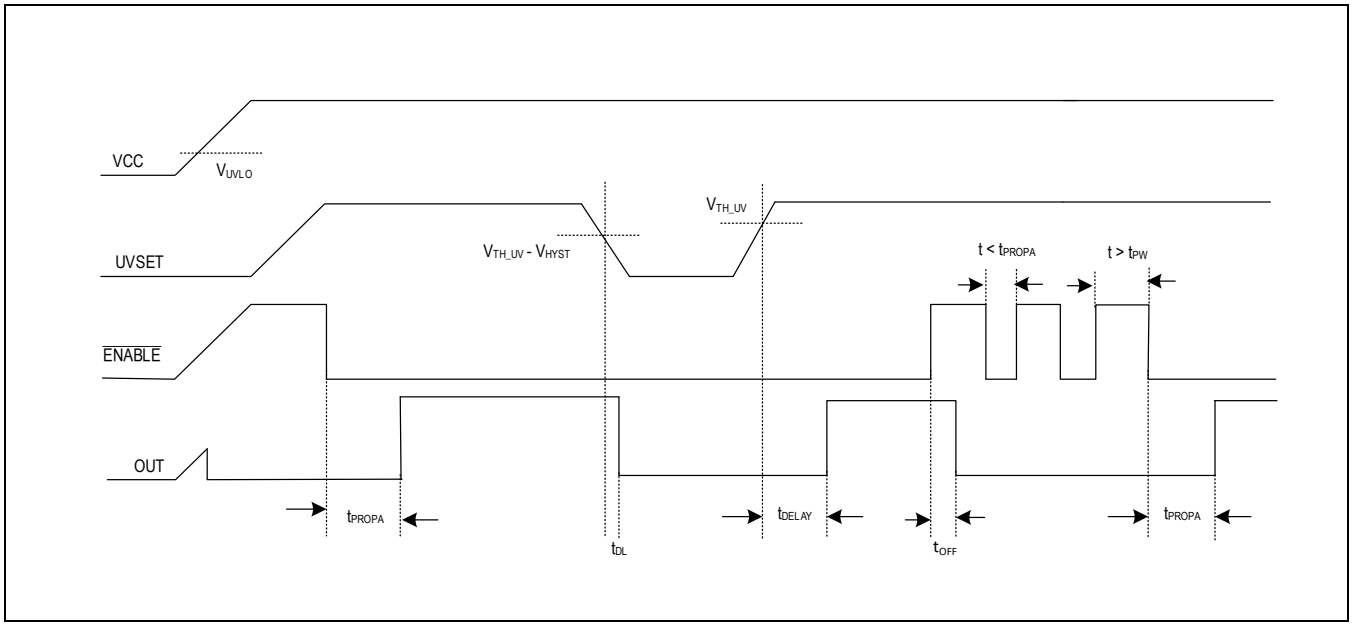


Figure 5. MAX16899A Timing Diagram

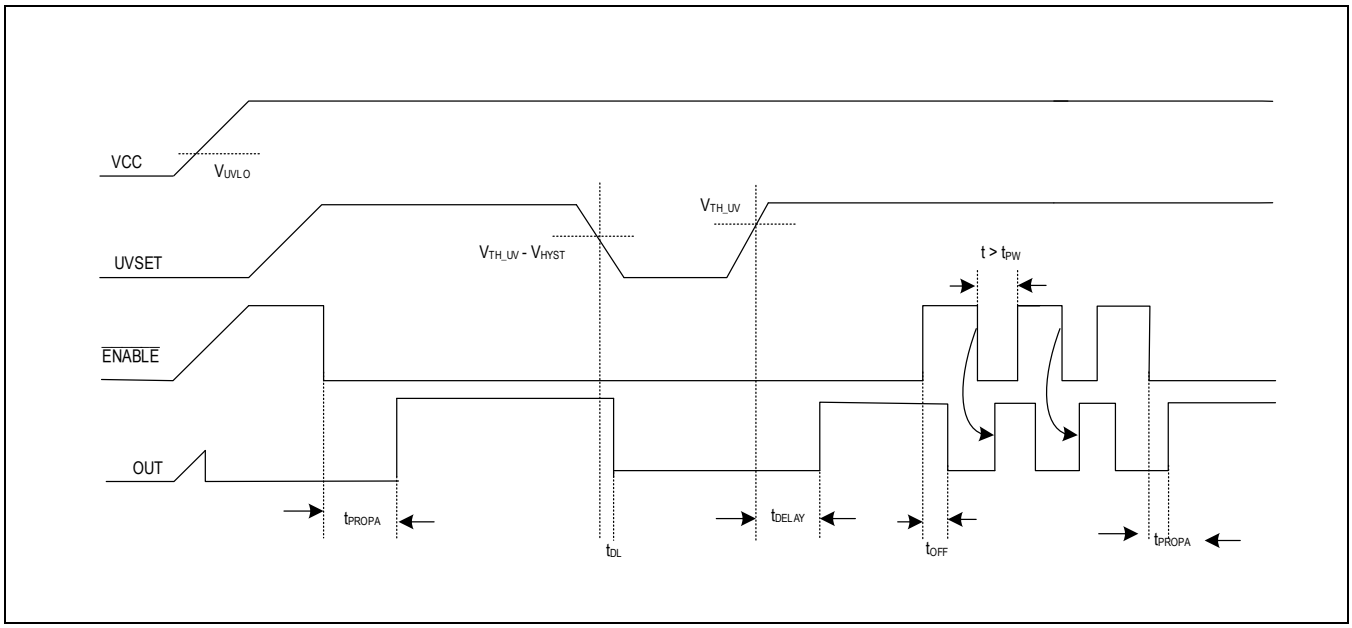


Figure 6. MAX16899P Timing Diagram

Enable Input (ENABLE or ENABLE)

The MAX16895/MAX16897 offer an active-high enable input (ENABLE), while the MAX16896/MAX16898/MAX16899 offer an active-low enable input (ENABLE). With V_{UVSET} above V_{TH}, drive ENABLE high (ENABLE low) to force OUT high (OUT low) after the adjustable delay time (A versions). For P version devices, when V_{UVSET} > 0.5V and enable is asserted, the output asserts after typically 150ns.

The enable input has logic-high and logic-low voltage thresholds of 1.4V and 0.4V, respectively. For both versions, when V_{UVSET} > 0.5V, drive ENABLE low (ENABLE high) to force OUT low (OUT high) within 150ns typ.

Output (OUT or OUT)

The MAX16895/MAX16899 offer an active-high, push-pull output (OUT), and the MAX16896 offers an active-low push-pull output (OUT). The MAX16897 offers an active- high open-drain output (OUT), and the MAX16898 offers an active-low open-drain output (OUT).

Push-pull output devices are referenced to VCC. Open-drain outputs can be pulled up to 28V.

Applications Information

Input Threshold

The MAX16895–MAX16899 monitor the voltage on UVSET with an external resistive divider (see R1 and R2 in the Typical Operating Circuit). Connect R1 and R2 as close to UVSET as possible. R1 and R2 can have very high valuesto minimize current consumption due to low UVSET leakage currents (±15nA max). Set R2 to some conveniently high value (1MΩ, for example) and calculate R1 based on the desired monitored voltage using the following formula:

$$R1 = R2 \times (\frac{V_{MONITOR}}{V_{UVSET}} - 1)$$

where $V_{MONITOR}$ is the desired monitored voltage and V_{UVSET} is the detector input threshold (0.5V).

Pullup Resistor Values (MAX16897/MAX16898)

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{CC} = 2.25V and the pullup voltage is 28V, it is ideal to keep the sink current less than 0.5mA as shown in the *Electrical Characteristics* table. As a result, the pullup resistor should be greater than 56kΩ. For a 12V pullup, the resistor should be larger than 24kΩ. It should be noted that the ability to sink current is dependent on the V_{CC} supply voltage.

Typical Application Circuits

Figures 7, 8, and 9 show the typical applications for the MAX16895–MAX16899. *Figure 7* shows the MAX16897 used with a p-channel MOSFET in an overvoltage protection circuit. *Figure 8* shows the MAX16895 in a low-voltage sequencing application using an n-channel MOSFET. *Figure 9* shows the MAX16895 used in a multiple-output sequencing application.

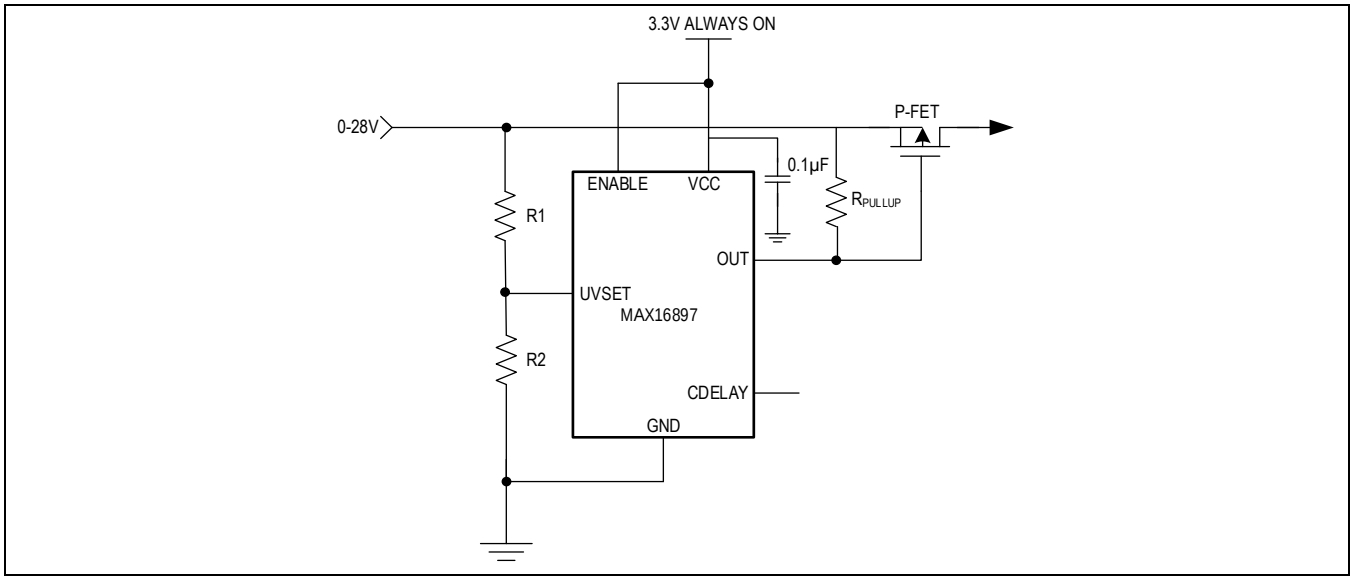


Figure 7. Overvoltage Protection

Using a n-Channel Device for Sequencing

In higher power applications, using a n-channel device reduces the loss across the MOSFETs as it offers a lower drain-to-source on-resistance. However, a n-channel MOSFET requires a sufficient VGS voltage to fully enhance it for a low RDS_ON. The application in *Figure 8* shows the MAX16895 in a switch sequencing application using a n-channel MOSFET.

Similarly, if a higher voltage is present in the system, the open-drain version can be used in the same manner.

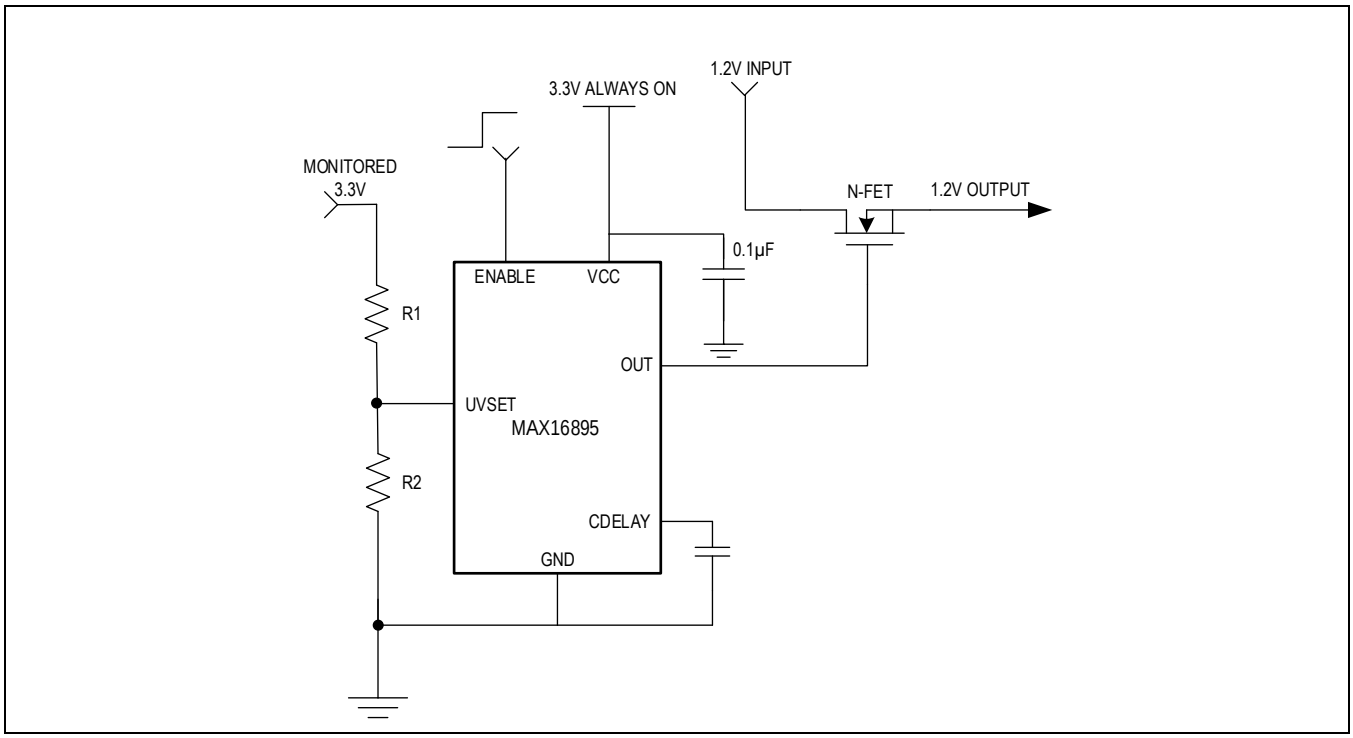


Figure 8. Low-Voltage Sequencing Using a n-Channel MOSFET

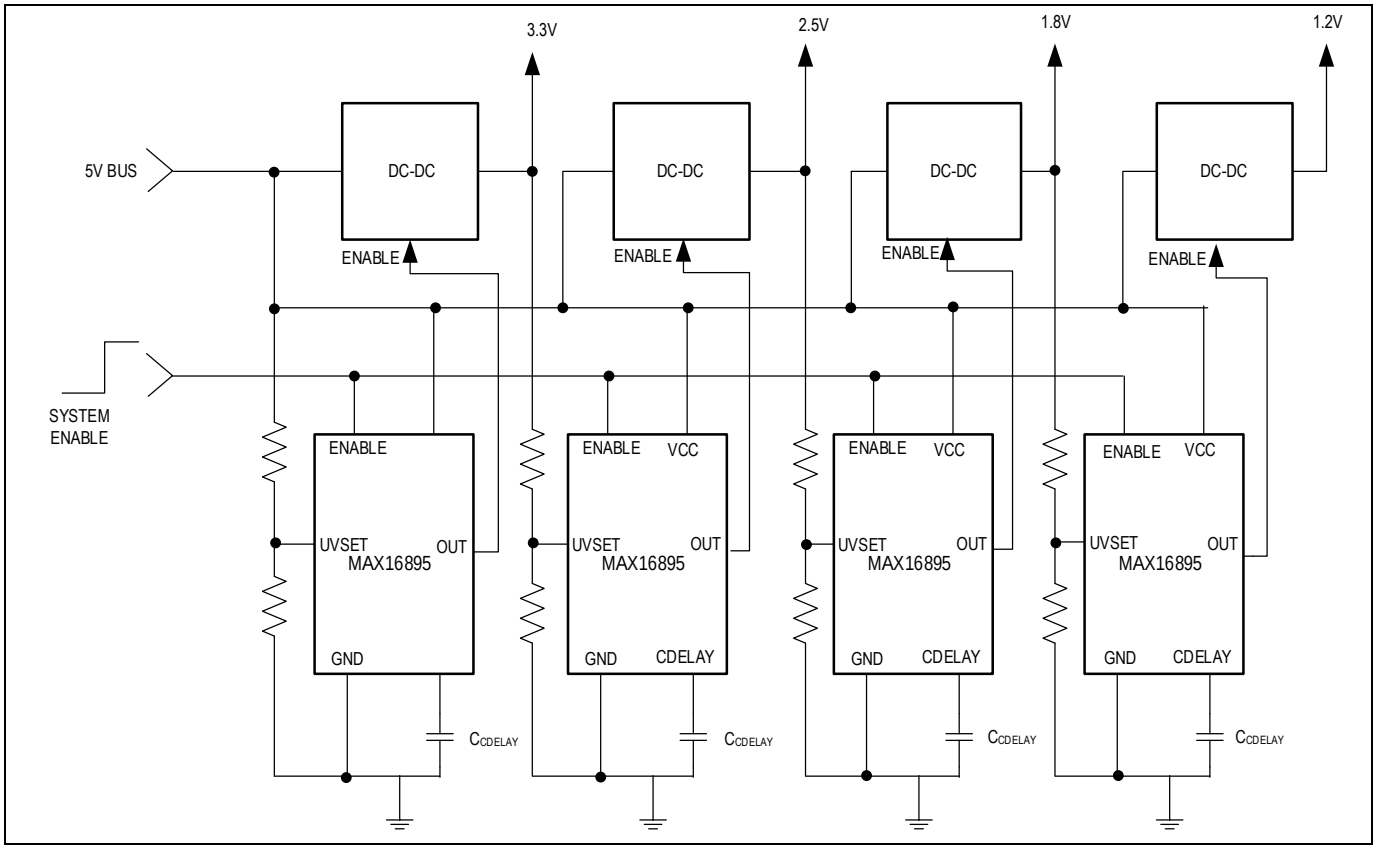
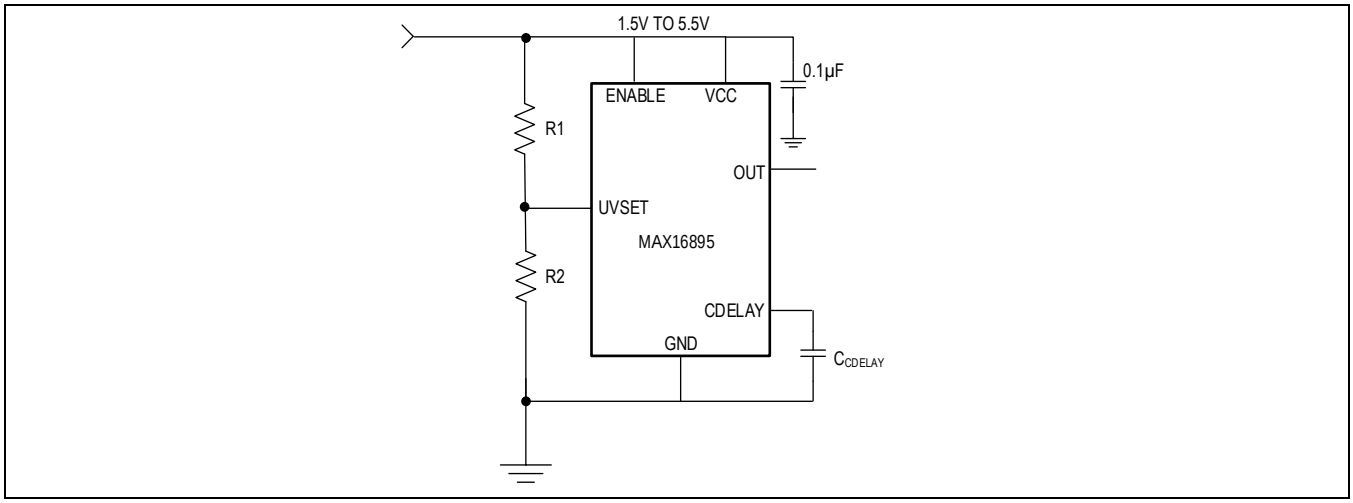


Figure 9. Multiple-Output Sequencing

Selector Guide

PART	ENABLE INPUT	OUTPUT	INPUT (UVSET) DELAY	ENABLE DELAY
MAX16895AALT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16895AAZT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16895PALT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX16895PAZT+T	Active-High	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX16896AALT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16896AAZT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16896PALT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	150ns Delay
MAX16896PAZT+T	Active-Low	Active-Low, Push-Pull	Capacitor Adjustable	150ns Delay
MAX16897AALT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX16897AAZT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX16897PALT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	150ns Delay
MAX16897PAZT+T	Active-High	Active-High, Open-Drain	Capacitor Adjustable	150ns Delay
MAX16898AALT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX16898AAZT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	Capacitor Adjustable
MAX16898PALT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	150ns Delay
MAX16898PAZT+T	Active-Low	Active-Low, Open-Drain	Capacitor Adjustable	150ns Delay
MAX16899AALT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16899AAZT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	Capacitor Adjustable
MAX16899PALT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay
MAX16899PAZT+T	Active-Low	Active-High, Push-Pull	Capacitor Adjustable	150ns Delay

Typical Operating Circuit



Ordering Information

PART NUMBER	PIN-PACKAGE	TOP MARK
MAX16895AALT+	6 µDFN	QT+
MAX16895_ _ _ _+*	—	—
MAX16896_ _ _ _+*	—	—
MAX16897_ _ _ _+*	—	—
MAX16898_ _ _ _+*	—	—
MAX16899_ _ _ _+*	—	—

Note: All devices are specified over the -40°C to +125°C operating temperature range.

+Denotes a lead (Pb) free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/21	Release for Market Intro	—
1	1/22	Updated Electrical Characteristics table	3