19-4685; Rev 0; 7/09

EVALUATION KIT AVAILABLE

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

MAX17106

General Description

The MAX17106 is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications. The device includes a high-performance 18V step-up regulator with integrated switch for the source-driver supply, a 38V step-up regulator with temperature compensation for the TFT gate-on supply (VON), a 300mA low-dropout 2.5V internal linear regulator for the logic supply, three high-speed operational amplifiers, a digitally adjustable VCOM calibration device with nonvolatile memory, two electrically erasable programmable read-only memory (EEPROM) blocks (2Kb extended display identification data (EDID) memory and 16Kb timing controller memory) with separate I²C interfaces, and a high-voltage level-shifting scan driver.

The main DC-DC step-up converter provides the regulated supply voltage for the panel source driver ICs. The converter is a 1.2MHz current-mode regulator with an integrated 20V n-channel power MOSFET. The high switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides fast transient response to pulsed loads. The step-up regulator features digital soft-start and cycle-by-cycle current limit.

The VON step-up regulator is a simple minimum off-time, pulse-skipping architecture with a variable peak-current threshold. The output voltage is adjusted according to the voltage on the NTC pins (temperature reading) and two voltage levels set by current sources on the VHI and VLO pins. See the *VON Positive Gate-Driver Step-Up Regulator* section for more information.

The MAX17106 is available in a 7mm x 7mm, 56-pin, lead-free TQFN package with exposed pad and operates over the -40°C to +85°C temperature range.

Applications

TFT LCD Notebook Panels

Simplified Operating Circuit appears at end of data sheet.

Features

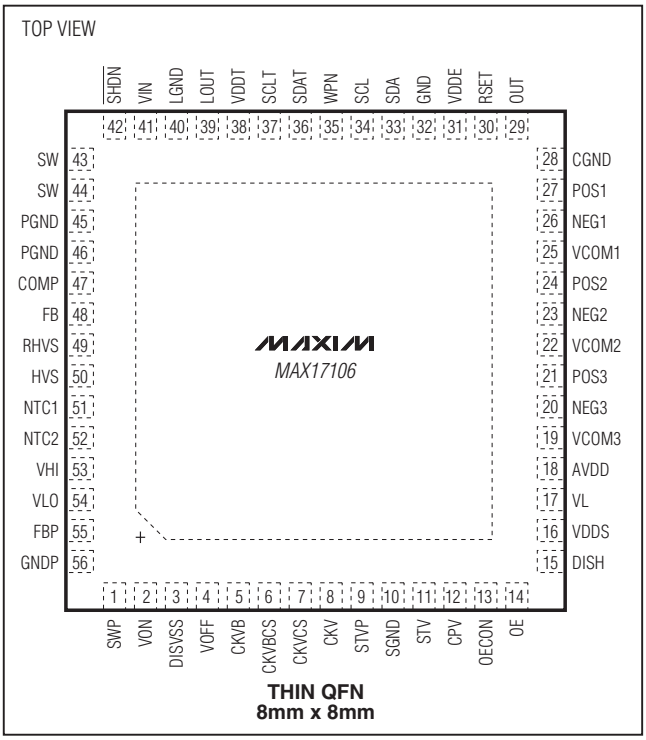
- **2.4V to 3.6V VDDS Input Voltage Range**
- **0.2mA VDDS Quiescent Current**
- **5mA VIN Quiescent Current (Switching)**
- **3mA AVDD Quiescent Current (for Op Amps)**
- **1.2MHz Current-Mode Step-Up Regulator**
- **VON Temperature-Compensated Step-Up Regulator**
- **Internal 300mA Low-Dropout (LDO) Linear Regulator**
- **Rail-to-Rail High-Speed Operational Amplifier**
- **High-Voltage Drivers with Scan Logic**
- **Programmable VCOM Calibrator**
- **2Kb EEPROM EDID Memory**
- **16Kb EEPROM Timing Controller Memory**
- **Thermal-Overload Protection**
- **56-Pin, 7mm x 7mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17106ETN+	-40°C to +85°C	56 Thin QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



THIN QFN
8mm x 8mm

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

ABSOLUTE MAXIMUM RATINGS

VIN, HVS, $\overline{SHDN}$ to LGND ..... -0.3V to +7.5V
LOUT to LGND ..... -0.3V to (V_{VIN} + 0.3V)
VL to GND ..... -0.3V to +3V
VDDE, VDDT to GND ..... -0.3V to +4V
RSET to LGND ..... -0.3V to (OUT + 0.3V)
SDAT, SCLT, SCL, SDA, WPN, RSET to GND ..... -0.3V to +4.0V
OECON, CPV, OE, STV, VDDS to SGND ..... -0.3V to +4.0V
COMP, FB, FBP, RHVS to LGND ..... -0.3V to (V_{VIN} + 0.3V)
NTC1, NTC2, VHI, VLO ..... -0.3V to (V_{VL} + 0.3V
DISH to SGND ..... -6V to (V_{VIN} + 0.3V)
AVDD to CGND ..... -0.3V to +20V
AVDD to LGND ..... -0.3V to (V_{VON} + 0.3V)
SW to PGND ..... -0.3V to +20V
SWP to PGND ..... -0.3V to +40V
OUT, VCOM1, VCOM2, VCOM3, NEG1, NEG2, NEG3, POS1, POS2, POS3 to CGND ..... -0.3V to (V_{AVDD} + 0.3V)
POS1, POS2, POS3 to NEG1, NEG2, NEG3 ..... -6V to +6V
VON to SGND ..... -0.3V to +40V
VOFF to SGND ..... -20V to +0.3V
CKV, CKVB, STVP, CKVCS, CKVBCS, DISVSS to SGND ..... (V_{VOFF} - 0.3V) to (V_{VON} + 0.3V)
PGND, CGND, SGND, GND to LGND ..... -0.3V to +0.3V
SW, PGND RMS Current Rating (total) 2.4A
VCOM1, VCOM2, VAVDD, CGND RMS Current 80mA
V_{COM3} RMS Current 5mA
SWP, GNDP RMS Current Rating 0.8A
POS_, NEG_ RMS Current Rating 5mA
Continuous Power Dissipation (T_A = +70°C)
56-Pin, 7mm x 7mm Thin QFN
(derate 40mW/°C above +70°C) 2400mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN Input Voltage Range	(Note 1)	2.4		6.0	V
VIN Undervoltage Lockout	V_{VIN} rising; typical hysteresis 100mV; SW remains off below this level		2.20	2.35	V
VDDS, VDDE, VDDT Input Voltage Range		2.4		3.6	V
VDDS Quiescent Current	V_{VDDS} = 3V		180	320	µA
VDDE Quiescent Current	V_{VDDE} = 3V (Note 2)		20	40	µA
VDDT Quiescent Current	V_{VDDT} = 3V		10	20	µA
VDDE Undervoltage Lockout	V_{VDDE} rising; typical hysteresis 100mV; communications with SCL/SDA remain off below this level		1.4	2.25	V
VDDT Undervoltage Lockout	V_{VDDT} rising; typical hysteresis 100mV; communications with SCLT/SDAT remain off below this level		1.4	2.25	V
FB, FBP, LOUT Undervoltage Fault-Timer Duration			50		ms
Duration to Restart After Fault			160		ms
Number of Restart Attempts Before Shutdown			3		Times
Thermal Shutdown	Rising edge, hysteresis = 15°C		160		°C
MEMORY BLOCK LINEAR REGULATOR (VL)					
VL Output Voltage	V_{VIN} or V_{VDDE} = 3V	2.3	2.5	2.7	V
VL Undervoltage Lockout	V_{VL} rising, typical hysteresis =100mV			2.1	V
VL Dropout Voltage	I_{VL} = 10mA		0.05	0.1	V
VL Maximum Output Current		10			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL 2.5V LINEAR REGULATOR					
Dropout Voltage	I_{LOUT} = 300mA		0.1	0.23	V
LOUT Regulation Voltage	I_{LOUT} = 100mA	2.44	2.48	2.52	V
LOUT Maximum Output Current	V_{LOUT} = 2.3V	300			mA
LOUT Load Regulation	V_{VIN} = 3.3V, 5mA < I_{LOUT} < 300mA, not in dropout		-0.35		%
LOUT Fault Timer Trip Threshold	Falling edge	1.9	2	2.2	V
Soft-Start Period	7-bit voltage ramp		3		ms
MAIN DC-DC CONVERTER					
VIN Supply Current	V_{FB} = 1.5V, SW not switching		3.0	5.5	mA
	V_{FB} = 1.1V, SW switching continuously		5.0	7.5	
Operating Frequency		1020	1200	1380	kHz
Oscillator Maximum Duty Cycle		88	92	96	%
FB Regulation Voltage		1.216	1.235	1.254	V
FB Load Regulation	0 < I_{LOAD} < 200mA, transient only		-1		%
FB Line Regulation	V_{VIN} = 2.6 to 6.0V	-0.4	-0.02	+0.4	%/V
FB Input-Bias Current	V_{FB} = 1.235V	50	125	200	nA
FB Transconductance	ΔI = 5µA at COMP	75	160	280	µS
FB Voltage Gain	FB to COMP		2400		V/V
FB Fault Timer Trip Threshold	Falling edge	0.98	1.02	1.06	V
SW On-Resistance	I_{SW} = 200mA		120	240	mΩ
SW Bias Current	V_{SW} = 18V		12	20	µA
SW Current Limit	Duty cycle = 65%	1.8	2.1	2.4	A
Current-Sense Transresistance		0.20	0.37	0.50	V/A
Soft-Start Period			13		ms
VON TEMPERATURE-COMPENSATED DC-DC CONVERTER					
FBP Regulation Voltage	Midrange	0.880	0.893	0.906	V
FBP Load Regulation	0 < I_{LOAD} < 40mA		-0.1		%
FBP Line Regulation	V_{MAIN} = 5V to 10V		-0.1		%/V
FBP Input-Bias Current	V_{FBP} = 0.9V , V_{HI} = V_{LO} = 0V	50	125	200	nA
FBP Fault-Timer Trip Threshold	Falling edge, relative to nominal regulation point		0.8 x Nom		V
SWP On-Resistance	I_{SWP} = 100mA		1.0	2.0	Ω
SWP Leakage Current	V_{SWP} = 38V		0.01	20	µA
SWP High Current Limit		700	1100	1500	mA
SWP Low Current Limit			400		mA
Minimum Off-Time			300		ns
Soft-Start Period			3		ms

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
NTC1 Source Current		45	50	55	µA
NTC2 Source Current		90	100	110	µA
VHI, VLO Source Current		98	100	102	µA
VHI, VLO Voltage Range		0		V_{VL} - 0.5	V
Thermistor Typical Value			10		kΩ
OPERATIONAL AMPLIFIERS					
AVDD Supply Range		5		18	V
AVDD Supply Current	For op amps, VCOM calibrator		3	7	mA
AVDD Overvoltage Fault Threshold	(Note 3)	18.1	18.6	19.1	V
AVDD Undervoltage Fault Threshold	(Note 3)			1.4	V
Input Offset Voltage	$V_{NEG\_}$, $V_{POS\_}$ = V_{AVDD}/2, T_A = +25°C	-10		+10	mV
Input-Bias Current	$V_{NEG\_}$, $V_{POS\_}$ = V_{AVDD}/2	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{AVDD}	V
Output Voltage Swing High (VCOM1,2)	$I_{VCOM1,2}$ = 5mA	V_{AVDD} - 100	V_{AVDD} - 50		mV
Output Voltage Swing High (VCOM3)	I_{VCOM3} = 5mA	V_{AVDD} - 300	V_{AVDD} - 150		V
Output Voltage Swing Low	$I_{VCOM\_}$ = -5mA		50	100	mV
Output Current High	$V_{VCOM1,2}$ = V_{AVDD} - 1V		-75		mA
Output Current Low	$V_{VCOM1,2}$ = 1V		+75		mA
Slew Rate			40		V/µs
-3dB Bandwidth			20		MHz
Output Short-Circuit Current	Short to V_{AVDD}/2, sourcing, $V_{COM1,2}$	50	150		mA
	Short to V_{AVDD}/2, sinking, $V_{COM1,2}$	50	150		
PROGRAMMABLE CALIBRATOR					
RSET Voltage Resolution		7			Bits
RSET Differential Nonlinearity	Monotonic overtemperature	-1		+1	LSB
RSET Zero-Scale Error		-1	+1	+3	LSB
RSET Full-Scale Error		-5		+5	LSB
RSET Current				120	µA
RSET External Resistance	To GND, V_{AVDD} = 18V	8.5		170	kΩ
	To GND, V_{AVDD} = 6V (Note 4)	2.5		50	
V_{RSET}/V_{AVDD} Voltage Ratio	DAC full scale		0.05		V/V
OUT Leakage Current	When OUT is off, T_A = +25°C			1	µA
OUT Settling Time	To ≤ 0.5 LSB error band		20		µs
OUT Voltage Range		V_{RSET} + 0.5V		18	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MEMORY BLOCKS					
EEPROM Write Cycles	(Note 5)	1000			Cycles
2Kb EDID EEPROM First-Byte Write Time	00xh location, 1-byte or 8-byte write			55	ms
2Kb EDID EEPROM Subsequent Write Time	All other locations			0.5	ms
16Kb TCON EEPROM Page Initial Byte Write Time	000xh or 200xh or 400xh or 600xh location			55	ms
16Kb TCON EEPROM Page Subsequent Write Time	All other locations			0.8	ms
Programmable Calibrator Nonvolatile Write Time	Data byte 8'bxxxxxxx0			55	ms
2-WIRE INTERFACES					
Logic Input Low Voltage	SDA, SCL, WPN			0.3 x V_{VDDE}	V
Logic Input High Voltage	SDA, SCL, WPN	0.7 x V_{VDDE}			V
Logic Input Low Voltage	SDAT, SCLT			0.3 x V_{VDDT}	V
Logic Input High Voltage	SDAT, SCLT	0.7 x V_{VDDT}			V
Logic Output Low Sink Current	SDA, SDAT forced to 3.3V	6			mA
Logic Input Current	SDA, SCL, SDAT, SCLT to VIN or GND, T_A = +25°C	-1		+1	µA
WPN Input Current	VWPN = 3.3V		14	35	µA
Input Capacitance	SDA, SCL, SDAT, SCLT		5	10	pF
SCL, SCLT Frequency		10		100	kHz
SCL, SCLT High Time	t_{CLH}	4			µs
SCL, SCLT Low Time	t_{CLL}	4.7			µs
Bus Rise Time	t_R: SDA, SCL, SDAT, SCLT , Cb = total capacitance of bus line in pF	20 + 10 x Cb		300	ns
Bus Fall Time	t_F: SDA, SCL, SDAT, SCLT , Cb = total capacitance of bus line in pF	20 + 10 x Cb		300	ns
START Condition Hold Time	t_{HDSTT}: 10% of SDA, SDAT to 90% of SCL, SCLT	4			µs
Data Input Hold Time	t_{HDDAT}: 10% SCL, SCLT to 90% SDA, SDAT	300			ns
Data Input Setup Time	t_{SUDAT}: 90% SDA, SDAT to 10% SCL, SCLT	250			ns
STOP Condition Setup Time	t_{SUSTP}: 90% of SCL, SCLT to 90% of SDA, SDAT	4			µs
Bus Free Time	t_{BF}	4.7			µs

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Filter Spike Suppression	SDA, SCL, SDAT, SCLT, not tested		700		ns
HIGH-VOLTAGE SCAN DRIVER					
VON Input Voltage Range		12		38	V
VOFF Input Voltage Range	(V_{ON} - V_{OFF}) ≤ 56V	-18		-3	V
VON Supply Current	STV, CPV, OE, OECON = GND		300	550	µA
VOFF Supply Current	STV, CPV, OE, OECON = GND		350	550	µA
Output Voltage Low	CKV, CKVB, STVP, -5mA output current	V_{VOFF} + 0.3	V_{VOFF} + 0.1		V
Output Voltage High	CKV, CKVB, STVP, 5mA output current		V_{VON} - 0.1	V_{VON} - 0.3	V
Propagation Delay Between OE Rising Edge and CKV/CKVB Edge	CPV = GND, STV = GND, OE = 100kHz, C_{LOAD} = 4.7nF + 50Ω, measured from input to 10% output change		100	200	ns
Output Slew Rate CKV, CKVB	Without charge sharing, STV = VDDS, C_{LOAD} = 4.7nF + 50Ω	16	25		V/µs
Propagation Delay Between STV and STVP	STV = 100Hz, C_{LOAD} = 4.7nF, measured from input to 10% output change		50	150	ns
Output Slew Rate STVP	C_{LOAD} = 4.7nF + 50Ω, R1 = R2 = 200Ω	18	30		V/µs
Charge-Sharing Switch Resistance	CKV to CKVCS and CKVB to CKVBCS		50	100	Ω
DISH Turn-On Threshold		-1	-0.6		V
DISH Switch Resistance	V_{OFF} = -3V V_{DISH} = -3V			500	Ω
	VOFF to GND, DISH = VIN			1	MΩ
DISVSS Switch Resistance	DISVSS to VON, switch on		10	20	Ω
	DISVSS to VON, switch off	0.1			MΩ
STV, CPV, OE, OECON Input Current	STV = VDDS or GND; CPV = VDDS or GND; OE = VDDS or GND; OECON = VDDS or GND; T_A = +25°C	-1		+1	µA
STV, CPV, OE Input Low Voltage				0.7	V
STV, CPV, OE Input High Voltage		1.8			V
OECON Input Threshold (Rising Edge)		0.5 x V_{VDDS}	0.58 x V_{VDDS}	0.66 x V_{VDDS}	
OECON Sink Current	OECON = STV = VDDS	0.4	0.8		mA
CKV, CKVB, CKVCS, CKVBCS, STVP Output Three-State Current	CKV, CKVB, STVP, CKVCS, CKVBCS at midrail, three-state, T_A = +25°C	-1		+1	µA
HVS FUNCTION					
HVS Input Low Voltage				0.8	V
HVS Input High Voltage		1.8			V
HVS Input Pulldown Resistance		5	25	50	kΩ
RHVS Output Switch Current	V_{HVS} = 3V, V_{RHVS} = 0.4V	20			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS					
Input Low Voltage	$\overline{SHDN}$			0.6	V
Input High Voltage	$\overline{SHDN}$	1.8			V
$\overline{SHDN}$ Resistance			1		MΩ

ELECTRICAL CHARACTERISTICS

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN Input-Voltage Range	(Note 1)	2.4		6.0	V
VIN Undervoltage Lockout	V_{VIN} rising, typical hysteresis 100mV, SW remains off below this level			2.35	V
VDDS, VDDE, VDDT Input-Voltage Range		2.4		3.6	V
VDDS Quiescent Current	V_{VDDS} = 3V			320	µA
VDDE Quiescent Current	V_{VDDE} = 3V (Note 2)			40	µA
VDDT Quiescent Current	V_{VDDT} = 3V			20	µA
VDDE Undervoltage Lockout	V_{VDDE} rising; typical hysteresis 100mV; communications with SCL/SDA remain off below this level			2.25	V
VDDT Undervoltage Lockout	V_{VDDT} rising; typical hysteresis 100mV; communications with SCLT/SDAT remain off below this level			2.25	V
MEMORY BLOCK LINEAR REGULATOR					
VL Output Voltage	V_{VIN} or V_{VDDE} = 3V	2.3		2.7	V
VL Undervoltage Lockout	V_{VL} rising, typical hysteresis 100mV			2.1	V
VL Dropout Voltage	I_{VL} = 10mA			0.1	V
VL Maximum Output Current		10			mA
INTERNAL 2.5V LINEAR REGULATOR					
Dropout Voltage	I_{LOUT} = 300mA			0.23	V
LOUT Regulation Voltage	I_{LOUT} = 100mA	2.44		2.52	V
LOUT Maximum Output Current	V_{LOUT} = 2.3V	300			mA
MAIN DC-DC CONVERTER					
VIN Supply Current	V_{FB} = 1.5V, SW not switching			5.5	mA
	V_{FB} = 1.1V, SW switching, continuously			7.5	
Operating Frequency		1020		1380	kHz
Oscillator Maximum Duty Cycle		88		96	%
FB Regulation Voltage		1.216		1.254	V
FB Fault Timer Trip Threshold	Falling edge	0.98		1.06	V
SW On-Resistance	I_{SW} = 200mA			240	mΩ
SW Current Limit	Duty cycle = 65%	1.8		2.4	A

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A =-40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VON TEMPERATURE-COMPENSATED DC-DC CONVERTER					
FBP Regulation Voltage	Midrange	0.880		0.906	V
SWP On-Resistance	I_{SWP} = 100mA			2.0	Ω
SWP High Current Limit		700		1500	mA
OPERATIONAL AMPLIFIERS					
AVDD Supply Range		5		18	V
AVDD Supply Current	For op amps, VCOM calibrator			8	mA
AVDD Overvoltage Fault Threshold	(Note 3)	18.1		19.9	V
AVDD Undervoltage Fault Threshold	(Note 3)			1.4	V
Input Common-Mode Voltage Range		0		V_{AVDD}	V
PROGRAMMABLE CALIBRATOR					
RSET Voltage Resolution		7			Bits
RSET Differential Nonlinearity	Monotonic overtemperature	-1		+1	LSB
RSET Zero-Scale Error		-1		+3	LSB
RSET Full-Scale Error		-5		+5	LSB
RSET Current				120	µA
RSET External Resistance (Note 4)	To GND, V_{AVDD} = 18V	8.5		170	kΩ
	To GND, V_{AVDD} = 6V	2.5		50	
OUT Voltage Range		V_{RSET} + 0.5V		18	V
MEMORY BLOCKS					
EEPROM Write Cycles	(Note 5)	1000			Cycles
2Kb EDID EEPROM First Byte Write Time	00xh location, 1 byte or 8 byte write			58	ms
2Kb EDID EEPROM Subsequent Write Time	All other locations			0.5	ms
16Kb TCON EEPROM Page Initial Byte Write Time	000xh or 200xh or 400xh or 600xh location			58	ms
16Kb TCON EEPROM Page Subsequent Write Time	All other locations			0.8	ms
Programmable Calibrator Nonvolatile Write Time	Data byte 8'bxxxxxxx0			58	ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-WIRE INTERFACES					
Logic Input Low Voltage	SDA, SCL, WPN			0.3 x V_{VDDE}	V
Logic Input High Voltage	SDA, SCL, WPN	0.7 x V_{VDDE}			V
Logic Input Low Voltage	SDAT, SCLT			0.3 x V_{VDDT}	V
Logic Input High Voltage	SDAT, SCLT	0.7 x V_{VDDT}			V
Logic Output Low Sink Current	SDA, SDAT forced to 3.3V	6			mA
Input Capacitance	SDA, SCL, SDAT, SCLT			10	pF
SCL, SCLT Frequency		10		100	kHz
SCL, SCLT High Time	t_{CLH}	4			µs
SCL, SCLT Low Time	t_{CLL}	4.7			µs
Bus Rise Time	t_R: SDA, SCL, SDAT, SCLT, Cb = total capacitance of bus line in pF	20 + 10 x Cb		300	ns
Bus Fall Time	t_F: SDA, SCL, SDAT, SCLT, Cb = total capacitance of bus line in pF	20 + 10 x Cb		300	ns
START Condition Hold Time	t_{HDSTT}: 10% of SDA, SDAT to 90% of SCL, SCLT	4			µs
Data Input Hold Time	t_{HDDAT}: 10% SCL, SCLT to 90% SDA, SDAT	300			ns
Data Input Setup Time	t_{SUDAT}: 90% SDA, SDAT to 10% SCL, SCLT	250			ns
STOP Condition Setup Time	t_{SUSTP}: 90% of SCL, SCLT to 90% of SDA, SDAT	4			µs
Bus Free Time	t_{BF}	4.7			µs
HIGH-VOLTAGE SCAN DRIVER					
VON Input-Voltage Range		12		38	V
VOFF Input-Voltage Range	(V_{VON} - V_{VOFF}) ≤ 56V	-18		-3	V
VON Supply Current	STV, CPV, OE, OECON = GND			550	µA
VOFF Supply Current	STV, CPV, OE, OECON = GND			550	µA
Output Voltage Low	CKV, CKVB, STVP, -5mA output current	V_{VOFF} + 0.3			V
Output Voltage High	CKV, CKVB, STVP, 5mA output current			V_{VON} - 0.3	V
Propagation Delay Between OE Rising Edge and CKV/CKVB Edge	CPV = GND, STV = GND, OE = 100kHz, C_{LOAD} = 4.7nF + 50Ω, measured from input to 10% output change			200	ns
Output Slew Rate CKV, CKVB	Without charge sharing, STV = VDDS, C_{LOAD} = 4.7nF + 50Ω	16			V/µs
Propagation Delay Between STV and STVP	STV = 100Hz, C_{LOAD} = 4.7nF, measured from input to 10% output change			150	ns

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

ELECTRICAL CHARACTERISTICS (continued)

(V_{VIN} = V_{VDDE} = V_{VDDT} = V_{VDDS} = $V_{\overline{SHDN}}$ = +3V, circuit of Figure 2, V_{AVDD} = 8V, V_{VON} = 23V, V_{VOFF} = -12V, $V_{POS\_}$ = $V_{NEG\_}$ = 4V, V_{CPV} = V_{STV} = V_{OECON} = V_{OE} = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate STVP	C_{LOAD} = 4.7nF + 50Ω, R1 = R2 = 200Ω	18			V/µs
Charge-Sharing Switch Resistance	CKV to CKVCS and CKVB to CKVBCS			100	Ω
DISH Turn-On Threshold		-1			V
DISH Switch Resistance	V_{OFF} = -3V V_{DISH} = -3V			500	Ω
	V_{OFF} to GND, DISH = V_{IN}			1	MΩ
DISVSS Switch Resistance	DISVSS to VON, switch on			20	Ω
	DISVSS to VON, switch off	0.1			MΩ
STV, CPV, OE Input Low Voltage				0.7	V
STV, CPV, OE Input High Voltage		1.8			V
HVS FUNCTION					
HVS Input Low Voltage				0.8	V
HVS Input High Voltage		1.8			V
HVS Input Pulldown Resistance		5		50	kΩ
CONTROL INPUTS					
Input Low Voltage	$\overline{SHDN}$			0.6	V
Input High Voltage	$\overline{SHDN}$	1.8			V
$\overline{SHDN}$ Resistance					MΩ

Note 1: For 5.5V < V_{VIN} < 6.0V, use IC for no longer than 1% of IC lifetime. For continuous operation, input voltage should not exceed 5.5V.

Note 2: If V_{VDDE} > V_{VIN}, the V_{VDDE} quiescent current increases to a max of 2mA.

Note 3: SW switching is not enabled until AVDD is above undervoltage threshold and below the overvoltage threshold.

Note 4: RSET external resistor range is verified at DAC full scale.

Note 5: Guaranteed by design, not production tested.

Note 6: T_A = -40°C specs are guaranteed by design, not production tested.

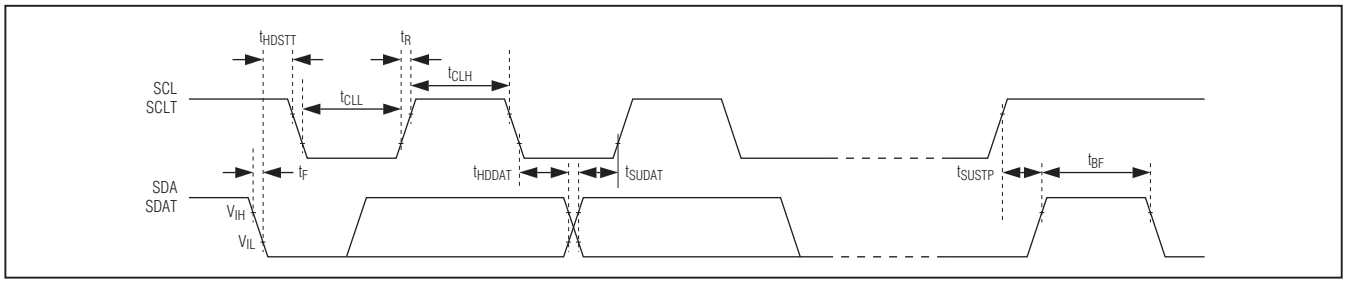
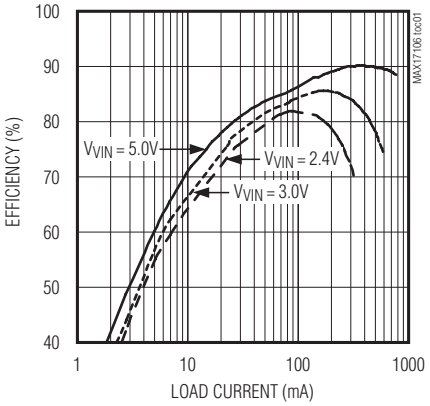


Figure 1. Timing Definitions Used in the Electrical Characteristics

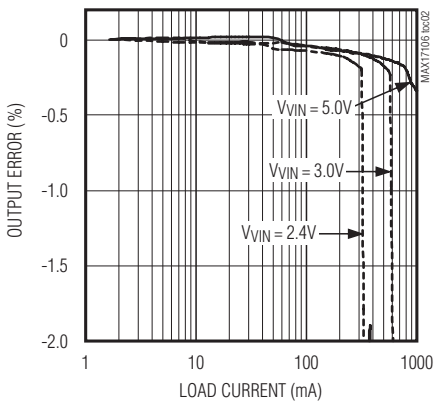
Typical Operating Characteristics

(Circuit of Figure 2, V_{VIN} = 3V, V_{MAIN} = 8V, T_A = +25°C, unless otherwise noted.)

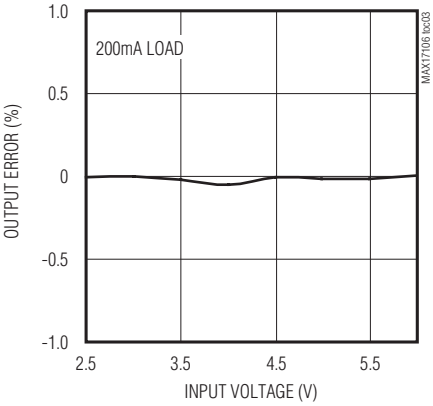
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 8V)



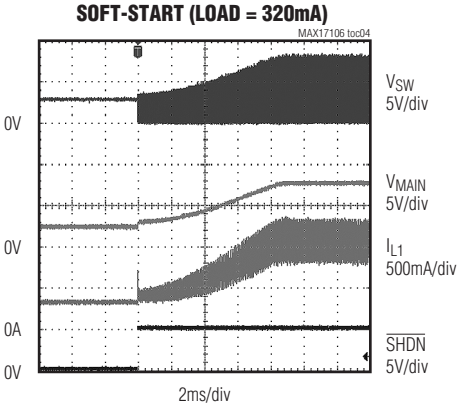
STEP-UP REGULATOR OUTPUT REGULATION vs. LOAD CURRENT



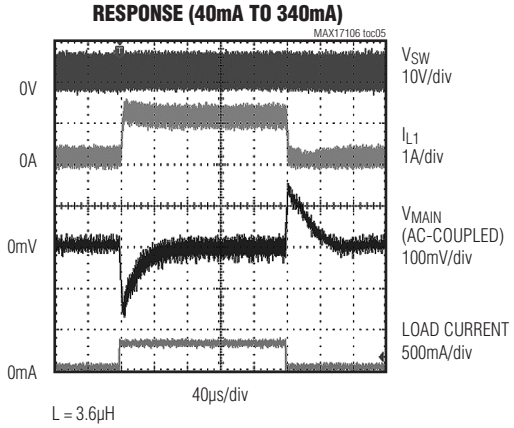
STEP-UP REGULATOR OUTPUT REGULATION vs. INPUT VOLTAGE



STEP-UP REGULATOR HEAVY-LOAD SOFT-START (LOAD = 320mA)

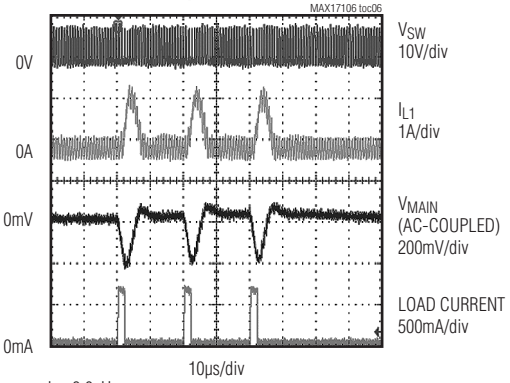


STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (40mA TO 340mA)



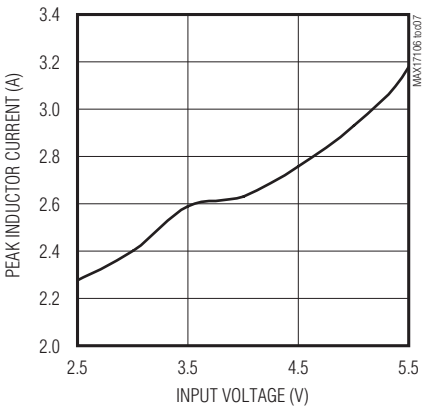
L = 3.6µH
R_{COMP} = 100kΩ
C_{COMP} = 220pF

STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (40mA TO 740mA)



L = 3.6µH
R_{COMP} = 100kΩ
C_{COMP} = 220pF

STEP-UP REGULATOR PEAK INDUCTOR CURRENT AT CURRENT LIMIT vs. INPUT VOLTAGE

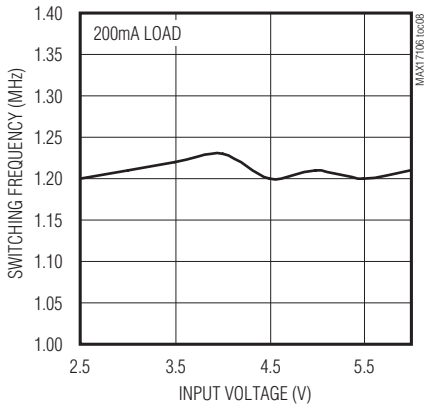


Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

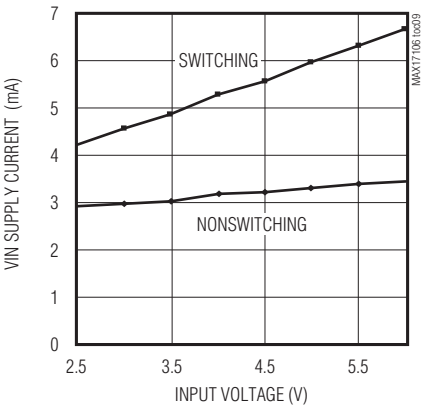
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{VIN} = 3V, V_{MAIN} = 8V, T_A = +25°C, unless otherwise noted.)

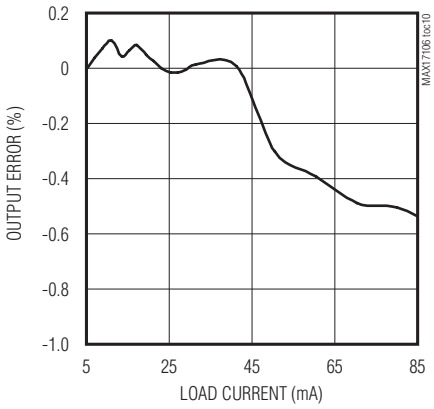
STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE



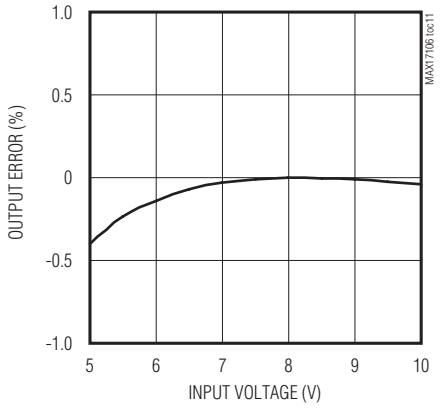
STEP-UP REGULATOR SUPPLY CURRENT vs. INPUT VOLTAGE



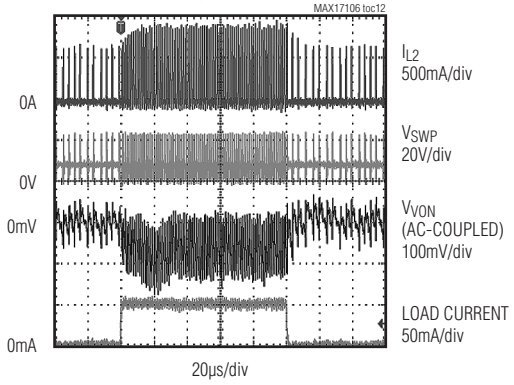
VON REGULATOR OUTPUT REGULATION vs. LOAD CURRENT



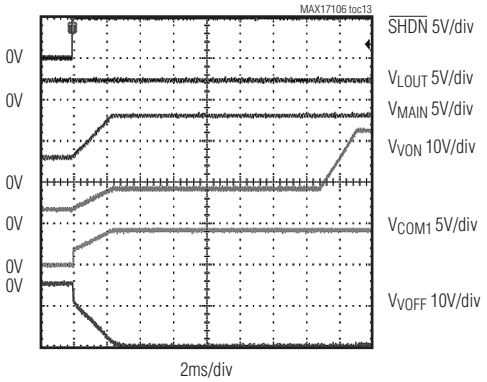
VON REGULATOR OUTPUT REGULATION vs. INPUT VOLTAGE



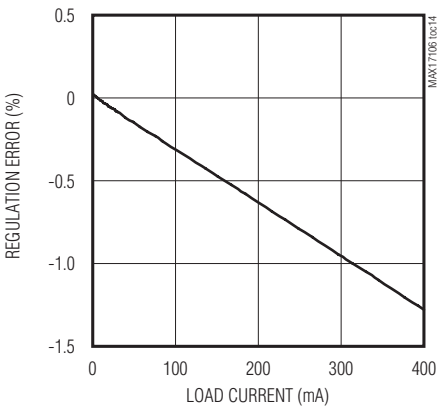
VON REGULATOR LOAD-TRANSIENT RESPONSE (10mA TO 60mA)



POWER-UP SEQUENCE OF ALL SUPPLY OUTPUTS



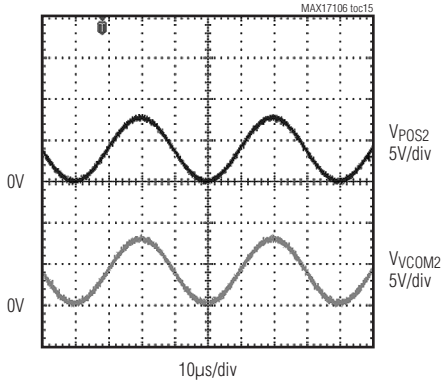
LDO VOLTAGE-LOAD REGULATION



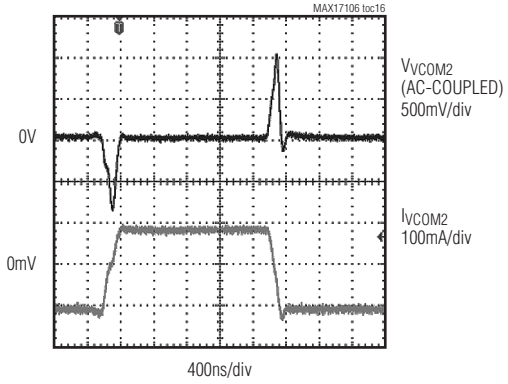
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{VIN} = 3V, V_{MAIN} = 8V, T_A = +25°C, unless otherwise noted.)

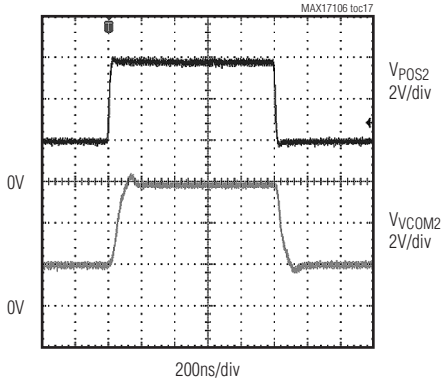
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT WAVEFORMS



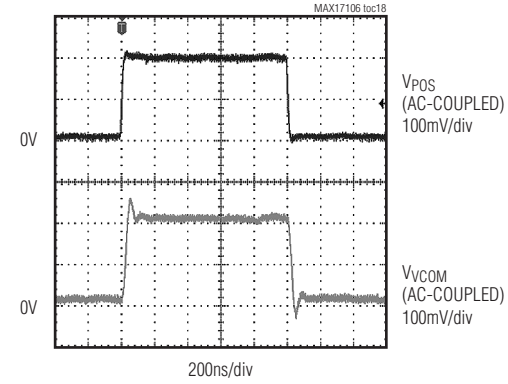
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



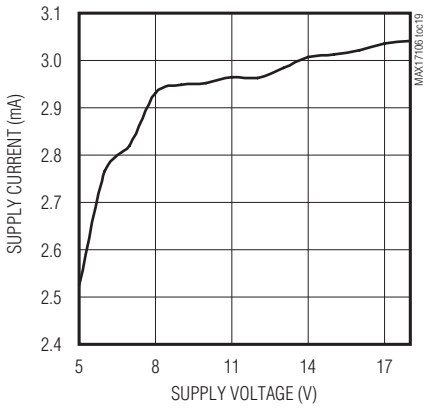
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



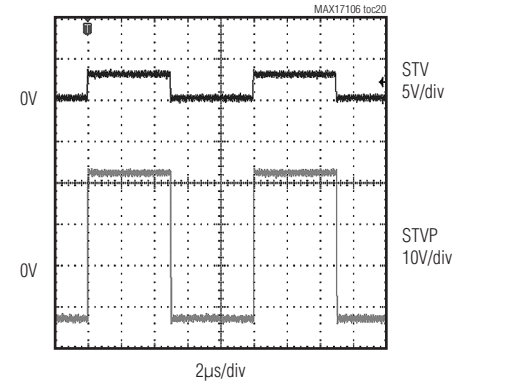
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



OPERATIONAL AMPLIFIER SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



STV/STVP INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT

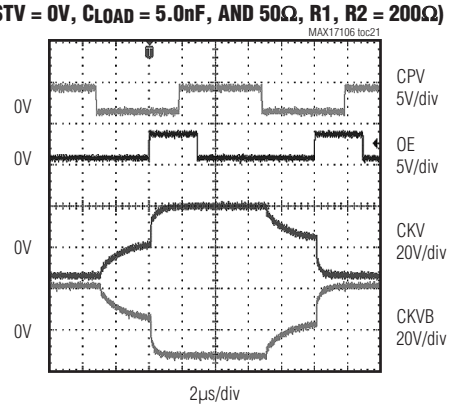


Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

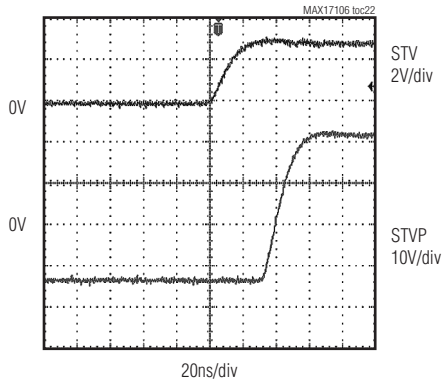
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{VIN} = 3V, V_{MAIN} = 8V, T_A = +25°C, unless otherwise noted.)

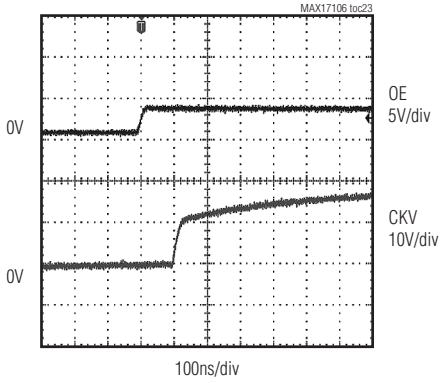
CPV, OE/CKV, AND CKVB INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT (STV = 0V, C_{LOAD} = 5.0nF, AND 50Ω, R1, R2 = 200Ω)



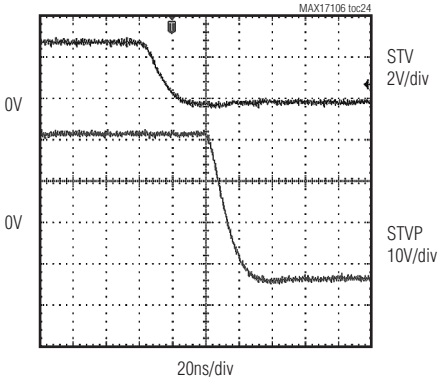
STV RISING EDGE PROPAGATION DELAY



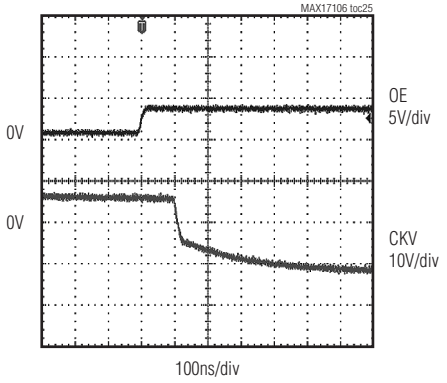
OE/CKV RISING EDGE PROPAGATION DELAY



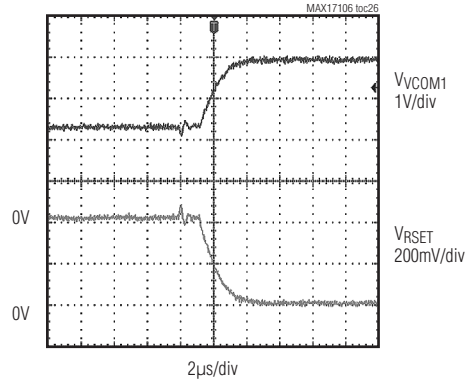
STV FALLING EDGE PROPAGATION DELAY



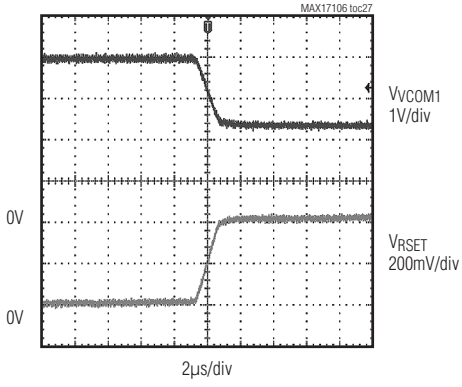
OE/CKV FALLING EDGE PROPAGATION DELAY



CALIBRATOR FULL-SCALE UPWARD STEP RESPONSE



CALIBRATOR FULL-SCALE DOWNWARD STEP RESPONSE



Pin Description

PIN	NAME	FUNCTION
1	SWP	VON Step-Up Regulator Switching Node. Connect inductor/catch diode here and minimize trace area for lowest EMI.
2	VON	Gate-On Supply Input. VON is the positive supply voltage for the CKV, CKVB, and STVP high-voltage scan-driver outputs. Bypass to SGND with a minimum of 0.1µF ceramic capacitor.
3	DISVSS	VSS Discharge Input
4	VOFF	Gate-Off Supply Input. VOFF is the negative supply voltage for the CKV, CKVB, and STVP high-voltage scan-driver outputs. Bypass to SGND with a minimum of 0.1µF ceramic capacitor.
5	CKVB	High-Voltage Gate-Pulse Output. CKVB is the inverse of CKV during active states and floats whenever CKV floats.
6	CKVBCS	CKVB Charge-Sharing Connection. CKVBCS connects to CKVB whenever CKVB floats to allow connection to CKV, sharing charge between the capacitive loads on these two outputs.
7	CKVCS	CKV Charge-Sharing Connection. CKVCS connects to CKV whenever CKV floats to allow connection to CKVB, sharing charge between the capacitive loads on these two outputs.
8	CKV	High-Voltage Gate-Pulse Output. When enabled, CKV toggles between its high state (connected to VON) or its low state (connected to VOFF) to float states on each falling edge of the CPV input. Further, CKV floats whenever CPV and OE are both low or whenever CPV is low and OECON is high.
9	STVP	High-Voltage Start-Pulse Output. STVP is low (connected to VOFF) whenever STV is low and is high (connected to VON) only when STV is high and CPV and OE are both low. When STV is high and either CPV or OE is high, STVP floats.
10	SGND	Scan Driver Ground
11	STV	Vertical Sync Input. The rising edge of STV begins a frame of data. The STV input is used to generate the high-voltage STVP output.
12	CPV	Vertical Clock-Pulse Input. CPV controls the timing of the CKV and CKVB outputs, which change state (by first sharing change) on its falling edge.
13	OECON	Active-Low Output Enable Timing Input. OECON is driven by an RC-filtered version of the OE input signal. If OE remains high long enough for the resistor to charge the capacitor up to the OECON threshold, the OE signal is masked until OE goes low and the capacitor is discharged below the threshold through the resistor.
14	OE	Active-High Gate-Pulse Output Enable Input. CKV and CKVB leave the floating charge-sharing state on the rising edge of OE.
15	DISH	VOFF Discharge Connection Input. Pulling DISH below ground activates an internal connection between VOFF and GND, rapidly discharging the VOFF supply. Typically, DISH is capacitively connected to VIN, so that when VIN falls, VOFF is discharged.
16	VDDS	Logic Supply Input. Supply input for the scan driver and other logic blocks. Bypass to SGND through a minimum 0.1µF capacitor.
17	VL	On-Chip 2.5V Regulator Output. This regulator powers the internal memory blocks. It is automatically powered by VIN or VDDE, whichever is present. Bypass VL to GND with a 1µF or greater ceramic capacitor.
18	AVDD	Operational Amplifier Supply Input. Connect to V_{MAIN} and bypass to CGND with a 1µF or greater ceramic capacitor.
19	VCOM3	Operational Amplifier Output
20	NEG3	Operational Amplifier Inverting Input
21	POS3	Operational Amplifier Noninverting Input

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Pin Description (continued)

PIN	NAME	FUNCTION
22	VCOM2	Operational Amplifier Output
23	NEG2	Operational Amplifier Inverting Input
24	POS2	Operational Amplifier Noninverting Input
25	VCOM1	Operational Amplifier Output
26	NEG1	Operational Amplifier Inverting Input
27	POS1	Operational Amplifier Noninverting Input
28	CGND	Amplifier Ground
29	OUT	Adjustable Sink-Current Output. OUT connects to the resistive voltage-divider (between AVDD and CGND) at one or more of the op amp inputs (POS_), which determine the VCOM output voltage. I_{OUT} lowers the divider voltage by a programmable amount.
30	RSET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{RSET}, from RSET to CGND to set the full-scale adjustable sink current. $I_{OUT} = V_{AVDD}/(20 \times R_{RSET})$.
31	VDDE	Logic Supply Input for the 2Kb EDID EEPROM and VCOM Calibrator. VDDE must be present (along with VDDE or VIN) to read from or write to the 2Kb EEPROM or VCOM calibrator. Logic levels for WPN, SCL, and SDA are relative to VDDE, although the memory is supplied by VL. Bypass VDDE to GND with a 0.1µF minimum ceramic capacitor.
32	GND	Logic Ground for I²C Interfaces
33	SDA	I²C-Compatible Serial Bidirectional Data Line. Data line for the 2Kb EDID EEPROM and VCOM calibrator settings.
34	SCL	I²C-Compatible Clock Input and Output for the 2Kb EDID EEPROM
35	WPN	Active-Low Write-Protect Input. When WPN is low, VCOM calibrator settings cannot be modified. WPN has a passive 240kΩ pulldown.
36	SDAT	I²C-Compatible Serial Bidirectional Data Line for 16Kb Timing Controller EEPROM
37	SCLT	I²C-Compatible Clock Input and Output for the 16Kb Timing Controller EEPROM
38	VDDT	Logic Supply Input for the 16Kb Timing Controller (TCON) EEPROM. VDDT must be present (along with VDDE or VIN) to read from or write to the 16Kb TCON EEPROM. Logic levels for SCLT and SDAT are relative to VDDT, although the memory is supplied by VL. Bypass VDDT to GND with a 0.1µF minimum ceramic capacitor.
39	LOUT	Internal 2.5V Linear Regulator Output. Bypass LOUT to LGND with a 10µF capacitor.
40	LGND	Linear Regulator Ground and IC Analog Ground
41	VIN	Main Step-Up Regulator Supply Input. Bypass VIN to LGND with a 4.7µF or greater ceramic capacitor. VIN is also the power input of the internal 2.5V linear regulator (LOUT).
42	$\overline{SHDN}$	Shutdown Control Input. Pull $\overline{SHDN}$ low to disable the step-up regulators. The memories, VCOM calibrator, op amps, LOUT, and scan drivers remain enabled.
43, 44	SW	Main Step-Up Regulator Switching Node. Connect the inductor and catch diode here and minimize the trace area for lowest EMI.
45, 46	PGND	Power Ground. Source connection of the internal main step-up regulator power switch.
47	COMP	Compensation Pin Output for Main Error Amplifier. Connect a series RC from this pin to LGND. Typical values are 100kΩ and 220pF.
48	FB	Main Feedback Pin Input. Connect external resistor-divider midpoint here and minimize trace area. Set V_{MAIN} according to: $V_{MAIN} = 1.235V (1 + R1/R2)$.
49	RHVS	HVS Open-Drain Output. Connect a resistor between RHVS and FB to adjust the main step-up regulator output voltage according to the logic input state of HVS.

Pin Description (continued)

PIN	NAME	FUNCTION
50	HVS	HVS Digital Control Input
51	NTC1	Thermistor Network Connection Input. Connect a network including a thermistor from NTC1 to LGND to control the temperature behavior of the VON output voltage. If thermal compensation is not used, connect NTC1 to LGND or LOUT.
52	NTC2	Thermistor Network Connection Input. Connect a network including a thermistor from NTC2 to LGND to control the temperature behavior of the VON output voltage. If thermal compensation is not used, connect NTC2 to VIN or LOUT.
53	VHI	VON High-Level (Low-Temperature) Reference Voltage Input. Connect a resistor from VHI to LGND to set the VON high-level reference level. The VHI output current is 100µA (typ). Connect to LGND if VON temperature compensation if not used.
54	VLO	VON Low-Level (High-Temperature) Reference Voltage Input. Connect a resistor from VLO to LGND to set the VON low-level reference level. The VLO output current is 100µA (typical). Connect to LGND if VON temperature compensation if not used.
55	FBP	VON Feedback Pin. Connect the external resistor-divider midpoint here and minimize trace area. Set the midtemperature VON output voltage according to: V_{VON} = 0.893V (1 + R3/R4).
56	GNDP	VON Step-Up Regulator Power Ground. Source connection of the internal VON step-up regulator power switch.
—	EP	Exposed Pad. Connect the exposed backside pad to LGND, GND, CGND, and PGND.

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

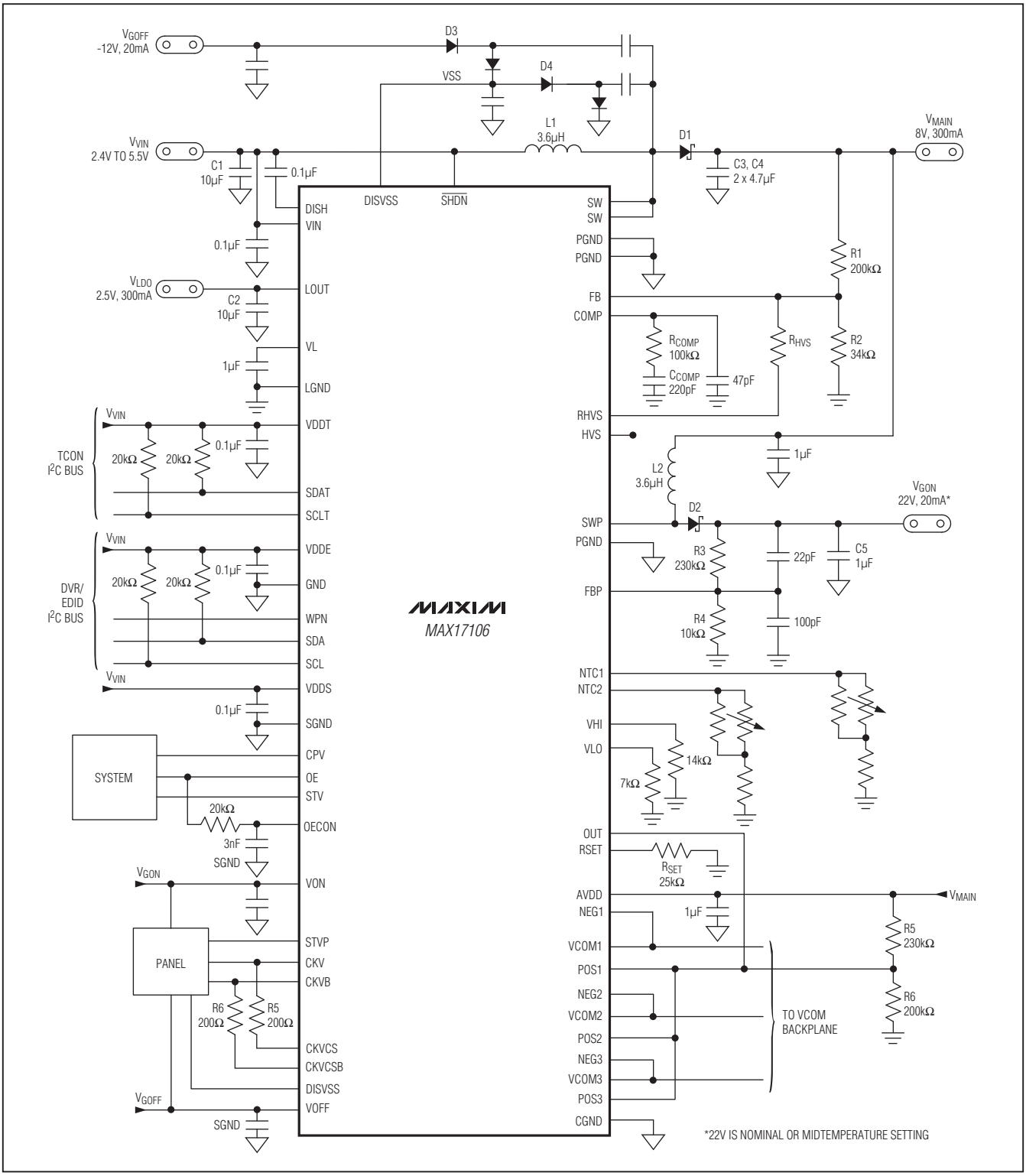


Figure 2. Typical Operating Circuit

Table 1. Components List

DESIGNATION	DESCRIPTION
C1, C2	10µF ±20% 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J106M or TDK C1608X5R0J106M
C3, C4	4.7µF ±10% 16V X5R ceramic capacitors (1206) Murata GRM319R61C475KA88D or TDK C3216X5R1C475K
C5	1µF ±20% 50V X5R ceramic capacitor (1206) Murata GRM31MR61H105M or TDK C3216X5R1H105M

DESIGNATION	DESCRIPTION
D1	3, 30V Schottky diode (M-Flat) Toshiba CMS02(TE12L,Q)
D2	1A ,60V Schottky diode (SOD-123F) Central CMMSH1-60+ Top mark CS60F
D3, D4	200mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE Central CMPD7000+
L1, L2	3.6µH, 1.8A power inductor Sumida CMD6D11BNP-3R6MC

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
Murata Electronics North America, Inc.	770-436-1300	www.murata.com
Sumida Corp.	847-545-6700	www.sumida.com
TDK Corp.	847-803-6100	www.component.tdk.com

Typical Operating Circuit

The typical operating circuit (Figure 2) of the MAX17106 is a complete power-supply system for TFT LCD panels in monitors. The circuit generates a +8V source driver supply from a +2.4V to +5.5V input. A second step-up regulator then generates a +22V positive gate-driver supply from this +8V source. The -12V negative gate-driver supply is derived using discrete components and the switching node (SW pin). An internal LDO regulator generates 2.5V at 300mA from the VIN supply voltage. Table 1 lists some selected components and Table 2 lists the contact information for the component suppliers.

Detailed Description

The MAX17106 contains a main fixed-frequency, current-mode, control step-up switching regulator to generate the source driver supply. A second step-up switching regulator generates the positive gate-driver supply. This regulator uses a minimum off-time, pulse-skipping architecture with a variable peak-current threshold. Its output is also temperature adjustable by connecting external temperature-sensing elements and resistors. The negative gate-driver supply can be easily derived using discrete components connected to the main step-up regulator's switching node (SW pin). An internal LDO regulator generates 2.5V at 300mA from the VIN supply voltage. The MAX17106 also includes three high-performance operational amplifiers designed to drive the LCD backplane (VCOM). The amplifier outputs are typically programmed using the IC's VCOM calibrator through an I²C interface. The 3-channel, high-voltage level-shifting scan driver is designed to drive active-matrix TFT panels. Figure 3 shows the MAX17106 functional diagram.

The low-dropout (LDO) linear regulator has a fixed output voltage of 2.5V and can supply at least 300mA. The high-current operational amplifiers are designed to drive the LCD backplane (VCOM). ODAMP1 and OPAMP2 feature high output current (±150mA), high slew rate (45V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs.

The programmable VCOM calibrator is externally attached to the middle of the VCOM amplifier's resistive voltage-divider and sinks a programmable current to adjust the VCOM voltage level. It is accessed through the 2Kb EDID EEPROM's I²C interface.

The high-voltage level-shifting scan driver is designed to drive the TFT panel gates. Its three outputs swing from +38V (maximum) to -18V (minimum) and can swiftly drive capacitive loads. To save power, the two complementary outputs (CKV and CKVB) are designed to allow charge sharing during state changes.

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

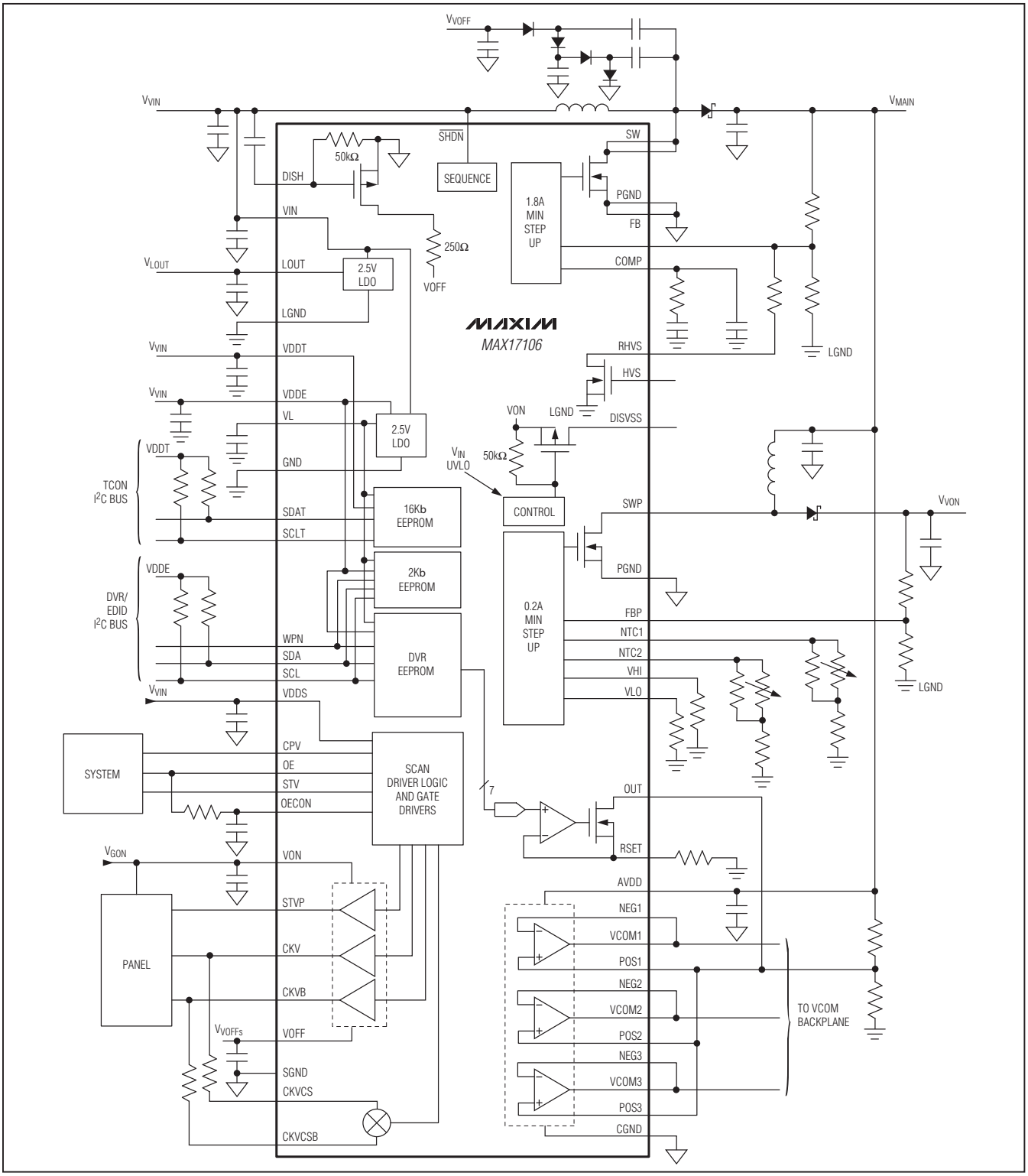


Figure 3. Functional Diagram

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Main Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads that are typical for TFT LCD panel source drivers. The 1.2MHz high-switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET reduces the number of external components required. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider.

The regulator controls the output voltage and the power delivered to the output by modulating duty cycle D of the internal power MOSFET in each switching cycle.

Figure 4 shows the functional diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on diode D1. The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

VON Positive Gate-Driver Step-Up Regulator

The VON step-up regulator employs a minimum off-time, modified fixed-current threshold, forced-discontinuous mode architecture for simple control and stable behavior with minimal output bypass. The fixed-current threshold was modified to a variable threshold that adjusts the threshold to lower losses when lightly loaded. Under light load, the VON regulator may also skip pulses.

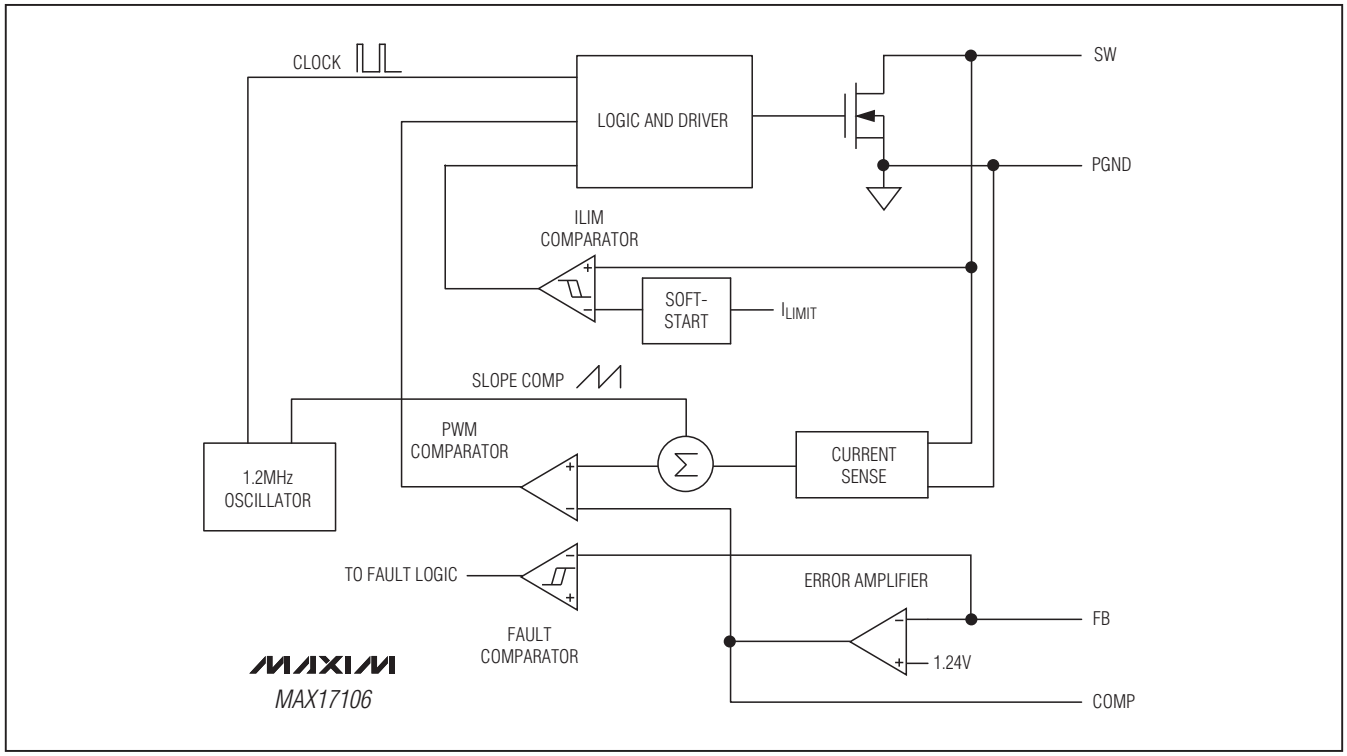


Figure 4. Main Step-Up Regulator Block Diagram

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

VON Temperature Compensation

The VON step-up regulator uses one or two NTC thermistors to adjust its output voltage for temperature changes. The feedback divider at FBP sets the nominal output voltage used only at midtemperatures. As temperature increases or decreases, the thermistor voltages are used to modify the VON output voltage. See the *VON Temperature-Compensated Step-Up Regulator* section for further information.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the input voltage at V_{IN} with the UVLO threshold (2.2V rising and 2.1V falling) to ensure that the input voltage is high enough for reliable operation. The 100mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator, VON step-up regulator, LOUT regulator, VCOM calibrator, and the op amp outputs are set to high impedance.

Power-Up Sequence and Soft-Start

During startup, once VIN or VDDE exceeds a rough internal UVLO, an internal reference starts. When the internal reference reaches regulation, VL starts. When VL reaches its UVLO and VIN exceeds its UVLO (2.2V), LOUT begins its 3ms soft-start and, if $\overline{SHDN}$ is high, the main step-up regulator begins its 13ms soft-start. After the main step-up soft-start is done, the VON step-up regulator begins its 3ms soft-start. Figure 5 shows the power-up sequence.

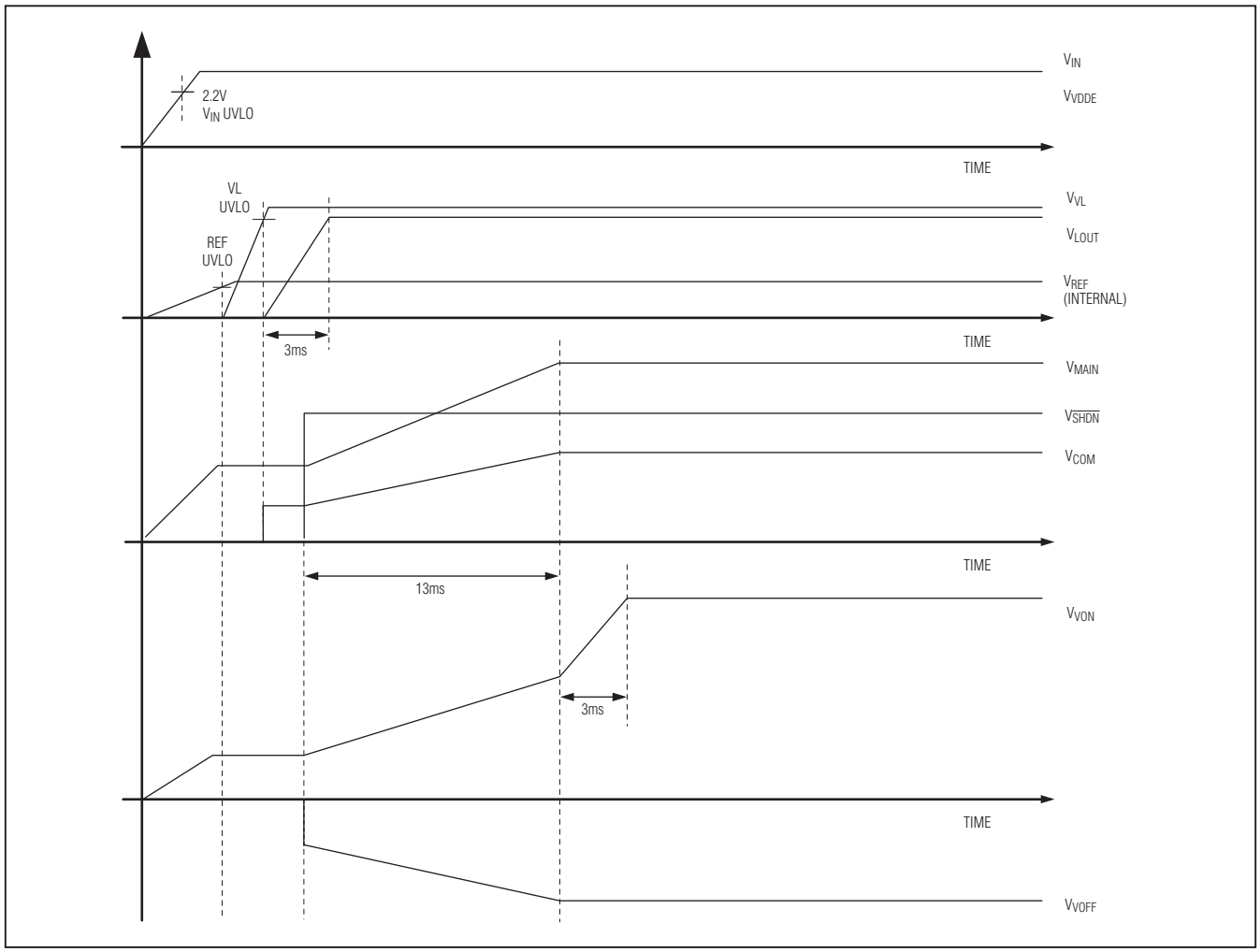


Figure 5. Power-Up Sequence

The soft-start routine minimizes the inrush current and voltage overshoot, and ensures a well-defined startup behavior. The LOUT and VON 3ms soft-start routines are a digitally controlled output voltage ramp. The main step-up's 13ms soft-start instead controls the step-up regulator's current limit, ramping it slowly from zero up to the full current limit over the 13ms period. The step-up regulator's output typically reaches regulation before the 13ms period finishes.

Operational Amplifiers

The MAX17106 has three operational amplifiers. These operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. OPAMP1 and OPAMP2 feature ±150mA output short-circuit current, 45V/µs slew rate, and 20MHz -3dB bandwidth. The rail-to-rail input and output capability maximizes system flexibility.

Short-Circuit Current Limit

The operational amplifiers deliver a minimum short-circuit current of ±150mA if the output is directly shorted to AVDD or to GND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor temporarily shuts off all the IC's outputs. See the *Thermal-Overload Protection* section for details.

Driving Pure Capacitive Loads

The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifiers. However, if an operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

VCOM Calibrator

The VCOM calibrator is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. A digitally controlled current source attaches to the external resistive voltage-divider at the POS_ terminals of the op amps and sinks a programmable current (I_{OUT}), which sets the VCOM level (Figure 6). An internal 7-bit digital-to-analog converter (DAC) controls the sink current and allows the user to increase or decrease the VCOM level. The DAC is ratiometrically 1/20 of V_{AVDD} and is monotonic over all operating conditions. The user can store the DAC setting in the internal nonvolatile EEPROM. On power-up, the EEPROM presets the DAC to the last stored setting. The 2-wire I²C interface between the system controller and the programming circuit is used to adjust the DAC and program the EEPROM when WPN is high.

The resistive voltage-divider and AVDD supply set the maximum value of VCOM. OUT sinks current from the voltage-divider to reduce the POS_ voltage level and VCOM_ output. The external resistor at RSET (R_{RSET}) sets the full-scale sink current and the minimum value of VCOM.

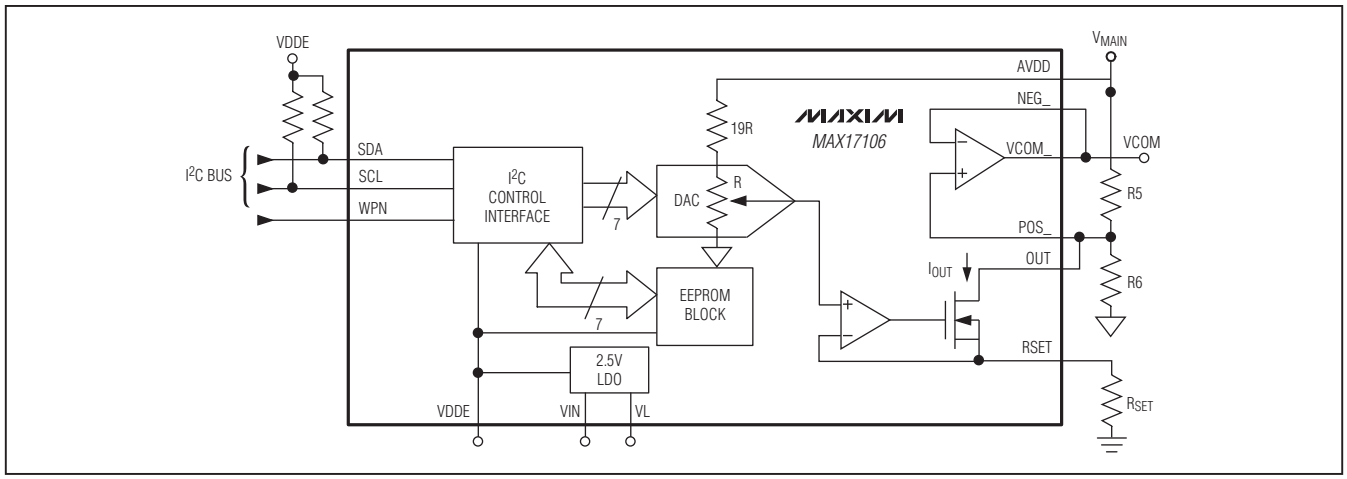


Figure 6. VCOM Calibrator Functional Diagram

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

The VL LDO powers the EEPROM. The LDO can be powered by VDDE or VIN. However, VDDE must be supplied to read or write the EEPROM.

High-Voltage Level-Shifting Scan Driver

The MAX17106 includes a 3-channel, high-voltage (56V) level-shifting scan driver that includes logic functions necessary to drive row driver functions on the panel glass (Figure 7). The driver outputs (CKV, CKVB, STVP) swing between their power-supply rails (VON and VOFF that have a maximum range of +38 and -18V) according to the input logic levels on the block's inputs (STV, CPV, OE, and OECON) and the internal logic of the block (Tables 3, 4). STV is the vertical sync signal. CPV is the horizontal sync signal. OE is the output enable signal. OECON is a timing signal derived from OE that blanks OE if it stays high too long. These signals have CMOS input logic levels set by the VDDS supply voltage. CKV and CKVB are complementary scan clock outputs. STVP is the output scan start signal. Their 20Ω (typ) output impedance enables them to swiftly drive capacitive loads. The complementary CKV and CKVB outputs feature power-saving, charge-sharing inputs (CKVCS, CKVBCS) that can be used to save power by shorting each output to its complement during transitions, making a portion of the transition lossless.

VOFF Rapid Discharge Function (DISH Input)

The DISH input controls a switch between VOFF and GND. When DISH is pulled below ground by at least 1V, VOFF is rapidly discharged to GND. Typically, DISH is capacitively coupled to VIN so that if VIN falls suddenly, VOFF is discharged to blank the display (Figure 3).

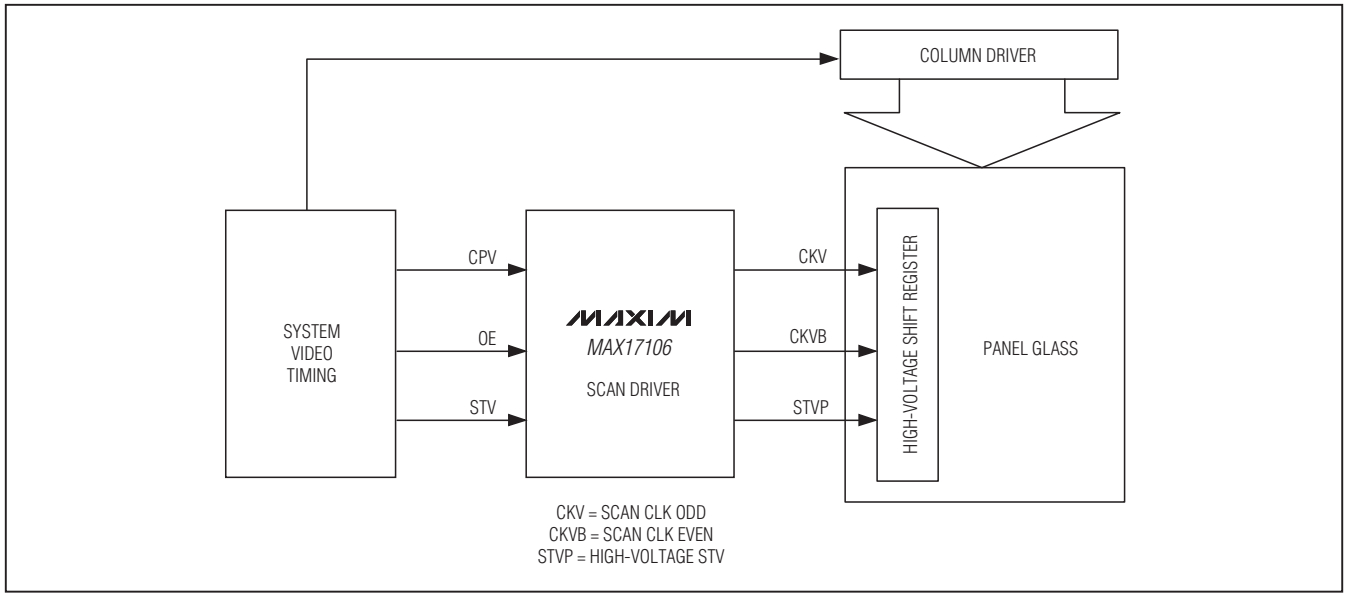


Figure 7. Scan Driver System Diagram

Table 3. STVP Logic

SIGNAL	LOGIC STATE			
STV	H	H	H	L
OECON	X	X	X	X
CPV	L	H	X	X
OE	L	X	H	X
STVP	H	High-Z	High-Z	L

X = Don't care.

Table 4. CKV, CKVB Logic

SIGNAL	LOGIC STATE							
STV	H	H	H	L	L	L	L	L
OECON	X	X	X	L	L	L	H	H
CPV	L	H	X	L	—	L	L	—
OE	L	X	H	L	L	—	X	X
CKV	L	H	H	CS	Toggle	Toggle	CS	Toggle
CKVB	H	L	L	CS	Toggle	Toggle	CS	Toggle

X = Don't care.
CS = Charge-share state.

VSS Rapid Discharge Function (DISVSS Input)

The DISVSS function shorts a negative panel terminal VSS connected at the DISVSS pin to the positive gate-driver rail VON when the IC powers down. Since these two supply rails have similar bypass capacitors (usually 20µF each), the final voltage on each supply should settle at the midvoltage between these two rails. The purpose of this function is to pull the negative rail substantially positive to discharge the LCD quickly. This function is only activated during power-down when VIN drops below its UVLO threshold.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds T_J = +160°C, a thermal sensor temporarily activates the fault protection, which shuts down all the IC's outputs, allowing the device to cool down. Once the device cools down by approximately 15°C, it automatically reactivates with a complete soft-start. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very-high-inductance values minimize the current ripple and therefore reduce the peak current, thereby decreasing core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost. The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 2's typical operating circuit, the LCD's negative gate-off supply voltage is generated from an unregulated charge pump driven by the main step-up regulator's SW node. The additional load on SW must therefore be considered in the inductance and current calculations. The LCD's positive gate-on supply voltage is generated through the VON step-up regulator that is also supplied by V_{MAIN}. Therefore, the main step-up's effective maximum output current, $I_{MAIN(EFF)}$ becomes the sum of the maximum load current of the step-up regulator's output, plus the contributions from the negative charge pump and the VON regulator:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + \eta_{NEG} \times I_{NEG} + \frac{V_{ON}}{V_{MAIN}} \times \frac{I_{VON(MAX)}}{\eta_{VON}}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, η_{NEG} is the number of negative charge-pump stages, I_{NEG} is the negative charge-pump output current, V_{ON} is the VON regulator's maximum output voltage, $I_{VON(MAX)}$ is the VON regulator's output current at the maximum output voltage, and η_{VON} is the VON regulator's efficiency under that condition and is approximately 90%.

Calculate the approximate inductor value using the typical input voltage (VIN), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency η_{MAIN} taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{MAIN}}{LIR}\right)$$

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point ($\eta_{MAIN(MIN)}$) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MAIN(MIN)}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17106's SW current limit should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit (Figure 2), the maximum load current ($I_{MAIN(MAX)}$) is 300mA, with an 8V output and a typical input voltage of 3V. Assume VON is 22V and its maximum load is 40mA. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 300mA + 2 \times 20mA + \frac{22V}{8V} \times \frac{40mA}{90\%} = 462mA$$

Choosing an LIR of 0.3 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{3V}{8V}\right)^2 \left(\frac{8V - 3V}{0.462A \times 1.2MHz}\right)\left(\frac{0.87}{0.3}\right) \approx 3.59\mu H$$

A 3.6µH inductor is chosen. Then, using the circuit's typical input voltage (3V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.462A \times 8V}{3V \times 0.8} \approx 1.54A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (8V - 2.4V)}{3.6\mu H \times 8V \times 1.2MHz} \approx 0.43A$$

$$I_{PEAK} = 1.54A + \frac{0.43A}{2} = 1.755A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C1) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. One 10µF ceramic capacitor is used in the typical operating circuit (Figure 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C1 can be reduced below the values used in the typical operating circuit. Ensure a low-noise supply at VIN by using adequate C_{IN}.

Rectifier Diode

The MAX17106's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Output Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to LGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{REF}} - 1\right)$$

where V_{REF}, the step-up regulator's feedback set point, is 1.235V (typ). Place R1 and R2 close to the IC.

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

HVS Function

Pulling the HVS pin high parallels R_{HVS} with the lower resistor-divider R2, thus regulating V_{MAIN} to a higher voltage $V_{MAIN(HIGH)}$. Pull the HVS pin to ground to disable this function:

$$(R2 \,||\, R_{HVS}) = \frac{R1}{\left(\frac{V_{MAIN(HIGH)}}{V_{REF}} - 1\right)}$$

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{1000 \times V_{IN} \times V_{MAIN} \times C_{MAIN}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{MAIN}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

VON Temperature-Compensated Step-Up Regulator

Selecting Component Values

The same procedure used to calculate the main step-up components can be used to calculate the VON regulator components. However, since the VON regulator application is very specific and the current is low, the component selection can be greatly simplified.

Choose an inductor with 2.7µH to 10µH inductance and a current rating of at least the SWP high-current limit value (2A typ). Within this range, a lower inductance value not only reduces cost and size, but also increases the single-cycle output ripple and thus improves stability. The output capacitor should be at least 1µF with a good dielectric that does not decrease in value excessively at high voltages. A larger capacitor value might be appropriate to account for the output capacitor's voltage coefficient.

Set the output voltage by selecting proper values for R3 and R4, the FBP divider resistors. Select R4 in the 10kΩ to 50kΩ range and calculate R3 with the following equation:

$$R3 = R4 \times \left(\frac{V_{ON(MID)}}{V_{REF}} - 1\right)$$

where $V_{ON(MID)}$ is the nominal midtemperature output voltage level and V_{REF} is 0.893V (typ).

To improve the regulator's performance, add a small feed-forward zero capacitor (for example, 20pF) in parallel with R3. This feed-forward capacitor increases the bandwidth of the regulator and reduces pulse grouping. An additional capacitor (for example, 100pF) placed in parallel with R4 can be used to filter out the noise and reduce jitter. A larger capacitor would excessively cancel the feed-forward zero in parallel with R3 and thus would not bring further improvement.

VON Temperature Compensation

The VON step-up regulator uses one or two NTC thermistors to adjust its output voltage for temperature changes. The feedback divider at FBP sets the nominal output voltage used only at midtemperatures. As the temperature increases or decreases, the NTC_ voltages are used to modify the VON output voltage.

The output has three level ranges and two sloped ranges over temperature (see Figure 8). The first level range is the high-level output voltage, which is set by the voltage on the VHI pin and is used at cold temperatures. The second level range is the nominal output voltage set by the 0.893V (typ) internal reference voltage. The lower level output is set by the voltage on the VLO pin and is used at high temperatures. The high level and low level are set by the current sources at the VHI and VLO pins, and the resistors placed between those pins and LGND. The sloped regions are used between the level ranges to create a smooth continuous curve and are created by the changing voltage levels on the NTC1 and NTC2 pins and the thermistor networks attached to those pins.

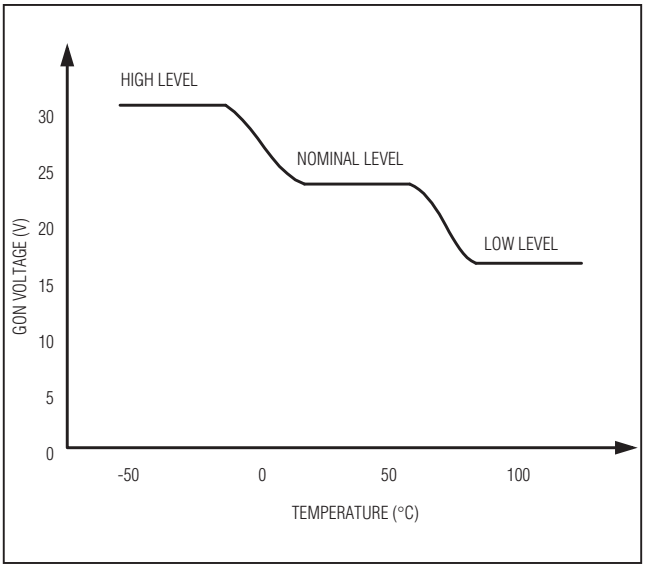


Figure 8. VON Temperature Compensation Curve

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

The VHI voltage is used as the reference for FBP whenever the voltage on NTC1 is greater than the voltage on VHI. The curve between the high-level range and the nominal-level range is determined directly by the voltage on the thermistor network at the NTC1 pin, which is used whenever the NTC1 pin voltage is both greater than the nominal internal reference voltage and less than the VHI voltage. The nominal reference voltage is used whenever the NTC1 voltage is less than the nominal reference. The curve between the nominal-level range and the low-level range is determined directly by the voltage on the thermistor network at the NTC2 pin, and is used whenever the NTC2 pin voltage is both less than the nominal FBP reference voltage and greater than the VLO voltage and NTC1 is also less than the nominal FBP reference level. The VLO voltage is used as the reference whenever the NTC2 voltage is less than the VLO voltage and the NTC1 voltage is less than the nominal reference voltage.

This can be described in a logic language as follows:

Feedback Reference = IF (V_{NTC1} > V_{VHI}) THEN use V_{HI}
ELSE IF (V_{NTC1} > REF) THEN use V_{NTC1}
ELSE IF (V_{NTC2}>REF) THEN use REF
ELSE IF (V_{NTC2} > V_{VLO}) THEN use V_{NTC2}
ELSE use V_{LO}

where REF is the internal 0.893V reference.

The result is that, with the proper external components, the FBP voltage level varies smoothly over temperature from VHI at low temperatures to VLO at high temperatures. The external components can be selected to adjust these levels and at what temperatures these transitions occur.

The high level and low level are set by the current sources at VHI and VLO, and the resistors placed there to LGND:

$$V_{HI} = I_{VHI} \times R_{VHI}$$
$$V_{LO} = I_{VLO} \times R_{VLO}$$

where I_{VLO} is the source current from the VLO pin and I_{VHI} is the source current from the VHI pin.

The NTC_ levels are created by the current sources at NTC1 and NTC2, and the thermistor networks placed there to LGND. Typically, the thermistor is a 10kΩ value and the network includes a series resistor and a parallel resistor. Two thermistor networks are proposed here (Figure 9); however, any suitable network can be used. For complete flexibility and independence on each curve, two thermistors are required. However, most applications can be adequately met with the single-thermistor network shown. This application works because the temperature-compensation network is designed to source current from only one NTC_ pin at a time.

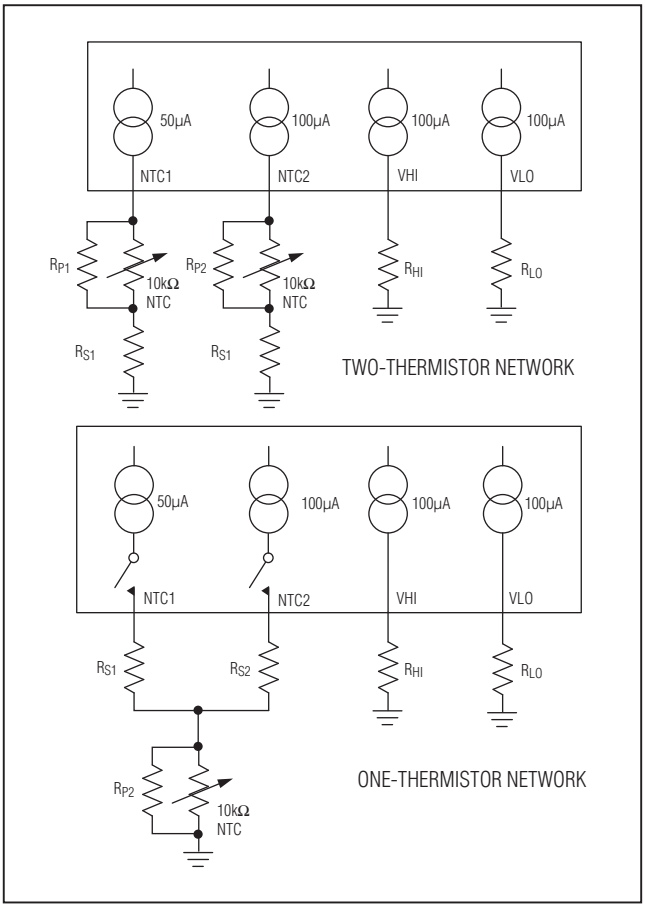


Figure 9. Thermistor Compensation Network

The current sources at NTC1 and NTC2 have different output currents to facilitate using two identical thermistors to create different temperature curve characteristics.

Setting the VCOM Adjustment Range

The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{RSET} sets the full-scale sink current, I_{SET}, which determines the minimum value of the VCOM adjustment range. Large R_{SET} values increase resolution but decrease the VCOM adjustment range. Calculate R5, R6, and R_{SET} using the following procedure:

Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the AVDD supply voltage (V_{AVDD}).

Select R5 between 10kΩ and 500kΩ based on the acceptable power loss from the V_{MAIN} supply rail connected to AVDD:

1) Calculate R6:

$$R6 \cong \frac{V_{MAX}}{AVDD - V_{MAX}} \times R5$$

2) Calculate R_{SET}:

$$R_{SET} = \frac{AVDD}{20} \times \frac{R5//R6}{V_{MAX} - V_{MIN}}$$

3) Verify that I_{SET} does not exceed 120µA:

$$I_{SET} = \frac{V_{AVDD}}{20 \times R_{SET}}$$

If I_{SET} exceeds 120µA, return to step 2 and choose a larger value for R5.

The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example is given below:

V_{MAX} = 4V, V_{MIN} = 2.4V, V_{MAIN} = 8V

If R5 = 200kΩ, then R6 = 200kΩ and R_{SET} = 25kΩ.

Resolution = 12.6mV

Fault Protection

If FB or FBP is lower than 0.1V, the relative step-up regulator is disabled. If FB or FBP is continuously below 80% of its regulation level for more than 50ms (typ), all three outputs (V_{MAIN}, V_{ON}, and V_{LOUT}) are disabled for 160ms and then go through a full soft-start process. If the fault remains, this process repeats up to three times. After the final shutdown, the fault condition is latched. Recycle the power to start the part again.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The 7mm x 7mm, 56-pin TQFN package can dissipate 2400mW (derated 40mW/°C above +70°C) for a single-layer board. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the two step-up regulators, the operational amplifiers, and the high-voltage scan-driver outputs.

Main Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal the MOSFET. It includes conduction loss and switching loss. The worst-case conduction loss occurs when the device is operating from the lowest expected input voltage, with the highest regulation output voltage, and at the maximum output current allowed by the current limit of the SW switch. The conduction loss can be estimated as:

$$PD_{CONDUCTION(MAIN)} = (I_{IN}^2 + \frac{I_{RIPPLE}^2}{12}) \times D \times R_{SW}$$

where:

$$I_{IN} = \frac{V_{MAIN} + V_{DIODE}}{V_{IN} - V_{SW}} \times I_{MAIN}$$

is the input current:

$$D = \frac{V_{MAIN} + V_{DIODE} - V_{IN}}{V_{MAIN} + V_{DIODE} - V_{SW}}$$

is the duty factor, V_{DIODE} is the voltage drop across diode, V_{SW} is the voltage drop across MOSFET. R_{SW} is the MOSFET on-resistance. I_{RIPPLE} is inductor ripple current, which is usually small compared to I_{IN} and thus can be ignored.

Assuming normal operation with V_{IN} = 3V, V_{MAIN} = 8V, I_{MAIN} = 300mA, f_{SW} = 1.2MHz, L_1 = 3.6µH, R_{SW} = 240mΩ, V_{DIODE} = 0.5V, V_{SW} = 240mV, the total conduction loss is $PD_{CONDUCTION(MAIN)}$ = 140mW.

The switching loss can be estimated as:

$$PD_{SWITCH(MAIN)} = V_{MAIN} \times I_{IN} \times \frac{t_{RSW} + t_{FSW}}{2} \times f_{SW}$$

where t_{RSW} is switching node rising time and t_{FSW} is switching node falling time. If $t_R = t_F$ = 15ns, the switching loss is PD_{SWITCH} = 134mW.

Operational Amplifiers

The power dissipated in the operational amplifiers depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM(SOURCE)} \times (V_{AVDD} - V_{COM})$$

$$PD_{SINK} = I_{VCOM(SINK)} \times V_{COM}$$

where V_{AVDD} is the supply voltage, $I_{VCOM(SOURCE)}$ is the output current sourced by one operational amplifier, and $I_{VCOM(SINK)}$ is the output current that the operational amplifier sinks.

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

In a typical case where the supply voltage is 8V and the output voltage is 4V with an output source current of 30mA, the power dissipated for all three op amps is 360mW.

Scan Driver Outputs

The power loss due to the scan driver outputs is:

$$PD_{SCAN} = C_{PANEL} \times (V_{VON} - V_{VOFF})^2 \times f_{SCAN} \times 3$$

where f_{SCAN} = 50kHz is the scan frequency and C_{PANEL} is the total panel capacitor.

However, it is unlikely that all this power is dissipated in the IC, since the total power dissipation is shared by both the level shifter switch resistances and the panel resistance.

VON Step-Up Regulator

Since the VON step-up regulator always runs in discontinuous conduction mode (DCM), the power-loss estimation is different from the main step-up regulator. The VON regulator operates by performing pulses asynchronously on demand, as long as the minimum off-time has expired. During the on-time, the inductor is charged and the load is serviced by the inductor discharge current. The output current is:

$$I_{VON} = \frac{I_{PK} \times t_{DIS}}{2 \times T}$$

where I_{PK} is the SWP current limit (1.2A typical for full output currents), t_{DIS} is the inductor discharge time, and T is the pulse period. Solving for T:

$$T = \frac{I_{PK} \times t_{DIS}}{2 \times I_{VON}}$$

and:

$$t_{DIS} = \frac{L2 \times I_{PK}}{V_{VON} - V_{MAIN}}$$

Therefore:

$$T = \frac{I_{PK}^2 \times L2}{2 \times I_{VON} \times (V_{VON} - V_{MAIN})}$$

The conduction losses are:

$$PD_{CONDUCTION\_GON} = \frac{t_{ON} \times I_{PK}^2 \times R_{SWP}}{3T}$$

where R_{SWP} is the on-resistance and:

$$t_{ON} = \frac{L2 \times I_{PK}}{V_{MAIN}}$$

So:

$$PD_{CONDUCTION\_GON} = \frac{2 \times I_{PK} \times R_{SWP} \times I_{VON} \times (V_{VON} - V_{MAIN})}{3 \times V_{MAIN}}$$

Assuming normal operation with V_{MAIN} = 8V, V_{ON} = 22V, I_{PK} = 12A, I_{VON} = 20mA, f_{SW} = 1.2MHz, L_2 = 3.6µH, R_{SWP} = 2Ω, $PD_{CONDUCTION\_VON}$ = 56mW.

Since the VON step-up regulator operates in DCM, the switch turn-on occurs at zero inductor current and it is lossless. Switching losses occur at the turn-off, where the inductor current is I_{PK}. The power loss can be estimated as:

$$PD_{SWITCH(VON)} = \frac{V_{VON} \times I_{PK} \times t_{FSWP}}{2T}$$

where t_{FSWP} is the SWP node falling time, estimated as 15ns.

Substituting for the period t:

$$PD_{SWITCH(VON)} = \frac{V_{VON} \times (V_{VON} - V_{MAIN}) \times t_{FSWP} \times I_{VON}}{I_{PK} \times L2}$$

Assuming normal operation with V_{VON} = 22V, V_{MAIN} = 8V, I_{VON} = 0.02A, I_{PK} = 1.2A, and L2 = 3.6 µH:

$$PD_{SWITCH(VON)} = 21mW$$

Total Power Dissipation

Combining all of the above together, the total power consumed by the IC is approximately 1W.

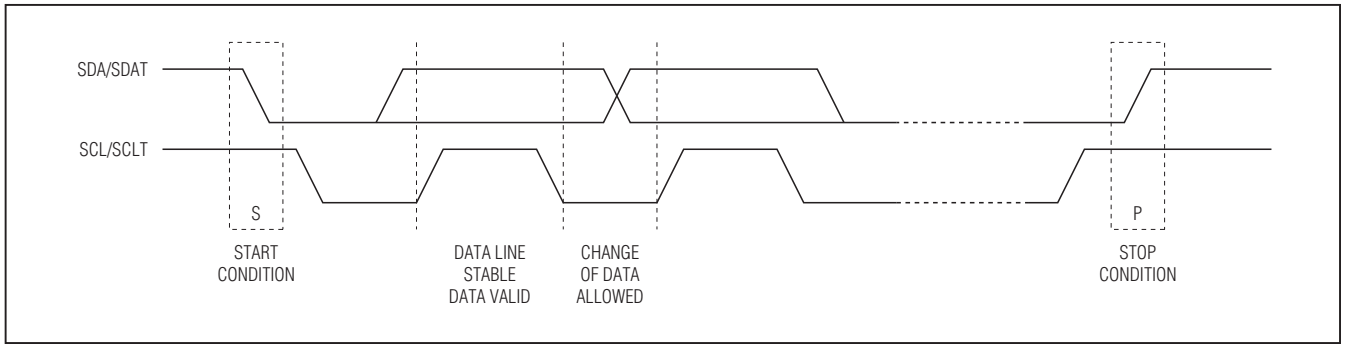


Figure 10. I²C Bus START, STOP, and Data Change Conditions

2-Wire I²C Interface

The MAX17106 is a slave-only device. There are two 2-wire I²C-bus-like serial interfaces (pin pair SCL/SDA and SCLT/SDAT). These interfaces are designed to attach to 2.4V to 3.6V I²C buses. Connect SCL and SDA to the VDDE supply through individual pullup resistors. Connect SCLT and SDAT to the VDDT supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics*, and C_{BUS} is the total capacitance on the bus.

The MAX17106 uses a nonstandard I²C interface protocol with standard voltage and timing parameters, as defined in the following subsections.

Bus Not Busy

Both data and clock lines remain high. Data transfers can be initiated only when the bus is not busy (Figure 10).

Start Data Transfers

Starting from an idle bus state (both SDA and SCL, or SDAT and SCLT, are high), a high-to-low transition of the SDA/SDAT line while the clock (SCL/SCLT) is high determines a START condition. All commands must be preceded by a START condition from a master device on the bus.

Stop Data Transfer (P)

A low-to-high transition of the SDA/SDAT line while the clock (SCL/SCLT) is high determines a STOP condition. All operations must be ended with a STOP condition from the master device.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. The master generates one clock pulse per bit of data during write operations and the slave device outputs 1 data bit per clock pulse during read operations. Each data transfer is initiated with a START condition and terminated with a STOP condition. Any number of bytes can be transferred between the START and STOP conditions.

Slave Address

The standard I²C slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 11). For a read operation, the R/$\overline{W}$ bit is 1 and for write operations, it is 0.

Set A2A1A0 = 000 and use SCL and SDA to access 2Kb EDID EEPROM. Set A2A1A0 to the proper block address and use SCLT and SDAT to access all the eight memory blocks of 16Kb TCON EEPROM. Since each memory block has its own I²C interface, there is no address conflict.

To access the VCOM calibrator (DVR), use SCL and SDA and set the slave address to 1001111x.

After generating a START condition, the bus master transmits the slave address to the MAX17106. The MAX17106 monitors the bus for its corresponding slave address continuously. It generates an acknowledge bit if it recognizes its slave address and it is not in busy processing another request.

An address byte is shown in Figure 11.

Write Single/Multiple Bytes

A data byte has 8 bits of information transferred from master to slave with MSB first. To write single or multiple bytes, the master generates a START condition, writes the IC's slave address byte with R/$\overline{W}$ = 0, waits for the slave to acknowledge, writes the memory start address, waits for the slave to acknowledge, writes some number of data bytes waiting for the slave to acknowledge each byte, and finally generates a STOP condition. See Figure 12.

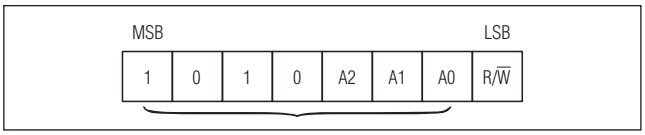


Figure 11. Address Byte

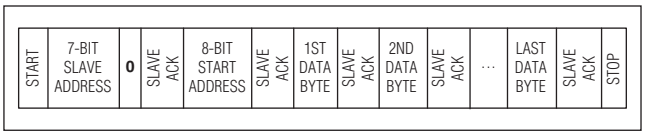


Figure 12. Writing Sequence

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Read Single/Multiple Bytes

Unlike writing, which requires a specified memory address to define where the data is to be written, the read operation reads the memory beginning with the last address read or written. To read data from a specific memory location, the master needs to use a dummy write operation to set the start address, and then read from that location. After every byte has been read out, the device waits for the master to acknowledge. After the last byte has been read out, instead of giving an acknowledge, the master gives out a STOP condition. See Figure 13.

Acknowledge/Polling

The MAX17106, when addressed, generates an acknowledge pulse after the reception of each byte. The master device generates an extra clock pulse, which is associated with this acknowledge bit. The device that acknowledges pulls down the SDA/SDAT line during the acknowledge clock pulse in such a way that the SDAT/SDA line is stable low during the high period of the acknowledge-related clock pulse (see Figure 14). Of course, setup and hold times must be taken into account. The master signals an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

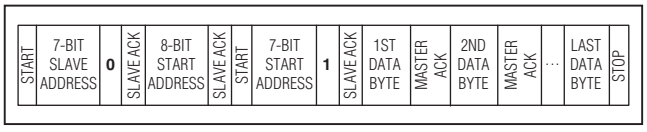


Figure 13. Reading Sequence

Memory Control

The 2Kb EDID memory and the VCOM calibrator DVR register share one I²C interface. Therefore, only one of them can be accessed at a time. The two devices are treated as a single memory block. The 16Kb timing controller (TCON) memory has its own independent I²C interface.

Simultaneous read operation of both memory blocks is supported. Both I²C interfaces output the corresponding memory data. For all the other simultaneous operations of the memory blocks, one of the I²C interfaces will NACK (not acknowledge) until the other has finished its operation. However, it cannot be predetermined which interface will receive a NACK.

Accessing the 16Kb TCON Memory

VDDT and either VDDE or VIN must be supplied in order to access the 16Kb TCON memory.

Both single and multiple-byte read operations are supported. For multiple-byte reads, the memory outputs data bits on each clock pulse from the master until an I²C STOP condition occurs. If the memory reaches the last byte of the physical memory, it restarts from the first byte again.

Write operations must start from the first byte and progress sequentially in 16-byte write operations without stopping until the end of the memory is reached. After the first 16 bytes is written, the master must wait 55ms before the next 16 bytes can be written. During this time, the entire 16 bytes of memory are erased. All subsequent write operations need only 0.8ms between each 16-byte operation.

Follow the above procedure to correctly read or write the 16Kb memory.

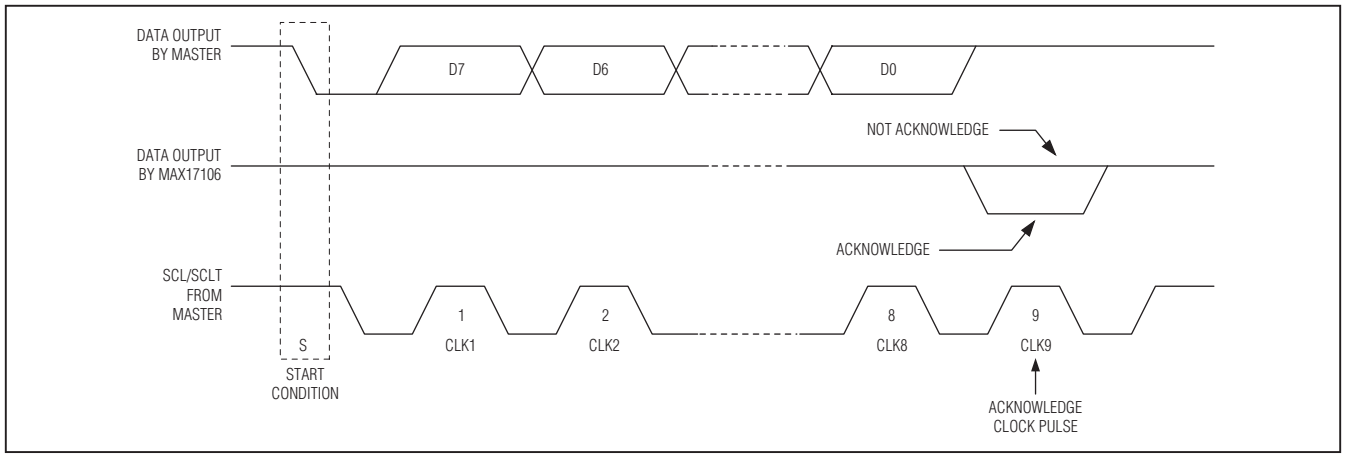


Figure 14. I²C Bus Acknowledge

Accessing the 2Kb EDID Memory

VDDE must be supplied to access the 2Kb EDID memory.

Both single- and multiple-byte read operations are supported. For multiple-byte reads, the memory outputs data bits on each clock pulse from the master until an I²C stop occurs. If the memory reaches the last byte of the physical memory, it restarts from the first byte again.

Write operations must start from the first byte and progress sequentially in either 1-byte or 8-byte operations without stopping until the end of the memory is reached. Once starting with a single-byte write operation, the complete memory must be written in single-byte operations. Similarly, once starting with an 8-byte write operation, the complete memory must be written in 8-byte operations. Switching between 1-byte and 8-byte operations is not supported.

After the first single-byte or 8-byte write operation, the master must wait 55ms before the following write operation. During this time, the entire 16Kb of memory are erased. All subsequent write operations need only 0.5ms between each write operation

Follow the above procedure to correctly read or write the 16Kb memory.

Accessing the VCOM Calibrator DVR 7-Bit Register

The VCOM calibrator register contains both a volatile register (VR) and nonvolatile register (NVR). The volatile register controls the VCOM calibrator operation. The nonvolatile register is automatically copied to the volatile register at power-up to set the VCOM output voltage.

VDDE must be present to access the nonvolatile register. When writing to the VCOM calibrator, the calibrator data byte contains a 7-bit setting and a program bit (LSB). If the program bit is 1, the data is written only into the volatile register. If the program bit is 0, the data is written into both the volatile and nonvolatile registers. For read operations, the program bit is a don't-care bit. WPN must be high to write to either the volatile or nonvolatile registers.

Read operations to the VCOM calibrator return the data stored in the nonvolatile register. Read operations can be performed whether WPN is low or high.

Table 5 lists the DAC values and the corresponding I_{SET}, V_{SET}, and V_{OUT} values.

Table 5. DAC Settings

7-BIT DATA BYTE	I_{RSET}	V_{RSET} (V)	V_{COMX} (V)
1111111	$I_{RSET(MAX)}$	$V_{RSET(MAX)}$	V_{MIN}
1111110	$I_{RSET(MAX)}$ - 1 LSB	$V_{RSET(MAX)}$ - 1 LSB	V_{MIN} + 1 LSB
. . .	. . .	. . .	. . .
00000001	$I_{RSET(MIN)}$ + 1 LSB	$V_{RSET(MIN)}$ + 1 LSB	V_{MAX} - 1 LSB
00000000	$I_{RSET(MIN)}$	$V_{RSET(MIN)}$	V_{MAX}

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the SW (SWP) and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's SW (SWP) pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode D1 (D2), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, try to use them only in the loop segments that have continuous current (not switched currents) and use many vias in parallel to reduce resistance and inductance. For a step-up converter, the segment between the input capacitor and the inductor has continuous current.

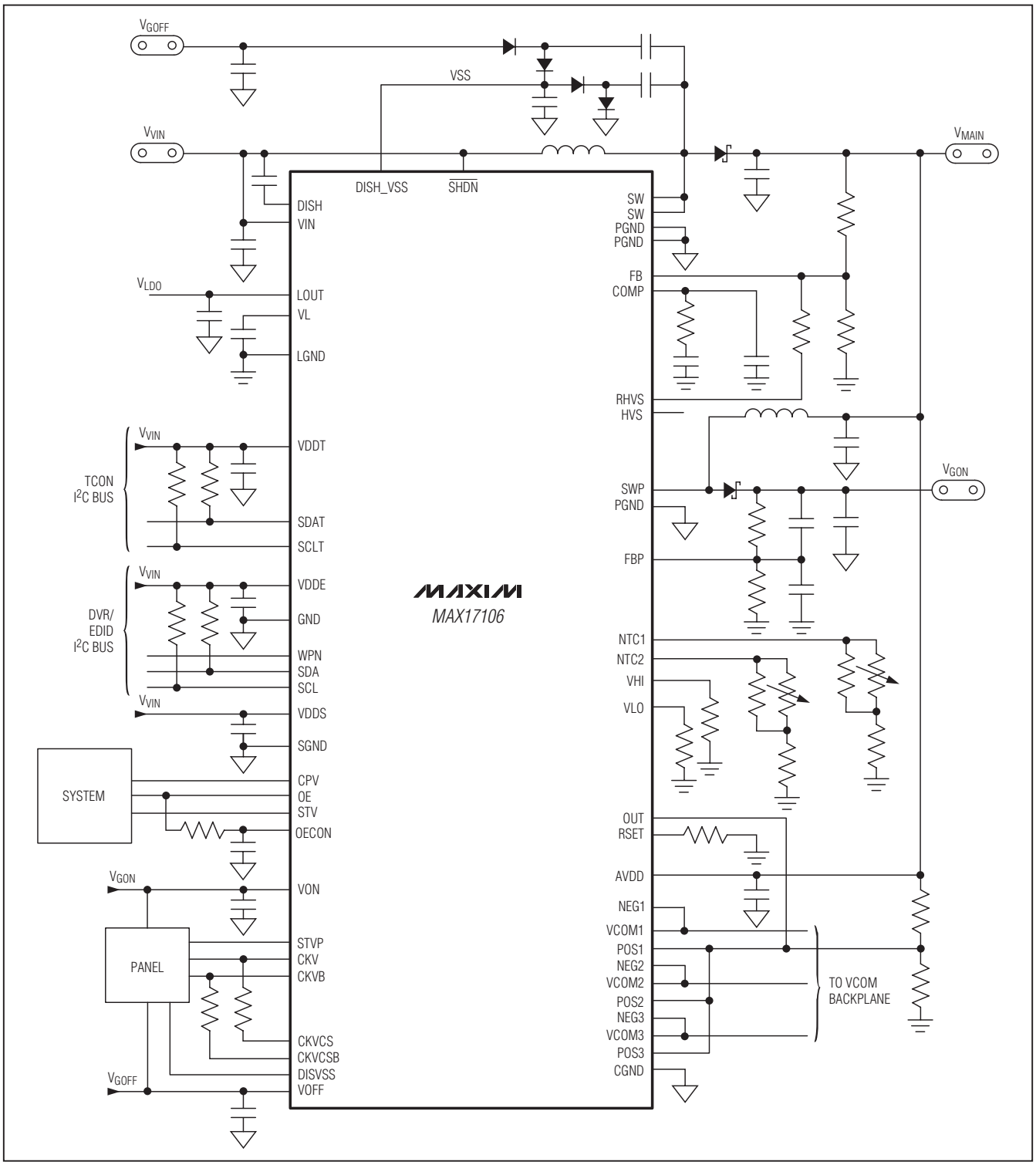
Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

- Create a power ground island for the main step-up converter consisting of the input and output capacitor grounds, PGND pins (45, 46) and any charge-pump component grounds. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create a second power ground island for the VON step-up converter consisting of the input and output capacitor grounds and the PGND pin (56). Connect these together with short, wide traces or a small ground plane. Since the VON step-up's input capacitor is in parallel with the main step-up's output capacitor, connect these two PGND islands together with a wide trace between these capacitor grounds or make it one big island or ground plane.
- Create an analog ground plane (LGND) consisting of the LGND pin, all the feedback-divider ground connections, the operational amplifier divider ground connections, the COMP capacitor ground connection, the AVDD capacitor ground connection, and the device's exposed backside pad. Connect the LGND island to the two PGND islands by connecting only one PGND pin (45) directly to the exposed backside pad. Make no other connections between these separate ground planes. Multiple connections cause PGND currents to pass through and disturb the LGND ground plane.
- Place the feedback-voltage-divider resistors as close as possible to the feedback pin. The divider's center trace should be kept short. Placing the resistors far away causes the feedback traces to become an antenna that can pick up switching noise. Care should be taken to avoid running a feedback trace near any step-up or charge-pump switching nodes.
- Place the VIN pin bypass capacitor as close as possible to the device. The ground connections of the VIN bypass capacitor should be connected directly to the LGND pin or the backside pad with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the step-up converter switching nodes while keeping them wide and short. Keep these nodes away from the feedback node and analog ground. Use DC traces as shields if necessary.

Refer to the MAX17106 evaluation kit for an example of proper board layout.

Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Simplified Operating Circuit



Step-Up Regulator and High-Voltage Step-Up with Temperature Compensation

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN	T5677MN+1	21-0144