MAX2990

10kHz to 490kHz OFDM-Based Power Line Communication Modem

General Description

The MAX2990 power line communication (PLC) baseband modem delivers a cost-effective, reliable, halfduplex asynchronous data communication over AC power lines at speeds up to 100kbps. The MAX2990 is a highly integrated system-on-chip (SoC) that combines the physical (PHY) and media access control (MAC) layers using Maxim's 16-bit MAXQ microcontroller core. The MAX2990 utilizes OFDM modulation techniques to enable robust data communication using the same electrical network that supplies power to all other devices on the network.

The MAX2990 includes the MAXQ microcontroller core. The MAXQ is a 16-bit RISC microcontroller with 32kB flash memory, 5.12kB of ROM, and 8kB SRAM, of which 4kB that can be simultaneously accessed by the MCU and the PHY. The MAX2990 is integrated with modules for serial communication (SPI™, I²C, UART) and a real-time clock (RTC) for time stamping, in addition to standard blocks such as timers, GPIO, and external interrupts.

The MAX2990 transceiver is based on an orthogonal frequency division multiplexing (OFDM) technique that allows robust data transmission over poor channel conditions specifically for environments with impulsive noise. OFDM with binary phase shift key (BPSK) and forward error correcting (FEC) blocks are used because of their inherent adaptability in the presence of frequency selective channels without the use of equalizers, resilience to jammer signals, robust communications in the presence of group delay spread, and robustness to impulsive noise. The MAX2990 features jammer cancellation that removes constant sinusoidal interference signals for FCC and ARIB bands. Privacy is provided by DES encryption.

The MAX2990 is available in a 64-pin LQFP package and is specified over the -40°C to +85°C extended temperature range.

Applications

- Automatic Meter Reading
- Home Automation
- Heating Ventilation and Air Conditioning (HVAC)
- Building Automation
- Industrial Automation
- Lighting Control
- Sensor Control and Data Acquisition
- Remote Monitoring and Control
- Voice-Over-Powerline
- Security Systems/Keyless Entry

SPI is a trademark of Motorola, Inc.

Features

- Combines the Physical Layer (PHY) and Media Access Controller (MAC)
- Integrated Microcontroller with 32kB Password-Protected Flash Memory and 8kB SRAM
- Maximum Effective Data Rate in Normal Mode
  32kbps at 10kHz to 95kHz and 100kbps at 10kHz to 490kHz
- Complies with
  CENELEC A (10kHz to 95kHz)
  CENELEC B (95kHz to 120kHz)
  CENELEC C (120kHz to 140kHz)
  FCC (10kHz to 490kHz)
  ARIB (10kHz to 450kHz)
- Includes Forward Error Correction (FEC) Mechanism and CRC16
- Includes Fast DES Engine as the Encryption/Decryption Coprocessor and CRC32
- Jammer Cancellation for FCC and ARIB
- User-Configured Start and End Operating Frequency
- Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) Channel Access Arbitration
- Automatic Repeat Request (ARQ) to Enhance Error Detection and Improve Data Reliability
- Supports SPI, I²C, and UART Interfaces
- Real-Time Clock (RTC)
- PWM Counters
- Built-In Test Mode Engine for Identifying Channel Conditions

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2990ECB+	-40°C to +85°C	64 LQFP

+Denotes a lead-free package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit appears at end of data sheet.

19-4116; Rev 0; 4/08

maxim integrated™

Absolute Maximum Ratings

V_{DDIO} to DGND .....-0.5V to +3.6V
V_{DDC} to DGND .....-0.5V to +1.98V
AV_{DD} to AGND .....-0.5V to +1.98V
Port0, Port1, Port2 to GPIO .....-0.5V to +5.5V
XTAL1S, XTAL2S, XTAL1A, XTAL2A.....-0.5V to +1.98V
All Other Pins .....-0.5V to +3.6V
Continuous Power Dissipation (T_A = +70°C)
64-Pin LQFP (derate 23.8mW/°C above +70°C) 1905mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
64-Pin LQFP.....8°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
64-Pin LQFP.....42°C/W
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+3.3V I/O Supply Voltage	V_{DDIO}		3.0	3.3	3.6	V
+1.8V Core Supply Voltage	V_{DDC}		1.70	1.80	1.98	V
+1.8V Analog Core Supply	AV_{DD}		1.70	1.80	1.98	V
High-Level Output Voltage	V_{OH}	I_{HIGH} = -4.0mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{LOW} = 8.0mA			0.4	V
High-Level Output Voltage: GPIO Clock Pad	V_{OHG}	I_{HIGH} = -8.0mA	2.4			V
Output Low Voltage GPIO	V_{OLG}	I_{LOW} = 8.0mA			0.4	V
Input High Voltage (Port0 to Port2)	V_{IH1}		0.7 x V_{DDIO}		5.5	V
Input High Voltage (Port3)	V_{IH2}		0.7 x V_{DDIO}		V_{DDIO}	V
Input High Voltage (XTAL1A, XTAL2A, XTAL1S, XTAL2S)	V_{IHXT}		0.7 x V_{DDC}		V_{DDC}	V
Input Low Voltage	V_{IL}		V_{SS}		0.3 x V_{DDC}	V
Input Hysteresis	V_{IHYS}		0.2	0.5		V
Input Leakage Current	I_I	Internal pullup disabled	-100		+100	µA
GPIO Pullup Resistance	R_{PU}	Internal pullup enabled		80		kΩ
	R_{PU3}			40		
V_{DDIO} Supply Current	I_{DDIO}				35	mA
V_{DDC} Supply Current	I_{DDC}				80	mA
Idle Mode Current	I_{IDLE}	No peripherals running		5		mA
Stop Mode Current	I_{STOP1}	Power monitor on		0.5		mA
	I_{STOP2}	Power monitor off		0.25		
V_{DDC}/AV_{DD} Brownout Trip Point	V_{RSTC}		1.62		1.70	V

DC Electrical Characteristics (continued)

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DDIO} Brownout Trip Point	V_{RSTIO}		2.75		3.00	V
V_{DDC}/AV_{DD} Power-Fail Warning Level	V_{PFWC}			V_{RSTC} + 0.04V		V
V_{DDIO} Power-Fail Warning Level	V_{PFWIO}			V_{RSTIO} + 0.1V		V

AC Electrical Characteristics

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Clock External Crystal Frequency	$1/t_{CLKS}$		1		20	MHz
System Clock External Crystal Frequency—PLL 2x Mode	$1/t_{CLKS}$		4.0		16.5	MHz
System Clock External Crystal Frequency—PLL 4x Mode	$1/t_{CLKS}$		2.0		8.25	MHz
System Clock External Clock Frequency	$1/t_{CLKS}$		0		33	MHz
System Clock External Clock Frequency—PLL 2x Mode	$1/t_{CLKS}$		4.0		16.5	MHz
System Clock External Clock Frequency—PLL 4x Mode	$1/t_{CLKS}$		2.0		8.25	MHz
System Clock External Clock Duty Cycle	$1/t_{CLKS\_DUTY}$		40		60	%
System Clock External Crystal Warmup Delay	t_{ECWS}			65,536		t_{CLKS}
System Clock PLL Warmup Delay	t_{PLLWS}			65,536		t_{CLKS}
AFE Clock External Crystal Frequency	$1/t_{CLKA}$		1		20	MHz
AFE Clock External Crystal Frequency—PLL 2x Mode	$1/t_{CLKA}$		4		18	MHz
AFE Clock External Crystal Frequency—PLL 4x Mode	$1/t_{CLKA}$		2		9	MHz
AFE Clock External Clock Frequency	$1/t_{CLKA}$		0		36	MHz
AFE Clock External Clock Frequency—PLL 2x Mode	$1/t_{CLKA}$		4		18	MHz
AFE Clock External Clock Frequency—PLL 4x Mode	$1/t_{CLKA}$		2		9	MHz

AC Electrical Characteristics (continued)

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AFE Clock External Clock Duty Cycle	$1/t_{CLKA\_DUTY}$		40		60	%
AFE Clock External Crystal Warmup Delay	t_{ECWA}			65,536		t_{CLKA}
AFE Clock PLL Warmup Delay	t_{PLLWA}			65,536		t_{CLKA}
Crystal Tolerance				25		ppm
Crystal Input Capacitance	C_{IN}			6		pF
Output Fall-Time GPIO I^2C Pad	t_{OF_I2C}		20 + 0.1 x C_L		250	ns
RTC Crystal Frequency	32KIN			32.768		kHz
MCU UART INTERFACE SYNCHRONOUS MODE (Note 4) (Figure 1)						
TXD Clock Period	t_{XLXL}	SM2 = 0		12 x t_{CLKS}		ns
		SM2 = 1		4 x t_{CLKS}		
TXD Clock High Time	t_{XHXL}	SM2 = 0		3 x t_{CLKS}		ns
		SM2 = 1		2 x t_{CLKS}		
RXD Output Valid to TXD Clock Rising Edge	t_{QVXH}	SM2 = 0		10 x t_{CLKS} - 10		ns
		SM2 = 1		3 x t_{CLKS} - 10		
RXD Output Data Hold from TXD Clock Rising Edge	t_{XHQH}	SM2 = 0		2 x t_{CLKS} - 10		ns
		SM2 = 1		t_{CLKS} - 10		
RXD Input Data Valid to TXD Clock Rising Edge	t_{XHDV}	SM2 = 0, SM2 = 1	t_{CLKS} + 50			ns
RXD Input Data Hold After TXD Clock Rising Edge	t_{XHDH}	SM2 = 0		0		ns
		SM2 = 1		0		
SPI MASTER (Note 4) (Figure 3)						
SPI Master Operating Frequency	$1/t_{MCK}$				1/2 x t_{CLKS}	kHz
I/O Rise/Fall Time	t_{RF}	C_L = 15pF, pullup = 560Ω			16	ns
SCLK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$ - t_{RF}			ns

AC Electrical Characteristics (continued)

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Output Valid to SCLK Sample Edge (MOSI Setup)	t_{MOH}		$t_{MCK}/2 - t_{RF}$			ns
MOSI Output Hold After SCLK Last Sample Edge	t_{MOV}		$t_{MCK}/2 - t_{RF}$			ns
SCLK Last Sample Edge to MOSI Output Change (MOSI Last Hold)	t_{MLH}		$t_{MCK}/2 - t_{RF}$			ns
MISO Input Valid to SCLK Sample Edge (MISO Setup)	t_{MIS}		40			ns
MISO Input Hold After SCLK Sample Edge	t_{MIH}		0			ns
SPI SLAVE (Note 4) (Figure 4)						
SPI Slave Operating Frequency	$1/t_{SCK}$				$1/8t_{CLKS}$	kHz
I/O Rise/Fall Time	t_{RF}	C_L = 15pF, pullup = 560Ω			16	ns
SCLK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}		$t_{SCK}/2 - t_{RF}$			ns
SPICS Active to First Shift Edge	t_{SSE}		t_{RF}			ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		t_{RF}			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		t_{RF}			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				50	ns
SPICS Inactive to Next SPICS Asserted	t_{SSH}		$t_{SCK} + t_{RF}$			ns
SCLK Inactive to SPICS Deasserted	t_{SD}		t_{RF}			ns
MISO Output Disabled After SPICS Edge Deasserted	t_{SLH}				$2 \times t_{SCK} + 2 \times t_{RF}$	ns
AFE INTERFACE SERIAL MODE (Note 5)						
AFE Interface Operating Frequency	$1/t_{TRCK}$				t_{CLKA}	MHz
Clock Rise/Fall Time	t_{CRF}	C_L = 20pF			6.5	ns
RCLK/TCLK Output Pulse-Width High/Low	t_{TRCH}, t_{TRCL}		$0.4 \times t_{TRCK}/2$		$0.6 \times t_{TRCK}/2$	ns
SDI Input Setup to RCLK Active Edge	t_{RIS}		5			ns
SDI Input Hold After RCLK Active Edge	t_{RIH}		0			ns

AC Electrical Characteristics (continued)

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RXEN/TXEN Active Level Output Pulse Width	t_{TREW}		t_{TRCK}			ns
RCLK/TCLK to RXEN/TXEN Active	t_{TRED}		0		10	ns
TCLK to SDO Output	t_{TOD}		0		10	ns
I²C FULL-SPEED TIMING						
SCL Clock Frequency	f_{SCL}				400	kHz
Input Low Voltage	V_{IL_I2C}				0.3 x V_{DDIO}	V
Input High Voltage	V_{IH_I2C}		0.7 x V_{DDIO}			V
Input Hysteresis	V_{IHYS_I2C}	V_{IO} > 2V	0.05 x V_{DDIO}			V
SDA Output Logic-Low	V_{OL_I2C}	V_L > 2V, 3mA sink current	0		0.4	V
Input Leakage Current	I_{IN_I2C}	0 < V_{IO} < V_L	-10		+10	µA
I/O Capacitance	C_{IO_I2C}			5		pF
SDA Output Fall Time	t_{OF_I2C}	(Note 6)		20 + 0.1C_b	250	ns
Hold Time After Repeated START	$t_{HD,STA}$		0.6			µs
Clock Low Period	t_{LOW_I2C}		1.3			µs
Clock High Period	t_{HIGH_I2C}		0.6			µs
Setup Time for Repeated START	$t_{SU,STA}$		0.6			µs
Hold Time for Data	$t_{HD,DAT}$				0.9	µs
Setup Time for Data	$t_{SU,DAT}$		100			ns
SDA/SCL Fall Time	t_F	(Note 6)		20 + 0.1C_b	300	ns
SDA/SCL Rise Time	t_R	(Note 6)		20 + 0.1C_b	300	ns
Setup Time for STOP	$t_{SU,STO}$		0.6			µs
Bus Free Time Between STOP and START	t_{BUF}		1.3			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP_I2C}	(Note 7)			50	ns

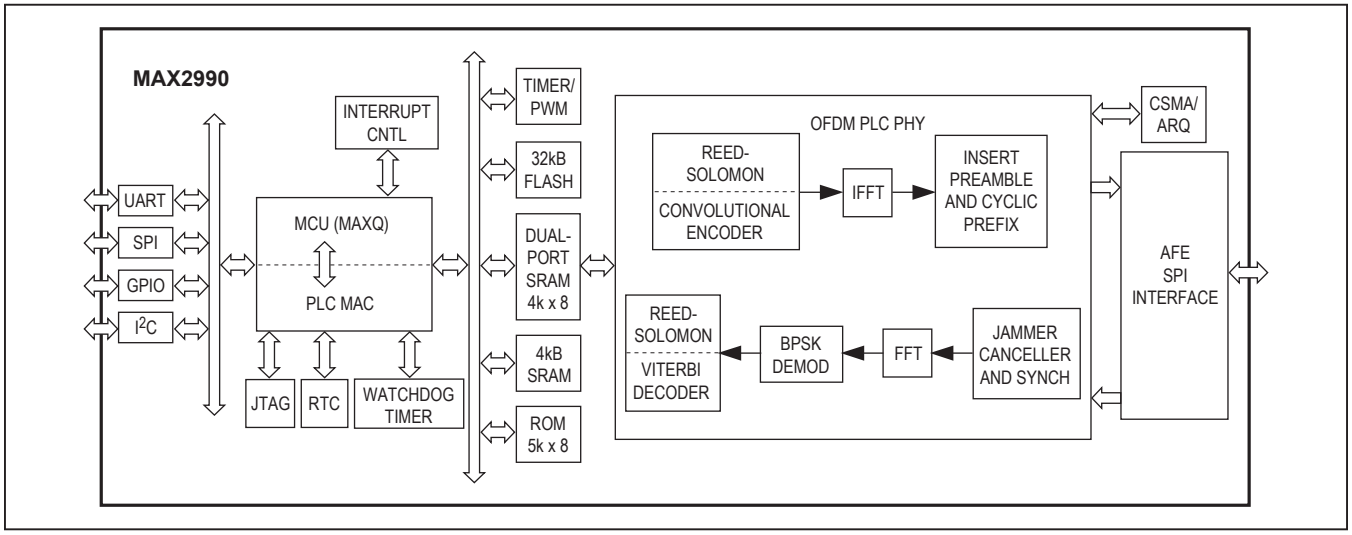
AC Electrical Characteristics (continued)

(V_{DDIO} = +3.0V to +3.6V, V_{DDC} = AV_{DD} = +1.62V to +1.98V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DDIO} = +3.3V, V_{DDC} = AV_{DD} = +1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V_{nL_I2C}		0.1 x V_{DDIO}			V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V_{nH_I2C}		0.2 x V_{DDIO}			V

Note 2: Specifications down to -40°C are guaranteed by design and not production tested.
Note 3: Timing specifications guaranteed by design.
Note 4: t_{CLKS} refers to the system clock without PLL multiplication.
Note 5: t_{CLKA} refers to the AFE clock without PLL multiplication.
Note 6: $I_{SINK} \le 6mA$, C_B = total capacitance of one bus line in pF. t_R and t_F are measured between 0.8V and 2.1V.
Note 7: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Functional Diagram



Pin Description

PIN	NAME	FUNCTION
1–4, 10–13	P0.0–P0.7	General-Purpose, Digital, I/O, Type-D Port*. Port0 functions as both an 8-bit I/O port and as an alternate interface for external interrupts. Each interrupt can be individually enabled and the active edge can be selected. The default reset condition of Port0 is a weak pullup (input). To drive Port0 as an output, the port direction register must be programmed to enable outputs or the alternate function module must be configured.

Pin/Port		Alternate Function	Alternate Function Description
1	P0.0	T0A/INT0	Timer 0 Inout A/External Interrupt 0
2	P0.1	T0B/INT1	Timer 0 Inout B/External Interrupt 1
3	P0.2	T1A/INT2	Timer 1 Inout A/External Interrupt 2
4	P0.3	T1B/INT3	Timer 1 Inout B/External Interrupt 3
10	P0.4	T2A/INT4	Timer 2 Inout A/External Interrupt 4
11	P0.5	T2B/AGC0/INT5	Timer 2 Inout B/AGC Control Bit 0/ External Interrupt 5
12	P0.6	T3A/AGC1/INT6	Timer 3 Inout A/AGC Control Bit 1/ External Interrupt 6
13	P0.7	T3B/AGC2/INT7	Timer 3 Inout B/AGC Freeze or AGC Control Bit 2/External Interrupt 7

5, 19, 30, 33, 53, 58	DGND	Digital Ground
6, 20, 34, 54, 59	V_{DDC}	+1.8V Digital Core Supply. Bypass V_{DDC} to DGND with a 0.1µF ceramic capacitor as close as possible to V_{DDC}.
7	32KIN	RTC Crystal Oscillator Input. Connect 32KIN to one side of a 32.768kHz crystal and a load capacitor to ground. 32KIN can be configured to be driven by an external clock source.
8	32KOUT	RTC Crystal Oscillator Output. Connect 32KOUT to the other side of a 32.768kHz crystal and a load capacitor to ground. Leave 32KOUT unconnected if 32KIN is driven by an external clock source.

Pin Description (continued)

PIN	NAME	FUNCTION
9, 25, 39, 56	V_{DDIO}	Input/Output Power Supply. V_{DDIO} is nominally +3.3V and can range from +3.0V to +3.6V. Bypass V_{DDIO} to DGND with a 0.1µF ceramic capacitor as close as possible to V_{DDIO}.
14	$\overline{RST}$	Active-Low Reset Input/Output. $\overline{RST}$ is an external active-low input that employs an internal pullup resistor. $\overline{RST}$ also acts as an output when the source of the reset is internal to the device, such as a watchdog timer and power-fail. In this case, $\overline{RST}$ is held low while the processor is in a reset state, and goes high as the processor exits this state.
15, 50	AV_{DD}	+1.8V Analog Power Supply. Bypass AV_{DD} to AGND with a 0.1µF ceramic capacitor as close as possible to AV_{DD}.
16, 49	AGND	Analog Ground
17	XTAL1S	System Crystal Oscillator Input. Connect XTAL1S to one side of a parallel resonant crystal and a load capacitor to ground. XTAL1S can be configured to be driven by an external clock source.
18	XTAL2S	System Crystal Oscillator Output. Connect XTAL2S to the other side of a parallel resonant crystal and a load capacitor to ground. Leave XTAL2S unconnected if XTAL1S is driven by an external clock source.
21–24, 26–29	P1.0–P1.7	General-Purpose, Digital, I/O, Type-C Port*. Port1 functions as both an 8-bit I/O port and as an alternate interface for serial protocols. The default reset condition of Port1 is a weak pullup (input). To drive Port1 as an output, the port direction register must be programmed to enable outputs or the alternate function module must be configured to drive the port. Pin/Port — Alternate Function — Alternate Function Description 21 P1.0 TXD MCU UART Transmit 22 P1.1 RXD MCU UART Receive 23 P1.2 SCL I^2C Clock 24 P1.3 SDA I^2C Data 26 P1.4 SCLK SPI SCLK 27 P1.5 MOSI SPI Master Out 28 P1.6 MISO SPI Master In 29 P1.7 MSSEL SPI Master/Slave Select
31	$\overline{PROG}$	UART Bootloader Input. $\overline{PROG}$ activates the UART bootloader by being held low for at least three system clock cycles or until the ready flag is detected on TXD. Activating the $\overline{PROG}$ function automatically sets the PSPE bit in the ICDF register and initiates an internal reset. Upon code load completion, the PSPE bit is cleared and an internal reset is issued.
32	TDO	JTAG Data Output

Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>35–38,
40–43</td><td>P2.7–P2.0</td><td>General-Purpose, Digital, I/O, Type-C Port*. Port2 functions as both an 8-bit I/O port and as an alternate interface for serial protocols. The default reset condition of Port2 is a weak pullup (input). To drive Port2 as an output, the port direction register must be programmed to enable outputs or the alternate function module must be configured to drive the port.
<table>
<tr><th>Pin/Port</th><th></th><th>Alternate Function</th><th>Alternate Function Description</th></tr>
<tr><td>43</td><td>P2.0</td><td>AFE_GP2/AGC0</td><td>AFE General Purpose 2/AGC Control Bit 0</td></tr>
<tr><td>42</td><td>P2.1</td><td>AFE_GP3/AGC1</td><td>AFE General Purpose 3/AGC Control Bit 1</td></tr>
<tr><td>41</td><td>P2.2</td><td>AFE_GP4/AGC2</td><td>AFE General Purpose 4/AGC Freeze or AGC Control Bit 2</td></tr>
<tr><td>40</td><td>P2.3</td><td>AFE_GP5</td><td>AFE General Purpose 5</td></tr>
<tr><td>38</td><td>P2.4</td><td>T5A/X1CK</td><td>Timer 5 Inout A/X1 External 3.3V Clock</td></tr>
<tr><td>37</td><td>P2.5</td><td>T5B</td><td>Timer 5 Inout B</td></tr>
<tr><td>36</td><td>P2.6</td><td>T4A/T6A/X2CK</td><td>Timer 4 Inout A/Timer 6 Inout A/X2 External 3.3V Clock</td></tr>
<tr><td>35</td><td>P2.7</td><td>T4B/T6B</td><td>Timer 4 Inout B/Timer 6 Inout B</td></tr>
</table></td></tr>
<tr><td>44</td><td>TDI</td><td>JTAG Data Input</td></tr>
<tr><td>45</td><td>TMS</td><td>JTAG Mode Select Input</td></tr>
<tr><td>46</td><td>TCK</td><td>JTAG Clock Input</td></tr>
<tr><td>47</td><td>XTAL2A</td><td>AFE Crystal Oscillator Output. Connect XTAL2A to the other side of a parallel resonant crystal and a load capacitor to ground. Leave XTAL2A unconnected if XTAL1A is driven by an external clock source.</td></tr>
<tr><td>48</td><td>XTAL1A</td><td>AFE Crystal Oscillator Input. Connect XTAL1A to one side of a parallel resonant crystal and a load capacitor to ground. XTAL1A can be configured to be driven by an external clock source.</td></tr>
<tr><td>51, 52, 55,
57, 60–64</td><td>P3.0–P3.8</td><td>General-Purpose, Digital, I/O Type-C Port*. Port3 functions as both a 9-bit I/O port and as an alternate interface for the AFE. The default reset condition of Port3 is a weak pullup (input). To drive Port3 as an output, the port direction register must be programmed to enable outputs or the alternate function module must be configured to drive the port.
<table>
<tr><th>Pin/Port</th><th></th><th>Alternate Function</th><th>Alternate Function Description</th></tr>
<tr><td>51</td><td>P3.0</td><td>AFE_TXEN</td><td>AFE Transmit Enable</td></tr>
<tr><td>52</td><td>P3.1</td><td>AFE_SDO</td><td>AFE Serial Data Out</td></tr>
<tr><td>55</td><td>P3.2</td><td>AFE_TXCLK</td><td>AFE Transmit Clock</td></tr>
<tr><td>57</td><td>P3.3</td><td>AFE_RXCLK</td><td>AFE Receive Clock</td></tr>
<tr><td>60</td><td>P3.4</td><td>AFE_SDI</td><td>AFE Serial Data In</td></tr>
<tr><td>61</td><td>P3.5</td><td>AFE_RXEN</td><td>AFE Receive Enable</td></tr>
<tr><td>62</td><td>P3.6</td><td>AFE_RSTN</td><td>AFE Reset</td></tr>
<tr><td>63</td><td>P3.7</td><td>AFE_GP1/RXPIN</td><td>AFE General Purpose 1/RXPIN</td></tr>
<tr><td>64</td><td>P3.8</td><td>AFE_GP0/TXPIN</td><td>AFE General Purpose 0/TXPIN</td></tr>
</table></td></tr>
</table>

*__Note:__ *Type-D ports are capable of interrupts while type-C ports are not.*

Timing Figures

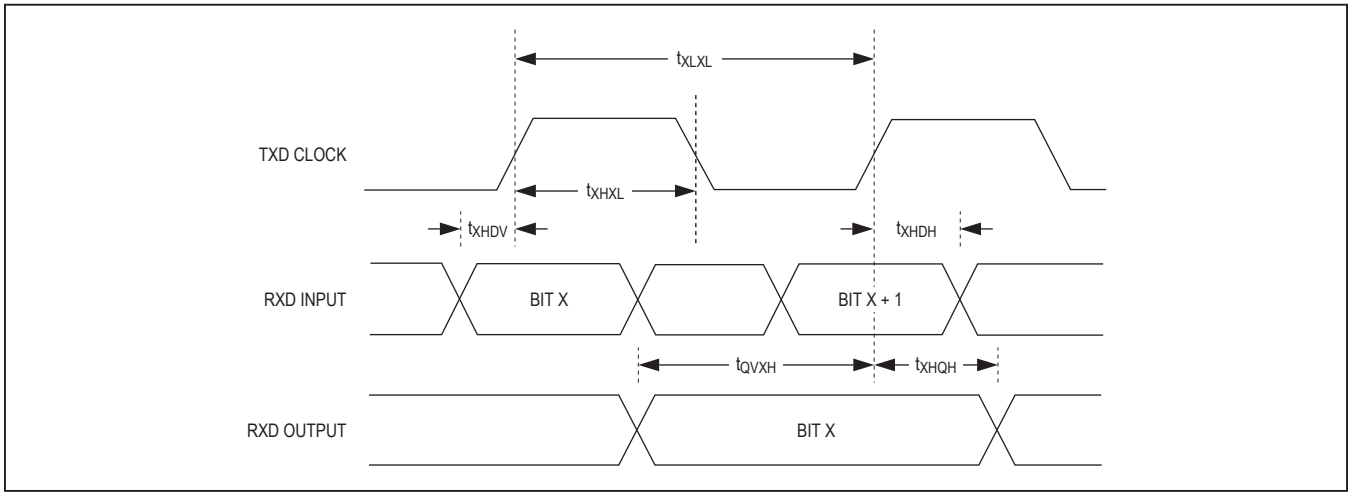


Figure 1. UART Timing Diagram for Synchronous Mode (Mode 0)

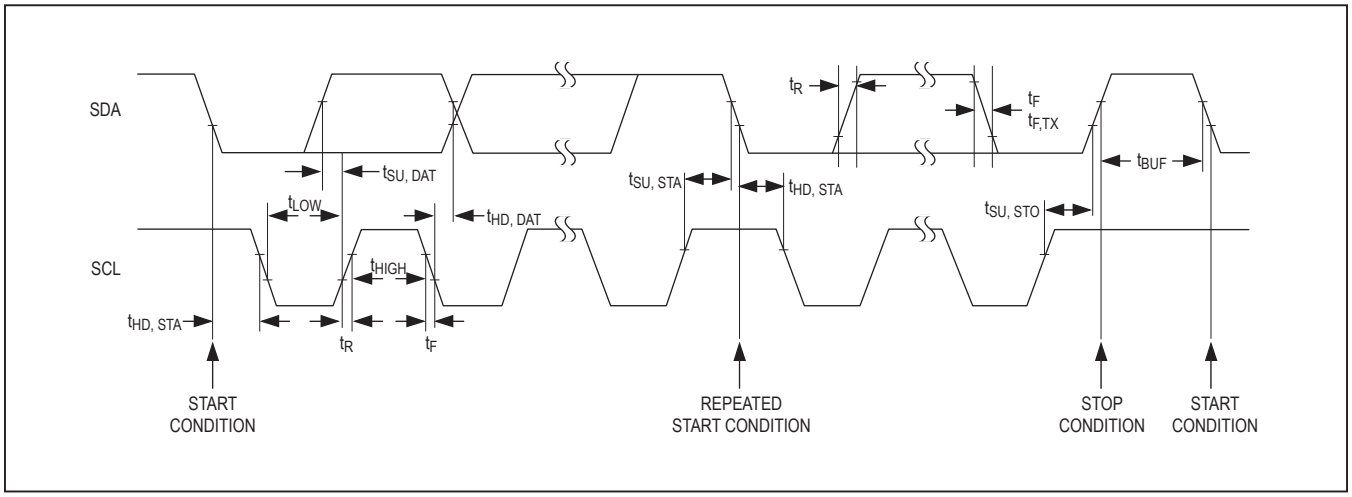


Figure 2. I^2C Timing Diagram

Timing Figures (continued)

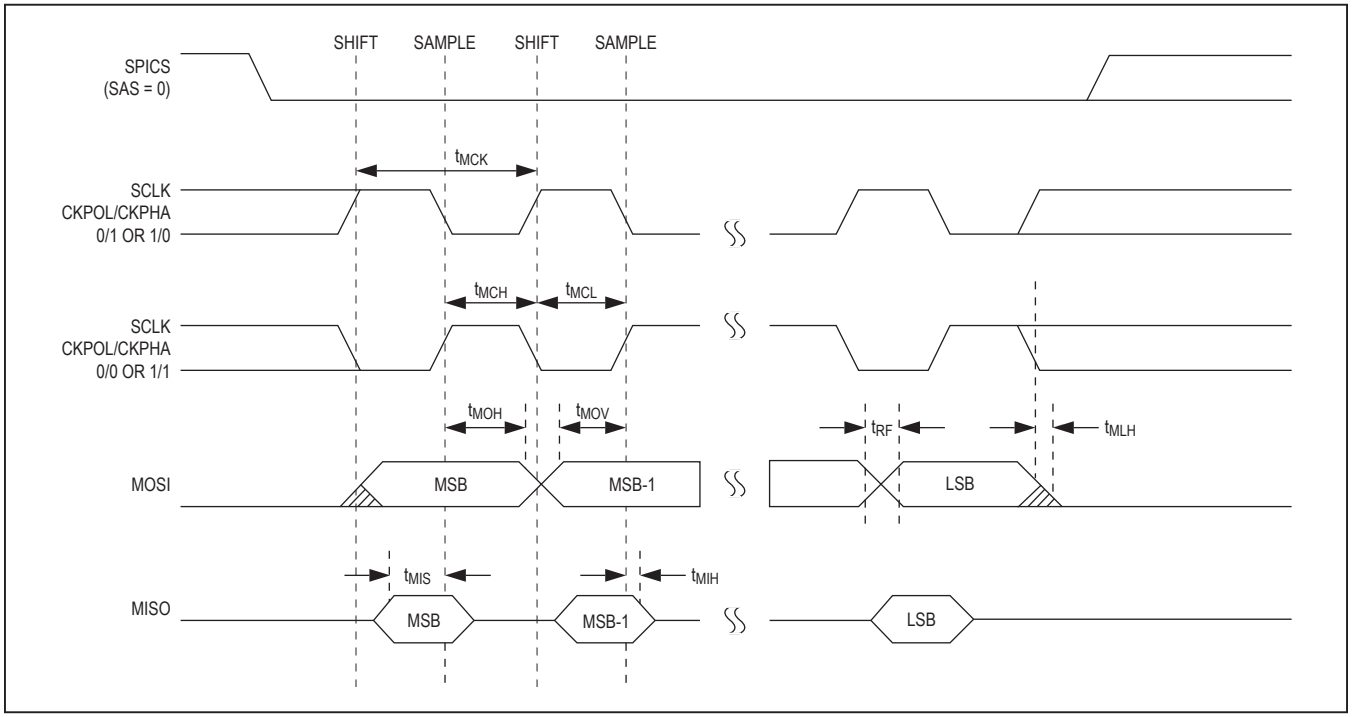


Figure 3. SPI Master Timing Diagram

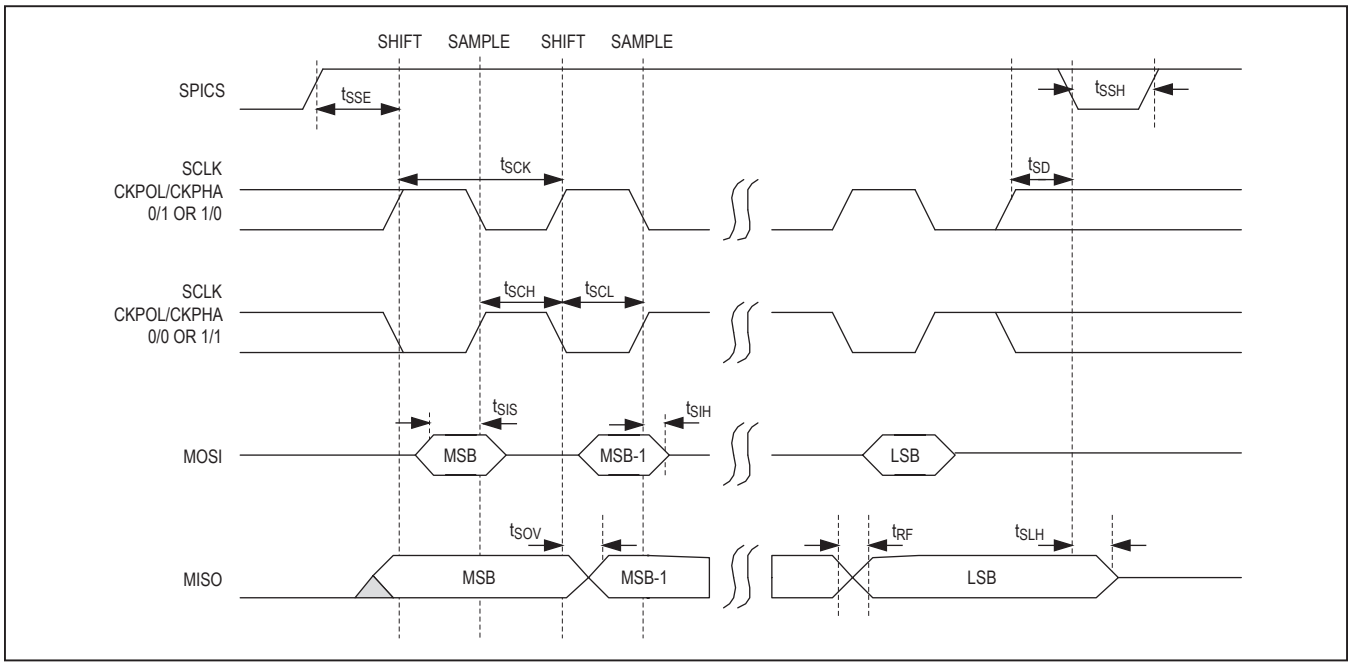


Figure 4. SPI Slave Timing Diagram

Detailed Description

The MAX2990 is an integrated SoC power line modem that utilizes advance modulation techniques for PLC. The MAX2990 enables robust data communication using the existing electrical wires, reducing the need for external cables for interconnections between nodes in a network.

The MAX2990 features a modem solution based on OFDM and the high-performance MAXQ microcontroller core. The MAX2990 encodes data at various carrier frequencies from 10kHz to 490kHz and uses advanced OFDM modulation techniques to send multiplexed data over the power line for overall high data throughput of 100kbps. The MAXQ core is a fully static CMOS, 16-bit RISC microcontroller with 32kB flash memory, 5.12kB of ROM, and 8kB of SRAM, of which 4kB can be simultaneously accessed by the internal microprocessor and the PHY. The MAXQ is integrated with modules for serial communication (SPI, I^2C, and UART) and RTC for time stamping, in addition to standard blocks such as timers for PWM, GPIO, and external interrupts.

The MAX2990 MAC features 48-bit and 16-bit addressing and organizes data into packets before transmission. The MAX2990 uses various registers for precise control over the PHY layer.

The MAX2990 automatically senses for collisions before it transmits over the power line. If multiple devices are connected in a star topology, collisions are not a problem. However, when multiple devices communicate to each other, collision avoidance becomes a primary issue. In peer-to-peer networks, it is possible for concurrent transmissions by multiple nodes to result in frame collisions. The multiple transmissions interfere with each other; therefore, all data is garbled and receivers are unable to distinguish the overlapping received signals from each other (Figure 5).

The MAX2990 features a carrier sense multiple access/collision avoidance (CSMA/CA) scheme that prevents collisions. If the channel is not clear, the node waits for a randomly chosen period of time and then checks again to see if the channel is clear. The MAX2990 accepts data from the user at any time, but transmits over the power line in accordance with CSMA/CA. The automatic repeat request (ARQ) feature improves data reliability by requesting packets with errors be retransmitted. The MAX2990 features a programmable ARQ that automatically detects and resends unsuccessful transmission packets without any user interface.

Orthogonal Frequency-Division Multiplexing (OFDM) Technique

The power line channel is a hostile environment. Channel characteristics and parameters vary with frequency, location, time, and the type of equipment connected. The lower frequency regions from 10kHz to 490kHz are especially susceptible to interference. Furthermore, the power line is a frequency selective channel. Besides background noise, it is subject to impulsive noise often occurring at 50/60Hz, narrowband interference, and group delays up to several hundred microseconds.

OFDM is a modulation technique that can utilize the allowed bandwidth for CENELEC, ARIB, and FCC bands very efficiently, allowing the use of advanced channel coding techniques. This combination enables a very robust power line communication in the presence of narrowband interference, impulsive noise, and frequency selective attenuation.

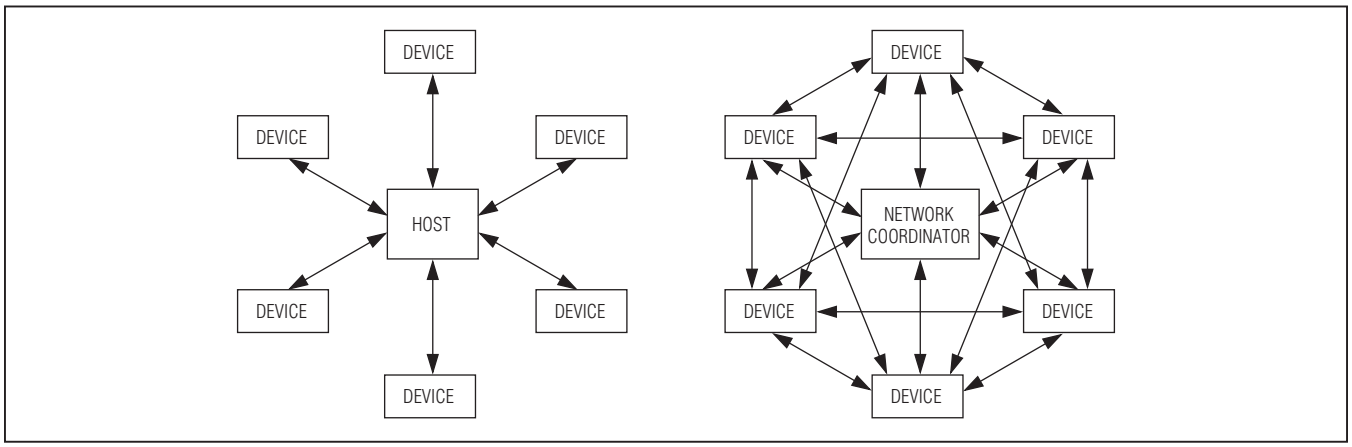


Figure 5. Carrier Sense Multiple Access/Collision Avoidance

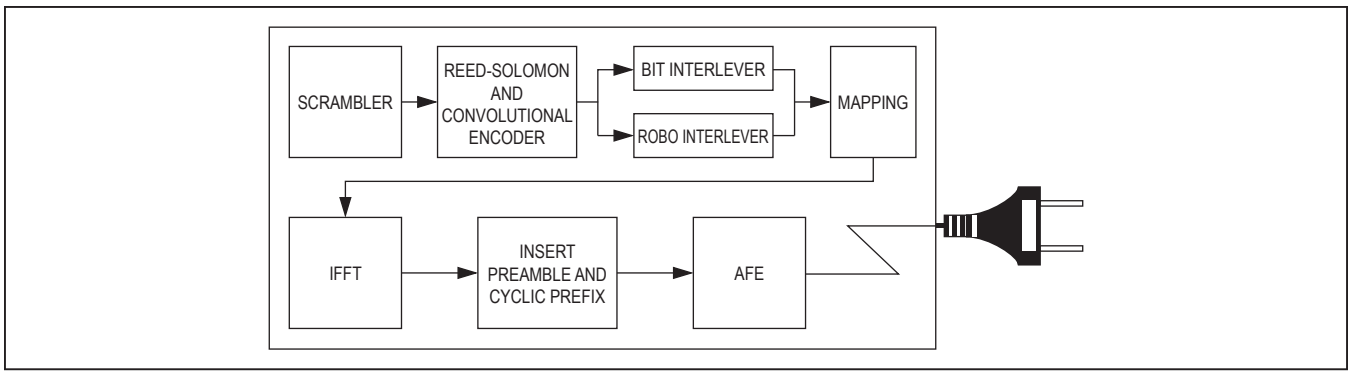


Figure 6. OFDM Transmit Path

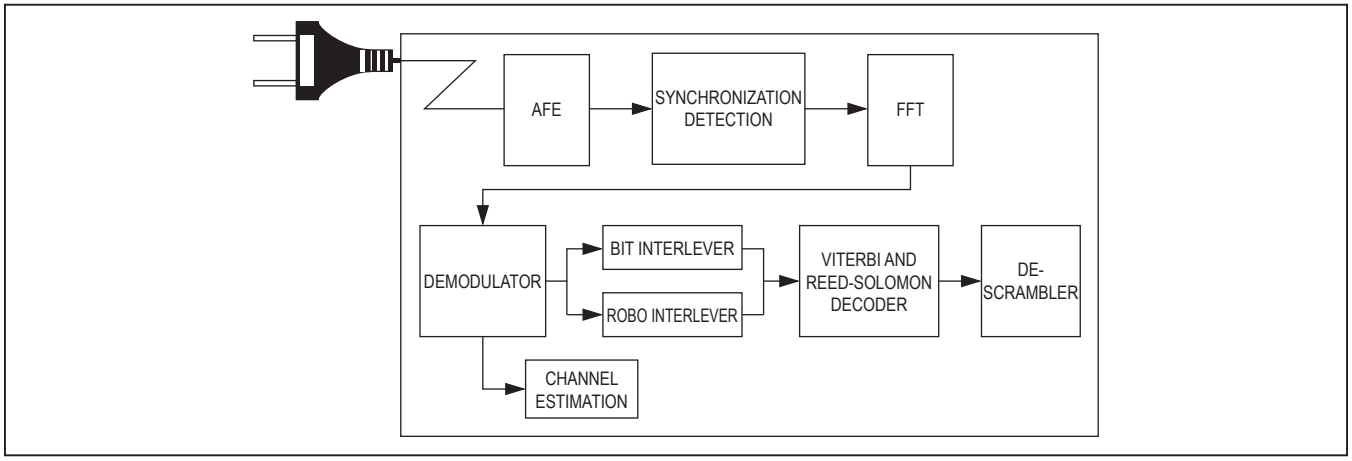


Figure 7. OFDM Receive Path

The approach shown in Figure 6 divides a user-defined bandwidth (such as CENELEC, FCC, or ARIB) into a number of subchannels that can be viewed as many independent BPSK modulated carriers with different non-interfering carrier frequencies.

Convolutional and Reed-Solomon coding provide redundancy bits. This allows the receiver to recover any lost or corrupted bits caused by background and impulsive noise. A time-frequency interleaving scheme is used to decrease the correlation of received noise at the input of the decoder.

Multicarrier signals are generated by performing IFFT on the complex-valued signal points produced by differentially encoded phase/amplitude modulation allocated into the individual subcarrier.

An OFDM symbol is built by appending a cyclic prefix to the beginning of each block generated by IFFT. The length of cyclic prefix, which is programmable from the MAC layer, is chosen so that a channel group delay does not cause successive OFDM-symbols or adjacent subcarriers to interfere. The start of the data frame carries multiple preamble symbols that contain the synchronization sequence. A synchronizer at the receiving end detects the sequences that indicate the beginning of the data frame (Figure 7).

Blind channel estimator technique is used to monitor the channel variation for each data frame. If a severe change in the power line channel condition occurs, the channel estimator switches the OFDM system into robust mode. In robust mode, data is repeated several times and includes convolutional coding and the Reed-Solomon encoder. In normal mode, the MAX2990 PLC modem can communicate up to 32kbps at 4dB SNR with a bit error rate of approximately 10^{-9} in the CENELEC A band. In robust mode, the system can provide an additional 5dB improvement.

Modes of Operation

In autoconfiguration, the MAX2990 operates in both normal and robust modes. In the robust mode, an extra encoder is used after the convolutional coder and repeats the bits several times.

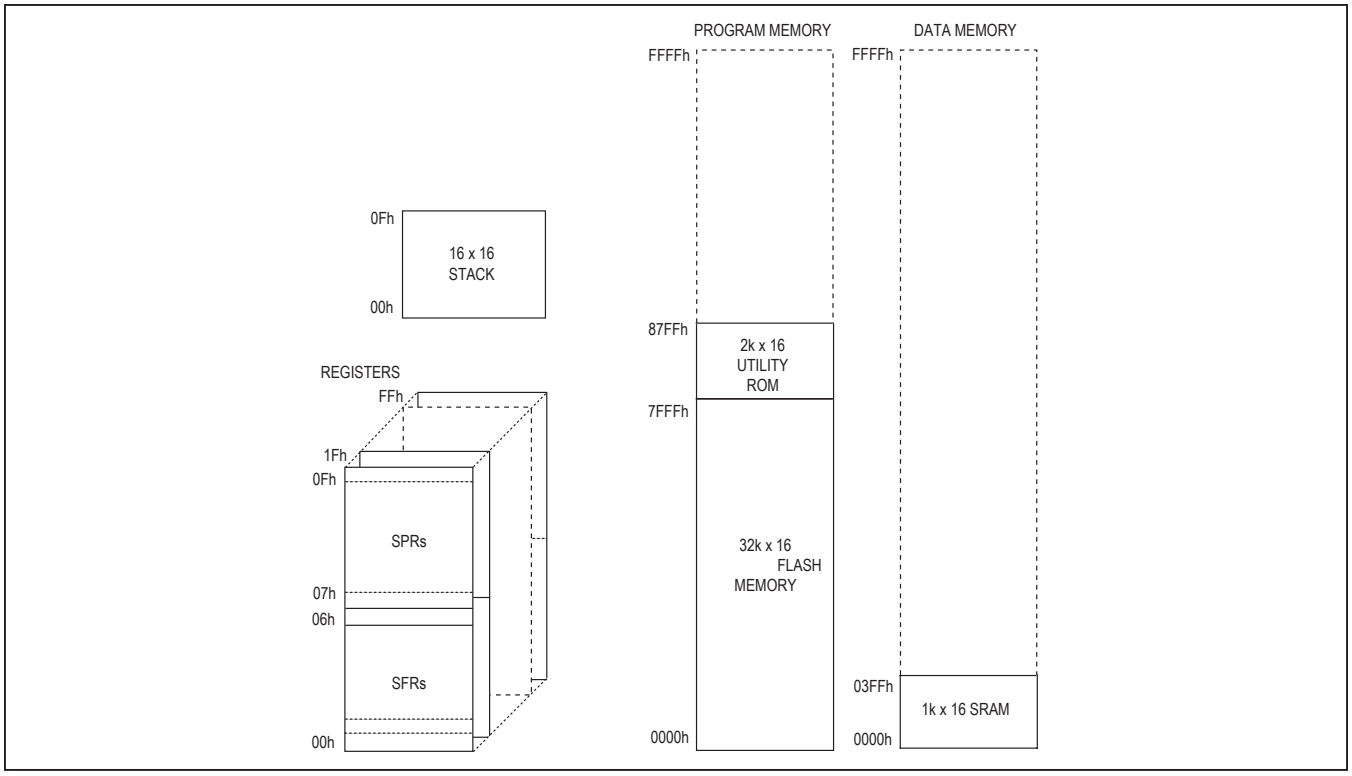


Figure 8. Memory Map

The MAC layer switches the mode of operation based on the channel estimation block output values. The channel estimation block estimates the SNR, input level fluctuations and potential in-band tone reductions. As input signal variation exceeds the predefined thresholds, the MAC layer switches the mode to either normal or robust.

Programmable Bandwidth Selection

The MAX2990 can operate in CENELEC, FCC, and ARIB bands capable of transmitting data from 10kHz to 490kHz frequency bands; however, in the wideband mode, the start and end frequencies are programmable through the registers. For example, the MAX2990 can be configured to establish data communication in the 95kHz to 190kHz frequency range. For best performance, it is recommended to select the frequency band that covers a minimum of 12 tones.

ACK Signal

The ACK signal is used when an acknowledgement is required to confirm whether data is correctly received. The transmitting unit waits for an acknowledgement during a predefined time span. The reception of the ACK signal is an indication that the data was delivered with no errors. If the waiting period exceeds the predefined time span and the ACK signal is not received, it indicates that the data was either lost or corrupted.

Programmable-Gain Amplifier (PGA)

The MAX2990 has three external outputs that can be used to control an external analog PGA. The purpose of these outputs is to specify the amount of gain needed from the analog PGA to compensate for fluctuations in the received signal levels. The algorithm used calculates the desired gain and outputs it as a 3-bit binary value. This module works in tandem with a digital AGC module that is implemented inside the PHY. The analog gain resolution can be programmed to 3dB or 6dB, and provides the MAX2990 with an additional dynamic range of 21dB and 42dB, respectively.

Preemphasis

The MAX2990 features preemphasis that is a linear equalization method where the transmit signal spectrum is shaped to compensate for amplitude distortion. The purpose of preemphasis is to provide frequency shaping to the transmit signal to compensate for attenuation introduced to the signal as it goes through the power line.

Jammer Canceller

A wide range of narrowband interfering signals are present in the AC power line channel. If these in-band signals are stronger than the OFDM signals, they may result in misdetection or data corruption. The jammer canceller detects the presence of in-band jamming signals and removes them from the OFDM signal.

Data Manager

The data manager handles the interface between the PHY and MAC. The data manager reduces CPU overhead by automating packet transfer to and from the PHY, automating encryption and decryption, CRC32 processing of packet data, and performing packet filtering without MAC code intervention.

Physical Layer (PHY)

The MAX2990 features a PLC modem-based solution that encodes and decodes data spanned over 10kHz to 490kHz using advanced OFDM techniques. The multiplexed data has a collective throughput of 100kbps, but each carrier individually transmits at a low data rate for high reliability. The MAX2990 communication is halfduplex.

The MAX2990 PLC modem can operate in normal and robust modes that trade off reliability with speed; detect jammer signals; block jammer signals; check the status of ACKs; and offer automatic gain control, signal-to-noise status, and multiple flags and interrupts for status checks.

The MAX2990 PLC modem has register settings for FCC, CENELEC, and ARIB frequency band compliance. The PLC registers can be programmed according to the compliance and coding required.

Data Encryption Standard (DES)/ Cyclic Redundancy Check (CRC32)

The MAX2990 ensures privacy through DES encryption and error checking through CRC32. The MAX2990 has registers for control over the DES and CRC32. DES and CRC32 can be enabled independently. The MAX2990 stores its 64-bit key, which can be changed to any key. When CRC32 is enabled, the 32-bit checksum is appended at the end of the packet before encryption.

Memory Organization

The MAX2990 incorporates several memory areas:

- 512kB utility ROM
- 32kB flash memory for program storage
- 4kB of SRAM for storage of temporary variables
- 4kB dual-port SRAM for packet buffering
- 16-level memory stack for storage of program return addresses and general-purpose use

The MAX2990 uses Harvard architecture for access of system memory, with separate address spaces for program and data memory. This allows overlapping addresses in program and data memory since they are accessed in different ways. The MAX2990 supports pseudo Von Neumann memory structure, which can merge program and data into a linear memory map. This is accomplished by logically mapping the data memory into the program space or logically mapping program memory segment into the data space.

The incorporation of flash memory as the main program memory allows the MAX2990 to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades. Flash memory can be password protected with a 32-byte key, denying access to program memory by unauthorized individuals.

Stack Memory

A 16-bit-wide, 16-word deep internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer (SP) initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM supports the following functions:

- Flash ISP loader to load program from JTAG and serial port
- User-callable flash API routines
- User-callable table lookup routines
- JTAG debugger support

Protected Access

Some applications require preventative measures to protect against simple access and viewing of program code memory. To address this need for code protection, the MAX2990 microcontroller is equipped with a utility ROM that permits in-system programming, in-application programming, or in-circuit debugging that grants full access to those utilities only after a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh. Note that using these memory locations for a password does not exclude their usage for general code space if a unique password is not needed.

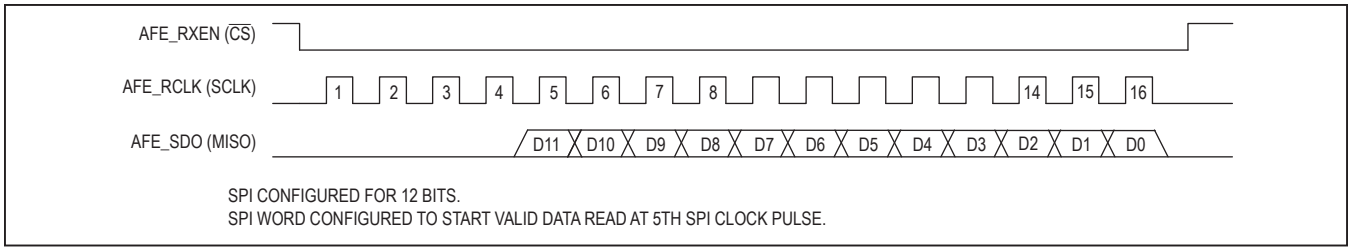


Figure 9. SPI-Compatible AFE Receive Path Configured for 12-Bit Word

A single Password Lock (PWL) bit is implemented in the SC register. When the PWL is set to 1, a password is required to access the ROM loader utilities that support read/write accessing of internal memory and debug functions. When PWL is cleared to 0, these utilities are fully accessible through the utility ROM without a password.

Programming

The flash memory of the microcontroller can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the life-cycle cost of the embedded system. These features can be password protected to prevent unauthorized access to code memory.

The MAX2990 can be programmed in C using Maxim's recommended C compiler. Contact the factory for more information.

In-System Programming

The MAX2990 supports two ways to enter bootloader mode. One way is using the JTAG board and asserting a system reset. The other way is by asserting the $\overline{PROG}$ input low. In bootloader mode, the MAX2990 supports test access port (TAP) and UART. TAP controllers communicate with a bus master, which can be either automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP, which is compatible to the JTAG IEEE standard 1149. If bootloader mode is entered through the $\overline{PROG}$ input, the bootloader can only be accessed by UART.

In-Application Programming

The in-application programming feature allows the microcontroller to modify its own flash program memory while simultaneously executing its application software through the use of the utility ROM data routines. This allows onthe-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible flash programming functions that erase and program flash memory.

Interfacing the MAX2990 to the Analog Front-End (AFE)

The MAX2990 interfaces to analog front-ends (AFEs) in SPI. The SPI frame size is fixed at 16 bits, but the data payload of the SPI frame is configurable as 8 bits, 10 bits, 12 bits, or 14 bits. The location of the data word within the SPI frame is user defined, as is the value of the other bits within the SPI frame. The MAX2990 AFE interface is flexible and supports a number of off-theshelf ADC and DAC solutions, as well as a future custom AFE. The AFE interface has separate SPI interfaces for the receive and transmit paths.

AFE Timing

The MAX2990 AFE interface supports 8-bit, 10-bit, 12-bit, or 14-bit SPI data streams. The AFE SPI interface can operate with an SPI clock up to 25MHz independent of the system clock and independent clock/phase polarity selection. The SPI frame size is fixed at 16 bits, but the data payload of the SPI frame is configurable as 8, 10, 12, or 14 bits (Figures 9, 10). The interface is designed as a half-duplex, SPI-compatible serial bus, and operates as a master. The location of the data word within the SPI frame is user defined, as is the value of the other bits within the SPI frame.

Receive Path (SPI)

The MAX2990 PHY block accepts data from the AFE interface block, internally, as signed or unsigned (biased) through the receive path SPI interface. If the external ADC delivers data in twos complement (signed), the data is passed directly to the internal gain-control function. If the ADC delivers unsigned (biased) data to the MAX2990 AFE interface, it can be configured to convert into twos complement internally. This data is then sent to the internal gain control where it is divided by 1 or 2, or multiplied by 2 or 4 depending on the gain setting, before being

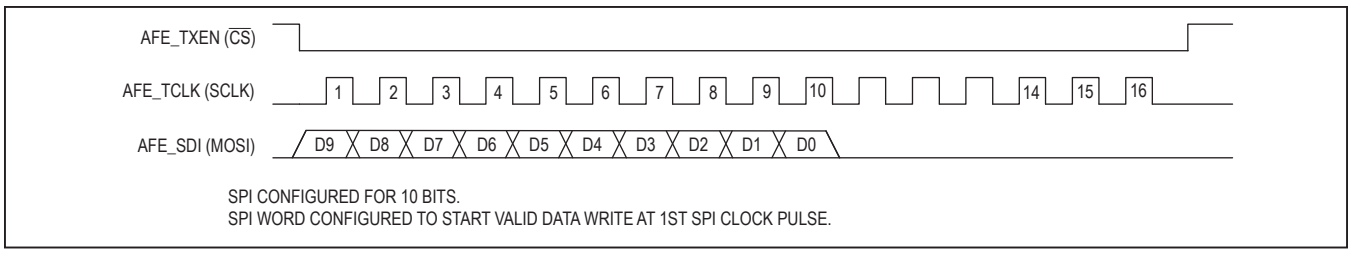


Figure 10. SPI-Compatible AFE Transmit Path Configured for 10-Bit Word

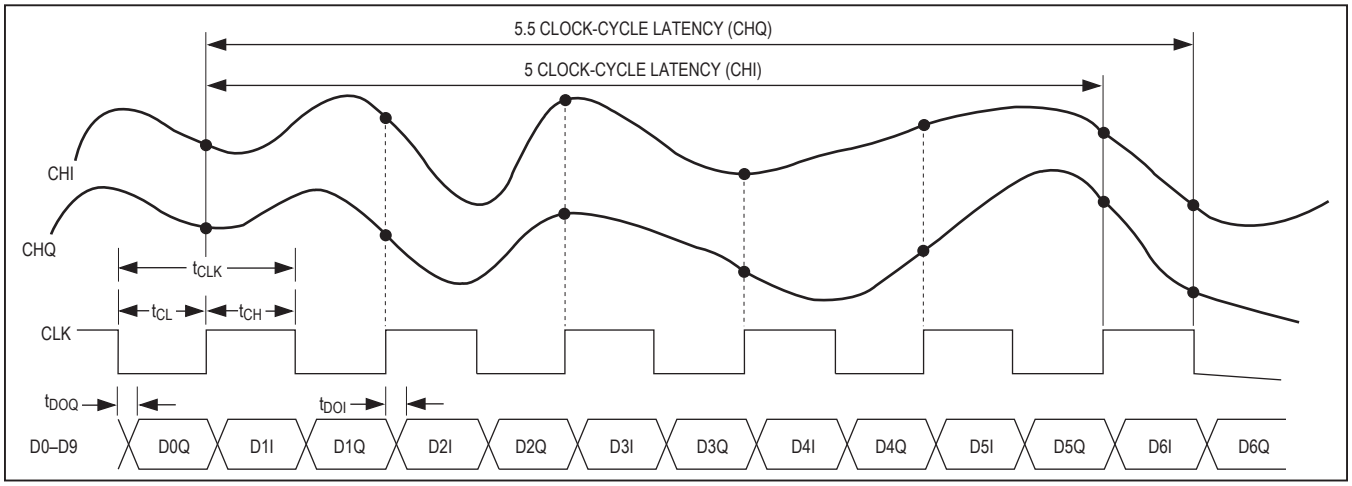


Figure 11. Receive ADC System Timing

passed on to the PHY block. Table 1 shows the AFE SPI pin mapping to an external SPI-compatible ADC.

Transmit Path (SPI)

The MAX2990 PHY delivers a 10-bit word on the transmit path to the internal AFE interface. The AFE SPI interface can be configured for 8, 10, 12, or 14-bit words (Figure 10), and a zero is added or taken off to fit the 10-bit word into the configured word length before being provided to the external analog front-end. The PHY provides the 10-bit word that is sent to the gain control where it is divided by 1 or 2, or multiplied by 2 or 4 depending on the gain setting. The MAX2990 features preemphasis; however, regardless of whether preemphasis is enabled, the internal AFE interface block receives a 10-bit word. Table 2 shows the AFE SPI pin mapping to an external SPI-compatible DAC.

Timing and Clocks

The MAX2990 has built-in oscillators for the system and AFE oscillators. The system oscillator and AFE oscillator both have similar structures. The system oscillator provides the clock to the MAX2990's internal microcontroller core while the AFE oscillator provides the clock to the AFE circuitry. The system oscillator has a default ring oscillator of 1MHz that asserts without a clock or crystal. Both oscillators have a PLL that can multiply the input by two times or four times. The minimum system clock and AFE clock is 4MHz with 2x multiplication and 2MHz with 4x multiplication. The maximum internal system clock is 33MHz while the maximum internal AFE clock is 36MHz. The system and AFE clock can also be divided down for power saving. The programmable multiplication and divide ratios provide the MAX2990 with the ability to adapt to different crystals and also to slow the system clock resulting in lower power consumption.

Table 1. MAX2990 to SPI ADC Pin Map

MAX2990	SPI-ENABLED ADC
AFE_RESETN	NC
AFE_TCLK	NC
AFE_RCLK	SCLK
AFE_SDI	DOUT
AFE_SDO	NC
AFE_RXEN	$\overline{CS}$
AFE_TXEN	NC
AFE_GP0	NC
AFE_GP1	NC

Table 2. MAX2990 to SPI DAC Pin Map

MAX2990	SPI-ENABLED DAC
AFE_RESETN	NC
AFE_TCLK	SCLK
AFE_RCLK	NC
AFE_SDI	NC
AFE_SDO	DIN
AFE_RXEN	NC
AFE_TXEN	$\overline{CS}$
AFE_GP0	NC
AFE_GP1	NC

System Oscillator (XTAL1S, XTAL2S)

The system oscillator is used for executing instructions, setting timers, and baud rate (SPI, I2C, UART). XTAL1S and XTAL2S connect an external crystal to the internal oscillator circuit. XTAL1S is the crystal oscillator input, and XTAL2S is the crystal oscillator output. Connect one side of a parallel resonant crystal to XTAL1S, and connect XTAL2S to the other side. Connect load capacitors (33pF, max) on both XTAL1S and XTAL2S to ground. XTAL1S can be configured to be driven with an external +1.8V clock. If driving XTAL1S with an external clock, leave XTAL2S unconnected. A +3.3V external clock can be applied to X1CK (P2.4) if the MAX2990 is configured to receive a +3.3V clock. If using X1CK for the clock input, XTAL1S is ignored and should be grounded. The external clock must meet the voltage characteristics depicted in the *Electrical Characteristics* table. Internal logic is single-edge triggered. The external clock should have a nominal 50% duty cycle.

AFE Oscillator (XTAL1A, XTAL2A)

The AFE oscillator provides the clock to the AFE interface. The AFE oscillator is used for setting the SPI baud rate to the external analog front-end. XTAL1A and XTAL2A connect an external crystal to the internal oscillator circuit. XTAL1A is the crystal oscillator input, and XTAL2A is the crystal oscillator output. Connect one side of a parallel resonant crystal to XTAL1A, and connect XTAL2A to the other side. Connect load capacitors (33pF, max) on both XTAL1A and XTAL2A to ground. XTAL1A can be configured to be driven with an external +1.8V clock. If driving XTAL1A with an external clock, leave XTAL2A unconnected. A +3.3V external clock can be applied to X2CK (P2.6) if the MAX2990 is configured to receive a +3.3V clock. If using X2CK for the clock input, XTAL1A is ignored and should be grounded. The external clock must meet the voltage characteristics depicted in the *Electrical Characteristics* table. Internal logic is single-edge triggered. The external clock should have a nominal 50% duty cycle.

RTC Oscillator (32KIN, 32KOUT)

The RTC oscillator provides the clock to the on-board RTC. 32KIN and 32KOUT connect an external crystal to an internal oscillator. The RTC oscillator clocks the RTC using integrated 6pF load capacitors, and gives the best performance when matched with a 32.768kHz crystal rated for 6pF series load. No external load capacitors are required. Higher accuracy can be obtained by configuring the 32KIN input to accept an external clock. If driving 32KIN with an external clock, leave 32KOUT unconnected. The external clock must meet the voltage characteristics depicted in the *Electrical Characteristics* table. Internal logic is single-edge triggered. The external clock should have a nominal 50% duty cycle.

The frequency accuracy of a crystal-based oscillator circuit is dependent upon crystal accuracy, the match between the crystal and the oscillator capacitor load, and ambient temperature. An error of 20ppm is equivalent to approximately 1 minute per month.

Interrupts

The MAX2990 supports interrupts through the Interrupt Vector (IV) register and Interrupt Control (IC) register. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up. If it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the Interrupt Identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the interrupts are evaluated by user software, the user can define a unique interrupt priority scheme for each application.

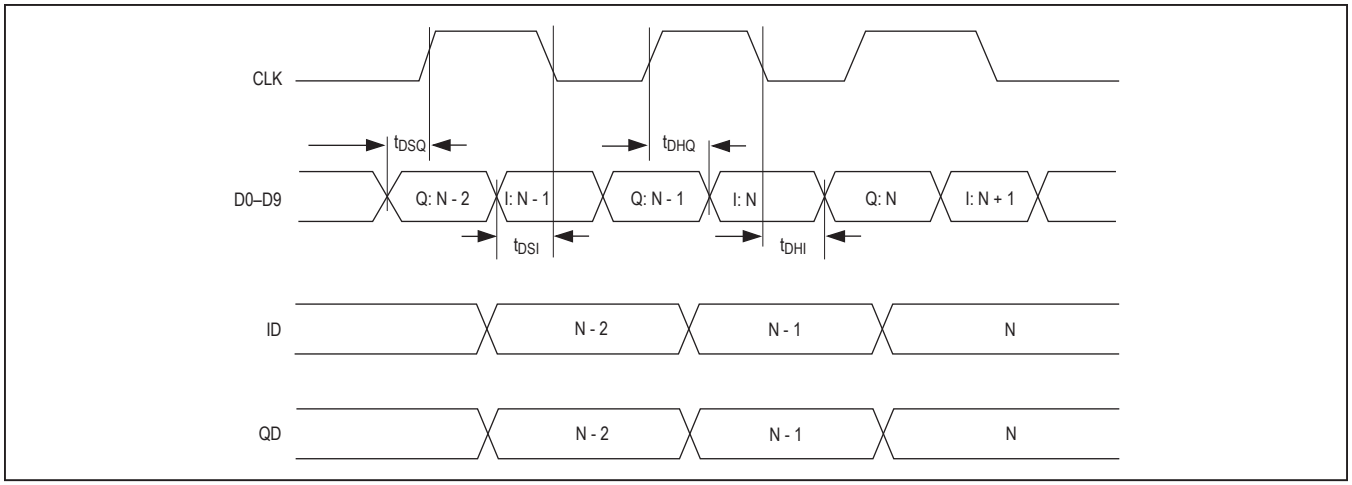


Figure 12. Transmit DAC System Timing

Reset Sources

The MAX2990 features several reset sources. $\overline{RST}$ is an open-drain I/O that serves as both a reset output that indicates a reset state and an input for manual reset that forces the internal microcontroller to its reset state.

Power-On Reset

An internal power-on reset circuit enhances system reliability. This circuit forces the device to perform a power-on reset whenever a rising voltage on V_{DDC} climbs above approximately +1.8V and V_{DDIO} climbs above approximately +3.0V. At this point the following events occur:

- All registers and circuits enter their reset state.
- The POR flag (WDCN.7) is set to indicate the source of the reset.
- The ring oscillator becomes the clock source.
- Code execution begins at location 8000h.

An independent power-up counter counts 65,536 cycles of the system oscillator from initial power-up. The MAX2990 is held in reset for this time period that starts after V_{DDC} and V_{DDIO} pass their POR threshold. The counter is active only during initial power-up and is completely shut off during normal operation. During operation, if the power drops below the power-fail threshold, reset is asserted.

Watchdog Timer Reset

The watchdog timer is a programmable hardware timer that can be set to reset the processor in the case of a software lockup or other unrecoverable error. Once the watchdog is enabled in this manner, the processor must reset the watchdog timer periodically to avoid a reset. The watchdog can be configured to fire an interrupt prior to a reset. If the watchdog timer is not reset after the first level interrupt, the watchdog initiates a reset state. If the processor does not reset the watchdog timer before it elapses, the watchdog will initiate a reset state. If the watchdog resets the processor, it remains in reset for four clock cycles. Once the reset condition is removed, the processor begins executing program code at address 8000h.

Manual Reset

During normal operation, the MAX2990 can be placed into external reset mode by asserting the $\overline{RST}$ input low for at least four clock cycles. After $\overline{RST}$ deasserts high, the processor exits the reset state within four clock cycles and begins program execution at address 8000h.

General-Purpose I/O Ports

The MAX2990 uses bidirectional I/O ports. Port0 supports interrupt detection. Port0, Port1, and Port2 have eight independent, general-purpose I/O pins, while Port3 has nine. All four ports have three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function.

Port0

Port0 is a type-D port with Schmitt Trigger receivers and full CMOS output drivers, and can support alternate functions. The pins are either three-stated or a weak pullup when defined as inputs dependent on the state of the corresponding bit in the output register. Type-D ports have interrupt capability.

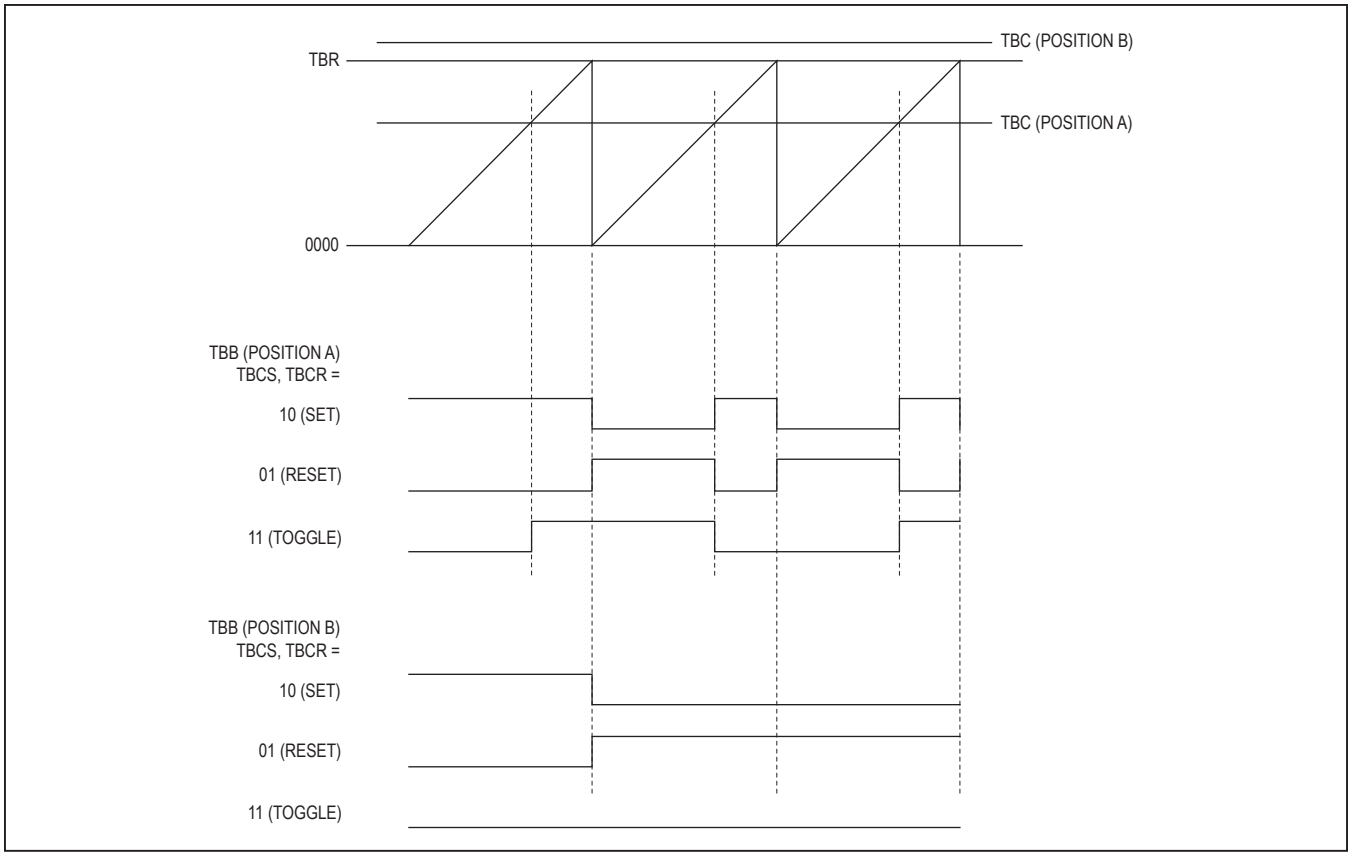


Figure 13. Up-Count PWM Mode

Port1, Port2, and Port3

Port1, Port2, and Port3 are type-C ports with Schmitt Trigger receivers and full CMOS output drivers, and can support alternate functions. The pins are either threestated or a weak pullup when defined as inputs, dependent on the state of the corresponding bit in the output register. Type-C ports do not have interrupt capability.

Real-Time Clock (RTC)

A binary real-time clock keeps the time of day in absolute seconds with 1/256-second resolution. The 32-bit second counter can count up to approximately 136 years and be translated to calendar format by the application software.

The independent subsecond alarm runs from the same RTC and allows the application to perform periodic interrupts up to a period of 1 second with a granularity of approximately 3.9ms. This creates an additional timer that can be used to measure long periods without performance degradations. Traditionally, long time periods have been measured using multiple interrupts from shorter programmable timers. Each timer interrupt required servicing, with each accompanying interruption slowing system operation. By using the RTC subsecond timer as a long-period timer, only one interrupt is needed, eliminating the performance hit associated with using a shorter timer.

Programmable Timers

The MAX2990 has seven type-B 16-bit programmable timers allowing precise control of internal and external events. Each timer can operate in two modes: countstop or wrap-around. In count-stop mode, the timer counts from its initial value to its maximum value or minimum value and then stops. In wrap-around mode, the counter rolls over when it reaches its extreme value and never stops (free-running mode). Timers can get enabled or disabled, and preserve their value while disabled. They can be loaded both in disable (pause) or enable (counting) states. Timers can be configured so they generate interrupts upon reaching an extreme value. Initial value can be determined by writing to the respective register. The timer B input clock is a divided version of the system clock.

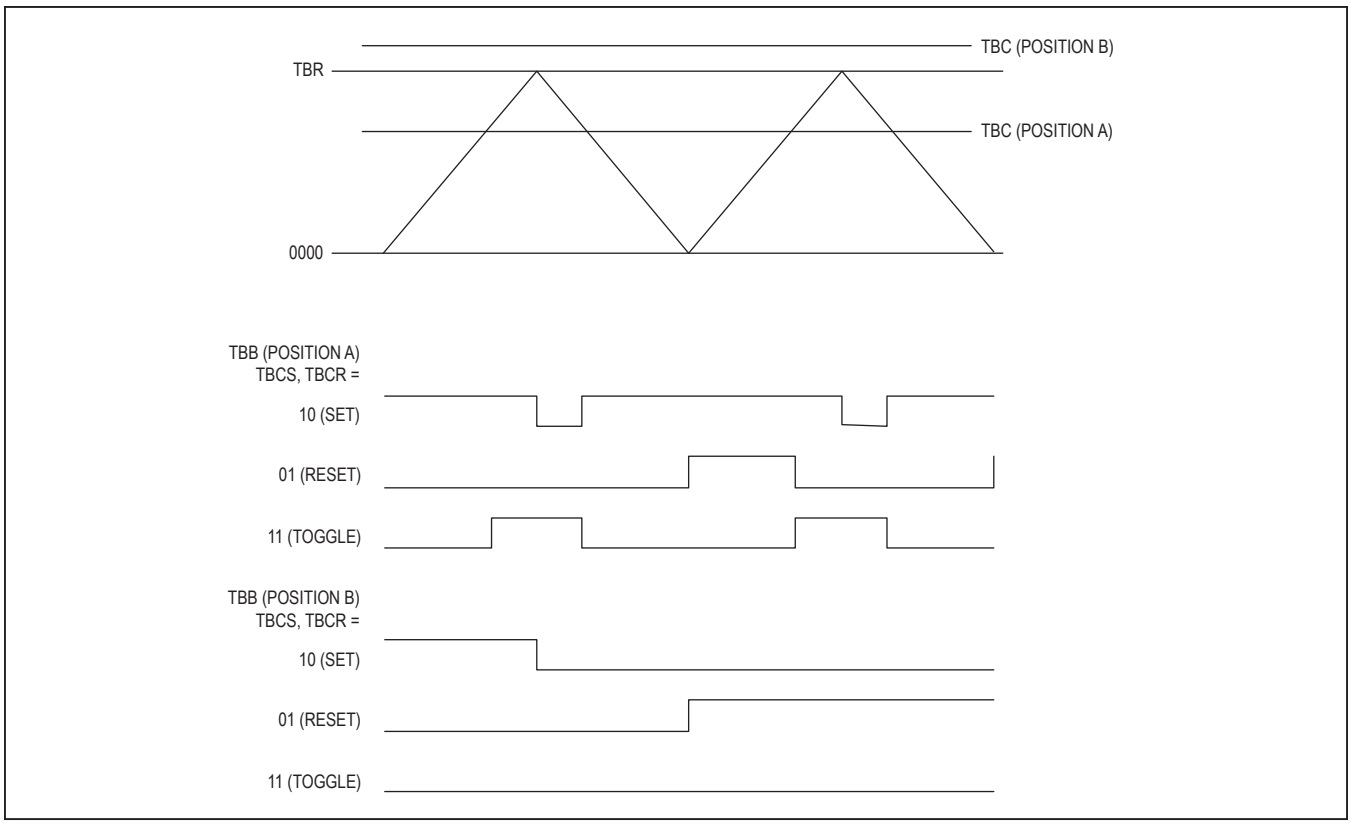


Figure 14. Up/Down Count PWM Mode

The MAX2990 supports PWM for LED light control. Type-B timers can be used for adjusting the duty cycle for PWM. The type-B timers can be configured for upcount (Figure 13) or up/down counting (Figure 14).

Interfaces

The MAX2990 incorporates several common serial interfaces in hardware. Multiple formats provide maximum flexibility and lower cost when designing a system.

SPI Interface

The MAX2990 uses SPI for both communication to the host and external interface (master or slave). This port is a common, high-speed, synchronous peripheral interface that shifts a bit stream of variable length and data rate between the microcontroller and other peripheral devices. Programmable clock frequency, character lengths, polarity, and error handling enhance the usefulness of the peripheral. The maximum baud rate of the SPI interface is half the system clock for master mode operation and 1/8th the system clock for slave mode operation.

UART Interface

A serial asynchronous communication protocol using the UART standard allows communication with other RS-232 devices to receive or transmit data. Some features are as following:

- Separate 16x8 transmit and 16x8 receive FIFOs to reduce CPU interrupts
- Programmable baud rate generator
- Programmable hardware flow control
- The MAX2990 works in UART mode 0 that features synchronous operation

I²C Interface

The MAX2990 features I²C implemented in hardware. I²C is a common 2-wire serial interface that supports bidirectional communication to multiple devices on the bus through 7-bit serial addressing. The number of devices on a bus is limited by the bus capacitance (400pF, max) and the maximum 7-bit serial addressing.

The I2C port can be initialized to be a master or slave. The microcontroller is typically initialized as a master, and peripheral devices are slaves by default. If programmed as a slave, the MAX2990 has a register to program a unique slave address. The I2C port requires external pullup resistors on the data and clock lines for operation. The I2C port features programmable clock, flags, interrupt, timeout, and direction. The maximum data rate is 400kbps.

Power Management

The MAX2990 features advanced power-management modes (PMM) to minimize power consumption by adjusting operational frequency to the required performance level per application. This means the devices can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the MAX2990 can increase its operating frequency. The device communicates in half-duplex and typically is in receive mode waiting for commands or data. To save power consumption, transmit path is switched off during data reception and receive path is idle during data transmission. Idle mode is available for applications requiring infrequent data transmission. Idle mode stops code execution in the core. Stop mode is applied to both the MAX2990 processor and PHY, and can be managed by an external processor.

Switch-Back

The system clock provides the standard baud rate generation for external interface. The clock affects all functional logic including timers and the baud rate generator in the serial port module. The switch-back feature allows low-power operation and quick response to events that require full processing capacity. The switch-back allows the system to switch back from a frequency established in the PMM registers.

Stop Mode

Stop mode disables all circuits within the processor except the 32kHz crystal oscillator and the AFE oscillator (if enabled). All on-chip clocks, timers, and serial port communication are stopped, and no processing is possible. In stop mode, all circuitry clocked by system clock is static and limited to leakage. Optionally the PHY can be clocked by the AFE oscillator in stop mode.

Chip Information

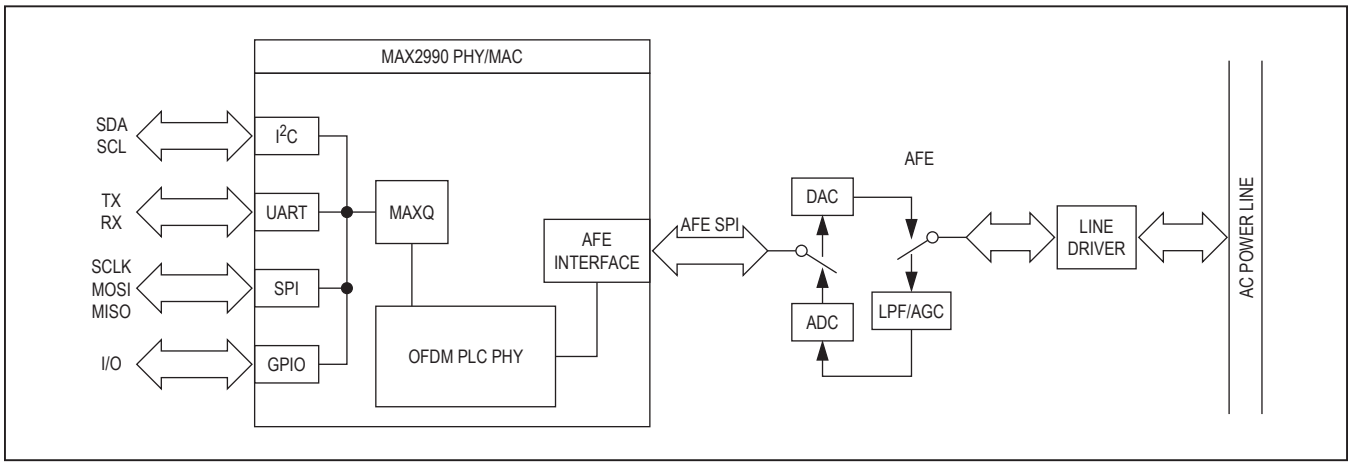
PROCESS: CMOS

Package Information

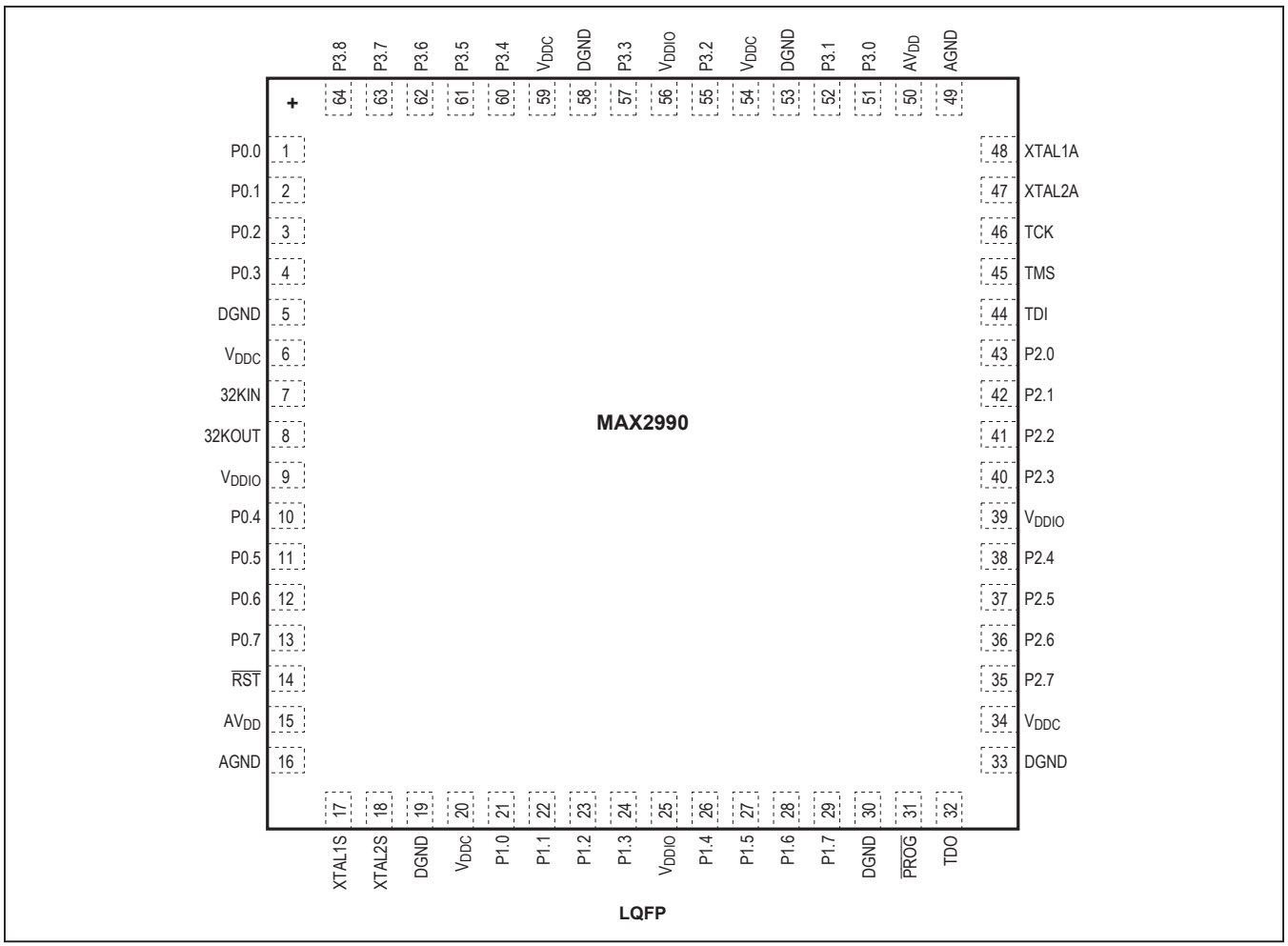
For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
64 LQFP	C64+5	**21-0083**

Typical Application Circuit



Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.