MAX32630 ERRATA SHEET

Revision B1 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc., intends to correct these errata when the opportunity to redesign the product presents itself.

This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at www.maximintegrated.com/errata.

1) PMU WRITE DESCRIPTOR MASK DOES NOT OPERATE AS EXPECTED

Description:
The PMU descriptor mask is expected to operate as:

(NEW_VALUE & MASK) | (ORIG_DATA & ~MASK)

but operates as:

NEW_DATA | (ORIG_DATA & ~MASK).

Workaround:
AND NEW_VALUE with MASK before writing to the WrData register.

2) SPI MASTER CAN TRANSMIT INCORRECT DATA IF Tx FIFO STALLS

Description:
An SPI master can transmit incorrect data under the following conditions:

1. The SPI master stalls (runs out of data in the middle of a transaction).

2. The SPI mode and SCK high or low settings do not match these combinations.

SPI MODE	SCK HIGH	SCK LOW
0	1	1–15
1	1–15	1
2	1–15	1
3	1	1–15

Workaround:
Use the SCK settings in the table shown above.

Slower baud rates are set through the SPIM clock scaling registers:

- CLKMAN_SYS_CLK_CTRL_11_SPI0.spi0_clk_scale
- CLKMAN_SYS_CLK_CTRL_12_SPI1.spi1_clk_scale
- CLKMAN_SYS_CLK_CTRL_13_SPI0.spi2_clk_scale

19-8684; Rev 0; 3/17

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/17	Initial release	—