# MAX32660
# ERRATA SHEET

## Revision A2 Errata

*The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.*

*This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at www.maximintegrated.com/errata.*

### 1) I²S IN SLAVE MODE CAN RECORD INCORRECT DATA IF A PARTIAL WORD IS RECEIVED DURING LEFT CHANNEL RECEPTION

**Description:**
While in slave mode, receipt of a partial/truncated word in the left data channel loads incorrect data into the I²S RX_FIFO.

**Workaround:**
1) Do not enable the I²S peripheral while the I²S master is transmitting.
2) Ensure that the I²S master begins all transmissions with a complete word.

### 2) I²S DOES NOT OPERATE AS EXPECTED IF SPIMSSn_DMA. tx_fifo_lvl IS SET TO 0b000

**Description:**
Transmit data can be corrupted if the I²S transmit FIFO is allowed to empty during a transaction.

**Workaround:**
The workaround for this erratum is incorporated in the relevant Analog Devices-supplied API. No user action is required when using the Analog Devices-supplied API.

In the case the user wants to implement their own API, the workaround is to set the SPIMSSn_DMA. tx_fifo_lvl to a value other than 0b000.

### 3) I²S PAUSE BIT MUST REMAIN SET A MINIMUM OF TWO LRCLK PERIODS

**Description:**
Software writes to the SPIMSSn_I2S_CTRL.i2s_pause bit require at least two LRCLK periods to be recognized.

**Workaround:**
Ensure software delays a minimum of two LRCLK periods between changes to SPIMSSn_I2S_CTRL. i2s_pause.

*419-100016; Rev 4; 4/22*

### 4) SPI MASTER DOES NOT OPERATE AS EXPECTED IF SPI TX_FIFO EMPTY FLAG IS USED

**Description:**
Transmit data may be corrupted if the TX_FIFO is allowed to empty during a transaction.

**Workaround:**
The workaround for this erratum is incorporated in the relevant Analog Devices-supplied API. No user action is required when using the Analog Devices-supplied API.

In the case the user wants to implement their own API, the workaround is to use the programmable TX_FIFO threshold interrupt instead of the TX_FIFO empty interrupt.

### 5) DISABLING THE $I^2C$ PERIPHERAL DURING A TRANSACTION ERRONEOUSLY SETS THE STOPI BIT

**Description:**
Disabling the $I^2C$ peripheral during a transaction erroneously sets I2Cn_INTFL0.stopi.

**Workaround:**
The workaround for this erratum is incorporated in the relevant Analog Devices-supplied API. No user action is required when using the Analog Devices-supplied API.

In the case the user wants to implement their own API, the I2Cn_INTFL0.stopi should always be cleared before enabling the $I^2C$ peripheral.

### 6) UART TX_FIFO DOES NOT GENERATE AN INTERRUPT IF EMPTY

**Description:**
UARTn_CTRL1.tx_fifo_lvlo = 0 does not cause an interrupt when the TX_FIFO becomes empty (ME11-162).

**Workaround:**
Set UARTn_CTRL1.tx_fifo_lvlo > 0 to cause an interrupt before the TX_FIFO becomes empty.

### 7) QSPI IN SLAVE MODE DOES NOT OPERATE CORRECTLY, SCK FALL TIME IS SLOW

**Description:**
SSEL must transition after SCK is already low. This is only an issue in designs with slow falling transitions on SCK (ME11-164).

**Workaround:**
Ensure the SPI master has sufficient drive capability to pull SCK low before SSEL goes low.

### 8) RTC_SSEC.ssec IS NOT ACCESSIBLE BY SOFTWARE

**Description:**
Read operations on the 12-bit RTC_SSEC.ssec field will return an indeterminate value. Write operations on that field will set it to an indeterminate value. The 12-bit subsecond counter itself is not affected and will update the RTC seconds counter RTC_SEC.sec correctly at one second intervals.

**Workaround:**
None. Do not use the RTC_SSEC.ssec field.

### 9) SOME GPIO DO NOT ISOLATE WHEN $V_{DD}$ = 0

**Description:**
The voltage on P0.[4–7, 9] must be equal to or less than $V_{DD}$ + 0.3V. (MBU424)

**Workaround:**
None.

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# REV A2 ERRATA

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/18 | Initial release | — |
| 1 | 2/19 | Added errata 6–8 | 2 |
| 2 | 8/21 | Added errata 9–11 | 3 |
| 3 | 3/22 | Removed errata 8–11; added errata 8, 9 | 2, 3 |
| 4 | 4/22 | Removed erratum 9 | 3 |