MAX32670/MAX32671 ERRATA SHEET

Revision A3 Errata

The errata listed below describe situations where components of this revision perform differently than expected or differently than described in the data sheet. Analog Devices may, at its own discretion, take future steps to correct these errata when the opportunity to redesign the product presents itself. Prior to that, Analog Devices has determined the following potential workarounds that customers may want to consider when addressing one of the situations described below.

*This errata sheet only applies to components of this revision. These components are branded on the topside of the package with a six-digit code in the form yywwRR, where yy and ww are two-digit numbers representing the year and work week of manufacture, respectively, and RR is the revision of the component. To obtain an errata sheet on other die revisions, visit the Maxim website at **www.maximintegrated.com/errata**.*

1) DEVICE PINS ASSOCIATED WITH LPTIMER AND LPUART INSTANCES WILL NOT FUNCTION AS GPIOS AFTER THE PERIPHERAL CLOCK IS ENABLED

Description:
All of the pins associated with an instance of an LPTIMER or LPUART will no longer operate with the GPIO functionality after the first time that peripheral clock is enabled. The alternate functions associated with the device pins operate correctly. (15276)

Workaround:
Do not use the device pins associated with an instance of an LPTIMER or LPUART once its peripheral clock has been enabled.

2) WDT FEED SEQUENCE NOT REQUIRED FOR ACCESS TO WDT_CTRL.en

Description:
The WDT_CTRL.en field is not write-protected by the WDT feed sequence. (15292)

Workaround:
None. On B version silicon, unique feed sequences will be required for resetting the WDT count, writing WDT_CTRL.en to 1, and writing WDT_CTRL.en to 0.

3) SOME GPIOS DO NOT ISOLATE WHEN V_{DD} = 0V

Description:
The maximum voltage on P0.[2, 4, 5, 7] must be equal to or less than V_{DD} + 0.3V.

Workaround:
None.

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4) ERFO CANNOT BE THE SYSTEM CLOCK SOURCE WHEN ENTERING DEEPSLEEP

Description:
The ERFO is disabled when entering DEEPSLEEP even if GCR_PM.erfo_pd is cleared to 0. (15275)

Workaround:
Switch to a different oscillator before entering DEEPSLEEP.

5) THE SYSTEM CLOCK SOURCE CANNOT BE SWITCHED DIRECTLY FROM IBRO TO INRO

Description:
The IPO must be clock-divided to a lower frequency when it is switched as the system oscillator. (15287)

Workaround:
Switch from IBRO to another clock source first, then switch from that clock source to INRO.

6) IPO DIVISOR MUST BE REDUCED BEFORE SWITCHING TO OR FROM IPO AS SYSTEM CLOCK SOURCE

Description:
The IPO clock into the system clock multiplexer must be less than full speed to correctly switch the system clock when IPO is selected or deselected as the system clock source. (15287)

Workaround:
When switching to the IPO as the system clock source:

1. Configure IPO divisor for divide by 4 or 8 (GCR_CLKCTRL.ipo_div to 0b10 or 0b11)
2. Enable IPO if not already enabled.
   a. Enable IPO (GCR_CLKCTRL.ipo_en to 1).
   b. Wait for the IPO clock ready bit (GCR_CLKCTRL.iop_rdy) to read 1.
3. Wait 1µs.
4. Select IPO as the system clock (GCR_CLKCTRL.sysclk_sel = 0b100).
5. Wait for the system clock ready bit (GCR_CLKCTRL.sysclk_rdy) to read 1.
6. Set GCR_CLKCTRL.sysclk_div to the desired prescaler value.

When switching from another system clock source to the IPO:

1. Configure IPO divisor for divide by 4 or 8 (GCR_CLKCTRL.ipo_div to 0b10 or 0b11)
2. Enable the target clock source if not already enabled.
   a. Set the corresponding enable bit in GCR_CLKCTRL.
   b. Wait for the corresponding ready bit in GCR_CLKCTRL to read 1.
3. Wait 1µs.
4. Set GCR_CLKCTRL.sysclk_sel to the desired clock source.
5. Wait for the system clock ready bit (GCR_CLKCTRL.sysclk_rdy) to read 1.
6. Set GCR_CLKCTRL.sysclk_div to the desired prescaler value.

7) STANDARD DMA OPERATIONS INVOLVING ECC-ENABLED SYSTEM RAM INSTANCES MAY TRANSFER INCORRECT DATA

Description:

Incorrect data may be transferred if operations are performed on system RAM instances with their ECC enabled. (21206)

Workaround:

Use a secondary DMA channel in conjunction with a primary DMA channel to perform DMA operations to and from ECC-enabled memory.

Considerations:

- The secondary DMA channel must be enabled before the primary DMA channel.
- The value of DMA_CHn_CNT.cnt for the secondary channel must be:

  (4 x number_of_primary_bursts) + 1

  For example, if both DMA_CHn_CNT.cnt = 2048 and DMA_CHn_CTRL.burst_size = 32 for the primary channel, then 64 bursts are required. DMA_CHn_CNT.cnt for the secondary channel is therefore:

  (4 x 64) + 1 = 257

Use the following steps to configure both the secondary and primary DMA channels:

1. Configure a secondary DMA channel for a dummy transfer of data. The destination is an unused location in the memory map, so this use of the secondary channel does not affect any usable memory.

   a) Set DMA_CHn_SRC.addr to 0x4000 0000.
   b) Set DMA_CHn_DST.addr to 0x4000 0200.
   c) Clear DMA_CHn_CTRL.srcinc to 0 to disable the source automatic incrementing.
   d) Clear DMA_CHn_CTRL.dstinc to 0 to disable the destination automatic incrementing.
   e) Set DMA_CHn_CTRL.srcwd to 0b10.
   f) Set DMA_CHn_CTRL.dstwd to 0b10.
   g) Set DMA_CHn_CTRL.burst_size to 0b00011.
   h) Configure DMA_CHn_CTRL.pri of the secondary DMA channel to the same value as DMA_CHn_CTRL.pri of the primary DMA channel.
   i) Configure DMA_CHn_CNT.cnt to the value calculated above.

2. Configure the primary DMA channel based on the transfer width. The source and destination address of the primary DMA channel must be aligned to a 32-bit boundary.

   - For a transfer width of 4 bytes:
     a) DMA_CHn_CNT.cnt must be a multiple of 4.
     b) DMA_CHn_CTRL.burst_size must be a multiple of 4 bytes.

   - For a transfer width of 2 bytes:
     a) DMA_CHn_CNT.cnt must be a multiple of 8.
     b) DMA_CHn_CTRL.burst_size must be a multiple of 8 bytes.

c) Set GCR_MEMCTRL.ramws_en to 1 to enable SRAM wait states.

- For a transfer width of 1 byte:
  a) DMA_CHn_CNT.cnt must be a multiple of 4.
  b) DMA_CHn_CTRL.burst_size must be a multiple of 4 bytes.
  c) Set GCR_MEMCTRL.ramws_en to 1 to enable SRAM wait states.

8) GPIO0_INEN AND GPIO0_PS RESET VALUES MAY DIFFER FROM USER GUIDE DESCRIPTION

Description:

On this die revision, the reset values for all reset events are:

GPIO0_INEN = 0xFFFFFFFF

GPIO0_PS = 0x00000000

Workaround:

None.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Initial release	—

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