*Click **here** to ask an associate for production status of specific part numbers.*

MAX32672

High-Reliability, Tiny, Ultra-Low-Power Arm Cortex-M4F Microcontroller with 12-Bit, 1Msps ADC

General Description

In the DARWIN family, the MAX32672 is an ultra-low-power, cost-effective, highly integrated, and highly reliable 32-bit microcontroller enabling designs with complex sensor processing without compromising battery life. It combines a flexible and versatile power management unit with the powerful Arm® Cortex®-M4 processor with a floating-point unit (FPU). The MAX32672 also offers legacy designs an easy and cost-optimal upgrade path from 8- or 16-bit microcontrollers.

The device integrates 1MB of flash and 200KB of SRAM to accommodate application and sensor code. Error correction coding (ECC) is implemented on the entire flash, RAM, and cache to ensure extremely reliable code execution even in the harshest of environments. Brownout detection ensures proper operation during power-down and power-up events and unexpected supply transients. The flash is organized into two equal-size physical banks to allow execute-while-write and facilitate "live upgrades."

Multiple high-speed peripherals such as 3.4MHz I^2C, 50MHz SPI, and UART are included to maximize communication bandwidth. In addition, a low-power UART (LPUART) is available for operation in the lowest power sleep modes to facilitate wake-up activity without any loss of data. A total of six timers with I/O capability are provided, including two low-power timers to enable pulse counting, capture/compare, and pulse-width modulation (PWM) generation, even in the lowest power sleep modes. An incremental/quadrature encoder interface with multiple diagnostics is included specifically for motor control applications. A 1Msps, 12-channel, 12-bit successive approximation register (SAR) ADC is integrated for the digitization of analog sensor signals or other analog measurements. Two low-power comparators, available in all low-power modes, allow energy-efficient monitoring and wake-up on external analog signals. An Elliptic Curve Digital Signature Algorithm (ECDSA)-based cryptographic secure bootloader is available in ROM. The device is available in a 5mm x 5mm, 40-pin TQFN-EP or 7mm x 7mm, 56-pin TQFN.

Applications

- Motion/Motor Control, Industrial Sensors
- Optical Communication Modules, Secure Radio Modem Controller
- Battery-Powered Medical Devices

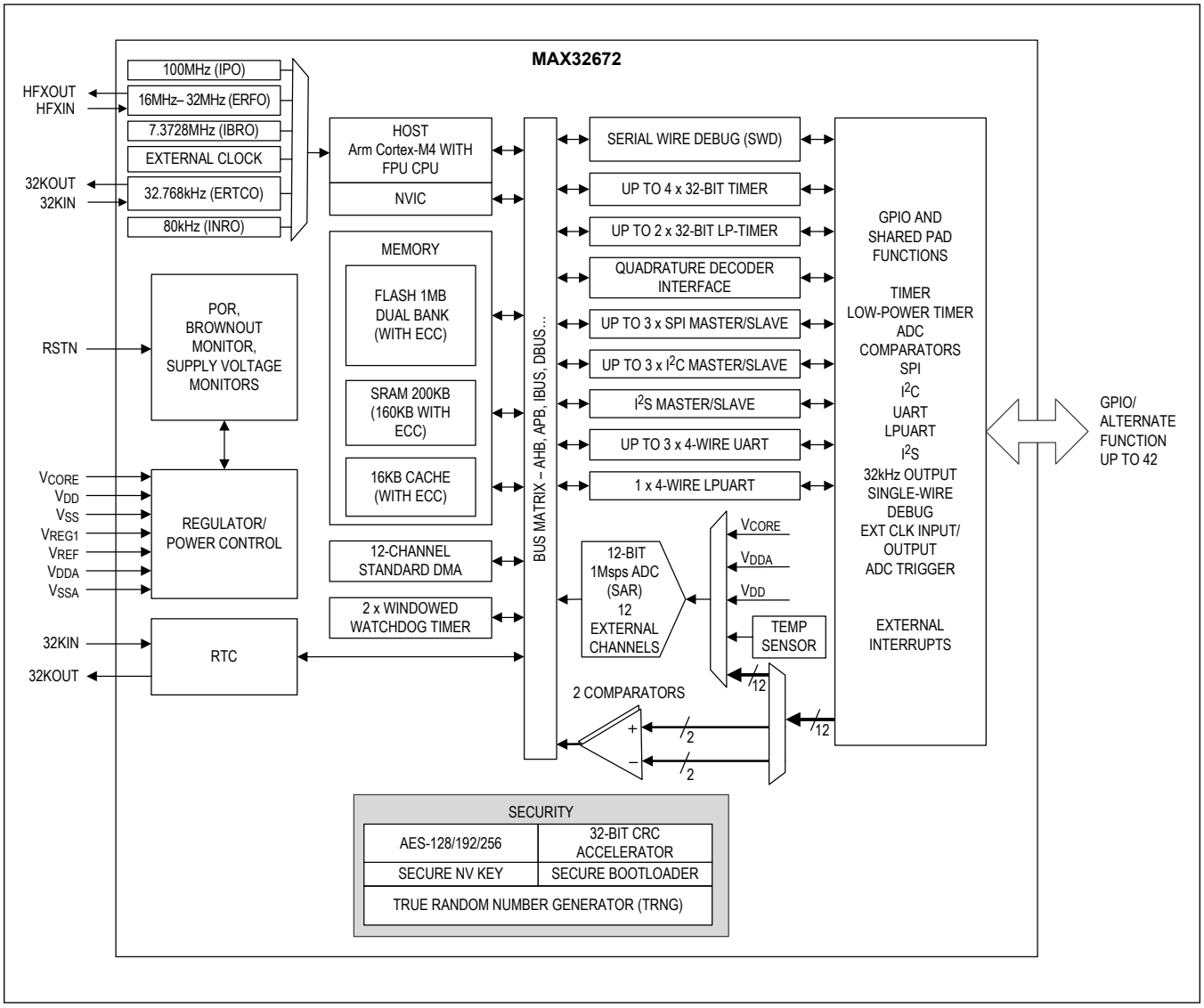
Benefits and Features

- High-Efficiency Microcontroller for Low-Power High-Reliability Devices
  - Arm Cortex-M4 Processor with FPU up to 100MHz
  - 1MB Dual-Bank Flash with Error Correction
  - 200KB SRAM (160KB with ECC Enabled), Optionally Preserved in Lowest Power Modes
  - EEPROM Emulation on Flash
  - 16KB Unified Cache with ECC
  - Resource Protection Unit (RPU) and Memory Protection Unit (MPU)
  - Dual- or Single-Supply Operation, 1.7V to 3.6V
  - Wide Operating Temperature: -40°C to +105°C
- Flexible Clocking Schemes
  - Internal High-Speed 100MHz Oscillator
  - Internal Low-Power 7.3728MHz and Ultra-Low-Power 80kHz Oscillators
  - 16MHz–32MHz Oscillator, 32.768kHz Oscillator (External Crystal Required)
  - External Clock Input for CPU, LPUART, LPTIMER
- Power Management Maximizes Uptime for Battery Applications
  - 53.2µA/MHz ACTIVE at 0.9V up to 12MHz (CoreMark®)
  - 61.5µA/MHz ACTIVE at 1.1V up to 100MHz
  - 2.94µA Full Memory Retention Power in BACKUP Mode at V_{DD} = 1.8V
  - 350nA Ultra-Low-Power RTC at V_{DD} = 1.8V
  - Wake from LPUART or LPTMR
- Optimal Peripheral Mix Provides Platform Scalability
  - Up to 42 General-Purpose I/O Pins
  - Up to Three SPI Master/Slave (up to 50Mbps)
  - Up to Three 4-Wire UART
  - Up to Three I^2C Master/Slave 3.4Mbps High Speed
  - Up to Four 32-Bit Timers (TMR)
  - Up to Two Low-Power 32-Bit Timers (LPTMR)
  - One I^2S Master/Slave for Digital Audio Interface
  - One 12-Channel, 12-Bit, 1Msps SAR ADC with On-Die Temperature Sensor
- Security and Integrity
  - Available ECDSA-Based Cryptographic Secure Bootloader in ROM
    - Secure Loader Interface over UART
  - AES-128/192/256 Hardware Acceleration Engine
  - TRNG Compliant to SP800-90B

***Ordering Information** appears at end of data sheet.*

19-101210; Rev 1; 1/22

Simplified Block Diagram



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Absolute Maximum Ratings

V_{CORE}, HFXIN, HFXOUT ..... -0.3V to +1.21V
V_{DD}, V_{DDA} ..... -0.3V to +3.63V
V_{REF} ..... -0.3V to V_{DDA} + 0.3V
32KIN, 32KOUT ..... -0.3V to V_{DD} + 0.3V
RSTN, GPIO ..... -0.3V to V_{DD} + 0.3V
Total Current into All GPIO Combined (sink) 100mA
V_{SS} 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA

Continuous Package Power Dissipation 40 TQFN-EP (multilayer board) T_A = +70°C (derate 35.7mW/°C above +70°C) 2857.10mW
Continuous Package Power Dissipation 56 TQFN-EP (multilayer board) T_A = +70°C (derate 40mW/°C above +70°C) 3200mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note: No device pins can exceed 3.63V. All voltages with respect to V_{SS}, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

40 TQFN-EP

Package Code	T4055+1
Outline Number	**21-0140**
Land Pattern Number	**90-0016**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	45°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	2°C/W

56 TQFN-EP

Package Code	T5677+1
Outline Number	**21-0144**
Land Pattern Number	**90-0042**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / BOTH SINGLE-SUPPLY OPERATION AND DUAL-SUPPLY OPERATION							
Supply Voltage	V_{DD}			1.71	1.8	3.63	V
Supply Voltage, Core	V_{CORE}	Dual-supply operation	OVR = [00]	0.855	0.9	0.945	V
			OVR = [01]	0.95	1.0	1.05	
			Default OVR = [10]	1.045	1.1	1.155	
		No power supply connection for single-supply operation			—		
Supply Voltage, Analog	V_{DDA}	V_{DDA} must be connected to V_{DD}		1.71		3.63	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}		1.58		1.71	V
		Monitors V_{CORE} during dual-supply operation		0.74		0.845	
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}			1.4		V
		Monitors V_{CORE} during dual-supply operation			0.6		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / SINGLE-SUPPLY OPERATION (V_{DD} ONLY); f_{SYS_OSC} = IPO							
V_{DD} Current ACTIVE Mode	I_{DD_DACTS}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		62.9		µA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		64.9		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		62.4		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		61.4		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		63		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		60.9		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		51.6		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		52.1		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		50.8		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		49.8		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		50.4		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		49.2		
	I_{DD_FACTS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		900		µA
			OVR = [01], internal regulator set to 1.0V		751		
			OVR = [00], internal regulator set to 0.9V		618		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		873		
			OVR = [01], internal regulator set to 1.0V		729		
			OVR = [00], internal regulator set to 0.9V		594		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current SLEEP Mode	I_{DD_DSLPS}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		36.6		μA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		38.3		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		38.7		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		36.5		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		37.9		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		38.7		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12.5		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11.6		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		12.9		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12.7		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		12		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		14.9		
	I_{DD_FSLPS}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		900		µA
			OVR = [01], internal regulator set to 1.0V		751		
			OVR = [00], internal regulator set to 0.9V		618		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		873		
			OVR = [01], internal regulator set to 1.0V		729		
			OVR = [00], internal regulator set to 0.9V		594		
SLEEP Mode Resume Time	t_{SLP_ONS}	f_{SYS_OSC} = IPO			0.1		µs
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	f_{SYS_OSC} = IPO	fast_wk_en = 1		74		µs
			fast_wk_en = 0		210		
BACKUP Mode Resume Time	t_{BKU_ONS}	f_{SYS_OSC} = IPO, includes system initialization and ROM execution time			1.08		ms
STORAGE Mode Resume Time	t_{STO_ONS}	f_{SYS_OSC} = IPO, includes system initialization and ROM execution time			1.08		ms

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / SINGLE-SUPPLY OPERATION (V_{DD} ONLY); f_{SYS_OSC} = IBRO							
V_{DD} Current ACTIVE Mode	I_{DD_DACTS}	Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		78		µA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		78		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		71		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		74.6		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		74.4		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		67.6		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		67.5		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		66.7		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		60.6		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		63.7		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		62.4		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		57.1		
	I_{DD_FACTS}	Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		423		µA
			OVR = [01], internal regulator set to 1.0V		357		
			OVR = [00], internal regulator set to 0.9V		298		
		Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		376		
			OVR = [01], internal regulator set to 1.0V		334		
			OVR = [00], internal regulator set to 0.9V		276		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current SLEEP Mode	I_{DD_DSLPS}	Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		51.8		µA/MHz
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		52		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		48.2		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		51.4		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		50.4		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		46.5		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		27.5		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		26		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		24.6		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		26.8		
			OVR = [01], internal regulator set to 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		24.4		
			OVR = [00], internal regulator set to 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		23		
	I_{DD_FSLPS}	Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		423		µA
			OVR = [01], internal regulator set to 1.0V		357		
			OVR = [00], internal regulator set to 0.9V		298		
		Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], internal regulator set to 1.1V		376		
			OVR = [01], internal regulator set to 1.0V		334		
			OVR = [00], internal regulator set to 0.9V		276		
SLEEP Mode Resume Time	t_{SLP_ONS}	f_{SYS_OSC} = IBRO			1.1		µs
DEEPSLEEP Mode Resume Time	t_{DSL_ONS}	f_{SYS_OSC} = IBRO	fast_wk_en = 1		182		µs
			fast_wk_en = 0		319		
BACKUP Mode Resume Time	t_{BKU_ONS}	f_{SYS_OSC} = IBRO, includes system initialization and ROM execution time			1.08		ms
STORAGE Mode Resume Time	t_{STO_ONS}	f_{SYS_OSC} = IBRO, includes system initialization and ROM execution time			1.08		ms
POWER / SINGLE-SUPPLY OPERATION (V_{DD} ONLY)							
V_{DD} Fixed Current, DEEPSLEEP Mode	I_{DD_FDSLS}	Standby state with full data retention and 200KB SRAM retained	V_{DD} = 3.3V		4.4		µA
			V_{DD} = 1.8V		4.1		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, BACKUP Mode	I_{DD_FBKUS}	V_{DD} = 3.3V, RTC disabled	0KB SRAM retained, retention regulator disabled		0.4		µA
			20KB SRAM retained		1.09		
			40KB SRAM retained		1.43		
			120KB SRAM retained		2.35		
			200KB SRAM retained		3.26		
		V_{DD} = 1.8V, RTC disabled	0KB SRAM retained, retention regulator disabled		0.138		
			20KB SRAM retained		0.81		
			40KB SRAM retained		1.15		
			120KB SRAM retained		2.07		
			200KB SRAM retained		2.97		
V_{DD} Fixed Current, STORAGE Mode	I_{DD_FSTOS}	V_{DD} = 3.3V			0.397		µA
		V_{DD} = 1.8V			0.123		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER / DUAL-SUPPLY OPERATION (V_{DD} AND V_{CORE}); f_{SYS_OSC} = IPO							
V_{CORE} Current, ACTIVE Mode	I_{CORE_DACTD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		61.5		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		63.1		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		53.2		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		50.3		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		50.5		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		54		
	I_{CORE_FACTD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		497		µA
			OVR = [01], V_{CORE} = 1.0V		335		
			OVR = [00], V_{CORE} = 0.9V		187		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current, ACTIVE Mode	I_{DD_DACTD}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.005		µA/MHz
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.004		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.003		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.0015		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.005		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.004		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 100MHz		0.003		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 50MHz		0.0015		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	I_{DD_FACTD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		420		µA
			OVR = [01], V_{CORE} = 1.0V		420		
			OVR = [00], V_{CORE} = 0.9V		420		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		400		
			OVR = [01], V_{CORE} = 1.0V		400		
			OVR = [00], V_{CORE} = 0.9V		400		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLPD}	Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		35.8		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		36.9		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		31.4		
		Dynamic, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		12		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		11		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		9		
	I_{CORE_FSLPD}	Fixed, IPO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR [10], V_{CORE} = 1.1V		497		µA
			OVR [01], V_{CORE} = 1.0V		335		
			OVR [00], V_{CORE} = 0.9V		187		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current, SLEEP Mode	I_{DD_DSLPD}	Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		0.001		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		0.001		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
		Dynamic, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 100MHz		0.001		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 50MHz		0.001		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 12MHz		0.001		
	I_{DD_FSLPD}	Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		420		µA
			OVR = [01], V_{CORE} = 1.0V		420		
			OVR = [00], V_{CORE} = 0.9V		420		
		Fixed, IPO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		400		
			OVR = [01], V_{CORE} = 1.0V		400		
			OVR = [00], V_{CORE} = 0.9V		400		
SLEEP Mode Resume Time	t_{SLP_OND}	f_{SYS_OSC} = IPO			0.1		µs
DEEPSLEEP Mode Resume Time	t_{DSL_OND}	f_{SYS_OSC} = IPO	fast_wk_en = 1		37		µs
			fast_wk_en = 0		184		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BACKUP Mode Resume Time	t_{BKU_OND}	f_{SYS_OSC} = IPO, includes system initialization and ROM execution time			1.05		ms
STORAGE Mode Resume Time	t_{STO_OND}	f_{SYS_OSC} = IPO, includes system initialization and ROM execution time			1.05		ms
POWER / DUAL-SUPPLY OPERATION (V_{DD} AND V_{CORE}); f_{SYS_OSC} = IBRO							
V_{CORE} Current, ACTIVE Mode	I_{CORE_DACTD}	Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		65.1		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		65.1		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		54.8		
		Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		53.1		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		53.1		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		44.1		
	I_{CORE_FACTD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		280		µA
			OVR = [01], V_{CORE} = 1.0V		235		
			OVR = [00], V_{CORE} = 0.9V		157		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current, ACTIVE Mode	I_{DD_DACTD}	Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0054		µA/MHz
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0045		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0045		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing CoreMark, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0036		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0027		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0027		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0054		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0045		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0045		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode, executing While(1), ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0036		
			OVR = [01], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0027		
			OVR = [00], $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0027		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	I_{DD_FACTD}	Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		131		µA
			OVR = [01], V_{CORE} = 1.0V		131		
			OVR = [00], V_{CORE} = 0.9V		131		
		Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in ACTIVE mode 0MHz execution, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		113		
			OVR = [01], V_{CORE} = 1.0V		113		
			OVR = [00], V_{CORE} = 0.9V		113		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Current, SLEEP Mode	I_{CORE_DSLPD}	Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.06		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.05		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.036		
		Dynamic, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, DMA disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.037		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.027		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.016		
	I_{CORE_FSLPD}	Fixed, IBRO enabled, total current into V_{CORE} pin, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR [10], V_{CORE} = 1.1V		280		µA
			OVR [01], V_{CORE} = 1.0V		235		
			OVR [00], V_{CORE} = 0.9V		157		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Current, SLEEP Mode	I_{DD_DSLPD}	Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0123		µA/MHz
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0116		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0116		
		Dynamic, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, standard DMA with two channels active, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0123		
			OVR = [01], V_{CORE} = 1.0V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0116		
			OVR = [00], V_{CORE} = 0.9V, $f_{SYS\_CLK(MAX)}$ = 7.3728MHz		0.0116		
	I_{DD_FSLPD}	Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 3.3V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		131		µA
			OVR = [01], V_{CORE} = 1.0V		131		
			OVR = [00], V_{CORE} = 0.9V		131		
		Fixed, IBRO enabled, total current into V_{DD} pin, V_{DD} = 1.8V, CPU in SLEEP mode, ECC disabled, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], V_{CORE} = 1.1V		113		
			OVR = [01], V_{CORE} = 1.0V		113		
			OVR = [00], V_{CORE} = 0.9V		113		
SLEEP Mode Resume Time	t_{SLP_OND}	f_{SYS_OSC} = IBRO			1.1		µs
DEEPSLEEP Mode Resume Time	t_{DSL_OND}	f_{SYS_OSC} = IBRO	fast_wk_en = 1		146		µs
			fast_wk_en = 0		295		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BACKUP Mode Resume Time	t_{BKU_OND}	f_{SYS_OSC} = IBRO, includes system initialization and ROM execution time		1.05		ms
STORAGE Mode Resume Time	t_{STO_OND}	f_{SYS_OSC} = IBRO, includes system initialization and ROM execution time		1.05		ms
POWER / DUAL-SUPPLY OPERATION (V_{DD} AND V_{CORE})						
V_{CORE} Fixed Current, DEEPSLEEP Mode	I_{CORE_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V		11		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V		4.1		
		V_{DD} = 1.8V, V_{CORE} = 1.1V		11		
		V_{DD} = 1.8V, V_{CORE} = 0.855V		4.1		
V_{DD} Fixed Current, DEEPSLEEP Mode	I_{DD_FDSLPD}	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
		V_{DD} = 1.8V, V_{CORE} = 1.1V		0.11		
		V_{DD} = 1.8V, V_{CORE} = 0.855V		0.11		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Fixed Current, BACKUP Mode	I_{CORE_FBKUD}	0KB SRAM retained, RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.28		µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.15		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.28		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.15		
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		1.256		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.52		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		1.256		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.52		
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		2.21		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.881		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		2.21		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.881		
		120KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		5.23		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		1.91		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		5.23		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		1.91		
		200KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		8.26		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		2.94		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		8.26		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		2.94		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, BACKUP Mode	I_{DD_FBKUD}	0KB SRAM retained with RTC disabled, retention regulator disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		µA
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.12		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.12		
		20KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.12		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.12		
		40KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.12		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.12		
		120KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.12		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.12		
		200KB SRAM retained with RTC disabled	V_{DD} = 3.3V, V_{CORE} = 1.1V		0.34		
			V_{DD} = 3.3V, V_{CORE} = 0.855V		0.34		
			V_{DD} = 1.8V, V_{CORE} = 1.1V		0.12		
			V_{DD} = 1.8V, V_{CORE} = 0.855V		0.12		
V_{CORE} Fixed Current, STORAGE Mode	I_{CORE_FSTOD}	V_{DD} = 3.3V, V_{CORE} = 1.1V			0.284		µA
		V_{DD} = 3.3V, V_{CORE} = 0.855V			0.15		
		V_{DD} = 1.8V, V_{CORE} = 1.1V			0.284		
		V_{DD} = 1.8V, V_{CORE} = 0.855V			0.15		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Fixed Current, STORAGE Mode	I_{DD_FSTOD}	V_{DD} = 3.3V; V_{CORE} = 1.1V		0.385		µA
		V_{DD} = 3.3V; V_{CORE} = 0.855V		0.385		
		V_{DD} = 1.8V; V_{CORE} = 1.1V		0.128		
		V_{DD} = 1.8V; V_{CORE} = 0.855V		0.128		
CLOCKS						
System Clock Frequency	f_{SYS_CLK}				100	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		µs
Internal Primary Oscillator (IPO)	f_{IPO}	Default OVR = [10]		100		MHz
External RF Oscillator (ERFO)	f_{ERFO}	Required crystal characteristics: C_L = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm	16		32	MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}	Measured at V_{DD} = 1.8V		70		kHz
External RTC Oscillator (ERTCO)	f_{ERTCO}	32.768kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 < 2pF		32.768		kHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled		0.35		µA
RTC Power-Up Time	t_{RTC_ON}			250		ms
External Clock Input Frequency	f_{EXT_CLK}	EXT_CLK1 selected			50	MHz
		EXT_CLK2 selected			1	
12-BIT SAR ADC						
Resolution				12		bits
Effective Number of Bits	ENOB	ADC_CLKCTRL.clkdiv = 0bX00. AINx input pk--pk = V_{REF} – 10mV		10		bits
External Reference Voltage	V_{REF}	V_{REF} ≤ V_{DDA}	2.048		V_{DDA}	V
Internal Reference Voltage	V_{INT_REF}	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0		1.25		V
	V_{INT_REF}	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 1		2.048		
ADC Clock Rate	f_{ACLK}			1		MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{AIN}	AIN[11:0], ADC_DATA.chan = [11:0]	ADC_CLKCTRL.clkdiv = 0bX00	V_{SSA} + 0.05		V_{REF}	V
			ADC_CLKCTRL.clkdiv = 0bX01	V_{SSA} + 0.05		min(2 x V_{REF},V_{DDA})	
			ADC_CLKCTRL.clkdiv = 0bX10	V_{SSA} + 0.05		min(2 x V_{REF},V_{DDA})	
Input Impedance	R_{AIN}	ADC_CLKCTRL.clkdiv = 0bX01			5		kΩ
		ADC_CLKCTRL.clkdiv = 0bX10			50		
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}			2		pF
		Dynamically switched capacitance			1.2		pF
Integral Nonlinearity	INL				±1.5		LSb
Differential Nonlinearity	DNL				±0.75		LSb
Offset Error	V_{OS}	Chopping disabled			±9		LSb
		Chopping enabled			±0.2		
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, ADC_CLKCTRL.clkdiv = 0bX00	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0, V_{DDA} = 1.8V		500		µA
			MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 1, V_{DDA} = 3.3V		788		
		ADC active, reference buffer enabled, ADC_CLKCTRL.clkdiv = 0bX01	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0, V_{DDA} = 1.8V		440		
			MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 1, V_{DDA} = 3.3V		670		
		ADC active, reference buffer enabled, ADC_CLKCTRL.clkdiv = 0bX10	MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 0, V_{DDA} = 1.8V		366		
			MCR_ADC_CFG0.ext_ref = 0, MCR_ADC_CFG0.ref_sel = 1, V_{DDA} = 3.3V		512		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Sample Rate	f_{ADC}	ADC_CLKCTRL.clkdiv = 0bX00			1	Msps
		ADC_CLKCTRL.clkdiv = 0bX01			0.625	
		ADC_CLKCTRL.clkdiv = 0bX10			0.125	
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart			500	µs
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected		0.4		nA
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		45		ppm
COMPARATORS						
Input Offset Voltage	V_{OFFSET}			±3		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00		22		mV
		AINCOMPHYST[1:0] = 01		50		
		AINCOMPHYST[1:0] = 10		2		
		AINCOMPHYST[1:0] = 11		7		
Input Voltage Range	V_{IN_CMP}	Common-mode range	0.6		1.35	V
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO, RSTN	V_{IL_GPIO}	Pin configured as GPIO			0.3 × V_{DD}	V
Input High Voltage for All GPIO, RSTN	V_{IH_GPIO}	Pin configured as GPIO	0.7 × V_{DD}			V
Output Low Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OL_GPIO}	V_{DD} = 1.71V, I_{OL} = 1mA, DS[1:0] = 00 (*Note 1*)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 2mA, DS[1:0] = 10 (*Note 1*)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 4mA, DS[1:0] = 01 (*Note 1*)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 6mA, DS[1:0] = 11 (*Note 1*)		0.2	0.4	
Output Low Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, P0.19	V_{OL_I2C}	V_{DD} = 1.71V, I_{OL} = 2mA, DS = 0 (*Note 1*)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 8mA, DS = 1 (*Note 1*)		0.2	0.4	
Output High Voltage for All GPIO Except P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_GPIO}	V_{DD} = 1.71V, I_{OH} = 1mA, DS[1:0] = 00 (*Note 1*)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 2mA, DS[1:0] = 10 (*Note 1*)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 4mA, DS[1:0] = 01 (*Note 1*)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 6mA, DS[1:0] = 11 (*Note 1*)	V_{DD} - 0.4			

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage for GPIO P0.6, P0.7, P0.12, P0.13, P0.18, and P0.19	V_{OH_I2C}	V_{DD} = 1.71V, I_{OH} = 2mA, DS = 0 (*Note 1*)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 8mA, DS = 1 (*Note 1*)	V_{DD} - 0.4			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				100	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-100			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	V_{IN} = 0V, internal pullup disabled	-500		+500	nA
Input Leakage Current High	I_{IH}	V_{IN} = 3.6V, internal pulldown disabled	-500		+500	nA
Input Pullup Resistor to RSTN	R_{PU_VDD}	Pullup to V_{DD} = V_{RST}, RSTN at V_{IH}		18.7		kΩ
		Pullup to V_{DD} = 3.63V, RSTN at V_{IH}		10.0		
Input Pullup Resistor for All GPIO	R_{PU}	Device pin configured as GPIO, pullup to V_{DD} = V_{RST}, device pin at V_{IH}		18.7		kΩ
		Device pin configured as GPIO, pullup to V_{DD} = 3.63V, device pin at V_{IH}		10.0		
Input Pulldown Resistor for All GPIO	R_{PD}	Device pin configured as GPIO, pulldown to V_{SS}, V_{DD} = V_{RST}, device pin at V_{IL}		17.6		kΩ
		Device pin configured as GPIO, pulldown to V_{SS}, V_{DD} = 3.63V, device pin at V_{IL}		8.8		
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	f_{SYS_CLK} = 100MHz, $f_{MCK(MAX)}$ = f_{SYS_CLK}/2			50	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				50	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid after SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time after SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I^2C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low-Period SCL Clock	t_{LOW}		4.7			µs
High-Time SCL Clock	t_{HIGH}		4.0			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low-Period SCL Clock	t_{LOW}		1.3			µs
High-Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low-Period SCL Clock	t_{LOW}		0.5			µs
High-Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—I²S Slave

(Timing specifications are guaranteed by design and not production tested, T_A = -40°C to +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLKS}				25	MHz
Bit Clock Period	t_{BCLKS}		$1/f_{BCLKS}$			ns
BCLK High Time	$t_{WBCLKHS}$			0.5		$1/f_{BCLKS}$
BCLK Low Time	$t_{WBCLKLS}$			0.5		$1/f_{BCLKS}$
LRCLK Setup Time	t_{LRCLK_BCLKS}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOS}			12		ns
Setup Time for SD (Input)	t_{SU_SDIS}			6		ns
Hold Time SD (Input)	t_{HD_SDIS}			3		ns

Electrical Characteristics—Quadrature Decoder

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Encoder Period	t_{EP}	Ensure at least one sample in each encoder state	4	8		t_{PCLK}
Encoder Pulse Width	t_{E}	Ensure at least one sample in each encoder state	2	4		t_{PCLK}
Encoder State Period	t_{ES}	Ensure at least one sample in each encoder state	1	2		t_{PCLK}
Index Signal Width	t_{IND}		1	1/4 x t_{EP}	t_{EP}	t_{PCLK}
Expected Glitch Time Window	t_{GL}	QDEC_CTRL.filter = 0b00	0			t_{PCLK}
		QDEC_CTRL.filter = 0b01		1		
Q DIRECTION	t_{QDIR}	After either QEA or QEB transition		4		t_{PCLK}
Q MATCH	t_{QM}	After either QEA or QEB transition		4		t_{PCLK}
Q MATCH Pulse Width	t_{QMP}	Until next state transition		1		t_{ES}
Q ERROR	t_{ER}	After either a faulty QEA or QEB transition		4		t_{PCLK}
Q ERROR Pulse Width	t_{ERP}	Until next state transition		1		t_{ES}

GPIO Drive Strength: **Note 1:** When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.62V.

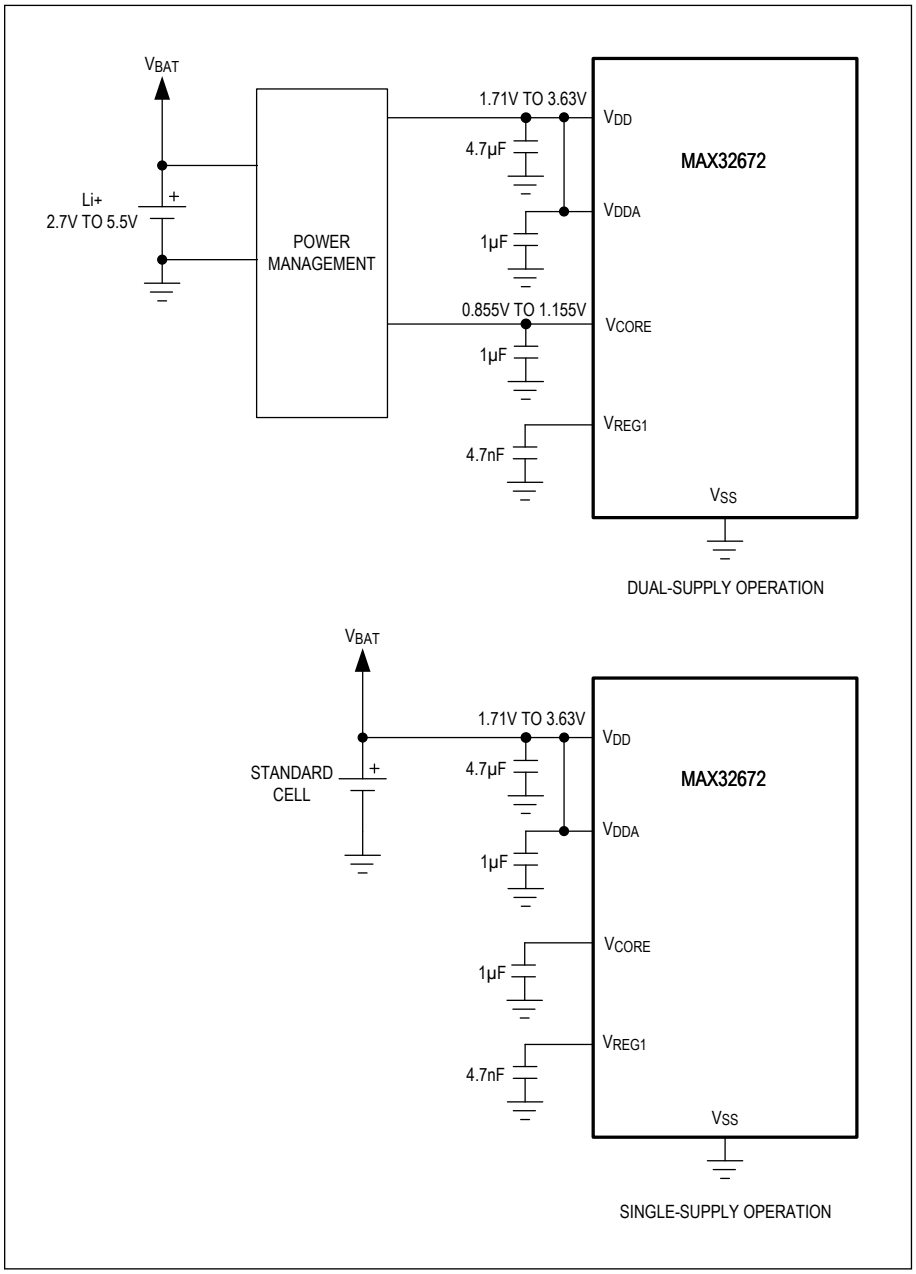


Figure 1. Power Supply Operational Modes

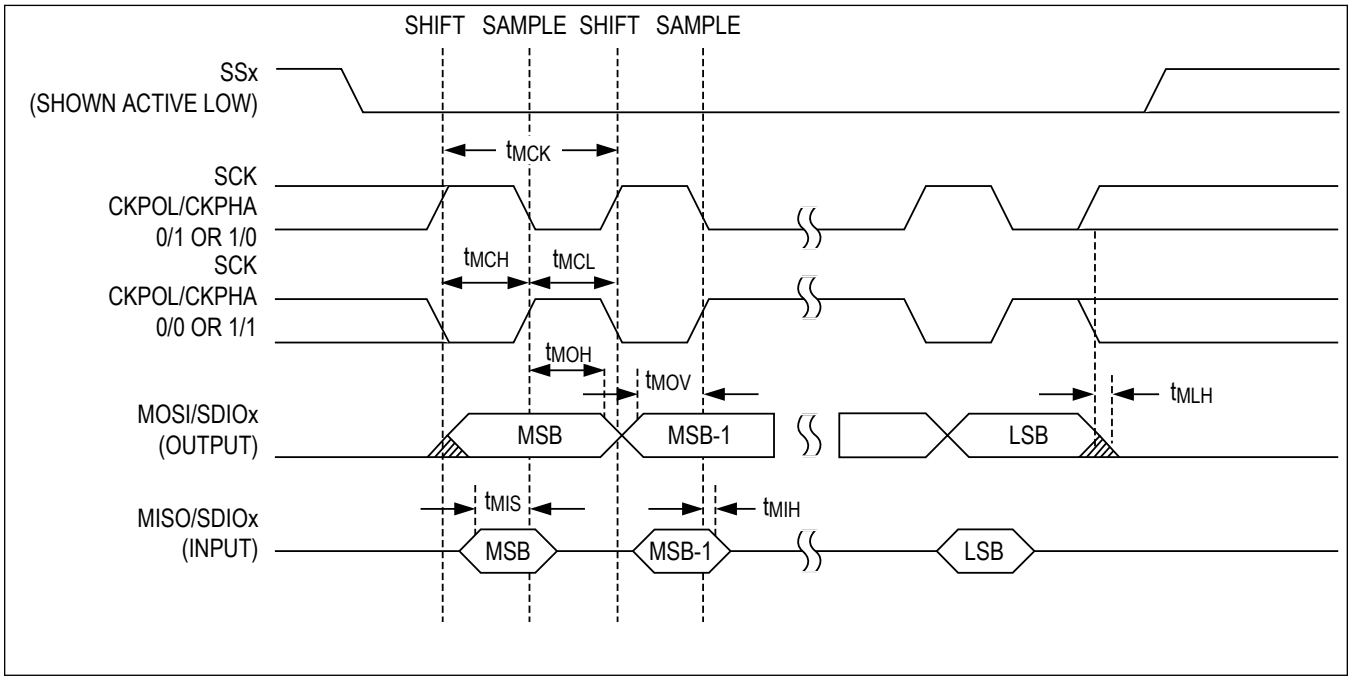


Figure 2. SPI Master Mode Timing Diagram

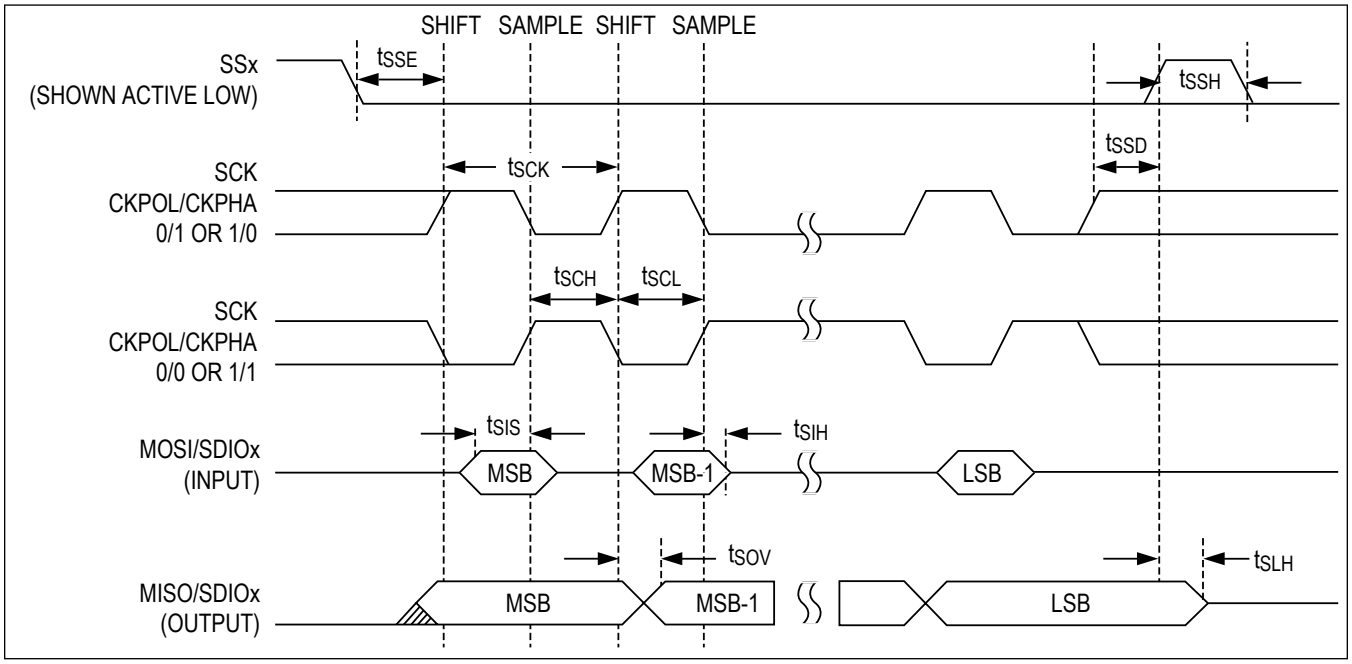


Figure 3. SPI Slave Mode Timing Diagram

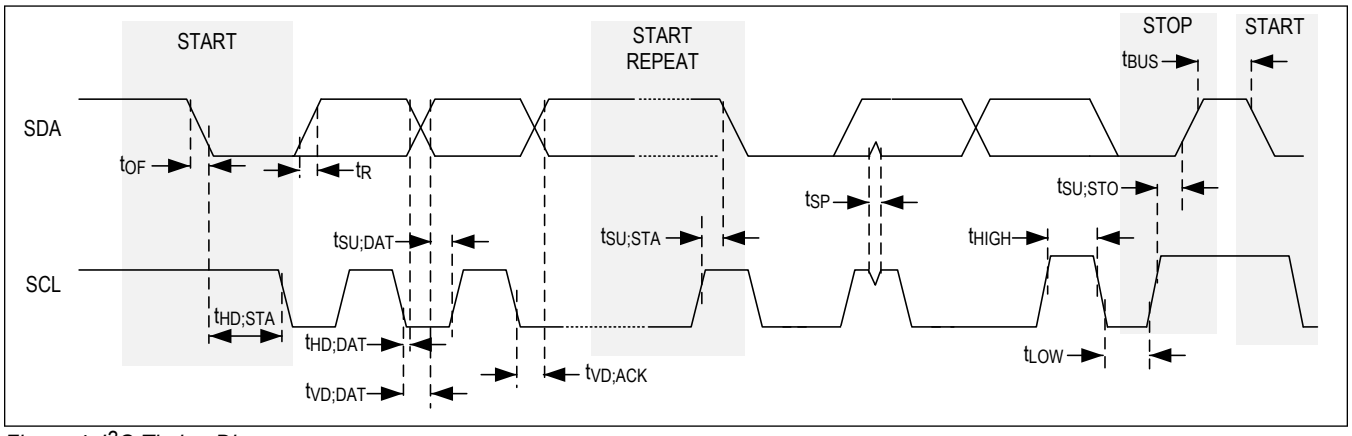


Figure 4. I²C Timing Diagram

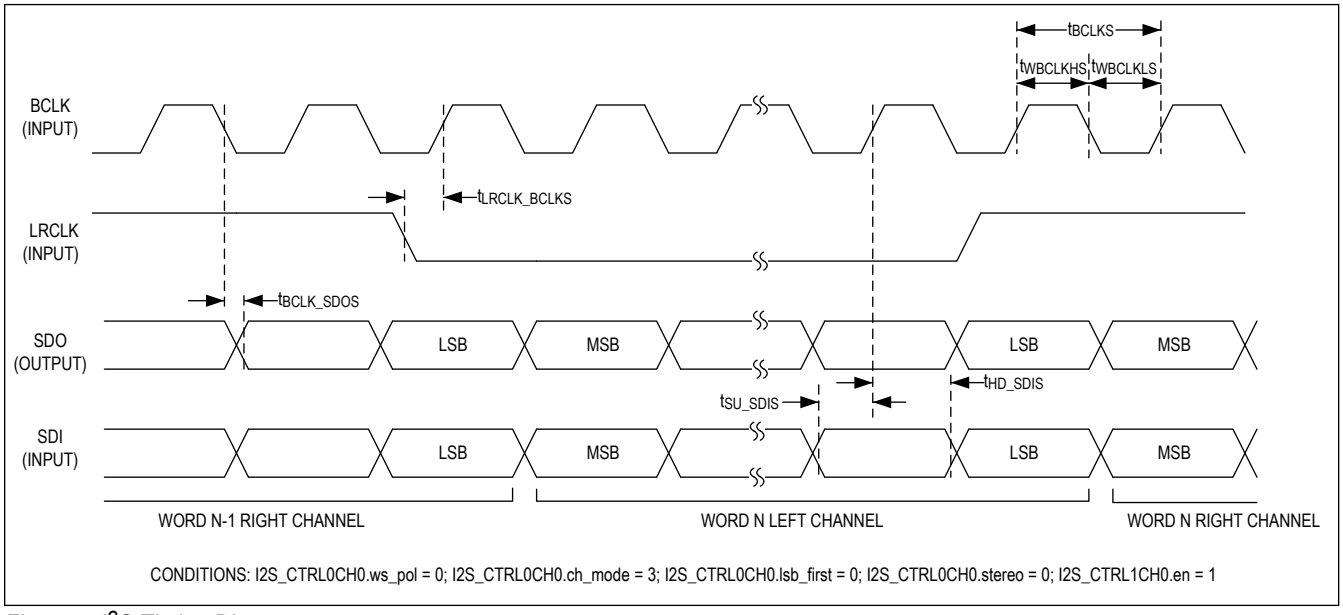


Figure 5. I²S Timing Diagram

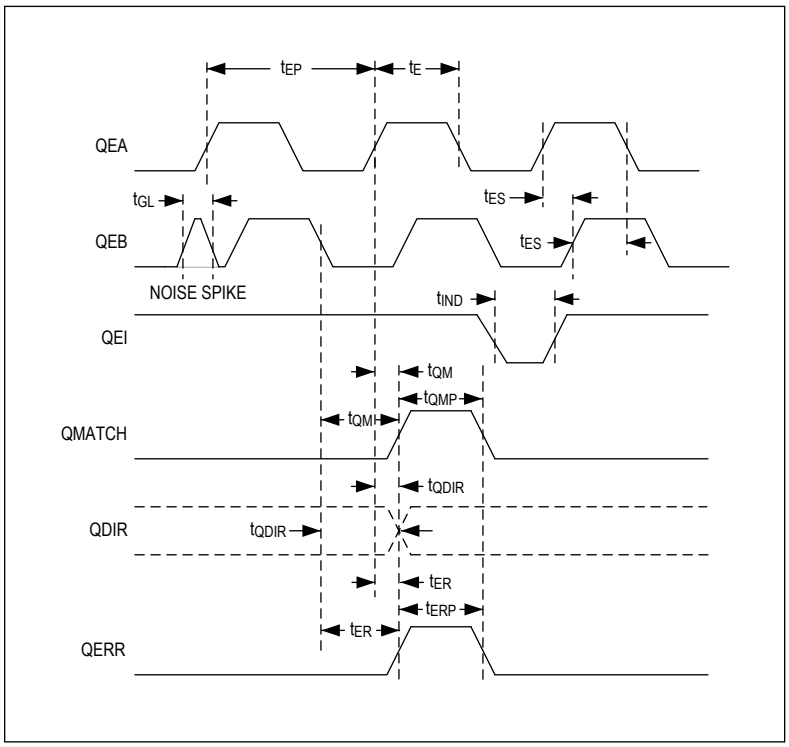
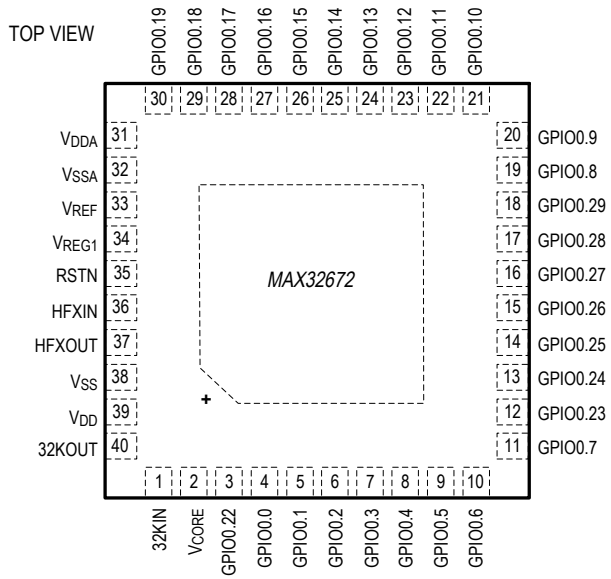


Figure 6. Quadrature Decoder Timing Diagram

Pin Configuration

40 TQFN



TQFN
5mm x 5mm

Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER AND SYSTEM PINS							
2	V_{CORE}	—	—	—	—	—	Digital Supply Voltage. Bypass with 1.0µF to V_{SS}.
34	V_{REG1}	—	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
39	V_{DD}	—	—	—	—	—	GPIO Supply Voltage. Bypass with 4.7µF to V_{SS}.
EP, 38	V_{SS}	—	—	—	—	—	Digital Ground. Exposed pad (TQFN only). This pad must be connected to V_{SS}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
33	V_{REF}	—	—	—	—	—	ADC External Reference Input. This is the reference input for the ADC. Bypass with 1.0µF to V_{SS}.

40 TQFN

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
31	V_{DDA}	—	—	—	—	—	Analog Supply Voltage. This pin must always be connected to the V_{DD} device pin at the PCB level. Bypass this pin to V_{SSA} with 1.0µF as close as possible to the package.
32	V_{SSA}	—	—	—	—	—	Analog Ground
35	RSTN	—	—	—	—	—	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
CLOCK PINS							
40	32KOUT	—	—	—	—	—	32kHz Crystal Oscillator Output. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors.
1	32KIN	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
36	HFXIN	—	—	—	—	—	RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square-wave source. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors.
37	HFXOUT	—	—	—	—	—	RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors.

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
GPIO AND ALTERNATE FUNCTION							
4	P0.0	P0.0	SWDIO	—	TMR0C_IA	—	Single-Wire Debug I/O; Timer0 Port Map C Input 32 Bits or Lower 16 Bits
5	P0.1	P0.1	SWDCLK	—	TMR0C_OA	—	Single-Wire Debug Clock; Timer0 Port Map C Output 32 Bits or Lower 16 Bits
6	P0.2	P0.2	SPI0A_MISO	UART1B_RX	TMR1C_IA	—	SPI0 Master In Slave Out; UART1 Port Map B RX; Timer1 Port Map C Input 32 Bits or Lower 16 Bits
7	P0.3	P0.3	SPI0A_MOSI	UART1B_TX	TMR1C_OA	—	SPI0 Master Out Slave In; UART1 Port Map B Tx; Timer1 Port Map C Output 32 Bits or Lower 16 Bits
8	P0.4	P0.4	SPI0A_SCK	UART1B_CTS	TMR2C_IA	—	SPI0 Serial Clock; UART1 Port Map B CTS; Timer2 Port Map C Input 32 Bits or Lower 16 Bits
9	P0.5	P0.5	SPI0A_SS0	UART1B_RTS	TMR2C_OA	HFX_CLK_OUT	SPI0 Slave Select 0; UART1 Port Map B RTS; Timer2 Port Map C Output; ERFO Buffered Output 32 Bits or Lower 16 Bits
10	P0.6	P0.6	I2C0A_SCL	LPTMR0B_IA	SPI0C_SS1	QEA	I2C0 Serial Clock; Low-Power Timer0 Port Map A Input 32 Bits or Lower 16 Bits; SPI0 Slave Select 1; Quadrature Decoder Phase A Input
11	P0.7	P0.7	I2C0A_SDA	LPTMR0B_OA	SPI0C_SS2	QEB	I2C0 Serial Data; Low-Power Timer0 Port Map A Output 32 Bits or Lower 16 Bits; SPI0 Slave Select 2; Quadrature Decoder Phase B Input
19	P0.8	P0.8	UART0A_RX	I2S0A_SDO	TMR0C_IA	AIN0/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A Rx; I2S0 Serial Data Output; Timer0 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Negative Input
20	P0.9	P0.9	UART0A_TX	I2S0A_LRCLK	TMR0C_OA	AIN1/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A Tx; I2S0 Left/ Right Clock; Timer0 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Negative Input
21	P0.10	P0.10	UART0A_CTS	I2S0A_BCLK	TMR1C_IA	AIN2/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A CTS; I2S0 Bit Clock; Timer Port Map C Input 32 Bits or Lower 16 Bits; Comparator Negative Input
22	P0.11	P0.11	UART0A_RTS	I2S0A_SDI	TMR1C_OA	AIN3/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A RTS; I2S0 Serial Data Input; Timer1 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Negative Input
23	P0.12	P0.12	I2C1A_SCL	EXT_CLK2	TMR2C_IA	AIN4/ AIN_C0_P/ AIN_C1_P	I2C1 Serial Clock; Low-Power External Clock Input; Timer2 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Positive Input

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
24	P0.13	P0.13	I2C1A_SDA	32KCAL	TMR2C_OA	AIN5/ AIN_C0_P/ AIN_C1_P	I2C1 Serial Data; 32.768kHz Calibration Output; Timer2 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Positive Input
25	P0.14	P0.14	SPI1A_MISO	UART2B_RX	TMR3C_IA	AIN6/ AIN_C0_P/ AIN_C1_P	SPI1 Master In Slave Out; UART2 Port Map B Rx; Timer3 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Positive Input
26	P0.15	P0.15	SPI1A_MOSI	UART2B_TX	TMR3C_OA	AIN7/ AIN_C0_P/ AIN_C1_P	SPI1 Master Out Slave In; UART2 Port Map B Tx; Timer3 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 7/Comparator Positive Input
27	P0.16	P0.16	SPI1A_SCK	UART2B_CTS	TMR0C_IA	AIN8	SPI1 Serial Clock; UART2 Port Map B CTS; Timer0 Port Map C Input 32 Bits or Lower 16 Bits; ADC Input 8
28	P0.17	P0.17	SPI1A_SS0	UART2B_RTS	TMR0C_OA	AIN9	SPI1 Slave Select 0; UART2 Port Map B RTS; Timer0 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 9
29	P0.18	P0.18	I2C2A_SCL	—	TMR1C_IA	AIN10	I2C2 Serial Clock; Timer1 Port Map C Input 32 Bits or Lower 16 Bits; ADC Input 10
30	P0.19	P0.19	I2C2A_SDA	—	TMR1C_OA	AIN11	I2C2 Serial Data; Timer1 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 11
3	P0.22	P0.22	LPTMR1A_IA	ADC_TRIG_B	TMR0C_IA	—	Low-Power Timer1 Port Map A Input; ADC Trigger Port Map B; Timer0 Port Map C Input 32 Bits or Lower 16 Bits
12	P0.23	P0.23	LPTMR1A_OA	—	SPI0C_SS3	QEI	Low-Power Timer1 Port Map A Output; SPI0 Slave Select 3; Quadrature Decoder Index Input
13	P0.24	P0.24	LPUART0A_CTS	UART0B_RX	I2S0A_SD0	QES	Low-Power UART0 CTS; UART0 Port Map B Rx; I2S0 Serial Data Output; Quadrature Decoder Capture Input
14	P0.25	P0.25	LPUART0A_RTS	UART0B_TX	I2S0A_LRCLK	QMATCH	Low-Power UART0 RTS; UART0 Port Map B Tx; I2S0 Left/Right Clock; Quadrature Decoder Match Output
15	P0.26	P0.26	LPUART0A_RX	UART0B_CTS	I2S0C_BCLK	QDIR	Low-Power UART0 Rx; UART0 Port Map B CTS; I2S0 Bit Clock; Quadrature Decoder Direction Output
16	P0.27	P0.27	LPUART0A_TX	UART0B_RTS	I2S0C_SDI	QERR	Low-Power UART0 Port Map A Tx; UART0 Port Map B Request to Send; I2S 0 Port Map C Serial Data Input; Quadrature Decoder Error Output

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
17	P0.28	P0.28	UART1A_RX	EXT_CLK1	TMR3C_IA	—	UART1 Port Map A Receive; Timer3 Port Map C Input 32 Bits or Lower 16 Bits; External Clock Input
18	P0.29	P0.29	UART1A_TX	SPI1_SS0	TMR3C_OA	ADC_TRIG_D	UART1 Port Map A Transmit; SPI1 Port Map B Slave Select 0; Timer3 Port Map C Output 32 Bits or Lower 16 Bits; ADC Trigger Port Map D

Pin Configuration

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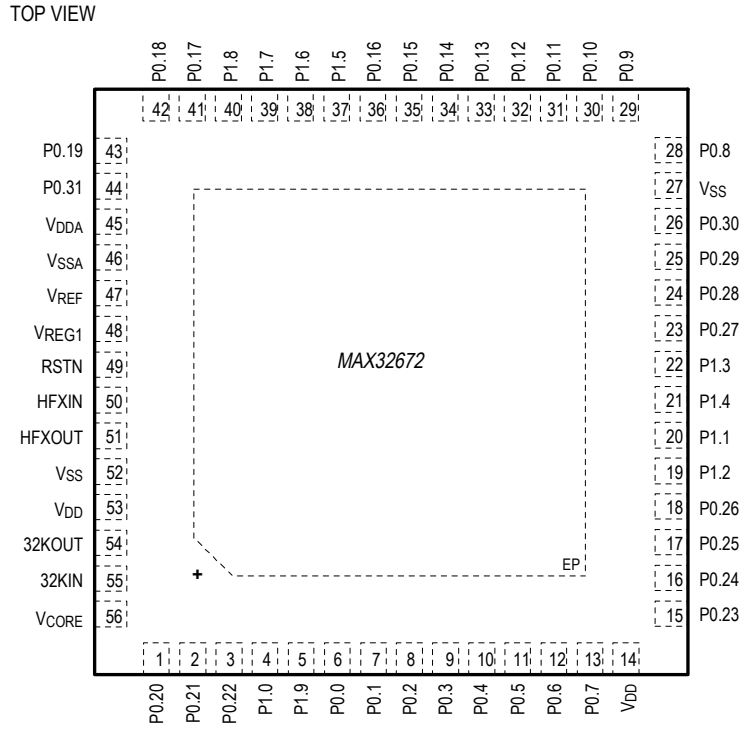

TQFN
7mm x 7mm

Pin Description

PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
POWER AND SYSTEM PINS							
56	V_{CORE}	—	—	—	—	—	Digital Supply Voltage. Bypass with 1.0µF to V_{SS}.
48	V_{REG1}	—	—	—	—	—	Bypass with 4.7nF to V_{SS}. Do not connect this device pin to any other external circuitry.
14, 53	V_{DD}	—	—	—	—	—	GPIO Supply Voltage. Bypass with 4.7µF to V_{SS}.
EP, 27, 52	V_{SS}	—	—	—	—	—	Digital Ground. Exposed pad (TQFN only). This pad must be connected to V_{SS}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
47	V_{REF}	—	—	—	—	—	ADC External Reference Input. This is the reference input for the ADC converter. Bypass with 1.0µF to V_{SS}.
45	V_{DDA}	—	—	—	—	—	Analog Supply Voltage. This pin must always be connected to the V_{DD} device pin at the PCB level. Bypass this pin to V_{SSA} with 1.0µF as close as possible to the package.
46	V_{SSA}	—	—	—	—	—	Analog Ground
49	RSTN	—	—	—	—	—	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
CLOCK PINS							
54	32KOUT	—	—	—	—	—	32kHz Crystal Oscillator Output. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors.
55	32KIN	—	—	—	—	—	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors Optionally, this pin can be configured as the input for an external CMOS-level clock source.

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
50	HFXIN	—	—	—	—	—	RF Crystal Oscillator Input. Connect the crystal between HFXIN and HFXOUT. Optionally, this pin can be configured as the input for an external square wave source. See the *Electrical Characteristics* table for details of the crystal requirements. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors.
51	HFXOUT	—	—	—	—	—	RF Crystal Oscillator Output. Connect the crystal between HFXIN and HFXOUT. See *Electrical Characteristics* for details of the crystal requirements. Refer to the *MAX32672 User Guide* for determination of the required external stability capacitors
GPIO AND ALTERNATE FUNCTION							
6	P0.0	P0.0	SWDIO	—	TMR0C_IA	—	Single-Wire Debug I/O; Timer0 Port Map C Input 32 Bits or Lower 16 Bits
7	P0.1	P0.1	SWDCLK	—	TMR0C_OA	—	Single-Wire Debug Clock; Timer0 Port Map C Output 32 Bits or Lower 16 Bits
8	P0.2	P0.2	SPI0A_MISO	UART1B_RX	TMR1C_IA	—	SPI0 Port Map A Master In Slave Out; UART1 Port Map B Rx; Timer1 Port Map C Input 32 Bits or Lower 16 Bits
9	P0.3	P0.3	SPI0A_MOSI	UART1B_TX	TMR1C_OA	—	SPI0 Master Out Slave In; UART1 Port Map B Tx; Timer1 Port Map C Output 32 Bits or Lower 16 Bits
10	P0.4	P0.4	SPI0A_SCK	UART1B_CTS	TMR2C_IA	—	SPI0 Serial Clock; UART1 Port Map B CTS; Timer2 Port Map C Input 32 Bits or Lower 16 Bits
11	P0.5	P0.5	SPI0A_SS0	UART1B_RTS	TMR2C_OA	HFX_CLK_OUT	SPI0 Slave Select 0; UART1 Port Map B RTS; Timer2 Port Map C Output 32 Bits or Lower 16 Bits; ERFO Buffered Output
12	P0.6	P0.6	I2C0A_SCL	LPTMR0B_IA	SPI0C_SS1	QEA	I2C0 Serial Clock; Low-Power Timer0 Port Map A Input 32 Bits or Lower 16 Bits; SPI0 Slave Select 1; Quadrature Decoder Phase A Input
13	P0.7	P0.7	I2C0A_SDA	LPTMR0B_OA	SPI0C_SS2	QEB	I2C0 Serial Data; Low-Power Timer0 Port Map A Output 32 Bits or Lower 16 Bits; SPI0 Slave Select 2; Quadrature Decoder Phase B Input

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
28	P0.8	P0.8	UART0A_RX	I2S0A_SDO	TMR0C_IA	AIN0/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A Rx; I2S0 Serial Data Output; Timer0 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Negative Input
29	P0.9	P0.9	UART0A_TX	I2S0A_LRCLK	TMR0C_OA	AIN1/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A Tx; I2S0 Left/ Right Clock; Timer0 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Negative Input
30	P0.10	P0.10	UART0A_CTS	I2S0A_BCLK	TMR1C_IA	AIN2/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A CTS; I2S0 Bit Clock; Timer1 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Negative Input
31	P0.11	P0.11	UART0A_RTS	I2S0A_SDI	TMR1C_OA	AIN3/ AIN_C0_N/ AIN_C1_N	UART0 Port Map A RTS; I2S0 Serial Data Input; Timer1 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Negative Input
32	P0.12	P0.12	I2C1A_SCL	EXT_CLK2	TMR2C_IA	AIN4/ AIN_C0_P/ AIN_C1_P	I2C1 Serial Clock; Low-Power External Clock Input; Timer2 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Positive Input
33	P0.13	P0.13	I2C1A_SDA	32KCAL	TMR2C_OA	AIN5/ AIN_C0_P/ AIN_C1_P	I2C1 Serial Data; 32.768kHz Calibration Output; Timer2 Port Map C Output 32 Bits or Lower 16 Bits; Comparator Positive Input
34	P0.14	P0.14	SPI1A_MISO	UART2B_RX	TMR3C_IA	AIN6/ AIN_C0_P/ AIN_C1_P	SPI1 Master In Slave Out; UART2 Port Map B Rx; Timer3 Port Map C Input 32 Bits or Lower 16 Bits; Comparator Positive Input
35	P0.15	P0.15	SPI1A_MOSI	UART2B_TX	TMR3C_OA	AIN7/ AIN_C0_P/ AIN_C1_P	SPI1 Master Out Slave In; UART2 Port Map B Tx; Timer3 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 7/Comparator Positive Input
36	P0.16	P0.16	SPI1A_SCK	UART2B_CTS	TMR0C_IA	AIN8	SPI1 Serial Clock; UART2 Port Map B CTS; Timer0 Port Map C Input 32 Bits or Lower 16 Bits; ADC Input 8
41	P0.17	P0.17	SPI1A_SS0	UART2B_RTS	TMR0C_OA	AIN9	SPI1 Slave Select 0; UART2 Port Map B RTS; Timer0 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 9
42	P0.18	P0.18	I2C2A_SCL	—	TMR1C_IA	AIN10	I2C2 Serial Clock; Timer1 Port Map C Input 32 Bits or Lower 16 Bits; ADC Input 10
43	P0.19	P0.19	I2C2A_SDA	—	TMR1C_OA	AIN11	I2C2 Serial Data; Timer1 Port Map C Output 32 Bits or Lower 16 Bits; ADC Input 11
1	P0.20	P0.20	CM4_RX	—	TMR2C_IA	—	CM4 Rx Event Input; Timer2 Port Map C Input 32 Bits or Lower 16 Bits

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
2	P0.21	P0.21	CM4_TX	—	TMR2C_OA	—	CM4 Tx Event Output; Timer2 Port Map C Output 32 Bits or Lower 16 Bits
3	P0.22	P0.22	LPTMR1A_IA	ADC_TRIG_B	TMR0C_IA	—	Low-Power Timer1 Port Map A Input; ADC Trigger Port Map B; Timer0 Port Map C Input 32 Bits or Lower 16 Bits
15	P0.23	P0.23	LPTMR1A_OA	—	SPI0C_SS3	QEI	Low-Power Timer1 Port Map A Output; SPI0 Slave Select 3; Quadrature Decoder Index Input
16	P0.24	P0.24	LPUART0A_CTS	UART0B_RX	I2S0A_SD0	QES	Low-Power UART0 CTS; UART0 Port Map B Rx; I2S0 Serial Data Output; Quadrature Decoder Capture Input
17	P0.25	P0.25	LPUART0A_RTS	UART0B_TX	I2S0A_LRCLK	QMATCH	Low-Power UART0 RTS; UART0 Port Map B Tx; I2S0 Left/Right Clock; Quadrature Decoder Match Output
18	P0.26	P0.26	LPUART0A_RX	UART0B_CTS	I2S0C_BCLK	QDIR	Low-Power UART0 Rx; UART0 Port Map B CTS; I2S0 Bit Clock; Quadrature Decoder Direction Output
23	P0.27	P0.27	LPUART0A_TX	UART0B_RTS	I2S0C_SDI	QERR	Low-Power UART0 Port Map A Tx; UART0 Port Map B Request to Send; I2S0 Port Map C Serial Data Input; Quadrature Decoder Error Output
24	P0.28	P0.28	UART1A_RX	EXT_CLK1	TMR3C_IA	—	UART1 Port Map A Receive; Timer3 Port Map C Input 32 Bits or Lower 16 Bits; External Clock Input
25	P0.29	P0.29	UART1A_TX	SPI1_SS0	TMR3C_OA	ADC_TRIG_D	UART1 Port Map A Transmit; SPI1 Port Map B Slave Select 0;Timer3 Port Map C Output 32 Bits or Lower 16 Bits; ADC Trigger Port Map D
26	P0.30	P0.30	UART1A_CTS	—	TMR3C_IA	—	UART1 Port Map A Clear to Send; Timer3 Port Map C Input 32 Bits or Lower 16 Bits
44	P0.31	P0.31	UART1A_RTS	—	TMR3C_OA	—	UART1 Port Map A Request to Send; Timer3 Port Map C Output 32 Bits or Lower 16 Bits
4	P1.0	P1.0	—	—	TMR1C_IA	—	Timer1 Port Map C Input 32 Bits or Lower 16 Bits
20	P1.1	P1.1	SPI2A_MISO	UART0B_RX	TMR3C_OA	—	SPI2 Port Map A Master In Slave Out; UART0 Port Map B Receive; Timer3 Port Map C Output 32 Bits or Lower 16 Bits

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PIN	NAME	FUNCTION MODE					FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4	
19	P1.2	P1.2	SPI2A_MOSI	UART0B_TX	TMR3C_IA	DIV_CLK_OUT	SPI2 Port Map A Master Out Slave In; UART0 Port Map B Transmit; Timer3 Port Map C Input 32 Bits or Lower 16 Bits; Divided_Clock_Output
22	P1.3	P1.3	SPI2A_SCK	UART0B_CTS	—	—	SPI2 Port Map A Serial Clock; UART0 Port Map B Clear to Send
21	P1.4	P1.4	SPI2A_SS0	UART0B_RTS	TMR0C_OA	ADC_TRIG_D	SPI2 Port Map A Slave Select 0; UART0 Port Map B Request to Send; Timer0 Port Map C Output 32 Bits or Lower 16 Bits; ADC Trigger Port Map D
37	P1.5	P1.5	UART2A_RX	—	—	—	UART2 Port Map A Receive
38	P1.6	P1.6	UART2A_TX	—	—	—	UART2 Port Map A Transmit
39	P1.7	P1.7	UART2A_CTS	—	—	—	UART2 Port Map A Clear to Send
40	P1.8	P1.8	UART2A_RTS	—	—	—	UART2 Port Map A Request to Send
5	P1.9	P1.9	—	—	TMR1C_OA	—	Timer1 Port Map C Output 32 Bits or Lower 16 Bits

Detailed Description

The MAX32672 is an ultra-low-power, cost-effective, highly integrated microcontroller designed for battery-powered devices and wireless sensors. It combines a flexible and versatile power management unit with the powerful Arm Cortex-M4 processor with FPU. The device enables designs with complex sensor processing without compromising battery life. It also offers legacy designs an easy and cost-optimal upgrade path from 8- or 16-bit microcontrollers. Error correction coding (single error correction, double error detection, or SEC-DED) for flash and SRAM provides extremely reliable code execution. The device integrates 1MB of dual-bank flash memory and 200KB (160KB with ECC enabled) of SRAM to accommodate application and sensor code. A 1Msps, 12-channel, 12-bit SAR ADC is integrated for the digitization of analog sensor signals or other analog measurements.

The device features five powerful and flexible power modes. It can operate from a single-supply battery or a dual-supply typically provided by a PMIC. The I^2C ports support standard, fast, fast-plus, and high-speed modes, operating up to 3400kbps. The SPI ports can run up to 50MHz in both master and slave mode. Four general-purpose 32-bit timers, two low-power 32-bit timers, two windowed watchdog timers, and a real-time clock (RTC) are also provided. An I^2S interface provides digital audio streaming to a codec.

Arm Cortex-M4 Processor with FPU Engine

The Arm Cortex-M4 with FPU processor combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction, multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

The 1MB internal flash memory with error correction provides nonvolatile storage of program and data memory. The flash is organized in two equal sizes, physically separate banks (dual bank) to allow execute-while-write operation and facilitate "live FW upgrades."

Internal SRAM

The internal 200KB SRAM provides low-power retention of application information in all power modes except STORAGE. The SRAM can be configured as 160KB with error correction coded (ECC) SEC-DED for enhanced system reliability. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and is configurable. This granularity allows the application to minimize its power consumption by only retaining the essential data.

Clocking Scheme

The internal primary oscillator (IPO) operates at a nominal frequency of 100MHz.

Optionally, the software can select one of five other oscillators depending upon power needs:

- 80kHz oscillator (INRO)
- 32.768kHz oscillator (external crystal required) (ERTC0)
- 7.3728MHz oscillator (IBRO)
- 16MHz–32MHz oscillator (external crystal required) (ERFO)
- External square-wave clocks up to 50MHz

This clock is the primary clock source for digital logic and peripherals.

An external 32.768kHz timebase is required when using the RTC. A separate external square-wave clock can be used as a source for LPTMR0/1 and LPUART0 in the Always-ON domain.

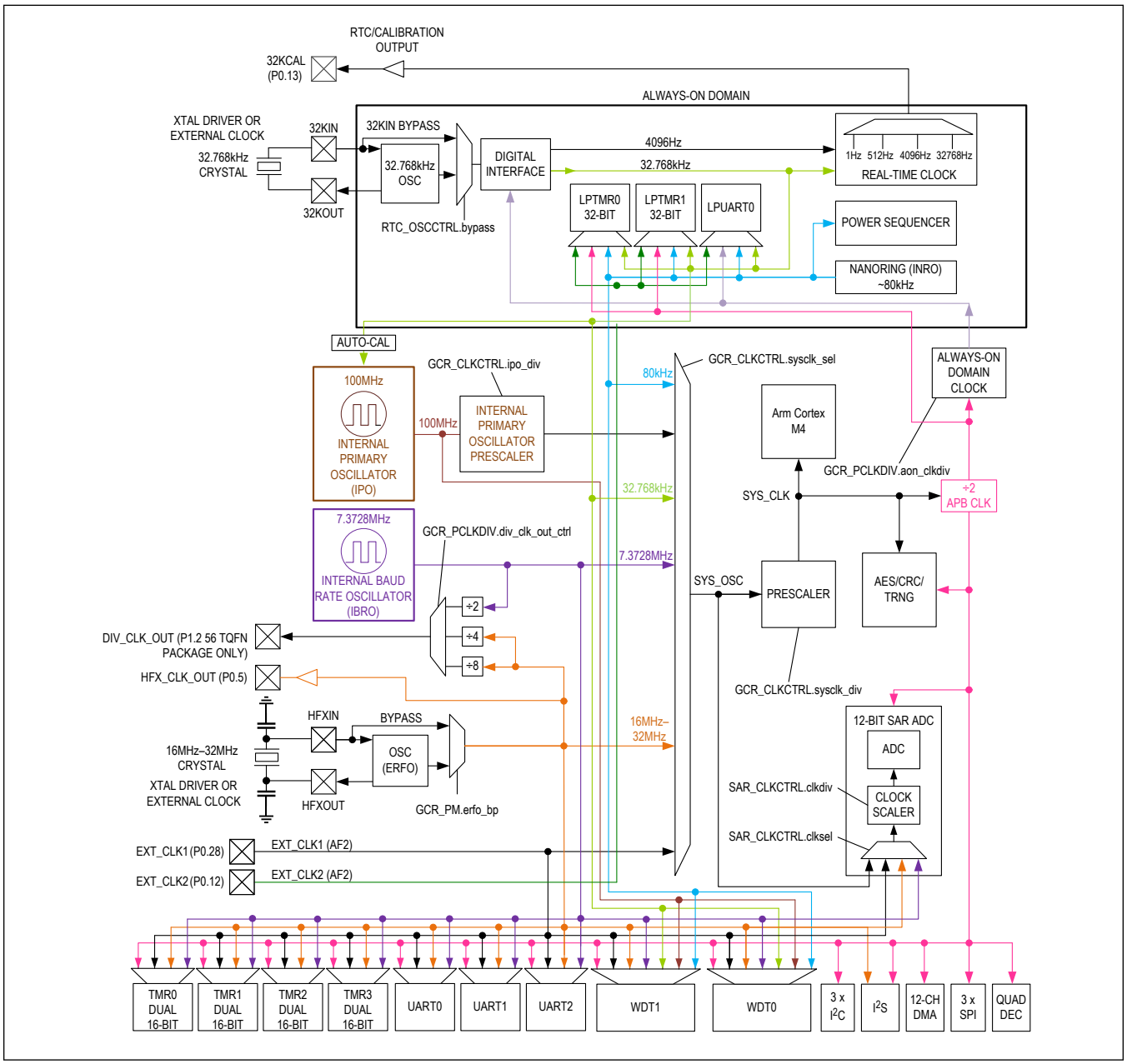

Figure 7. Clocking Scheme

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Software can individually enable pins for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a software-controlled I/O. Multiplexing between peripheral and GPIO functions is usually static but can also be done dynamically by software. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where

explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled by software and configured as a level- or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32672 provides up to 28 GPIOs for the 40-pin TQFN.

Standard DMA Controller

The standard direct memory access (DMA) controller provides a means to offload the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 12 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit

The power management unit (PMU) provides the optimal mix of high-performance and low-power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wakeup of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, the CPU executes software and all digital and analog peripherals are available on demand. Dynamic clocking disables local clocks in peripherals that are not in use. This mode corresponds to the Arm Cortex-M4 processor with FPU ACTIVE mode.

SLEEP Mode

This mode allows for lower power consumption operations than ACTIVE mode. The CPU is asleep, peripherals are on, and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause a transition to the ACTIVE mode. This mode corresponds to the Arm Cortex-M4 processor with FPU SLEEP mode.

DEEPSLEEP Mode

In this mode, CPU and critical peripheral configuration settings and all volatile memory are preserved.

The device status is as follows:

- CPU is powered down. System state and all SRAM is retained.

- The GPIO pins retain their state.
- The transition from DEEPSLEEP to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The system oscillators are all disabled to provide additional power savings over SLEEP mode.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

This mode corresponds to the Arm Cortex-M4 with FPU DEEPSLEEP mode.

BACKUP Mode

This mode places the CPU in a static, low-power state. The BACKUP mode supports the same wake-up sources as DEEPSLEEP mode.

The device status is as follows:

- CPU is powered down.
- SRAM retention as per Table 1.
- LPUART0 and LPTMR0/1 can be active and are optional wake-up sources.

Table 1. BACKUP Mode RAM Retention

RAM BLOCK	RAM SIZE	TYPE
SYSRAM0	20KB	16KB + 4KB ECC
SYSRAM1	20KB	16KB + 4KB ECC
SYSRAM2	80KB	64KB + 16KB ECC
SYSRAM3	80KB	64KB + 16KB ECC

STORAGE Mode

The device status is as follows:

- CPU is powered off.
- All peripherals are powered off.
- Wake-up from GPIO interrupt.
- The RTC can be enabled by software before entering STORAGE mode.
- No SRAM retention.

Real-Time Clock (RTC)

An RTC keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm programmed by software to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode but still awaken periodically to perform assigned tasks. Software can program a second independent 32-bit 1/4096 sub-second alarm between 244µs and 12 days. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

An RTC calibration feature allows the software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with a 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Windowed Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed WDT, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically

reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific time window.

The WDT supports multiple clock option:

- 100MHz oscillator
- 16MHz–32MHz (external crystal required)
- 7.3728MHz oscillator
- 80kHz oscillator
- 32.768kHz oscillator (external crystal required)
- External square-wave clocks up to 50MHz
- Pixel clock (PCLK)

The MAX32672 provides two instances of the windowed watchdog timer: WDT0 and WDT1.

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generate pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down auto-reload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0-TMR3 configurable as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32672 provides six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, LPTMR1). The LPTMR0 and LPTMR1 are capable of operation in the SLEEP, DEEPSLEEP, and BACKUP low-power modes.

The I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See Table 2 for individual timer features.

Table 2. Timer Configuration Options

INSTANCE	32-BIT ONLY	DUAL 16-BIT	MODE	CLOCK SOURCE						
				PCLK	7.3728MHz	16MHz–32MHz	80kHz	32.768kHz	EXT_CLK1	EXT_CLK2
TMR0	YES	YES	ACTIVE	YES	YES	YES	NO	NO	YES	NO
TMR1	YES	YES	ACTIVE	YES	YES	YES	NO	NO	YES	NO
TMR2	YES	YES	ACTIVE	YES	YES	YES	NO	NO	YES	NO
TMR3	YES	YES	ACTIVE	YES	YES	YES	NO	NO	YES	NO
LPTMR0	YES	NO	ACTIVE/ SLEEP/ DEEPSLEEP/ BACKUP	YES	NO	NO	YES	YES	NO	YES
LPTMR1	YES	NO	ACTIVE/ SLEEP/ DEEPSLEEP/ BACKUP	YES	NO	NO	YES	YES	NO	YES

Serial Peripherals

I2C Interface

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. These engines support standard-mode, fast-mode, fast-mode plus, and high-speed mode I2C speeds. It provides the following features:

- Master or slave mode operation
  - Supports up to four different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
  - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32672 provides three instances of the I2C peripheral (I2C0, I2C1, and I2C2).

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface between multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, and 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing relative to leading/trailing SCK edge

The MAX32672 provides two instances of this SPI peripheral (SPI0 and SPI1). See Table 3 for configuration options.

Table 3. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES	MAXIMUM FREQUENCY (MASTER MODE) (MHz)	MAXIMUM FREQUENCY (SLAVE MODE) (MHz)
SPI0	3 wire, 4 wire	4	50	50
SPI1	3 wire, 4 wire	1	50	50

I2S Interface

The I2S interface is a bidirectional, 4-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I2S Bus Specification, June 5, 1996. It provides the following features:

- Slave mode operation
- Support for four channels

- 8-, 16-, 24-, and 32-bit frames
- Receive and transmit DMA support
- Wakeup on FIFO status (full/empty/threshold)
- Pulse density modulation support for the receive channel
- Word select polarity control
- First-bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32672 provides one instance of the I^2S peripheral (I2S0).

UART

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request-to-send (RTS) and clear-to-send (CTS) flow control signaling. Each LPUART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32672 provides four instances of the UART peripheral (UART0, UART1, UART2, and LPUART0). LPUART0 is capable of operation in the SLEEP, DEEPSLEEP, and BACKUP low-power modes. See Table 4 for configuration options.

Table 4. UART Configuration Options

INSTANCE	MODE	CLOCK SOURCE						
		PCLK	7.3728MHz	16MHz–32MHz	80kHz	32.768kHz	EXT_CLK1	EXT_CLK2
UART0	ACTIVE	YES	YES	YES	NO	NO	YES	NO
UART1	ACTIVE	YES	YES	YES	NO	NO	YES	NO
UART2	ACTIVE	YES	YES	YES	NO	NO	YES	NO
LPUART0	ACTIVE/ SLEEP/ DEEPSLEEP/ BACKUP	ALWAYS-ON DOMAIN CLOCK	NO	NO	YES	YES	NO	YES

Quadrature Decoder

The quadrature decoder converts rotational information derived from optical or magnetic encoders to counts representing a shaft's angle and rotational velocity.

The following features are provided:

- x1, x2, and x4 mode selection
- 32-bit counter
- Index input
- Rotational direction and error outputs
- On-chip deglitch filters

Analog-to-Digital Converter (ADC)

The 12-bit SAR ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the 12 external analog input signals (AIN0–AIN11), the internal power supply inputs, or an internal temperature sensor.

The reference for the ADC can be:

- External V_{REF} input
- V_{DDA} analog supply

The ADC measures the following voltages:

- AIN[11:0] up to 3.3V
- V_{DD}
- V_{CORE}
- V_{DDA}
- Internal die temperature sensor input

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in a dedicated flash region to protect against tampering. Key generation and storage are transparent to the user.

True Random Number Generator (TRNG)

Random numbers are a vital part of a secure application, providing random numbers useable for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This helps thwart replay attacks or key search approaches. A high-entropy source must continuously update an effective TRNG.

A physically unpredictable entropy source continuously drives the provided TRNG. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Maxim for details of compliance with specific standards.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Root of Trust

The root of trust starts with trusted software and the microcontroller's complement of security features. Communications between a host and the device must be secure and authenticated, and program integrity must be verified each time before execution to ensure the device's trustworthiness. The device's root of trust is based on a Maxim Integrated master root verification key and a signed customer verification key (CVK). Customers submit their public CVK to Maxim Integrated, which is then signed, and this public key is sent back to the customer. This process is quick and required only once, before the software is released for the first time, and is unnecessary during the software development. A customer can then load their own key and download their signed binary executable code. A life-cycle scheme allows the device to be permanently disabled to deactivate a deployed application.

Secure Communications Protocol Bootloader (SCPBL)

Communication between a host system and the device uses a system of digitally signed packets. This guarantees the integrity and authenticity of all communication before executing configuration commands and the loading or verification of program memory. One or more serial interfaces are available for communication. This also enables the assembly and programming of the customer's final product by third-party assembly houses without the required cost and complexity of ensuring that the assembly house implements and maintains a secure production facility. It also allows for in-field software upgrades to deployed products, thus eliminating the costly need to return a product to the manufacturer for any software changes.

The serial interfaces available for SCPBL communication are shown in Table 5. Following any reset, the device will test the assigned stimulus pin and, if active, begin an SCPBL session. Unless otherwise specified, the SCPBL must first be configured through the default interface to activate any other interfaces and/or redefined stimulus pins other than the default assignment. Software can disable the bootloader interface before deployment to prevent any changes to program memory.

Secure Boot

Following every reset, the device performs a secure boot to confirm the root of trust has not been compromised. The secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted, ensuring the trustworthiness of the application software. Failure to verify the digital signature will transition the device to safe mode, which prevents execution of the customer code. During the development phase, the bootloader can be reactivated and a new, trusted program memory loaded.

Debug and Development Interface

The serial wire debug (SWD) interface is used for code loading and in-circuit emulator (ICE) debug activities. All devices in mass production have the debugging/development interface enabled.

Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The pin description table indicates which pins should be connected to bypass capacitors and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the pin description table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins which recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

Bootloader Activation

Following any reset, the SCPBL is activated while applying a logic-high to the default stimulus pin, as indicated in Table 5. The design must ensure that the bootloader communication port and default stimulus pin are available or the SCPBL cannot be activated.

Table 5. Bootloader Activation Summary

PART NUMBER	BOOTLOADER COMMUNICATION PORT		DEFAULT STIMULUS PIN
	RECEIVE	TRANSMIT	
All versions	UART0A_RX	UART0A_TX	P0.10 (Active Low)

Ordering Information

PART NUMBER	FLASH (KB)	SRAM (KB)	SECURE BOOT	SWD	GPIO	PIN-PACKAGE
MAX32672GTL+	1024 with ECC	160 with ECC	No	Unlocked	Up to 28	40 TQFN-EP 5mm x 5mm 0.4mm pitch
MAX32672GTL+T	1024 with ECC	160 with ECC	No	Unlocked	Up to 28	40 TQFN-EP 5mm x 5mm 0.4mm pitch
MAX32672GTLBL+	1024 with ECC	160 with ECC	Yes	Unlocked	Up to 28	40 TQFN-EP 5mm x 5mm 0.4mm pitch
MAX32672GTLBL+T	1024 with ECC	160 with ECC	Yes	Unlocked	Up to 28	40 TQFN-EP 5mm x 5mm 0.4mm pitch
MAX32672GTNBL+	1024 with ECC	160 with ECC	Yes	Unlocked	Up to 42	56 TQFN-EP 7mm x 7mm 0.4mm pitch
MAX32672GTNBL+T	1024 with ECC	160 with ECC	Yes	Unlocked	Up to 42	56 TQFN-EP 7mm x 7mm 0.4mm pitch

T = Tape and reel. Full reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Release for Market Intro	—
1	1/22	Updated the *General Description*, *Benefits and Features*, and *Simplified Block Diagram*. Added Continuous Package Power Dissipation and *Package Information* for the 56 TQFN-EP. Added *Pin Configurations* and *Pin Descriptions* for the 56 TQFN-EP. Updated the *Clocking Scheme*. Updated the *Secure Communications Protocol Bootloader (SCPBL)* section. Updated *Bootloader Activation* Table 5. Added the 56 TQFN part numbers to the *Ordering Information*.	1–2, 7, 47–52, 54, 61–62