



MAX3420E

USB Peripheral Controller with SPI Interface

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REVISION 0 ERRATA

The errata listed below describe situations where the MAX3420E components perform differently than expected or differently than described in the data sheet. Maxim Integrated Products, Inc. intends to address these errata in subsequent die revisions.

Note: The version of the MAX3420E can be determined electrically (by firmware) by reading the Die Revision register (R18); e.g., 0x01 is version 01, 0x02 is version 02. The die revision 4 may also be discovered by reading the top mark as described below. If no die revision digit is present, then the part is version 03 or earlier.

CHIP REVISION IDENTIFICATION

Top Mark:

MAX3420EECJ (32-pin TQFP package):

MAX3420E

ECJ

yww XXX4

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yww is the date code

where y = last digit of year

ww = work week (01 to 52)

4 denotes die revision 4

MAX3420EETG (24-pin TQFN package):

3420EE

TGyww < date code

XXXX4

yww is the date code

where y = last digit of year

ww = work week (01 to 52)

4 denotes die revision 4

ERRATA ITEMS	DIE REVISIONS AFFECTED	FIX STATUS
SS# pin is sensitive to undershoot	0x01, 0x02	Use work around. Fixed in rev 0x03.
HIGH I _{LSUS}	0x01, 0x02	Fixed in rev 0x03
Double buffering does not work properly on EP1-OUT	0x01, 0x02, 0x03	Will be fixed in rev 0x04
Contention on the MOSI pin when used as a bidirectional data pin (FDUPSPI = 0)	0x01, 0x02, 0x03	Use work around. Will be fixed in rev 0x04.

1. SS# PIN IS SENSITIVE TO UNDERSHOOT

Description:

The MAX3420E is put into an internal test mode when a) the GPIN-0 pin is at logic-high, and b) a negative voltage is placed on the SS# pin. The negative threshold voltage on SS# is set to a low negative threshold voltage, so that even a slight amount of undershoot on this pin can disrupt operation if the GPIN-0 pin is high, enabling the test mode.

Work Around:

There are two work arounds.

- (Preferred). If the design does not require four MAX3420E general-purpose inputs, ground GPIN0 and use GPIN[3:1] as inputs. This disables the test mode.
- Placing a small capacitor from the SS# pin to ground can eliminate the undershoot. Note that the undershoot will be magnified if the MAX3420E is connected to a breadboard using wires rather than short PC traces. This

can easily happen with the MAX3420E EVKIT-1 board, which has a 20-pin connector for wiring the MAX3420E into a user system. If wires are used with this board, the 33pF capacitor from SS# to ground may need to be increased in value if wires are used to connect the board to a target system.

Fix:

The negative threshold voltage on SS# to enter test mode will be increased.

Status:

Fixed in Die Revision 0x03.

2. HIGH I_{LSUS}

Description:

USB-specified suspend current cannot be guaranteed over all operating conditions. The MAX3420E draws excess current when in suspend mode; this impacts bus-powered designs (peripherals that draw power from V_{BUS}) from meeting USB suspend current requirements.

Work Around:

High I_{LSUS} does not impact self-powered designs. There is no work around for bus-powered designs. Bus-powered peripherals designed using the MAX3420E (Revision 0x02) will function normally but will not pass USB-compliance testing for suspend current.

Status:

Fixed in Die Revision 0x03.

3. DOUBLE BUFFERING DOES NOT WORK PROPERLY ON EP1-OUT

Description:

If both FIFO buffers of endpoint 1-OUT contain USB packets, and the SPI master clears the OUT1DAVIRQ flag while a third packet is transmitted by the host over the bus, the FIFO data is corrupted. This situation is most often encountered when bulk-out data transfers of > 64 bytes are attempted.

Work Around:

Some USB applications (e.g., HID) do not require an OUT endpoint and are unaffected by this problem. There is no work around for applications that use EP1-OUT.

Status:

Will be fixed in Die Revision 0x04.

4. CONTENTION ON THE MOSI PIN WHEN USED AS A BIDIRECTIONAL DATA PIN (FDUPSPI = 0)

Description:

When the MOSI pin operates in bidirectional data mode (FDUPSPI = 0), the MOSI pin driver begins driving on the eighth positive SCLK edge. This is the same clock edge that transfers the eighth bit of the command byte from the SPI master to the MAX3420E. Therefore, to avoid bus contention, the SPI master must drive MOSI with the eighth command byte bit and then immediately turn off its driver, all on the same SCLK positive edge. Most systems require some time to turn off the SPI master MOSI pin driver, so contention can result.

Work Around:

Any system that uses the full duplex mode (FDUPSPI = 1, separate MISO and MOSI pins) does not have this problem since the data pins are unidirectional. For systems that use MOSI as a bidirectional data pin, a series resistor between the MOSI pin and SPI MISO driver limits the current to a safe limit during the brief contention interval.

Fix:

The MOSI pin driver will turn its pin driver on one-half clock later, on the eighth falling edge of SCLK.

Status:

Will be fixed in Die Revision 0x04.