# EVALUATION KIT AVAILABLE High-Output-Current, Differential Line Driver

## **General Description**

The MAX4142 differential line driver combines highspeed performance with fully symmetrical differential inputs and outputs. With an internally set +2V/V closedloop gain, the MAX4142 is ideal for driving backterminated cables and transmission lines.

This device utilizes laser-trimmed thin-film resistors and common-mode cancellation circuitry to deliver an outstanding 67dB at 10MHz common-mode rejection (CMR). Using current-feedback techniques, the MAX4142 achieves a 250MHz -3dB (A<sub>V</sub> = +2V/V) bandwidth, a 70MHz 0.1dB bandwidth, and a 1400V/µs slew rate. Excellent differential gain/phase error and noise specifications make this amplifier an excellent choice for a wide variety of video and RF signal-processing applications.

The MAX4142 operates from  $\pm 5V$  power supplies and requires only 12.5mA of quiescent current. The output stage is capable of driving a 100 $\Omega$  load to  $\pm 6V$  (differentially) or to  $\pm 3V$  (single-ended). The MAX4142 is available in a space-saving 14-pin SO package. For a pin-compatible, higher speed differential line driver, see the MAX4147 data sheet.

#### Applications

Video Twisted-Pair Driver Differential Pulse Amplifier High-Speed Instrumentation Amplifier Low-Noise Differential Receivers

Differential ADC Driver

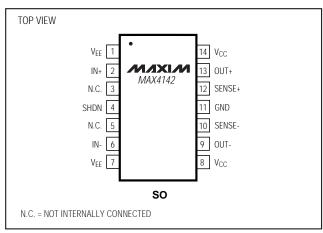
#### \_Features

- 250MHz -3dB Bandwidth (Av = +2V/V)
- 1400V/µs Slew Rate
- + 67dB at 10MHz CMR
- 0.01%/0.01° Differential Gain/Phase
- + ±6V Differentially into 100Ω Output Drive
- 1mA Shutdown Capability
- + 12.5mA Quiescent Supply Current
- ♦ Available in 14-Pin Narrow SO Package

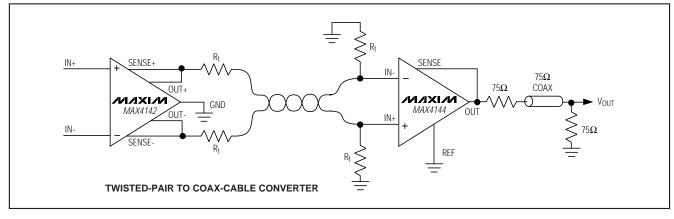
#### \_Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4142ESD	-40°C to +85°C	14 SO

## Pin Configuration



## **Typical Application Circuit**



#### M/X/W

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## **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V <sub>CC</sub> to V <sub>EE</sub> )+1	2V
Voltage on Any Pin to Ground(VEE - 0.3V) to (VCC + 0.3	3V)
Input Current (IN_)±10r	nΑ
Short-Circuit Duration (VOUT to GND)10s	ec
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
Plastic SO (derate 8.3mW/°C above +70°C)667m	۱W

Operating Temperature Range	40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +5V, V<sub>EE</sub> = -5V, SHDN = 0, R<sub>L</sub> = ∞ T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values specified at T<sub>A</sub> = +25°C.)

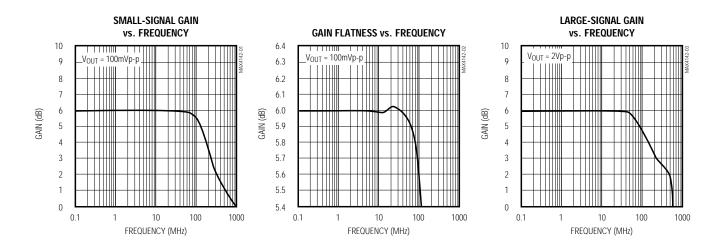
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage		Guaranteed by PSR test	±4.5		±5.5	V
Input Offset Voltage	Vos	$V_{IN} = 0$		0.4	8	mV
Input Offset Voltage Drift	TCvos	$V_{IN} = 0$		3		µV/°C
Input Bias Current	lΒ	VIN = 0		10	25	μΑ
Input Offset Current	los	V <sub>IN</sub> = 0		0.2	2.5	μA
Input Capacitance	CIN			1		pF
Differential Input Resistance	RIN			1		MΩ
Differential Input Voltage Range		Guaranteed by output voltage swing test	-3.0		3.0	V
Common-Mode Input Voltage Range	Vcm	Guaranteed by CMR test	-1.7		1.7	V
Gain	Av	$-1V \le V_{OUT} \le 1V$ , $R_L = 53\Omega$		2		V/V
Gain Error		$-1V \le V_{OUT} \le 1V$ , $R_L = 53\Omega$		0.3	2	%
Gain Drift		$R_L = 53\Omega$		20		ppm/°C
Common-Mode Rejection	CMR	$V_{CM} = \pm 1.7 V$	55	80		dB
Power-Supply Rejection	PSR	$V_{S} = \pm 4.5 V \text{ to } \pm 5.5 V$	65	95		dB
Quiescent Supply Current	ICC, IEE	$V_{IN} = 0$		12.5	18	mA
Shutdown Supply Current	ICC, SHDN	$V_{SHDN} \ge 2V, V_{IN} = 0$		1.0	2.0	mA
Output Voltage Swing	Vout	Single-ended, $R_L = \infty$	3.0	3.4		- V
		Differential, R <sub>L</sub> = ∞	6.0	6.8		
		Single-ended, $R_L = 26.5\Omega$	2.0	2.4		
		Differential, $R_L = 53\Omega$	4.0	4.8		
Output Current Drive	lout	$R_L = 20\Omega$	120	75		mA
Output Resistance	Rout			0.1		Ω
SHDN Logic-High Threshold	Vih				2.0	V
SHDN Logic-Low Threshold	VIL		0.8			V
Enable Time from Shutdown	ton			500		ns
Disable Time to Shutdown	toff			3.5		μs
SHDN Input Current	ISHDN	V <sub>SHDN</sub> = 0		66	150	μA

PARAMETER	SYMBOL	CONDITION	6	MIN	TYP	MAX	UNITS	
-3dB Bandwidth	BW(-3dB)	Vout ≤ 0.1V <sub>RMS</sub>			250		MHz	
Full-Power Bandwidth	FPBW	V <sub>OUT</sub> = 2Vp-p			180		MHz	
0.1dB Bandwidth	BW(0.1dB)	V <sub>OUT</sub> ≤ 0.1V <sub>RMS</sub> 70			MHz			
Common-Mode Rejection	CMR	f = 10MHz, V <sub>CM</sub> = ±2V 67			dB			
Slew Rate	SR	Differential, $-2V \le V_{OUT} \le +2V$			1400		V/µs	
Settling Time	ts	$-1V \le V_{OUT} \le +1V$	to 0.1%		25		ns	
			to 0.01%		45			
Differential Gain	DG	f = 3.58MHz			0.01		%	
Differential Phase	DP	f = 3.58MHz			0.01		degrees	
Input Valtage Naise		f = 10kHz			8		nV/√Hz	
Input Voltage Noise	en	f = 1MHz to 100MHz			80		μV <sub>RMS</sub>	
	in	f = 10kHz			2		pA√Hz	
Input Current Noise		f = 1MHz to 100MHz			20		nA <sub>RMS</sub>	
Spurious-Free Dynamic	SFDR	$f_{C} = 500 \text{kHz}, V_{OUT} = 1 \text{Vp-p}, R_{S} = 50 \Omega$ , Figure1			-84		dBc	
Range		$f_{C}$ = 10MHz, $V_{OUT}$ = 1Vp-p, $R_{S}$ = 50 $\Omega$ , Figure1			-76			

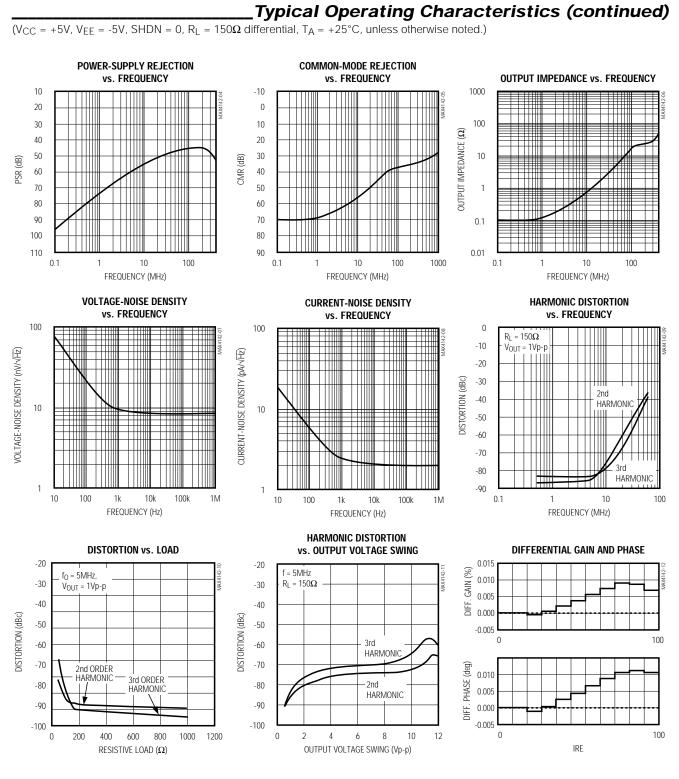
#### **AC ELECTRICAL CHARACTERISTICS**

## **Typical Operating Characteristics**

 $(V_{CC} = +5V, V_{EE} = -5V, SHDN = 0, R_L = 150\Omega$  differential,  $T_A = +25^{\circ}C$ , unless otherwise noted.)





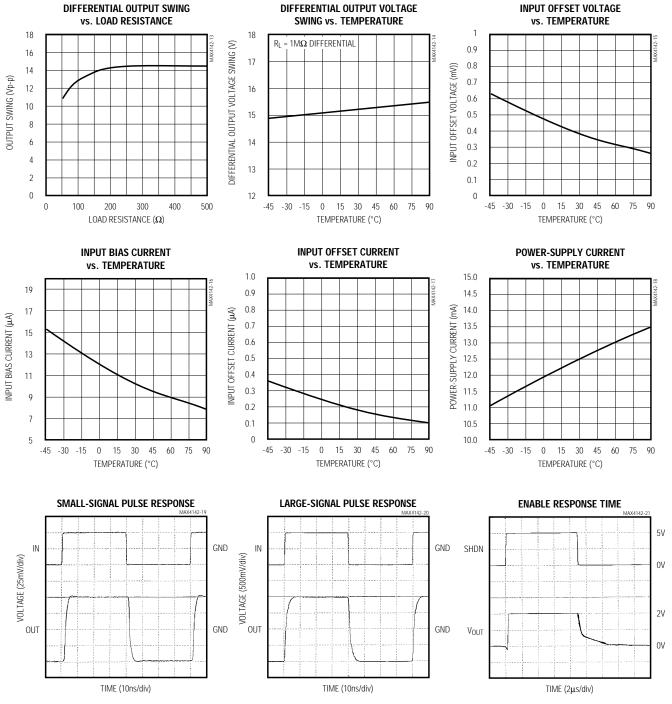


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MAX4142



 $(V_{CC} = +5V, V_{EE} = -5V, SHDN = 0, R_L = 150\Omega$  differential,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



MAX4142

Pin	Desci	ription	

PIN	NAME	FUNCTION
1, 7	V <sub>EE</sub>	Negative Power Supply. Connect $V_{EE}$ to -5V.
2	IN+	Noninverting Input
3, 5	N.C.	No Connect. Not internally connected.
4	SHDN	Logic Input for Shutdown Circuitry. A logic low enables the amplifier. A logic high disables the amplifier.
6	IN-	Inverting Input
8, 14	Vcc	Positive Power Supply. Connect $V_{CC}$ to +5V.
9	OUT-	Inverting Output
10	SENSE-	Inverting Output Sense. Connect to OUT- close to the pin for normal operation.
11	GND	Ground
12	SENSE+	Noninverting Output Sense. Connect to OUT+ close to the pin for normal operation.
13	OUT+	Noninverting Output

#### /VI/IXI/VI IN MAX4142 OUT+ A1 SENSE RG GND $\frac{R_F}{R_C}$ VIN VIN V<sub>OUT</sub> = A3 RG SENSE RF OUT A2 IN Figure 1. MAX4142 Functional Diagram

### **Detailed Description**

The MAX4142 differential line driver features 250MHz bandwidth and 67dB common-mode rejection (CMR) at 10MHz. This part achieves a 1400V/µs slew rate, and power dissipation is only 125mW. The MAX4142 has an internally set +2V/V closed-loop gain, making it ideal as a back-terminated line driver. The output stage can drive  $\pm$ 6V into a 100 $\Omega$  load.

The MAX4142 utilizes a three-amplifier topology to provide differential inputs/outputs and common-mode feedback (Figure 1), making it ideal for applications with high common-mode noise, such as for driving T1 or xDSL transmissions over a twisted-pair cable. The MAX4142's differential noninverting structure uses two noninverting amplifiers (A1 and A2) to provide a single device with differential inputs and outputs. The use of two amplifiers effectively doubles the output voltage swing and bandwidth, and improves slew rate when compared to the single op-amp differential amplifier. Excellent gain and phase, along with low noise, also make the MAX4142 suitable for video applications and RF-signal processing.

For a complete differential transmission link, use the MAX4142 line driver with the MAX4144/MAX4146 line receivers, as shown in the *Typical Application Circuit*.

## **Applications Information**

#### **Balanced Transmission Lines**

Differential (balanced) transmission lines use two conductors to transmit high-speed signals over low-cost cable or twisted-pair wire with minimal signal degradation. The transmit side of the balanced transmission line is driven by an amplifier with differential outputs, while the signal is received by an amplifier with differential inputs. In an ideal balanced system, each conductor has the same impedance from input to output and from the conductor to the system ground. Since the impedance from each conductor to ground is equivalent, any noise or other interference coupled into the transmission line will be equal in magnitude in each conductor, appearing as a common-mode signal to the amplifier at the receiving end of the transmission line. Since the receiving amplifier subtracts the signals on each side of the transmission line to obtain the desired information, common-mode signals are effectively canceled out by the receiving amplifier.

#### Common-Mode Feedback

In nonideal balanced systems, impedance mismatches between the conductors of a transmission line can degrade system common-mode rejection (CMR) by converting a portion of any common-mode signal to a



differential signal that is amplified by the receiver. The unique topology of the MAX4142 (Figure 1) utilizes two amplifiers (A1 and A2) to provide differential inputs and outputs, and a third amplifier (A3) to provide commonmode feedback. The common-mode feedback amplifier senses common-mode voltage at the MAX4142 output and forces this voltage to zero, effectively removing common-mode voltages from the transmission line. This technique improves CMR for systems with imperfectly balanced transmission-line impedances.

#### Grounding, Bypassing, and PC Board Layout

Observe the following guidelines when designing your PC board:

- High-frequency design techniques must be followed when designing the PC board for the MAX4142.
- The printed circuit board should have at least two layers: the signal layer and the ground plane.
- Do not use wire-wrap boards; they are too inductive.
- Do not use IC sockets; they increase parasitic capacitance and inductance.
- Use surface-mount power-supply bypass capacitors instead of through-hole capacitors. Their shorter lead lengths reduce parasitic inductance, leading to superior high-frequency performance.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

#### Input Stage Circuitry

The MAX4142 includes internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of five back-to-back Schottky protection diodes between IN+ and R<sub>G</sub>, and IN- and R<sub>G</sub> (Figure 2). The diodes limit the differential voltage applied to the amplifiers' internal circuitry to no more than 10V<sub>F</sub>, where V<sub>F</sub> is the diode's forward voltage drop (about 0.4V at +25°C).

For a large differential input voltage (exceeding 4V), the MAX4142 input bias current (at IN+ and IN-) increases according to the following equation:

Input current = [( $V_{IN+} - V_{IN-}$ ) - 10V<sub>F</sub>] / 1.4k $\Omega$ 

A differential input voltage as high as 10V will cause only 2.1mA to flow—much less than the 10mA absolute maximum rating.

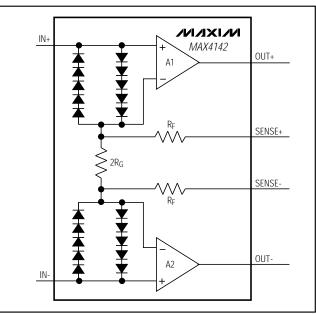


Figure 2. MAX4142 Input Protection Circuit

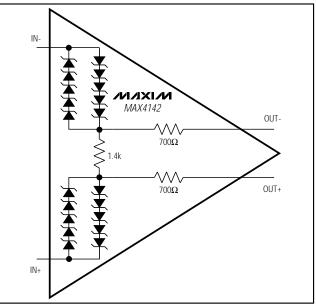


Figure 3. MAX4142 Shutdown Equivalent Circuit

#### Shutdown Mode

The MAX4142 can be put into low-power shutdown mode by driving SHDN high. The amplifier output is high impedance in this mode; thus the impedance at OUT is that of the feedback resistors (2.8k $\Omega$ ) (Figure 3).

MAX4142

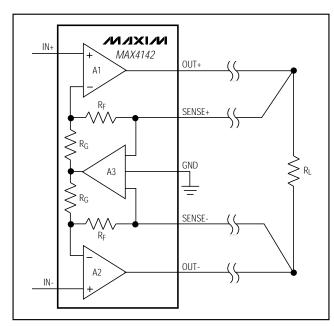


Figure 4. Connection of SENSE+ and SENSE- to a Remote Load

#### Using SENSE+ and SENSE-

The MAX4142 has two output voltage-sense pins, SENSE+ and SENSE-. These pins are normally connected to the MAX4142'S OUT+ and OUT- pins. In some long-line applications, it may be desirable to connect SENSE+ to OUT+ and SENSE- to OUT- at the load, instead of the typical connection at the part (Figure 4). This compensates for the long line's resistance, which otherwise leads to an IR voltage error.

When using this technique, keep the sense lines' impedance low to minimize gain errors. Also, keep capacitance low to maximize frequency response. The gain of the MAX4142 is approximated by the following equation:

$$A_{V} = 1 + \left[\frac{R_{F} + (\Delta R_{SENSE+}) + (\Delta R_{SENSE-})}{R_{G}}\right]$$

where  $\Delta RSENSE_{+}$  and  $\Delta RSENSE_{-}$  are the SENSE+ and SENSE- trace impedances, respectively. For the MAX4142, RF is 700 $\Omega$  and RG is 700 $\Omega$ .

Additionally, mismatches in the SENSE+ and SENSEtraces lead to common-mode gain errors. However, these errors are effectively eliminated by the MAX4142's common-mode feedback (see the *Common-Mode Feedback* section).

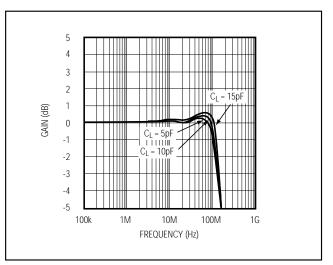


Figure 5. MAX4142 Small-Signal Response with Capacitive Load

#### **Driving Capacitive Loads**

The MAX4142 provides maximum AC performance when driving no output load capacitance. This is the case when driving a correctly terminated transmission line (i.e., a back-terminated cable).

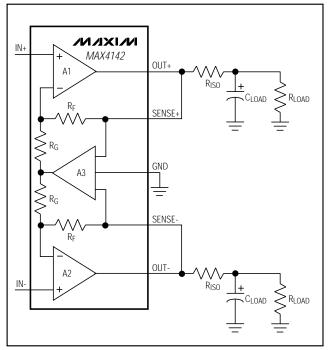
In most amplifier circuits, driving large-load capacitance increases the chance of oscillations. The amplifier's output impedance and the load capacitor combine to add a pole and excess phase to the loop response. If the pole's frequency is low enough and phase margin is degraded sufficiently, oscillations may occur. A second concern when driving capacitive loads results from the amplifier's output impedance, which looks inductive at high frequencies. The inductance forms an L-C resonant circuit with the capacitive load. This causes peaking in the frequency response and degrades the amplifier's phase margin.

The MAX4142 drives capacitive loads up to 25pF without oscillation. However, some peaking may occur in the frequency domain (Figure 5).

To drive larger-capacitance loads or to reduce ringing, add isolation resistors between the amplifier's outputs and the load (Figure 6).

The value of R<sub>ISO</sub> depends on the capacitive load (Figure 7). With higher capacitive values, bandwidth is dominated by the RC network formed by R<sub>ISO</sub> and C<sub>L</sub>; the bandwidth of the amplifier itself is much higher. Also note that the isolation resistor forms a divider that decreases the voltage delivered to the load.

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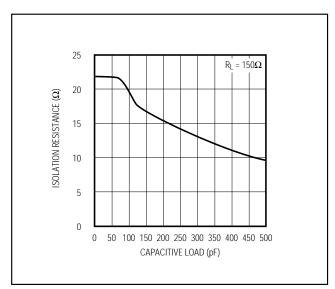


Figure 7. Isolation Resistance vs. Capacitive Load

Figure 6. Addition of RISO to Amplifier Output

Chip Information

TRANSISTOR COUNT: 243 SUBSTRATE CONNECTED TO V<sub>EE</sub> **MAX4142** 

Package Information ł ΕН 1 Ħ F Ħ Π 0°-8° B INCHES MILLIMETERS INCHES MILLIMETERS MIN MAX N MS012 MIN MAX MIN MAX MIN MAX 
 A
 0.053
 0.069
 1.35
 1.75

 A1
 0.004
 0.010
 0.10
 0.25

 B
 0.014
 0.019
 0.35
 0.49

 D
 0.189
 0.197
 4.80
 5.00
 8

 D
 0.337
 0.344
 8.55
 8.75
 14

 D
 0.386
 0.394
 9.80
 10.00
 16
А В С C 0.007 0.010 0.19 0.25 0.050 1.27 e NETES: NDTES: 1. D&E DD NDT INCLUDE MDLD FLASH 2. MDLD FLASH OR PROTRUSIONS NDT TO EXCEED .15mm (.006') 3. LEADS TO BE COPLANAR WITHIN .102mm (.004') 4. CONTROLLING DIMENSION: MILLIMETER 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE 6. N = NUMBER OF PINS E 0.150 0.157 3.80 4.00 H 0.228 0.244 5.80 6.20 h 0.010 0.020 0.25 0.50 L 0.016 0.050 0.40 1.27 //////////// PACKAGE FAMILY DUTLINE: SDIC .150" | 1 21-0041 A

**MAX4142** 

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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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