MAX4936A/MAX4937A Octal High-Voltage Transmit/Receive Switches

General Description

The MAX4936A/MAX4937A are octal, high-voltage, transmit/receive (T/R) switches. The T/R switches are based on a diode bridge topology, and the amount of current in the diode bridges can be programmed by three digital inputs (S0, S1, and S2). Two control inputs (EN1 and EN2) allow enabling/disabling channels 1–4 and channels 5–8, respectively. The MAX4936A includes the T/R switch and grass-clipping diodes, performing both transmit and receive operations. The MAX4937A includes just the T/R switch and performs the receive operation only.

These devices feature low on-impedance in the entire ultrasound frequency range with extremely low power dissipation of 15mW (typ) per channel.

The receive path for both devices is low impedance during low-voltage receive and high impedance during high-voltage transmit, providing protection to the receive circuitry. The low-voltage receive path is high bandwidth, low noise, low distortion, and low jitter.

The MAX4936A SWC_ pins can be driven with high-voltage signals using the anti-parallel diodes as grass clippers while connecting the SWB_ pins to the low-noise amplifier (LNA). Connecting SWC_ to GND allows the internal anti-parallel diodes to be used as clamps. Grass-clipping diodes can then be connected to SWB_ and the LNA to SWA_; see the *Applications Information* section.

Both devices are available in a small, 42-pin, 3.5mm x 9mm TQFN package, and are specified over the commercial 0°C to +70°C temperature range.

Applications

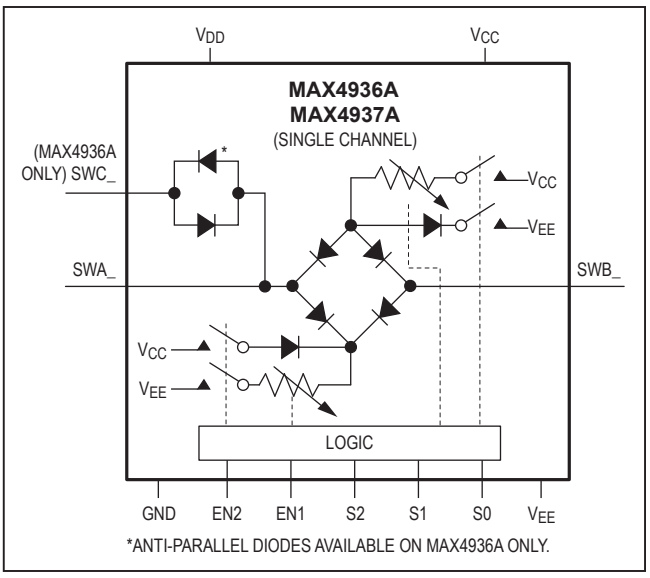
- Medical/Industrial Imaging
- Ultrasound
- High-Voltage Transmit and Low-Voltage Isolation

***Ordering Information/Selector Guide* appears at end of data sheet.**

Benefits and Features

- Save Space—Optimized for High-Channel-Count Systems
  - High Density (Eight Transmit/Receive Switches per Package)
  - Two Banks of Four Channels with Independent Enable Control (EN1, EN2)
  - Low-Capacitance Anti-Parallel Diodes to Be Used as Grass-Clipping or Clamping Diodes (MAX4936A Only)
  - Small, 42-Pin, 3.5mm x 9mm, TQFN Package
- Save Power
  - Low 6Ω (typ) On-Impedance with 1.5mA Bias Current Only
  - Adjustable Bias Resistors Allow Operation with Different Voltage Supplies
- High Performance—Designed to Enhance Image Quality
  - Low Noise at Low Power Consumption (< 0.5nV/√Hz (typ) with 1.5mA Bias Current)
  - Wide -3dB Bandwidth 100MHz (typ)
- Low-Voltage Receive Path with High-Voltage Protection

Functional Diagram



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Absolute Maximum Ratings

(All voltages referenced to GND unless otherwise noted.)
V_{DD} Positive Supply Voltage.....-0.3V to +6V
V_{CC} Positive Supply Voltage.....-0.3V to +6V
V_{EE} Negative Supply Voltage .....-6V to +0.3V
S0, S1, S2, EN1, EN2 Input Voltage.....-0.3V to +6V
SWC_ Input Voltage.....-120V to +120V
SWA_ Input/Output Voltage .....-120V to +120V
SWB_ Input/Output Voltage .....-120V to +120V
Voltage Difference Between SWC_ and SWA_ .....±1V
Voltage Difference Across Any or All SWC_ .....±230V
Voltage Difference Across Any or All SWA_.....±230V
Voltage Difference Across Any or All SWB_.....±230V
Continuous Current (SWC_ to SWA_) .....±250mA
Continuous Current (any other terminal).....±100mA
Peak Current (SWC_ to SWA_)
(pulsed at 1ms, 0.1% duty cycle) .....±2.5A
Continuous Power Dissipation (T_A = +70°C)
TQFN (single-layer board)
(derate 25mW/°C above +70°C) 2000mW
TQFN (multilayer board)
(derate 34.5mW/°C above +70°C) 2758mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.5V to +5.5V, V_{EE} = -2.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS						
SWA_, SWB_, SWC_ Input Voltage Range	$V_{IRSW\_}$	(SWC_ input voltage range for MAX4936A only)	-115		+115	V
Voltage Difference Across Any or All |SWA_, SWB_, SWC_|	ΔV_{DIFF}	(SWC_ voltage difference for MAX4936A only)			220	V
SWA_ Output Voltage Range	$V_{SWA\_}$	$V_{SWC\_} \geq \lvert \pm 2V \rvert$, $I_{SWC\_}$ = ±100mA (MAX4936A only)	$V_{SWC\_}$ - 1	$V_{SWC\_}$ ±0.85	$V_{SWC\_}$ + 1	V
SWA_ Output Clamp Voltage	$V_{CLMPSWA\_}$	V_{CC} = +5V, V_{EE} = -5V, $\lvert V_{SWB\_} \rvert \geq \pm 2V$, $V_{SWC\_}$ = 0V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA (MAX4936A only) (Note 3)	-1	±0.75	+1	V
SWC_ to SWA_ Continuous Current	I_{CN}	$V_{SWA\_}$ = 0V, (MAX4936A only)	-200		+200	mA
SWC_ to SWA_ Voltage Drop	V_{CN}	$V_{SWA\_}$ = 0V, I = ±2A (MAX4936A only)		±2		V

Electrical Characteristics (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.5V to +5.5V, V_{EE} = -2.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Diode Bridge Voltage Offset	V_{OFF}	V_{CC} = +5V, V_{EE} = -5V, SWA_ = unconnected, SWB_ = unconnected, I_{CH} = 1.5mA (Note 3)	-100		+100	mV
SWC_ Off-Leakage Current	$I_{LSWC\_}$	$\lvert V_{SWC\_} - V_{SWA\_} \rvert \le \pm 0.3V$, $V_{SWA\_}$ = 0V, (MAX4936A only)	-3		+3	µA
SWA_ Off-Leakage Current	$I_{LSWA\_}$	$\lvert V_{SWC\_} - V_{SWA\_} \rvert \le \pm 0.3V$, $V_{SWC\_}$ = 0V, (MAX4936A only)	-3		+3	µA
		SWC_ = unconnected (MAX4936A only)	-1		+1	
SWB_ Off-Leakage Current	$I_{LSWB\_}$		-1		+1	µA
DYNAMIC CHARACTERISTICS						
Diode Bridge Turn-On Time	t_{ON}	V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, $V_{SWA\_}$ = ±0.4V, Figure 1			200	ns
Diode Bridge Turn-Off Time	t_{OFF}	V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, $V_{SWA\_}$ = ±0.4V, Figure 1			5	µs
Reverse Recovery Time	t_{RR}	I_{FWD} = I_{RVR} = 1.5mA		450		ns
Bias Current Settling Time after Programming Change [S0, S1, S2]	t_{SET}				3	µs
Small-Signal SWA_ to SWB_ On-Impedance	$R_{ISWA\_}$	V_{CC} = +5V, V_{EE} = -5V, $V_{SWB\_}$ = 0V, I_{CH} = 1.44mA, f = 5MHz (Note 3)		6		Ω
-3dB Bandwidth	BW	SWA_ to SWB_, switch on, $\lvert V_{SWA\_} \rvert \le \pm 0.4V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, I_{CH} = 1.5mA (Note 3)		100		MHz
Off-Isolation	V_{ISO}	SWC_ to SWA_, $\lvert V_{SWC\_} - V_{SWA\_} \rvert \le \pm 0.4V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 100pF, f = 1MHz, (MAX4936A only)		-45		dB
		SWA_ to SWB_, switch off, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, f = 1MHz		-65		

Electrical Characteristics (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.5V to +5.5V, V_{EE} = -2.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk	V_{CT}	Between any two SWC_ to SWA_ channels, $\|V_{SWC\_}\| \geq \pm 2V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 100pF, f = 5MHz, (MAX4936A only)			-65		dB
		Between any two SWA_ to SWB_ channels, switch on, $\|V_{SWA\_}\| \geq \pm 0.4V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 5MHz (Note 3)			-80		
2nd Harmonic Distortion	HD2	SWC_ to SWA_, $\|V_{SWA\_}\| \geq \pm 2V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 100pF, f = 5MHz, (MAX4936A)			-70		dBc
		SWA_ to SWB_, switch on, $\|V_{SWA\_}\| < \pm 0.4V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 5MHz (Note 3)			-81		
Two-Tone Intermodulation Distortion	IMD3	SWA_ to SWB_, switch on, $\|V_{SWA\_}\| < \pm 0.4V$, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, I_{CH} = 1.5mA, f1 = 5MHz, f2 = 5.01MHz (Notes 3 and 4)			-57		dBc
SWC_ Off-Capacitance	$C_{SWC\_(OFF)}$	$\|V_{SWC\_} - V_{SWA\_}\| < \pm 50mV$ (MAX4936A only)			14		pF
SWA_ Off-Capacitance	$C_{SWA\_(OFF)}$	$V_{SWC\_}$ = 0V (MAX4936A only)			18		pF
		(MAX4937A only)			11		
SWB_ On-Capacitance	$C_{SWB\_(ON)}$	$\|V_{SWB\_}\| < \pm 0.4V$	(MAX4936A only)		20		pF
			(MAX4937A only)		13		
SWB_ Off-Capacitance	$C_{SWB\_(OFF)}$	$\|V_{SWB\_}\| < \pm 0.4V$			4.5		pF
DIGITAL I/Os (S2, S1, S0, EN1, EN2)							
Input High Voltage	V_{IH}	V_{DD} = +2.25V to +5.5V		V_{DD} - 0.5			V
		V_{DD} = +1.62V to +1.98V		1.4			
Input Low Voltage	V_{IL}	V_{DD} = +2.25V to +5.5V				0.6	V
		V_{DD} = +1.62V to +1.98V				0.4	
Input Hysteresis	V_{IL}	V_{DD} = +3V			50		mV
		V_{DD} = +1.8V			90		
Input Leakage Current	I_{IL}	S_, EN_ = GND or V_{DD}		-1		+1	µA
Input Capacitance	C_{IN}				5		pF

Electrical Characteristics (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.5V to +5.5V, V_{EE} = -2.5V to -5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (V_{DD}, V_{CC}, V_{EE})						
Positive Logic Supply Voltage	V_{DD}		+1.62		+5.5	V
Positive Analog Supply Voltage	V_{CC}		+2.5		+5.5	V
Negative Analog Supply Voltage	V_{EE}		-5.5		-2.5	V
Positive Logic Supply Current	I_{DD}	S_, EN_ = GND or V_{DD}			+1	µA
Positive Analog Supply Current	I_{CC}	Per channel, switch on, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA (Note 3)	+1.15	+1.5	+2	mA
Positive Analog Shutdown Supply Current	I_{CC_SHDN}	EN_ = GND			+1	µA
Negative Analog Supply Current	I_{EE}	Per channel, switch on, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA (Note 3)	-2	-1.5	-1.15	mA
Negative Analog Shutdown Supply Current	I_{EE_SHDN}	EN_ = GND	-1			µA
On Power-Supply Rejection Ratio	$PSRR_{ON}$	V_{CC} or V_{EE} to SWB_, switch on, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 1MHz (Note 3)		-36		dB
Off Power-Supply Rejection Ratio	$PSRR_{OFF}$	V_{CC} or V_{EE} to SWB_, switch off, V_{CC} = +5V, V_{EE} = -5V, R_L = 50Ω, C_L = 30pF, f = 1MHz		-65		dB

Note 2: All specifications are 100% production tested at T_A = +70°C, unless otherwise noted. Specifications at 0°C are guaranteed by design.

Note 3: I_{CH} equals the bias current through one channel.

Note 4: See the *Ultrasound-Specific IMD3 Specification* in the *Applications Information* section.

Timing Diagram

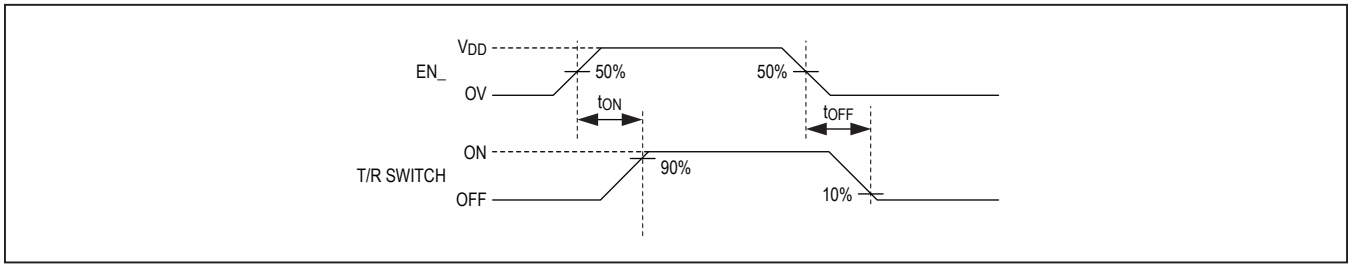
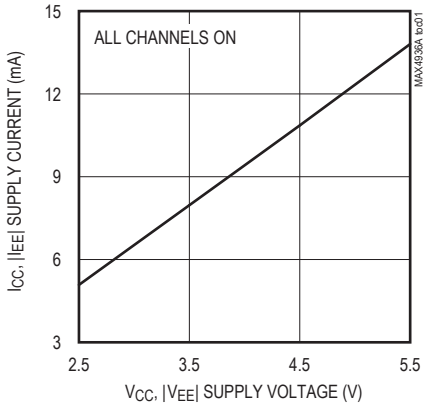


Figure 1. Turn-On/Turn-Off Time

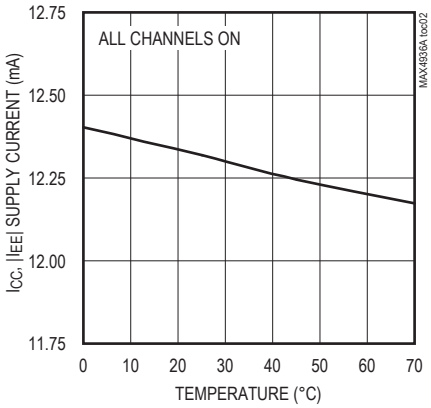
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, I_{CH} = 1.5mA, $R_{SWA\_}$ = 50Ω, $R_{SWB\_}$ = 50Ω, f = 5MHz, T_A = +25°C, unless otherwise noted.)

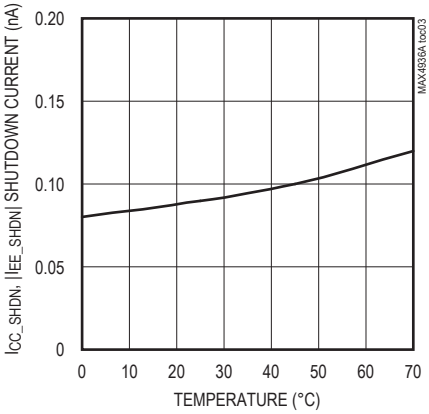
ICC, |IEE| SUPPLY CURRENT vs. VCC, |VEE| SUPPLY VOLTAGE



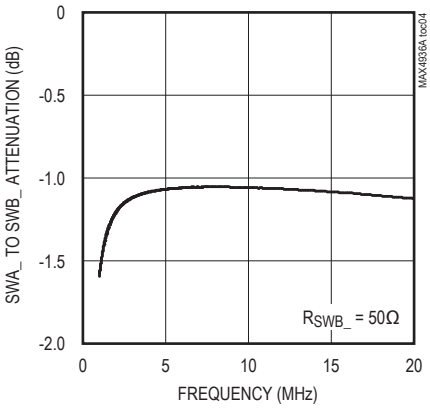
ICC, |IEE| SUPPLY CURRENT vs. TEMPERATURE



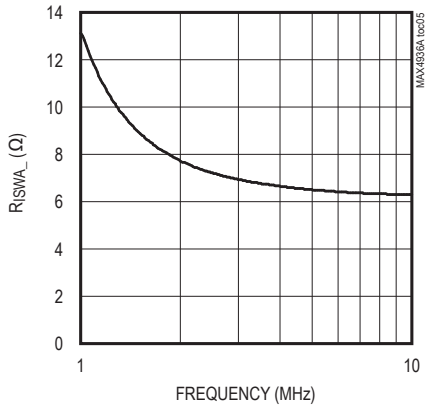
ICC_SHDN, |IEE_SHDN| SUPPLY SHUTDOWN CURRENT vs. TEMPERATURE



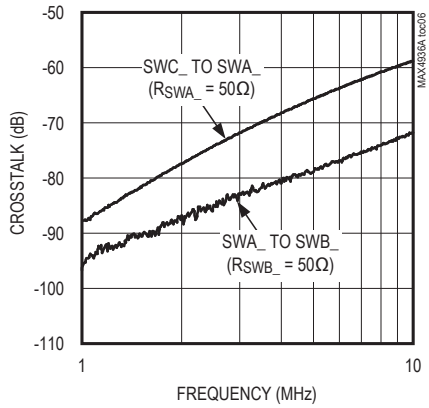
SWA_ TO SWB_ SMALL-SIGNAL TRANSFER FUNCTION vs. FREQUENCY



SWA_ TO SWB_ SMALL-SIGNAL ON-IMPEDANCE vs. FREQUENCY



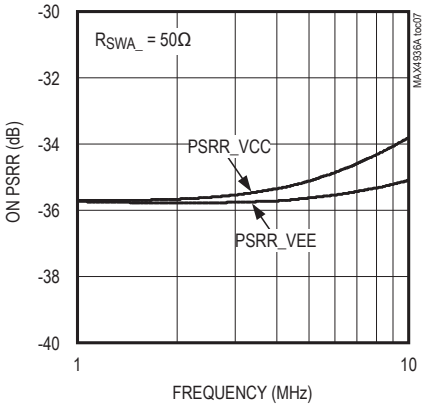
CROSSTALK vs. FREQUENCY



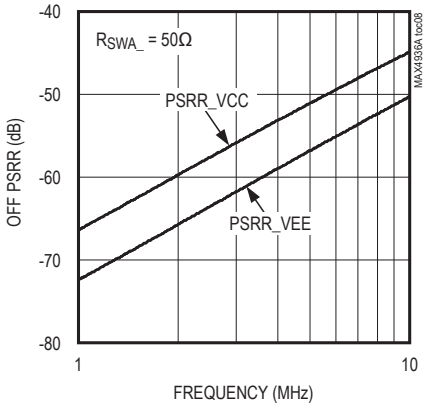
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +3.3V, I_{CH} = 1.5mA, $R_{SWA\_}$ = 50Ω, $R_{SWB\_}$ = 50Ω, f = 5MHz, T_A = +25°C, unless otherwise noted.)

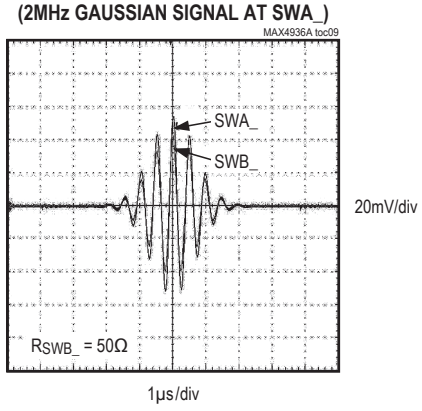
ON PSRR vs. FREQUENCY



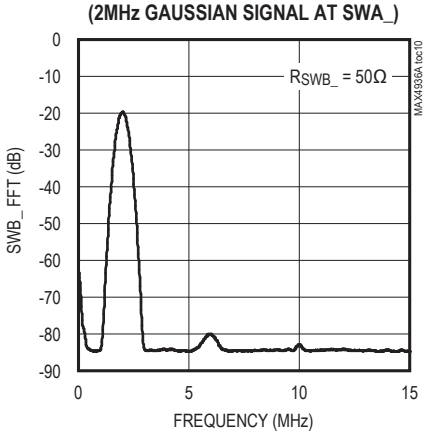
OFF PSRR vs. FREQUENCY



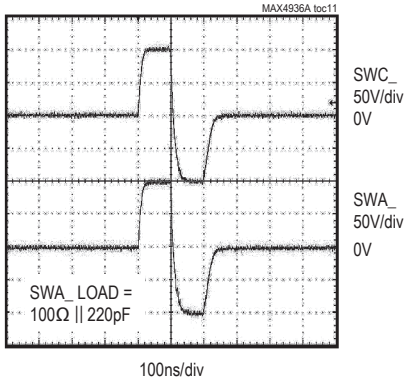
SWA_/SWB_ SMALL SIGNAL vs. TIME (2MHz GAUSSIAN SIGNAL AT SWA_)



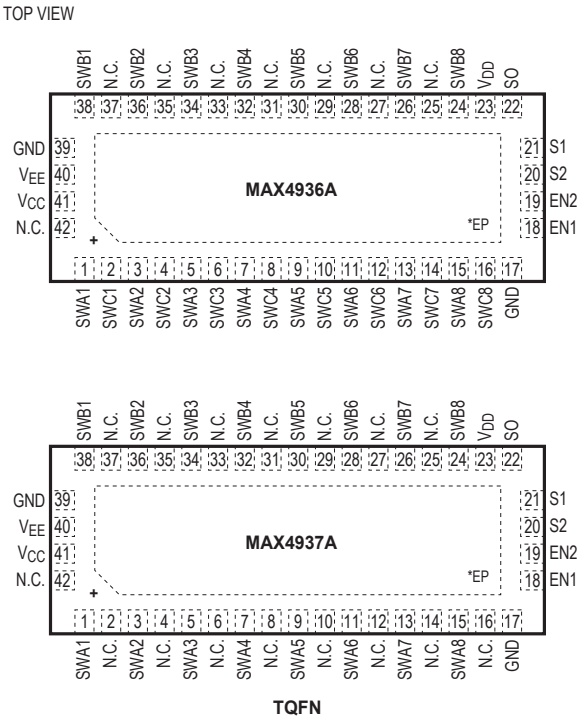
SWB_ FFT vs. FREQUENCY (2MHz GAUSSIAN SIGNAL AT SWA_)



SWC_/SWA_ vs. TIME



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
MAX4936A	MAX4937A		
1	1	SWA1	T/R Switch 1 Terminal A. When the switch is on, low-voltage signals are passed through from SWA1 to SWB1 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
2	—	SWC1	T/R Switch 1 Terminal C. Two diodes in anti-parallel configuration are connected between SWA1 and SWC1. Connect SWC1 to GND to clamp SWA1 and absorb leakage flowing through the diode bridge. Connect SWC1 to the transmitter output to use the diodes as grass clippers.
3	3	SWA2	T/R Switch 2 Terminal A. When the switch is on, low-voltage signals are passed through from SWA2 to SWB2 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936A	MAX4937A		
4	—	SWC2	T/R Switch 2 Terminal C. Two diodes in anti-parallel configuration are connected between SWA2 and SWC2. Connect SWC2 to GND to clamp SWA2 and absorb leakage flowing through the diode bridge. Connect SWC2 to the transmitter output to use the diodes as grass clippers.
5	5	SWA3	T/R Switch 3 Terminal A. When the switch is on, low-voltage signals are passed through from SWA3 to SWB3 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
6	—	SWC3	T/R Switch 3 Terminal C. Two diodes in anti-parallel configuration are connected between SWA3 and SWC3. Connect SWC3 to GND to clamp SWA3 and absorb leakage flowing through the diode bridge. Connect SWC3 to the transmitter output to use diodes as grass clippers.
7	7	SWA4	T/R Switch 4 Terminal A. When the switch is on, low-voltage signals are passed through from SWA4 to SWB4 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
8	—	SWC4	T/R Switch 4 Terminal C. Two diodes in anti-parallel configuration are connected between SWA4 and SWC4. Connect SWC4 to GND to clamp SWA4 and absorb leakage flowing through the diode bridge. Connect SWC4 to the transmitter output to use diodes as grass clippers.
9	9	SWA5	T/R Switch 5 Terminal A. When the switch is on, low-voltage signals are passed through from SWA5 to SWB5 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
10	—	SWC5	T/R Switch 5 Terminal C. Two diodes in anti-parallel configuration are connected between SWA5 and SWC5. Connect SWC5 to GND to clamp SWA5 and absorb leakage flowing through the diode bridge. Connect SWC5 to the transmitter output to use diodes as grass clippers.
11	11	SWA6	T/R Switch 6 Terminal A. When the switch is on, low-voltage signals are passed through from SWA6 to SWB6 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
12	—	SWC6	T/R Switch 6 Terminal C. Two diodes in anti-parallel configuration are connected between SWA6 and SWC6. Connect SWC6 to GND to clamp SWA6 and absorb leakage flowing through the diode bridge. Connect SWC6 to the transmitter output to use diodes as grass clippers.
13	13	SWA7	T/R Switch 7 Terminal A. When the switch is on, low-voltage signals are passed through from SWA7 to SWB7 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936A	MAX4937A		
14	—	SWC7	T/R Switch 7 Terminal C. Two diodes in anti-parallel configuration are connected between SWA7 and SWC7. Connect SWC7 to GND to clamp SWA7 and absorb leakage flowing through the diode bridge. Connect SWC7 to the transmitter output to use diodes as grass clippers.
15	15	SWA8	T/R Switch 8 Input A. When the switch is on, low-voltage signals are passed through from SWA8 to SWB8 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
16	—	SWC8	T/R Switch 8 Terminal C. Two diodes in anti-parallel configuration are connected between SWA8 and SWC8. Connect SWC8 to GND to clamp SWA8 and absorb leakage flowing through the diode bridge. Connect SWC8 to the transmitter output to use diodes as grass clippers.
17, 39	17, 39	GND	Ground
18	18	EN1	Enable Input 1. Set EN1 high to enable channels 1–4.
19	19	EN2	Enable Input 2. Set EN2 high to enable channels 5–8.
20	20	S2	Bias Select Input 2. Assert S2, S1, and S0 to set the bias current of the switch. See Table 1.
21	21	S1	Bias Select Input 1. Assert S2, S1, and S0 to set the bias current of the switch. See Table 1.
22	22	S0	Bias Select Input 0. Assert S2, S1, and S0 to set the bias current of the switch. See Table 1.
23	23	V_{DD}	Positive Logic Supply. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
24	24	SWB8	T/R Switch 8 Terminal B. When the switch is on, low-voltage signals are passed through from SWA8 to SWB8 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
25, 27, 29, 31, 33, 35, 37, 42	2, 4, 6, 8, 10,12,14,16, 25, 27, 29, 31, 33, 35, 37, 42	N.C.	No Connect. Not internally connected. Leave N.C. unconnected or connect N.C. to GND.
26	26	SWB7	T/R Switch 7 Terminal B. When the switch is on, low-voltage signals are passed through from SWA7 to SWB7 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
28	28	SWB6	T/R Switch 6 Terminal B. When the switch is on, low-voltage signals are passed through from SWA6 to SWB6 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936A	MAX4937A		
30	30	SWB5	T/R Switch 5 Terminal B. When the switch is on, low-voltage signals are passed through from SWA55 to SWB5 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
32	32	SWB4	T/R Switch 4 Terminal B. When the switch is on, low-voltage signals are passed through from SWA4 to SWB4 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
34	34	SWB3	T/R Switch 3 Terminal B. When the switch is on, low-voltage signals are passed through from SWA3 to SWB3 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
36	36	SWB2	T/R Switch 2 Terminal B. When the switch is on, low-voltage signals are passed through from SWA2 to SWB2 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
38	38	SWB1	T/R Switch 1 Terminal B. When the switch is on, low-voltage signals are passed through from SWA1 to SWB1 and vice-versa, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
40	40	V_{EE}	Negative Analog Supply. Bypass V_{EE} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
41	41	V_{CC}	Positive Analog Supply. Bypass V_{CC} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Do not use EP as the only GND connection.

Detailed Description

The MAX4936A/MAX4937A are octal, high-voltage, transmit/receive (T/R) switches. The T/R switches are based on a diode bridge topology, and the amount of current in the diode bridges can be programmed by three digital inputs (S0, S1, and S2). Two control inputs (EN1 and EN2) allow enabling/disabling channels 1–4 and channels 5–8, respectively. The MAX4936A includes the T/R switch and grass-clipping diodes, performing both transmit and receive operations. The MAX4937A includes just the T/R switch and performs the receive operation only.

These devices feature a low on-impedance in the entire ultrasound frequency range with extremely low power dissipation 15mW (typ) per channel.

The receive path for both devices is low impedance during low-voltage receive and high impedance during high-voltage transmit, providing protection to the receive circuitry. The low-voltage receive path is high bandwidth, low noise, low distortion, and low jitter. The MAX4936A SWC_ pins can be driven with high-voltage signals using the anti-parallel diodes as grass clippers while connecting the SWB_ pins to the low-noise amplifier (LNA); see Figure 3. Connecting SWC_ to GND allows the internal anti-parallel diodes to be used as clamps. Grass-clipping diodes can then be connected to SWB_ and the LNA to SWA_; see Figure 4.

Transmit/Receive Switch

The T/R switch is based on a diode bridge topology. The amount of bias current into each diode bridge is adjustable be setting the S0–S2 switches (see Figure 2 and Table 1).

Enable Inputs (EN1, EN2)

Two control inputs (EN1 and EN2) allow enabling/disabling channels 1–4 and channels 5–8, respectively. Drive EN1 high to enable channels 1–4; drive EN1 low to disable channels 1–4. Drive EN2 high to enable channels 5–8; drive EN2 low to disable channels 5–8. See Table 2.

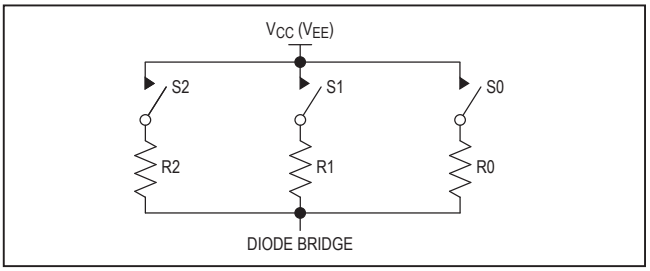


Figure 2. Diode Bias Current Control

Table 1. Diode Bias Current

DIODE BRIDGE CURRENT CONTROL BITS			RESISTORS (Ω)			RESISTOR COMBINATION	TYPICAL DIODE BRIDGE CURRENT (mA) vs. S[2:0] CONTROL BITS (*)	
S2	S1	S0	R2	R1	R0	(Ω)	V_{CC} = +3.3V	V_{CC} = +5V
0	0	0	2,200	4.400	8,800	—	0	0
0	0	1	2,200	4.400	8,800	8,800	0.31	0.52
0	1	0	2,200	4.400	8,800	4,400	0.61	1.02
0	1	1	2,200	4.400	8,800	2,933	0.91	1.53
1	0	0	2,200	4.400	8,800	2,200	1.20	2.03
1	0	1	2,200	4.400	8,800	1,760	1.50	2.54
1	1	0	2,200	4.400	8,800	1,467	1.80	3.04
1	1	1	2,200	4.400	8,800	1,257	2.09	3.53

*V_{EE} = -V_{CC}

Table 2. Enable Truth Table

EN1	EN2	CHANNELS 1–4	CHANNELS 5–8
0	0	Disabled (Off)	Disabled (Off)
0	1	Disabled (Off)	Enabled (On)
1	0	Enabled (On)	Disabled (Off)
1	1	Enabled (On)	Enabled (On)

Applications Information

For medical ultrasound applications, see Figures 3–6.

Ultrasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, F1 represents reflections from tissue and F2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude, and hence the measurement is defined with one input tone 25dB lower than the other. The IMD3 product of interest (F1 - (F2 - F1)) presents itself as an undesired Doppler error signal in ultrasound applications. See Figure 7.

Logic Levels

The digital inputs S0, S1, S2, EN1, and EN2 are tolerant of up to +5.5V, independent of the V_{DD} supply voltage, allowing compatibility with higher voltage controllers.

Supply Sequencing and Bypassing

The devices do not require special sequencing of the V_{DD}, V_{CC}, and V_{EE} supply voltages; however, analog switch inputs must be unconnected, or satisfy $V_{EE} \le (V_{SWA\_}, V_{SWB\_}, V_{SWC\_}) \le V_{CC}$ during power-up and power-down. Bypass V_{DD}, V_{CC}, and V_{EE} to GND with a 1FF ceramic capacitor as close as possible to the device.

PCB Layout

The pin configuration is optimized to facilitate a very compact physical layout of the device and its associated discrete components. A typical application for this device might incorporate several devices in close proximity to handle multiple channels of signal processing.

The exposed pad (EP) of the TQFN-EP package provides a low thermal resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP must be soldered to a ground plane on the PCB, either directly or through an array of plated through holes.

Single-Supply Operation

For single-supply operation, connect V_{EE} to GND and apply +2.5V to +5.5V to V_{CC}.

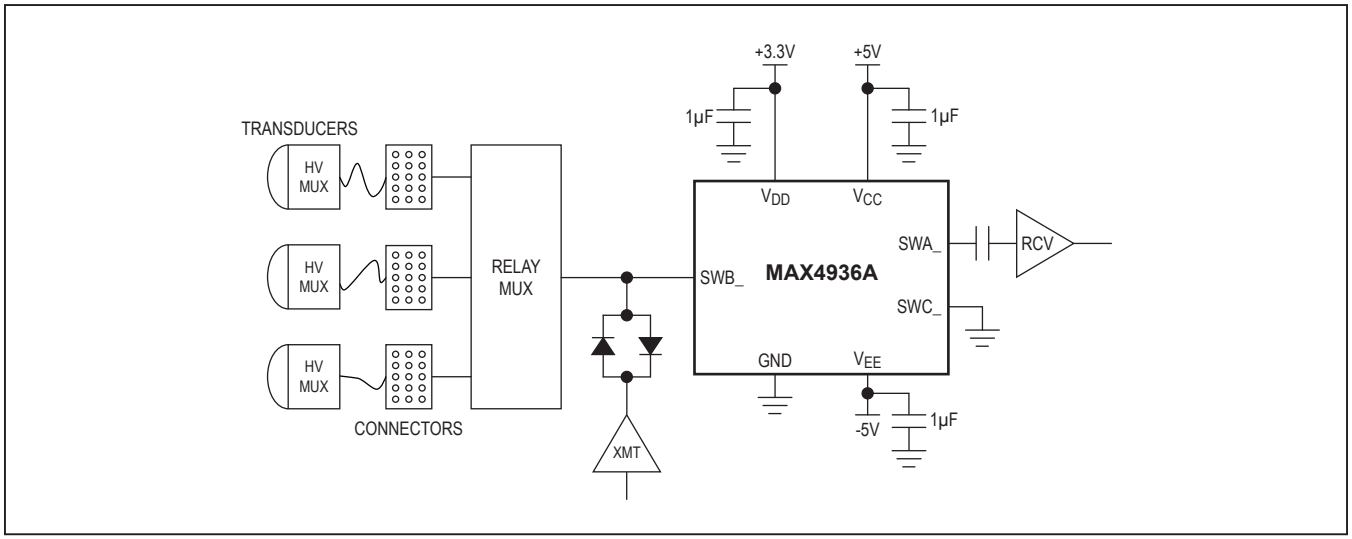


Figure 3. Ultrasound T/R Path. Anti-parallel diodes used as grass clippers.
SWC_ = Transmitter Output, SWA_ = Input, SWB_ = Output. (One channel only.)

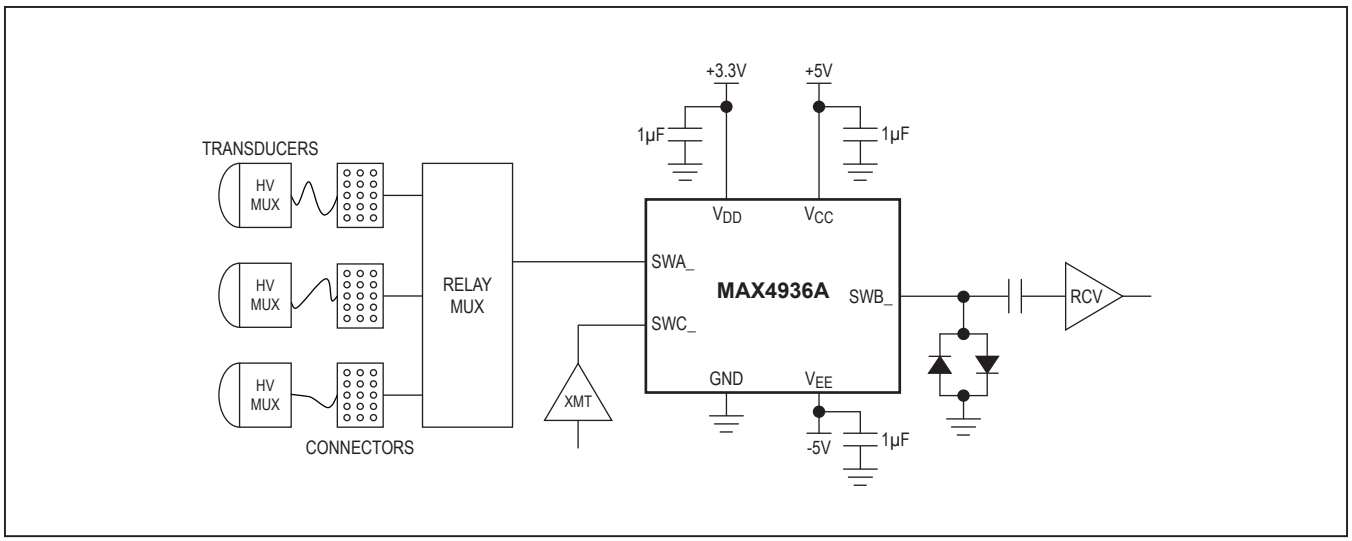


Figure 4. Ultrasound T/R Path. Anti-parallel diodes used as clamping diodes. SWC_ = GND, SWB_ = Input, SWA_ = Output. (One channel only.)

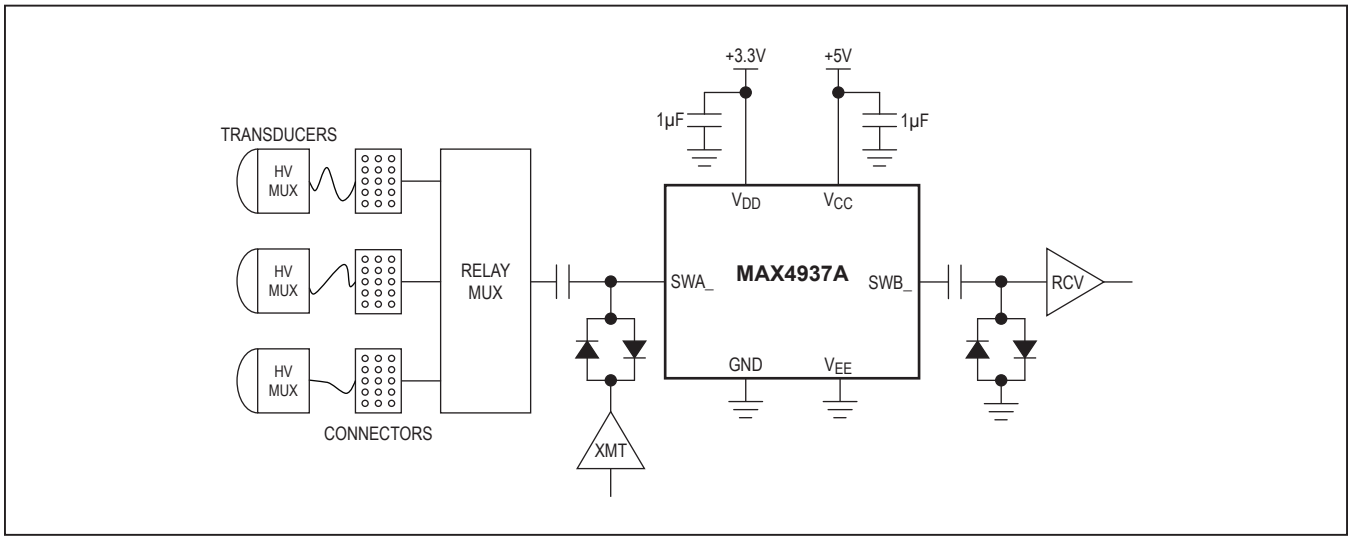


Figure 5. Ultrasound T/R Path. Operation from a single supply (V_{CC} = +5V). (One channel only.)

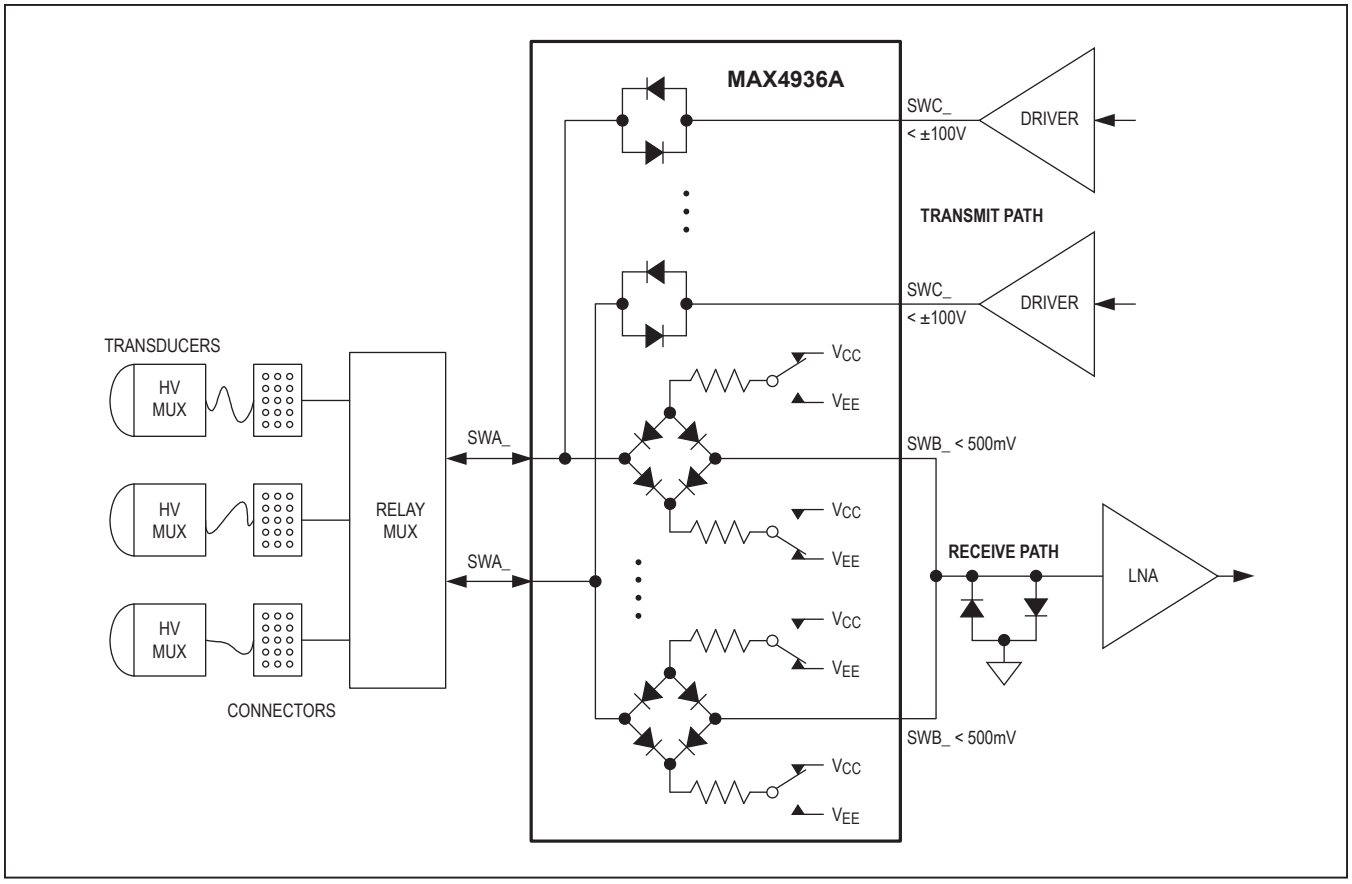


Figure 6. Ultrasound T/R Path with Multiple Transmits per Receive Channel

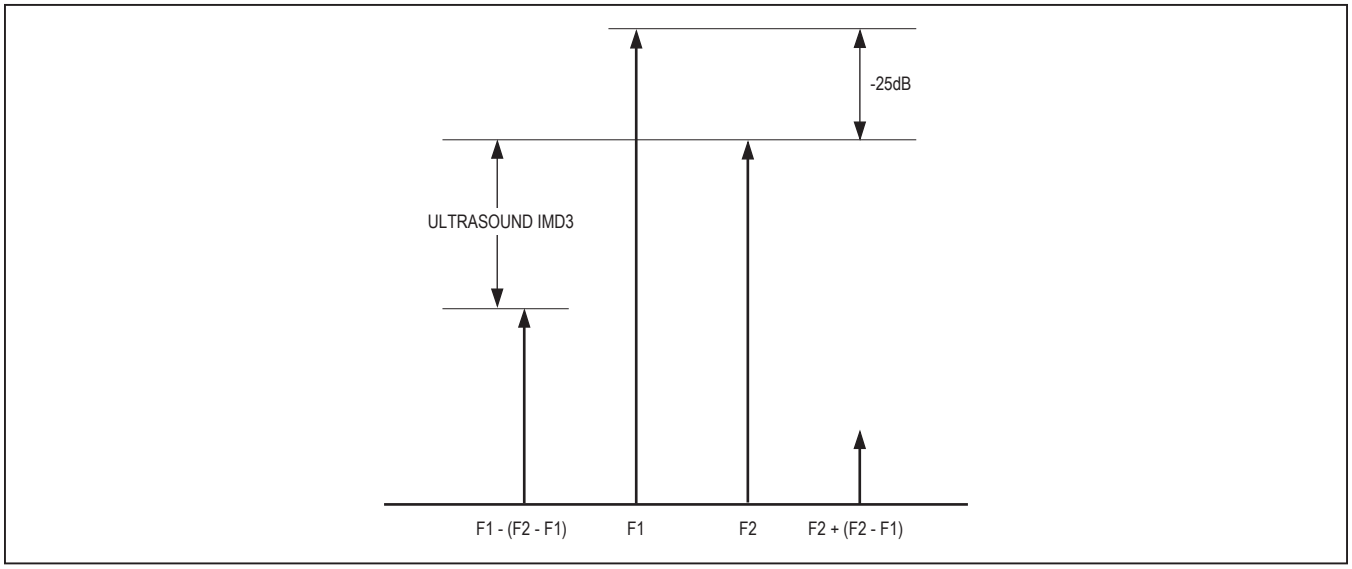


Figure 7. Ultrasound IMD3 Measurement Technique

Ordering Information/Selector Guide

PART	ANTI-PARALLEL DIODES	TEMP RANGE	PIN-PACKAGE
MAX4936ACTO+	Yes	0°C to +70°C	42 TQFN-EP*
MAX4937ACTO+	No	0°C to +70°C	42 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
42 TQFN-EP	T423590+1	21-0181	90-0078

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/11	Initial release	—

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