EVALUATION KIT AVAILABLE

MAX5879

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

General Description

The MAX5879 is a high-performance, 14-bit, 2.3Gsps digital-to-analog converter (DAC) capable of synthesizing high-frequency and wideband signals in baseband and higher-order Nyquist zones. The 2.3Gsps update rate, combined with the selectable frequency-response modes (NRZ, RZ, RF, and RFZ), allows digital generation of signals to more than 2GHz output frequency. The unique RFZ mode allows generation up to the 6th Nyquist zone, with update rates to 1150Msps. The device features excellent spurious, noise, and intermodulation distortion performance, and can directly synthesize signal bandwidths to more than 1GHz.

The device has four 14-bit, multiplexed, low-voltage differential signaling (LVDS) input ports that each operates up to 1150Mwps. The DAC operates with a clock rate (f_{CLK}) up to 2.3GHz. The device has a selectable 2:1 or 4:1 input multiplexer that allows the user to select two data ports up to 1150Mwps each, or four data ports up to 575Mwps each. In turn, the input data rate is 1/2 or 1/4 the DAC update rate at each port. The device features a delay-locked loop (DLL) to ease data synchronization with FPGAs or ASICs. The parity input and parity error flag output can be used to detect bit errors between the data source and the DAC. The device also features a data clock reset circuit for aligning the data-capture clocks of multiple DACs.

The device has four selectable frequency-response output modes:

- Nonreturn-to-zero (NRZ) mode provides the highest dynamic range/output power in the 1st Nyquist zone.
- Return-to-zero (RZ) mode trades off SNR for improved gain flatness in the 1st, 2nd, and 3rd Nyquist zones.
- Radio-frequency (RF) mode provides higher SNR and excellent dynamic performance in the 2nd and 3rd Nyquist zones.
- Radio-frequency-return-to-zero (RFZ) mode provides high dynamic range and improved gain flatness in the 3rd through 6th Nyquist zones at a maximum update rate of $f_{CLK}/2$.

The device is a current-steering DAC with an integrated 50Ω differential output termination to ensure optimum dynamic performance. Operating from 3.3V and 1.8V power supplies, the device dissipates 1.8W at 40mA full-scale current and 2.3W at 80mA full-scale current. The device is specified over the -40°C to +85°C extended temperature range and is offered in a 256-ball (17mm x 17mm) CSBGA package.

***Ordering Information* appears at end of data sheet.**

Features

- **Industry-Leading Performance**
  - **WCDMA ACLR: 70dB at 2.14GHz**
  - **DOCSIS ACP: -70dBc at 400MHz, 8 Channel (256 QAM)**
  - **Noise Density: -165dBc/Hz at 200MHz**
- **High Output Power: 9dBm (CW)**
- **Frequency-Response Modes: NRZ, RZ, RF, RFZ**
- **2GHz Output Bandwidth**
- **2:1 or 4:1 Multiplexed LVDS Inputs**
  - **Up to 1150MHz Each Port**
  - **Single or Double Data-Rate Operation**
- **On-Chip DLL for Input Data Synchronization**
- **Reset Function for Multiple DAC Synchronization**

Applications

Broadband Communications

Edge QAM and CMTS

Digital Video Broadcast

Wireless Infrastructure

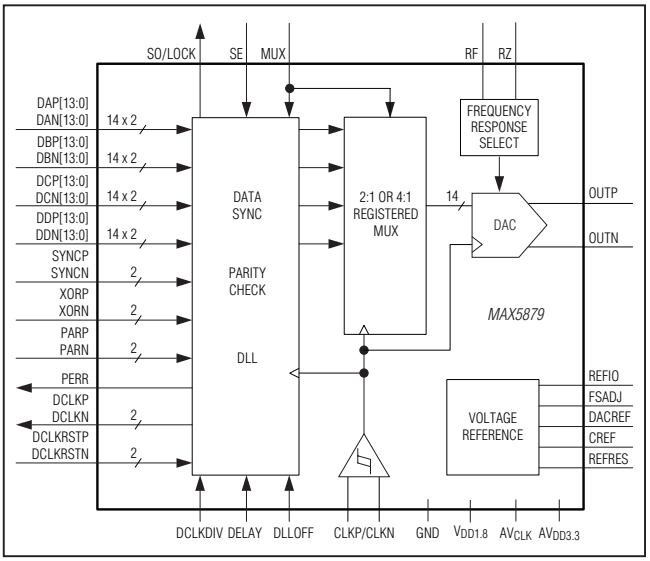
Software-Defined Radio

Direct Digital Synthesis

Radar and Avionics

Arbitrary Waveform Generators

Functional Diagram



For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX5879.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5874; Rev 1; 10/12

ABSOLUTE MAXIMUM RATINGS

$AV_{DD3.3}$ to GND, DACREF ..... -0.3V to +3.6V
$V_{DD1.8}$, AV_{CLK} to GND, DACREF ..... -0.3V to +2.0V
REFIO, FSADJ to GND, DACREF ..... -0.3V to ($V_{AVDD3.3}$ + 0.3V)
OUTP, OUTN to GND, DACREF ..... -0.3V to ($V_{AVDD3.3}$ + 1.0V)
CREF to GND, DACREF ..... -0.3V to +2.0V
DCLKDIV, DLLOFF, DELAY, REFRES to GND, DACREF ..... -0.3V to ($V_{AVDD3.3}$ + 0.3V)
SE, MUX, RF, RZ to GND, DACREF. -0.3V to ($V_{AVDD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF ..... -0.3V to (V_{AVCLK} + 0.3V)
DAP0–DAP13, DBP0–DBP13, DCP0–DCP13 to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
DDP0–DDP13, XORP, SYNCP, PARP to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
DAN0–DAN13, DBN0–DBN13, DCN0–DCN13 to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
DDN0–DDN13, XORN, SYNCN, PARN to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
DCLKP, DCLKN to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
DCLKRSTP, DCLKRSTN to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
SO/LOCK, PERR to GND, DACREF ..... -0.3V to ($V_{DD1.8}$ + 0.3V)
SO/LOCK, PERR Continuous Current 8mA
DCLKP, DCLKN Continuous Current 8mA
Continuous Power Dissipation (T_A = +70°C)
256-Ball CSBGA
(derate 38.6mW/°C above +70°C) 3088mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution					14		Bits
Full-Scale Output Current Range	I_{OUT}	(Note 2)		10		80	mA
Output-Power Gain Error	GE			-0.7		+0.7	dB
Output-Power Drift		Internal reference			-0.003		dB/°C
		External reference			-0.0025		
Maximum Output Power	P_{OUT}	Differential, into 50Ω load, f_{OUT} = 100MHz			+9		dBm
Output Resistance	R_{OUT}	Differential			50		Ω
DYNAMIC PERFORMANCE (Note 3)							
Clock Frequency Range	f_{CLK}	DCLKDIV = 1, 2:1 mux mode		50		2300	MHz
		DCLKDIV = 0, 2:1 mux mode		50		2200	
		4:1 mux mode		50		2300	
Output Update Rate	f_{DAC}	NRZ, RZ, RF mode	1.8V ≤ (V_{DD}, V_{AVCLK}) ≤ 1.9V	2300			Msps
			1.7V ≤ (V_{DD}, V_{AVCLK}) ≤ 1.8V	2200			
		RFZ mode	4:1 mux mode only (f_{CLK} = f_{DAC} x 2)	1150			

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range f_{OUT} ±200MHz	SFDR	f_{CLK} = 2300MHz, NRZ mode	f_{OUT} = 500MHz, -1dBFS		73		dBc
		f_{CLK} = 1500MHz, RZ mode	f_{OUT} = 1000MHz, -1dBFS		76		
		f_{CLK} = 2300MHz, RF mode	f_{OUT} = 1800MHz, -1dBFS		73		
		f_{CLK} = 1500MHz, RFZ mode	f_{OUT} = 1750MHz, -1dBFS		73		
DOCSIS DRFI Out-of-Band Noise and Spurious, Eight 6MHz QAM Channels, Average Total Power = -10dBFS		f_{OUT} = 400MHz, f_{CLK} = 2048MHz, T_J = +30°C to +110°C, 2:1 mux mode	Adjacent channel power (750kHz from channel-block edge to 6MHz from channel-block edge)		-71	-62	dBc
			Next-adjacent channel power (6MHz from channel block edge to 12MHz from channel-block edge)		-72	-64	
			Third-adjacent channel power (12MHz from channel-block edge to 18MHz from channel-block edge)		-73	-66	
			Noise in any other channel		-74		
		f_{OUT} = 860MHz, f_{CLK} = 2048MHz, 2:1 mux mode	Adjacent channel rejection (750kHz from channel-block edge to 6MHz from channel-block edge)		-65		
			Next-adjacent channel rejection (6MHz from channel-block edge to 12MHz from channel-block edge)		-65		
			Third-adjacent channel rejection (12MHz from channel-block edge to 18MHz from channel block edge)		-65		
			Noise in any other channel		-65		

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DOCSIS DRFI Harmonic Distortion, Four 6MHz QAM Channels, Average Total Power = -10dBFS		f_{OUT} = 300MHz, f_{CLK} = 2048MHz, 4:1 mux mode	In each of eight 6MHz channels coinciding with 2nd harmonic components		-70		dBc
			In each of twelve 6MHz channels coinciding with 3rd harmonic components		-75		
DOCSIS DRFI Harmonic Distortion, Four 6MHz QAM Channels, Average Total Power = -10dBFS		f_{OUT} = 700MHz, f_{CLK} = 2048MHz, 2:1 mux mode	In each of eight 6MHz channels coinciding with 2nd harmonic components		-68		dBc
			In each of twelve 6MHz channels coinciding with 3rd harmonic components		-69		
Two-Tone IMD	TTIMD	f_{CLK} = 2300MHz, NRZ mode	f_{OUT1} = 500MHz, -7dBFS, f_{OUT2} = 501MHz, -7dBFS		-78		dBc
		f_{CLK} = 1500MHz, RZ mode	f_{OUT1} = 1000MHz, -7dBFS, f_{OUT2} = 1001MHz, -7dBFS		-69		
		f_{CLK} = 2334.72MHz, RF mode	f_{OUT1} = 1834MHz, -12dBFS, f_{OUT2} = 1835MHz, -12dBFS		-71		
		f_{CLK} = 2300MHz, RFZ mode	f_{OUT1} = 2100MHz, -12dBFS, f_{OUT2} = 2101MHz, -12dBFS		-71		
4-Carrier ACLR for WCDMA, TM1, -18dBFS per Carrier at DAC Input	ACLR	f_{CLK} = 2334.72MHz, RF mode	f_{OUT1} = 1952.5MHz, f_{OUT2} = 1957.5MHz, f_{OUT3} = 1962.5MHz, f_{OUT4} = 1967.5MHz		67		dB
Gain Flatness	GF	f_{CLK} = 2300MHz, f_{OUT} ≤ 1000MHz	Over any single 6MHz channel		0.02		dB
			Within 50MHz to 1000MHz band		3		
Clock Spurs		2:1 mux mode	f_{CLK}/4 spur		-90		dBm
			f_{CLK}/8 spur		-98		
		4:1 mux mode	f_{CLK}/4 spur		-75		
			f_{CLK}/8 spur		-97		
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.1	1.2	1.3	V
Reference Input-Voltage Compliance Range	V_{REFIOR}	(Note 4)		0.5		1.8	V

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Drift	TCO_{REF}				50		ppm/°C
ANALOG OUTPUT TIMING							
Output Fall Time	t_{FALL}	90% to 10% (Note 5)			300		ps
Output Rise Time	t_{RISE}	10% to 90% (Note 5)			300		ps
Settling Time	t_S	Settling to 0.1% (Note 6)			26		ns
Output Bandwidth	t_{BW}	(Note 7)			2		GHz
Output Propagation Delay	t_{PD}	(Note 8)			1.5		ns
Output Data Latency	t_{LAT}	DAP[13:0]/DAN[13:0] to output			11.5		Clock cycles
		DBP[13:0]/DBN[13:0] to output			12.5		
		DCP[13:0]/DCN[13:0] to output			13.5		
		DDP[13:0]/DDN[13:0] to output			14.5		
TIMING CHARACTERISTICS							
DLL Frequency Range	f_{DLL}	f_{DLL} = f_{CLK}/2 2:1 mux mode (MUX = 0)	DLLOFF = low, DELAY = high	1075		1150	MHz
			DLLOFF = low, DELAY = open	950		1075	
			DLLOFF = open, DELAY = low	825		950	
			DLLOFF = open, DELAY = high	700		825	
			DLLOFF = open, DELAY = open	625		700	
			DLLOFF = resistor to ground, DELAY = low	550		625	
			DLLOFF = resistor to ground, DELAY = high	475		550	
			DLLOFF = resistor to ground, DELAY = open	400		475	
		f_{DLL} = f_{CLK}/4 4:1 mux mode (MUX = 1)	DLLOFF = resistor to ground, DELAY = low	550		575	
			DLLOFF = resistor to ground, DELAY = high	475		550	
			DLLOFF = resistor to ground, DELAY = open	400		475	

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Data Skew	t_{SKEW}	Allowed skew of any LVDS input (DAP[13:0]/DAN[13:0], DBP[13:0]/DBN[13:0], DCP[13:0]/DCN[13:0], DDP[13:0]/DDN[13:0], XORP/XOR, and PARP/PARN), with respect to the SYNC input; this parameter only applies when DLLOFF is not driven high (Note 9)	-310		+315	ps
Input Data to Clock Setup Time	t_{SETUP}	DLLOFF = 1.8V; data on the LVDS input pins must be stable for t_{SETUP} before the next edge of DCLKP/DCLKN; this parameter only applies when DLLOFF is driven high, V_{MUX} = 0V (Note 9)	1.53			ns
Input Data to Clock Hold Time	t_{HOLD}	DLLOFF = 1.8V; data on the LVDS input pins must remain stable for t_{HOLD} after an edge of DCLKP/DCLKN; this parameter only applies when DLLOFF is driven high, V_{MUX} = 0V (Note 9)	-0.9			ns
Parity Error Pulse Width	t_{ERR}	Pulse width of PERR when a parity error is detected		48		Data periods
Parity Pipeline Delay	$t_{PIPE,P}$	Pipeline delay in the internal parity calculation; delay the incoming PARP/PARN bit by this amount	3		3	Data periods
XOR Pipeline Delay	$t_{PIPE,X}$	Pipeline delay in the XOR path; delay the in coming XORP/XORN bit by this amount	1		1	Data periods
DIFFERENTIAL LOGIC INPUTS (DAP13–DAP0, DAN13–DAN0, DBP13–DBP0, DBN13–DBN0, DCP13–DCP0, DCN13–DCN0, DDP13–DDP0, DDN13–DDN0, XORP, XORN, PARP, PARN, SYNCP, SYNCN) SPECIFIED FOR LVDS INPUT						
Differential Input Logic-High	V_{IH}		100			mV
Differential Input Logic-Low	V_{IL}				-100	mV
Input Common-Mode Voltage Range	V_{COM}		1.125		1.375	V
Differential Input Resistance	R_{IN}		85	107	125	Ω
Input Capacitance	C_{IN}			1.5		pF

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL LOGIC INPUTS (DAP13–DAP0, DAN13–DAN0, DBP13–DBP0, DBN13–DBN0, DCP13–DCP0, DCN13–DCN0, DDP13–DDP0, DDN13–DDN0, XORP, XORN, PARP, PARN, SYNCP, SYNCN) SPECIFIED FOR DIFFERENTIAL-HSTL INPUT						
Differential Input Logic-High	$V_{IH(DC)}$		160			mV
Differential Input Logic-Low	$V_{IL(DC)}$				-160	mV
Input Common-Mode Voltage Range	V_{COM}		0.456		1.0	V
Differential Input Resistance	R_{IN}		85	107	125	Ω
Input Capacitance	C_{IN}			1.5		pF
1.8V LVDS OUTPUTS (DCLKP, DCLKN)						
Differential Output	$V_{DIFF,LVDS}$	$V_{DIFF,LVDS}$ = V_{DCLKP} - V_{DCLKN}, with 100Ω differential termination	±250	±350	±450	mV
Output Rise and Fall Time	t_R, t_F	With 100Ω differential termination		0.3		ns
Common-Mode Voltage Range	$V_{COM,LVDS}$		1.125	1.28	1.375	V
DATA CLOCK RESET INPUTS (DCLKRSTP, DCLKRSTN)						
Differential Input Logic-High	$V_{IH(RST)}$		250			mV
Differential Input Logic-Low	$V_{IL(RST)}$				-250	mV
Input Common-Mode Voltage Range	V_{COM}		1.125		1.375	V
Differential Input Resistance	R_{IN}		85		125	Ω
Input Capacitance	C_{IN}			1.5		pF
Input Data to Clock Setup Time	$t_{SETUPRST}$	(Note 9)	0.3			ns
1.8V CMOS LOGIC INPUTS (DCLKDIV, MUX, RF, RZ, SE)						
Input Logic-High	$V_{IH1.8}$		0.7 x $V_{DD1.8}$			V
Input Logic-Low	$V_{IL1.8}$				0.3 x $V_{DD1.8}$	V
Input Leakage Current	$I_{IN1.8}$		-5		+5	µA
Input Capacitance	$C_{IN1.8}$			3		pF

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8V 4-LEVEL LOGIC INPUTS (DELAY, DLLOFF)						
Input 4-Level Logic-High	V_{IH4}		27/32 x $V_{DD1.8}$ + 50mV		$V_{DD1.8}$	V
Input 4-Level Logic-Open	V_{OC4}		17/32 x $V_{DD1.8}$ + 50mV		27/32 x $V_{DD1.8}$ - 50mV	V
Input 4-Level Logic-Res	V_{RC4}		7/32 x $V_{DD1.8}$ + 50mV		17/32 x $V_{DD1.8}$ - 50mV	V
Input 4-Level Logic-Low	V_{IL4}		0		7/32 x $V_{DD1.8}$ - 50mV	V
Input Pullup Current	I_{PU4}		10	14.3	18.6	µA
Input Pulldown Current	I_{PD4}		18.9	27	35.1	µA
Input Capacitance	C_{IN4}			3		pF
1.8V CMOS LOGIC OUTPUTS (SO/LOCK, PERR)						
Output Logic-High	$V_{OH1.8}$	I_{SOURCE} = 200µA	$V_{DD1.8}$ - 0.2			V
Output Logic-Low	$V_{OL1.8}$	I_{SINK} = 200µA			0.2	V
CLOCK INPUTS (CLKP, CLKN)						
Minimum Clock Input Power	$P_{CLK,MIN}$	(Note 10)		6		dBm
Maximum Clock Input Power	$P_{CLK,MAX}$	Power measured into the MAX5879 clock input with 100Ω external differential termination resistor		12		dBm
Common-Mode Voltage Range	V_{COMCLK}	Input is self biased		V_{AVCLK}/3		V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF
POWER SUPPLIES						
Analog Supply Voltage Range	$AV_{DD3.3}$		3.2	3.3	3.5	V
1.8V Supply Voltage Range	$V_{DD1.8}$	10MHz ≤ f_{CLK} ≤ 2200MHz	1.7	1.8	1.9	V
		2200MHz ≤ f_{CLK} ≤ 2300MHz	1.8		1.9	
Clock Supply Voltage Range	AV_{CLK}	10MHz ≤ f_{CLK} ≤ 2200MHz	1.7	1.8	1.9	V
		2200MHz ≤ f_{CLK} ≤ 2300MHz	1.8		1.9	

ELECTRICAL CHARACTERISTICS (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, V_{DELAY} = 1.8V, $V_{DCLKDIV}$ = V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, R_{REFRES} = 500Ω, transformer-coupled differential output, $T_{A(MIN)}$ = -40°C to $T_{J(MAX)}$ = +110°C, unless otherwise noted.) (Note 1)

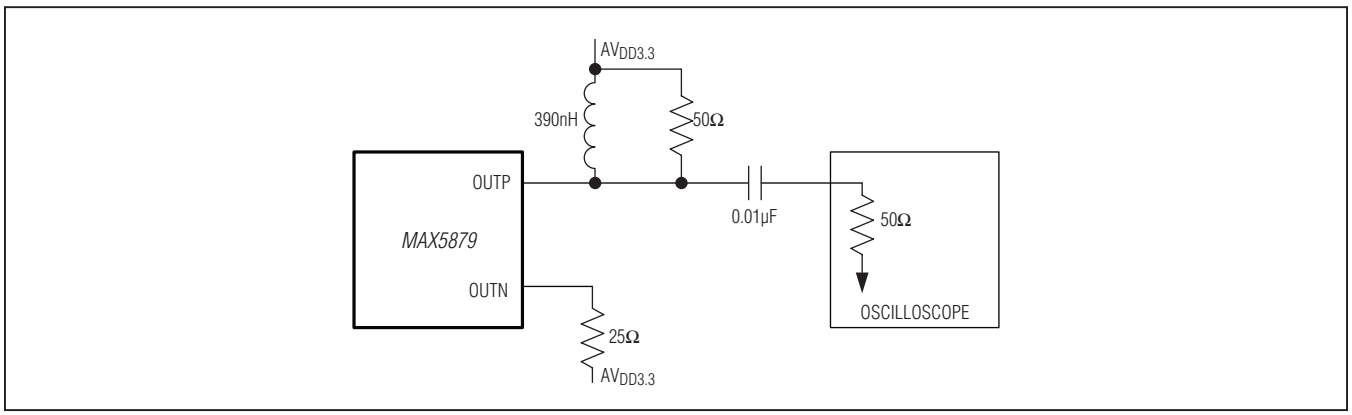
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Current	$I_{AVDD3.3}$	f_{CLK} = 2048MHz, f_{OUT} = 400MHz, eight 6MHz QAM channels, average total power = -10dBFS		340	360	mA
1.8V Supply Current	$I_{VDD1.8}$	f_{CLK} = 2048MHz, f_{OUT} = 400MHz, eight 6MHz QAM channels, average total power = -10dBFS		225	260	mA
Clock Supply Current	I_{AVCLK}	f_{CLK} = 2048MHz, f_{OUT} = 400MHz, eight 6MHz QAM channels, average total power = -10dBFS		420	460	mA
Power Dissipation	P_{DISS}	f_{CLK} = 2048MHz, f_{OUT} = 400MHz, eight 6MHz QAM channels, average total power = -10dBFS		2.3	2.5	W
		f_{CLK} = 2048MHz, f_{OUT} = 400MHz, eight 6MHz QAM channels, full-scale current = 40mA, average total output power = -16dBFS, R_{REFRES} = 1kΩ, R_{SET} = 4kΩ		1.8		

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature	T_A	(Note 11)	-40		+85	°C
Junction Temperature	T_J		-40		+110	°C
Thermal Resistance, Junction-to-Ambient (Note 11)	θ_{JA}	Air flow 0m/s		25.9		°C/W
		Air flow 1m/s		23.1		
		Air flow 2.5m/s		21.9		
Thermal Resistance, Junction-to-Case	θ_{JC}			5.6		°C/W
Thermal Resistance, Junction-to-Board	θ_{JB}			15.9		°C/W
Thermal Characterization Parameter, Junction-to-Board	Ψ_{JB}			15		°C/W
Thermal Characterization Parameter, Junction-to-Top	Ψ_{JT}			1		°C/W

Note 1: All specifications are 100% tested at T_J = +65°C and T_J = +110°C to an accuracy of ±15°C, unless otherwise noted. Typical values are at T_J = +65°C ±15°C. Specifications at T_J < +65°C are guaranteed by design and characterization.
Note 2: Nominal full-scale current I_{OUT} = 128 x I_{REF}.
Note 3: CLK input = +9dBm, AC-coupled sine wave.
Note 4: REFIO voltage less than 0.5V shuts down the internal clock circuitry of the device.

Note 5: Measured single-ended into a double-terminated 50Ω load.

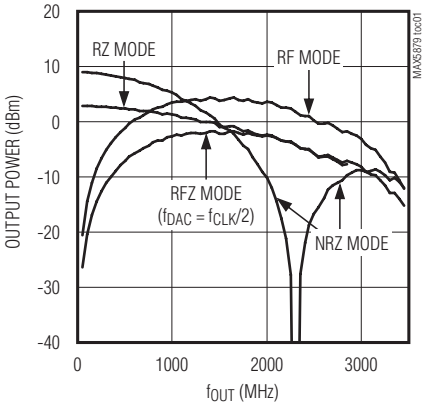


Note 6: From the application of a step at DAC input until corresponding DAC output is settled to the specified accuracy.
Note 7: Measured differentially into a 50Ω load.
Note 8: Referenced to rising edge of DAC update clock. Excludes data latency.
Note 9: Guaranteed by design and characterization.
Note 10: Transformer-coupled clock input (Figure 4).
Note 11: The package is mounted on a four-layer JEDEC standard test board, dissipating maximum power.

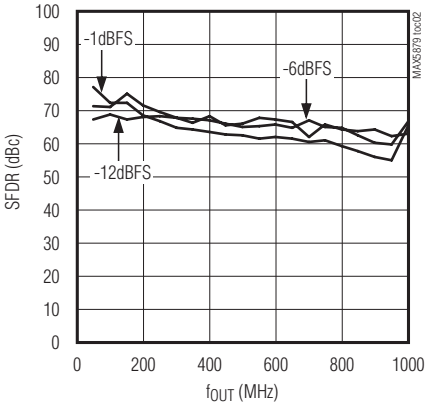
Typical Operating Characteristics

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

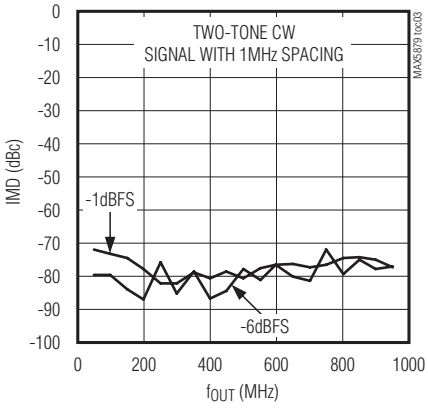
FULL-SCALE OUTPUT POWER vs. OUTPUT FREQUENCY (f_{CLK} = 2.3GHz)



SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 2GHz, NRZ MODE)



TWO-TONE IMD vs. OUTPUT FREQUENCY (f_{CLK} = 2GHz, NRZ MODE)

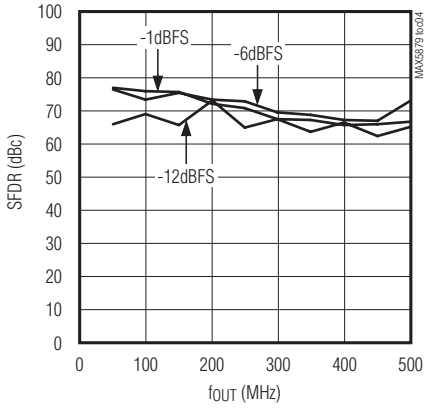


14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

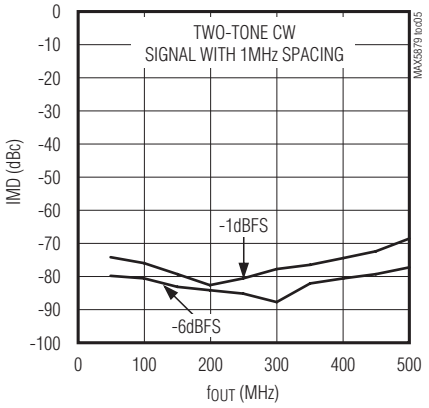
Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

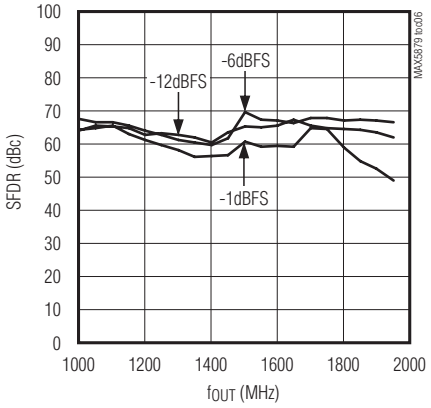
SFDR vs. OUTPUT FREQUENCY (f_{CLK} = 1GHz, NRZ MODE)



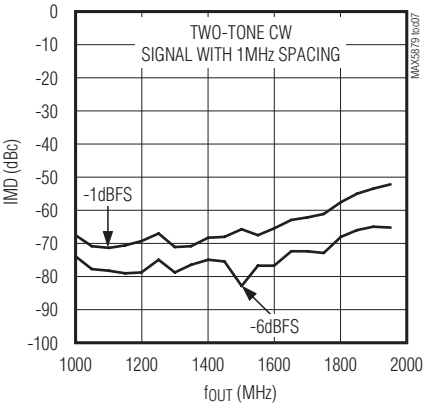
TWO-TONE IMD vs. OUTPUT FREQUENCY (f_{CLK} = 1GHz, NRZ MODE)



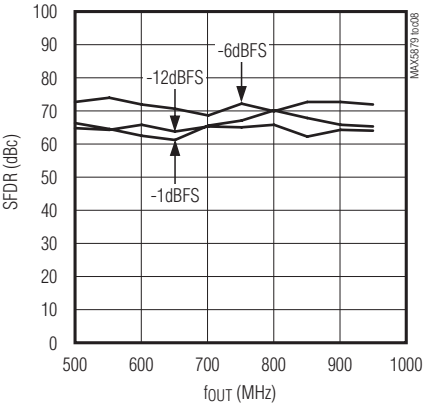
SFDR vs. OUTPUT FREQUENCY (2ND NYQUIST ZONE, f_{CLK} = 2GHz, RF MODE)



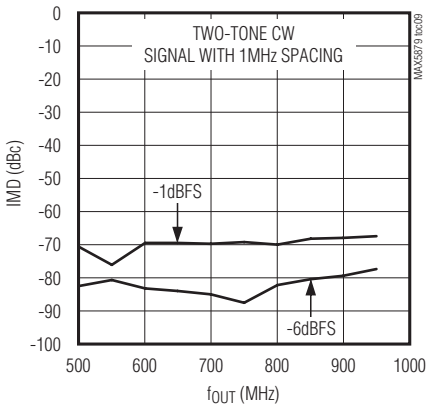
TWO-TONE IMD vs. OUTPUT FREQUENCY (2ND NYQUIST ZONE, f_{CLK} = 2GHz, RF MODE)



SFDR vs. OUTPUT FREQUENCY (2ND NYQUIST ZONE, f_{CLK} = 1GHz, RF MODE)



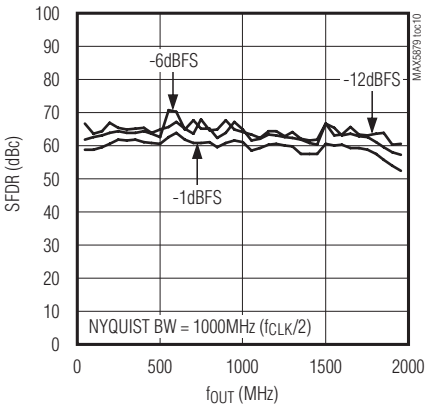
TWO-TONE IMD vs. OUTPUT FREQUENCY (2ND NYQUIST ZONE, f_{CLK} = 1GHz, RF MODE)



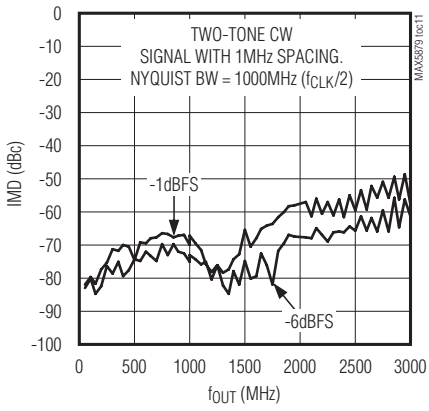
Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

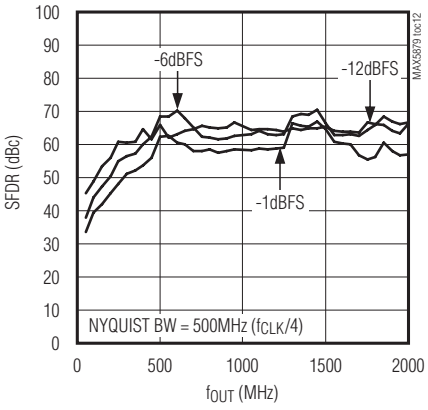
SFDR vs. OUTPUT FREQUENCY (WITHIN A GIVEN NYQUIST ZONE) (f_{CLK} = 2GHz, RZ MODE)



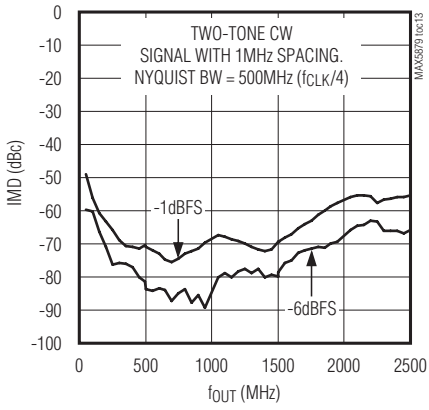
TWO-TONE IMD vs. OUTPUT FREQUENCY (WITHIN A GIVEN NYQUIST ZONE) (f_{CLK} = 2GHz, RZ MODE)



SFDR vs. OUTPUT FREQUENCY (WITHIN A GIVEN NYQUIST ZONE) (f_{CLK} = 2GHz, RFZ MODE)



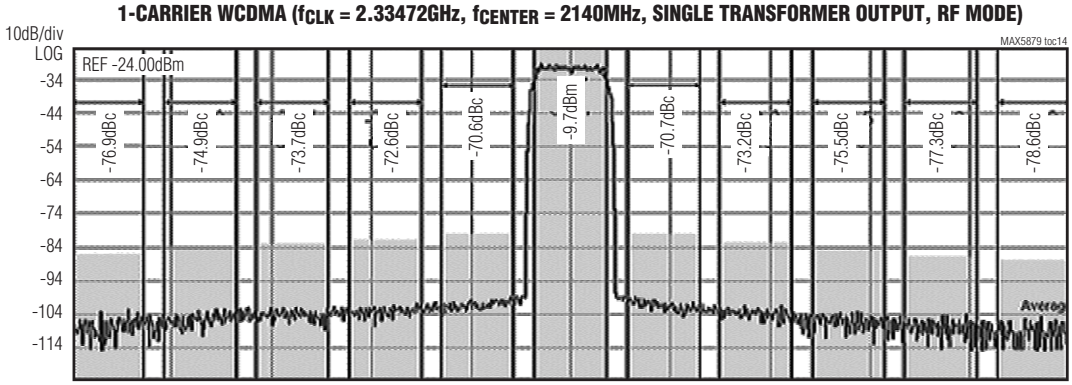
TWO-TONE IMD vs. OUTPUT FREQUENCY (WITHIN A GIVEN NYQUIST ZONE) (f_{CLK} = 2GHz, RFZ MODE)



Typical Operating Characteristics (continued)

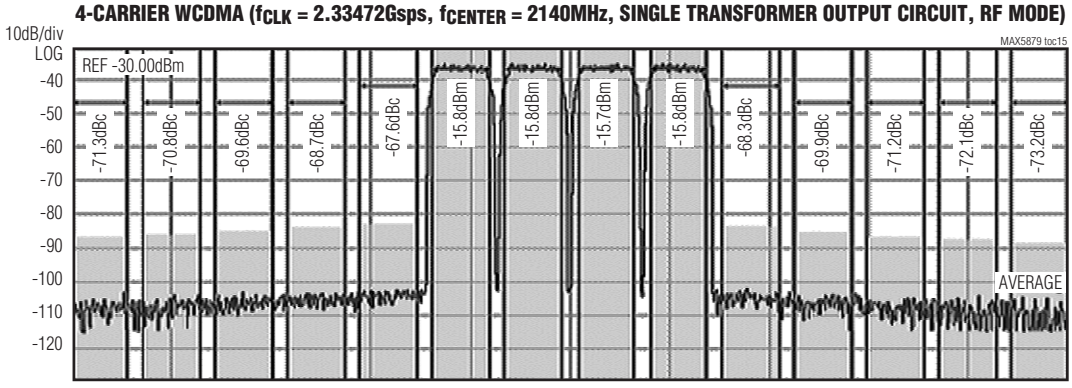
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

1-CARRIER WCDMA (f_{CLK} = 2.33472GHz, f_{CENTER} = 2140MHz, SINGLE TRANSFORMER OUTPUT, RF MODE)



CENTER = 2.14GHz, SPAN = 53.84MHz, RBW = 30kHz, VBW = 300kHz, SWEEP = 2s

4-CARRIER WCDMA (f_{CLK} = 2.33472Gsps, f_{CENTER} = 2140MHz, SINGLE TRANSFORMER OUTPUT CIRCUIT, RF MODE)

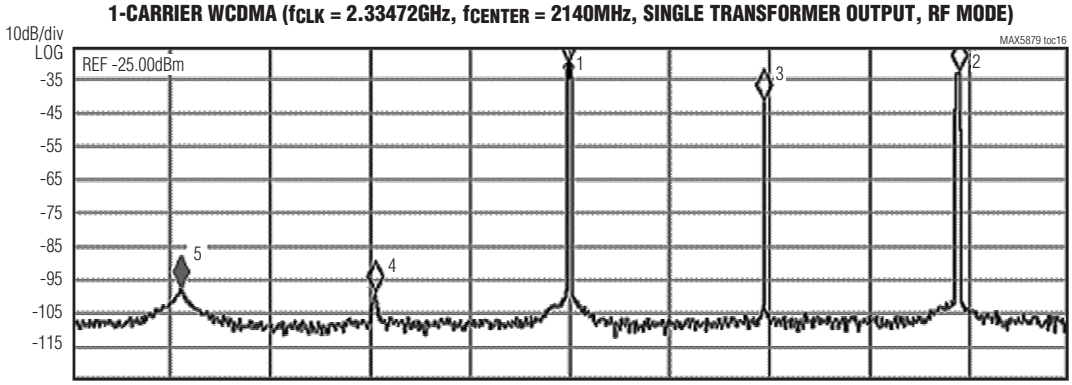


CENTER = 2.14GHz, SPAN = 68.84MHz, RBW = 30kHz, VBW = 300kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

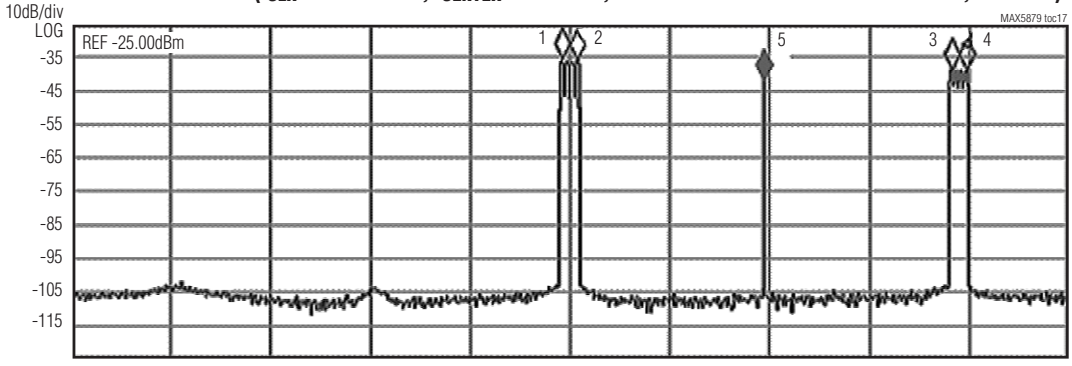
1-CARRIER WCDMA (f_{CLK} = 2.33472GHz, f_{CENTER} = 2140MHz, SINGLE TRANSFORMER OUTPUT, RF MODE)



CENTER = 2.14GHz, SPAN = 1GHz, RBW = 30kHz, VBW = 3kHz, SWEEP = 11.3s (1001pts)

MARKER	SIGNAL	FREQUENCY (GHz)	POWER (dBm)
1	IMAGE, 2ND NYQUIST	2.139	-30.18
2	IMAGE, 3RD NYQUIST	2.530	-33.09
3	CLOCK	2.335	-41.92
4	HD2, 2ND NYQUIST	1.945	-99.12
5	HD3, 2ND NYQUIST	1.751	-97.63

4-CARRIER WCDMA (f_{CLK} = 2.33472GHz, f_{CENTER} = 2140MHz, SINGLE TRANSFORMER OUTPUT CIRCUIT, RF MODE)



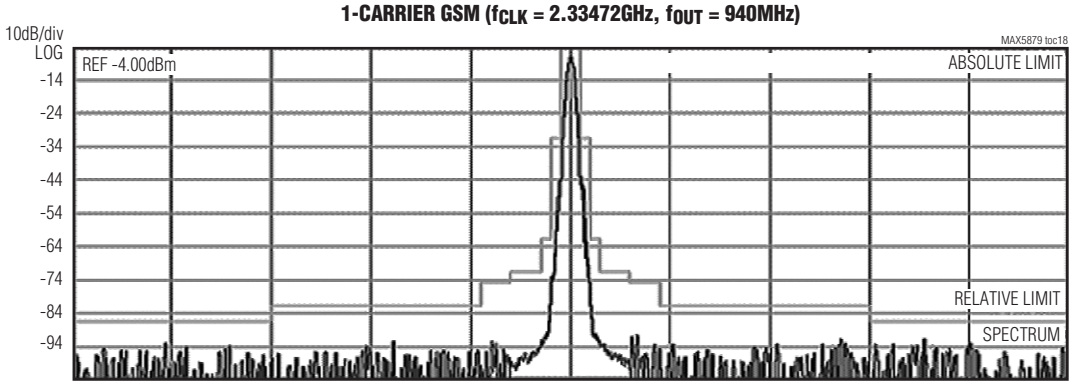
CENTER = 2.14GHz, SPAN = 1GHz, RBW = 30kHz, VBW = 3kHz, SWEEP = 11.3s (1001pts)

MARKER	SIGNAL	FREQUENCY (GHz)	POWER (dBm)
1	CH 4 IMAGE, 2ND NYQUIST	2.132	-36.25
2	CH 1 IMAGE, 2ND NYQUIST	2.148	-36.51
3	CH 1 IMAGE, 3RD NYQUIST	2.523	-39.20
4	CH 4 IMAGE, 3RD NYQUIST	2.538	-39.14
5	CLOCK	2.335	-42.43

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

1-CARRIER GSM (f_{CLK} = 2.33472GHz, f_{OUT} = 940MHz)

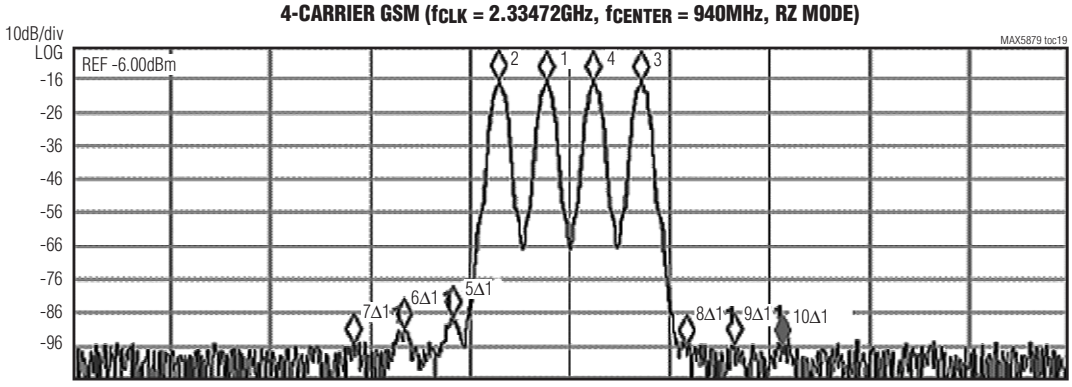


CENTER = 940.5MHz, SPAN = 20MHz

TOTAL POWER REF -1.66dBm/0.4MHz

START FREQ	STOP FREQ	INTEG BW	dBc	LOWER ΔLIM(dB)	<- PEAK -> FREQ (Hz)	dBc	UPPER ΔLIM(dB)	FREQ (Hz)
200.0kHz	400.0kHz	30.00kHz	-42.53	(-12.53)	-200.0k	-41.41	(-11.41)	202.0k
400.0kHz	600.0kHz	30.00kHz	-79.86	(-19.86)	-400.0k	-77.46	(-17.46)	400.0k
600.0kHz	1.200MHz	30.00kHz	-92.37	(-22.37)	-610.0k	-91.74	(-21.74)	690.0k
1.200MHz	1.800MHz	30.00kHz	-90.85	(-17.85)	-1.570M	-89.03	(-16.03)	1.330M
1.800MHz	6.000MHz	30.00kHz	-90.77	(-10.77)	-3.550M	-90.29	(-10.29)	5.410M
6.000MHz	10.00MHz	30.00kHz	-91.65	(-6.65)	-8.120M	-90.37	(-5.37)	7.090M

4-CARRIER GSM (f_{CLK} = 2.33472GHz, f_{CENTER} = 940MHz, RZ MODE)



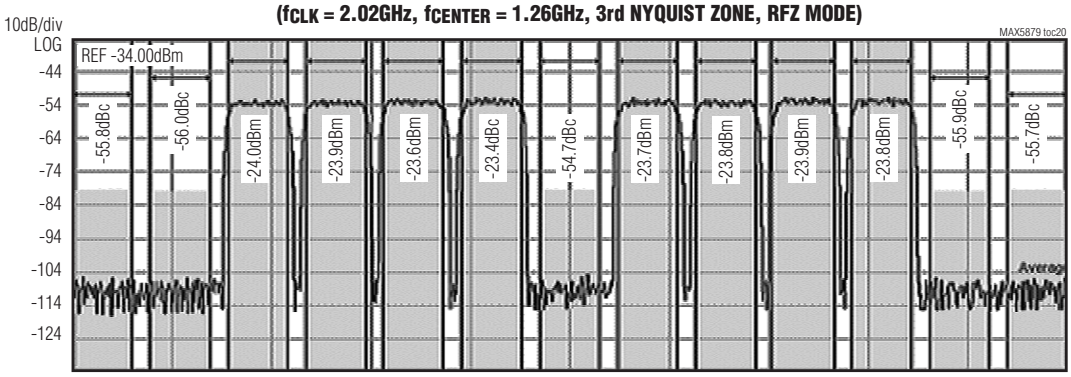
CENTER = 940.450MHz, SPAN = 12MHz, RBW = 30kHz, VBW = 3kHz, SWEEP = 2s (1001pts)

MARKER	POWER	MARKER	POWER
1	-17.36dBm	6	(Δ) -74.11dB
2	-17.20dBm	7	(Δ) -78.54dB
3	-17.43dBm	8	(Δ) -79.01dB
4	-17.32dBm	9	(Δ) -78.73dB
5	(Δ) -70.48dB	10	(Δ) -78.75dB

Typical Operating Characteristics (continued)

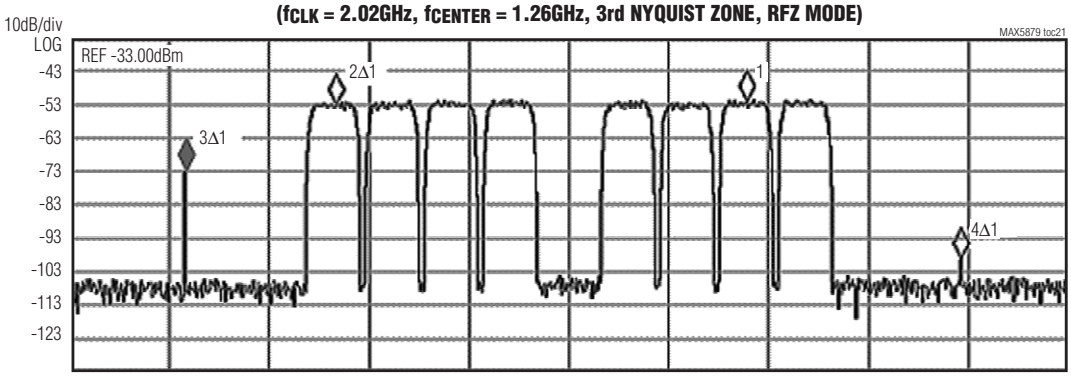
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

8-CARRIER 8 PSK, 28.86MBd, 38.36MHz SPACING
(f_{CLK} = 2.02GHz, f_{CENTER} = 1.26GHz, 3rd NYQUIST ZONE, RFZ MODE)



CENTER = 1.26GHz, SPAN = 489.2MHz, RBW = 30kHz, VBW = 3kHz, SWEEP = 2s

8-CARRIER 8 PSK, 28.86MBd, 38.36MHz SPACING
(f_{CLK} = 2.02GHz, f_{CENTER} = 1.26GHz, 3rd NYQUIST ZONE, RFZ MODE)



CENTER = 1.2598GHz, SPAN = 650MHz, RBW = 30kHz, VBW = 3kHz, SWEEP = 2s (1001pts)

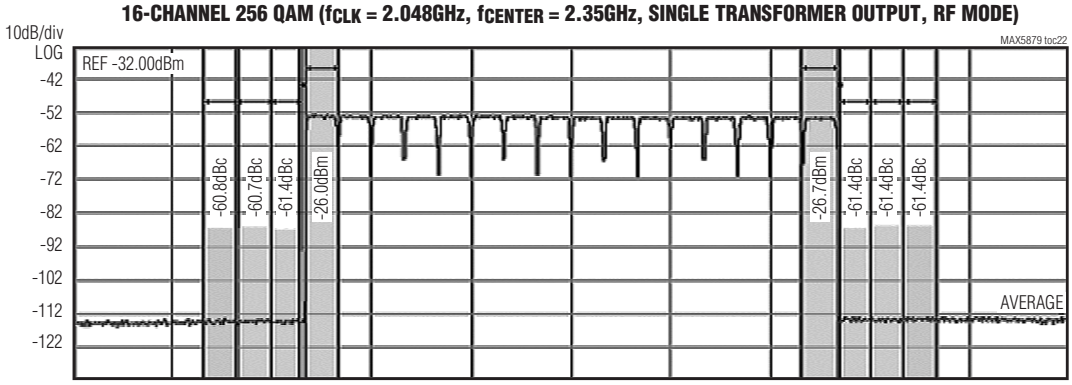
MARKER	FREQUENCY	POWER
1	1.3758GHz	-52.53dBm
2	(Δ) -267.0MHz	(Δ) -1.01dB
3	(Δ) -365.4MHz	(Δ) -20.68dB
4	(Δ) 139.7MHz	(Δ) -46.92dB

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

Typical Operating Characteristics (continued)

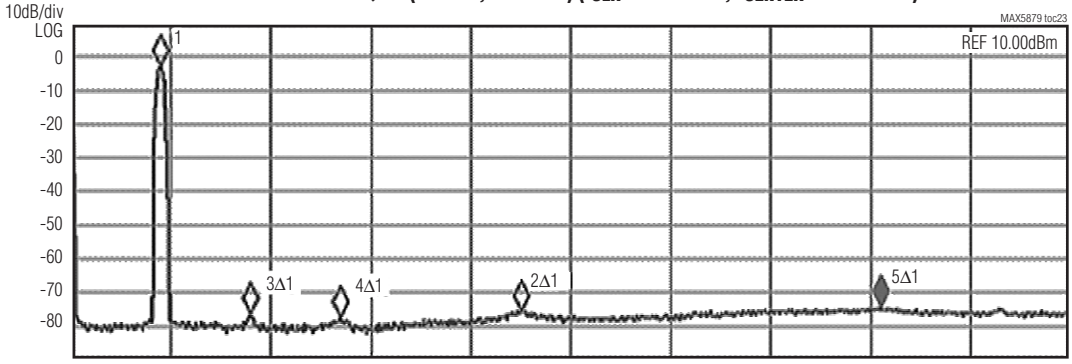
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

16-CHANNEL 256 QAM (f_{CLK} = 2.048GHz, f_{CENTER} = 2.35GHz, SINGLE TRANSFORMER OUTPUT, RF MODE)



CENTER = 2.348GHz, SPAN = 180MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 44.69s

1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 98.99MHz)



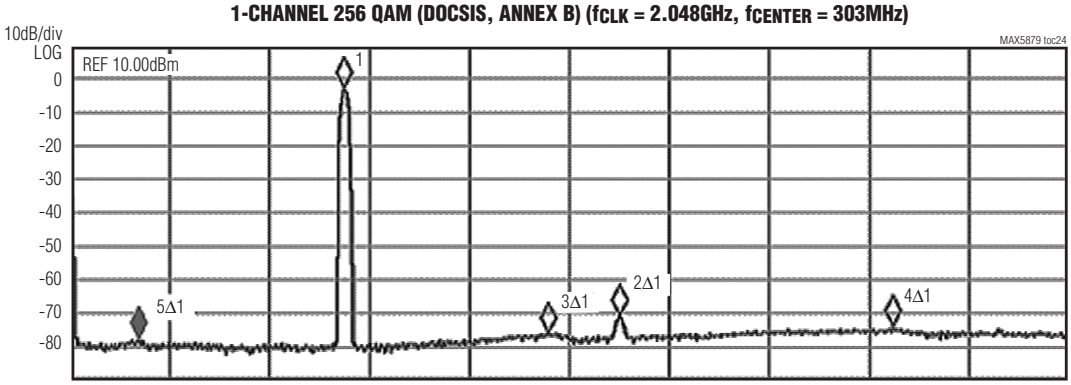
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	99.0	-3.23dBm
2	HD5	(Δ) 397.1	(Δ) -72.78dB
3	HD2	(Δ) 99.0	(Δ) -73.63dB
4	HD3	(Δ) 198.0	(Δ) -74.49dB
5	HD9	(Δ) 198.0	(Δ) -71.35dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

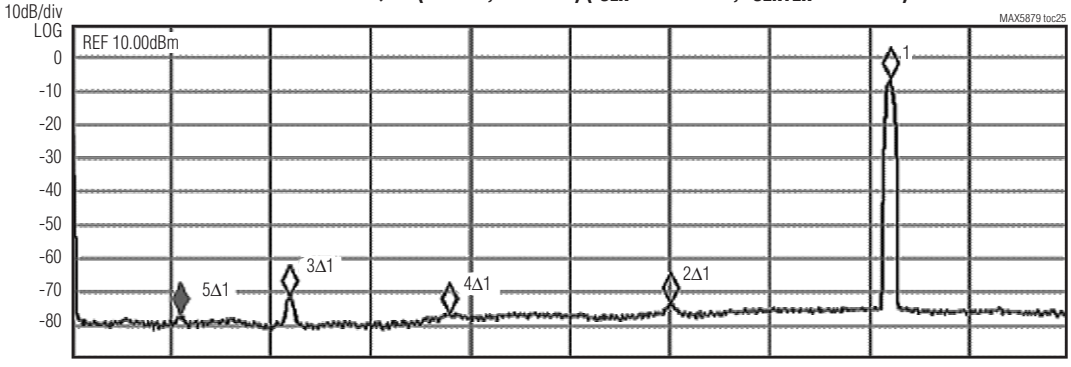
1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 303MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	302.5	-3.31dBm
2	HD2	(Δ) 303.6	(Δ) -67.77dB
3	HD5	(Δ) 224.4	(Δ) -72.92dB
4	HD3	(Δ) 603.9	(Δ) -71.11dB
5	HD7	(Δ) -226.6	(Δ) -74.63dB

1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 903MHz)



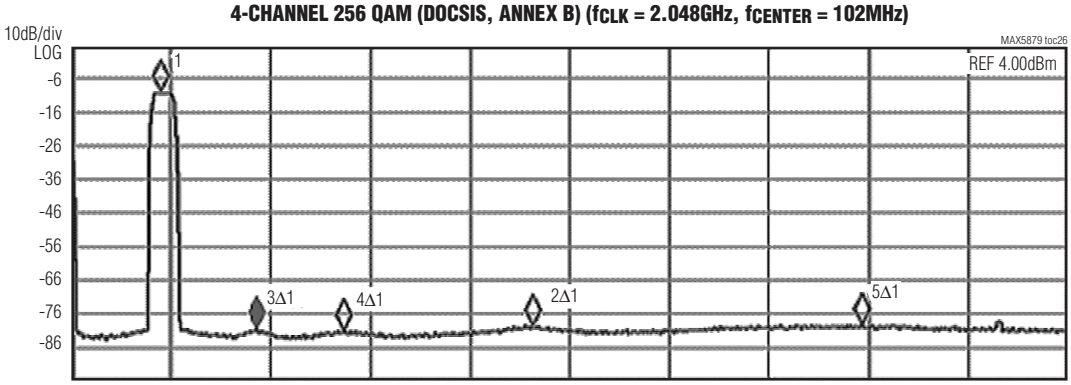
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	903.1	-6.93dBm
2	HD3	(Δ) -242.0	(Δ) -66.97dB
3	HD2	(Δ) -662.2	(Δ) -64.91dB
4	HD5	(Δ) -486.2	(Δ) -70.08dB
5		(Δ) -782.1	(Δ) -70.21dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

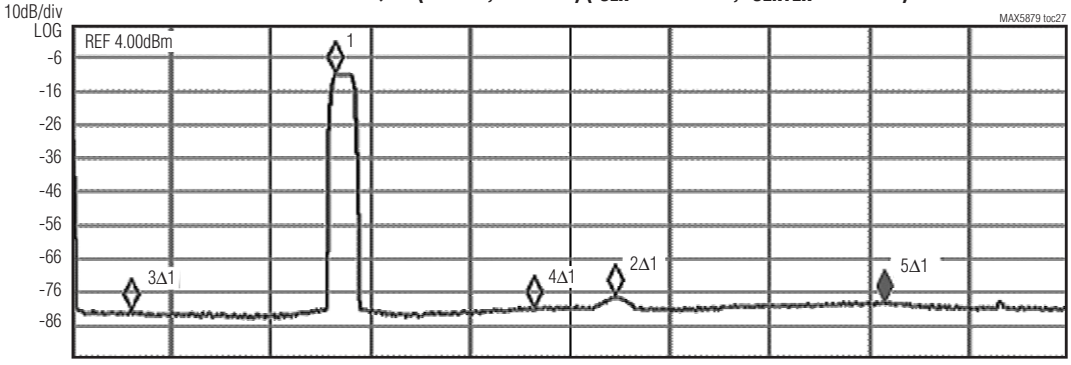
4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	99.0	-10.43dBm
2	HD5	(Δ) 410.3	(Δ) -69.56dB
3	HD2	(Δ) 105.6	(Δ) -70.14dB
4	HD3	(Δ) 202.4	(Δ) -70.93dB
5	HD9	(Δ) 773.3	(Δ) -69.10dB

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz)



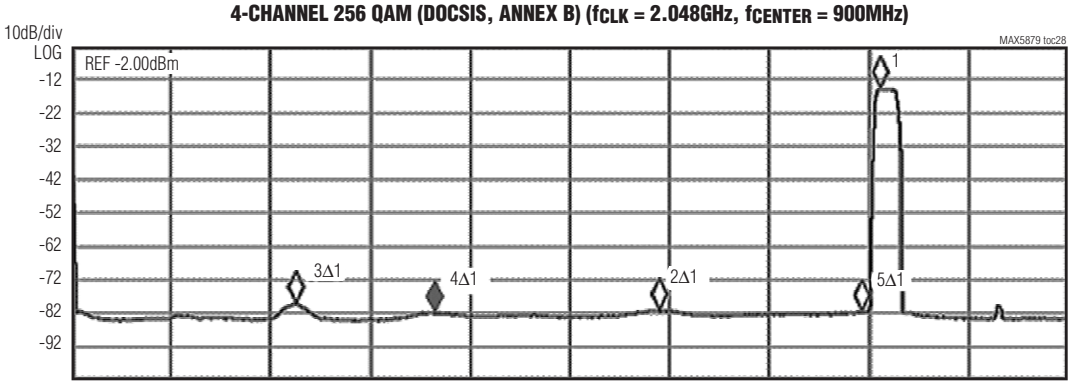
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	291.5	-11.11dBm
2	HD2	(Δ) 308.0	(Δ) -66.47dB
3		(Δ) -225.5	(Δ) -70.45dB
4		(Δ) 218.9	(Δ) -70.00dB
5		(Δ) 605	(Δ) -68.09dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

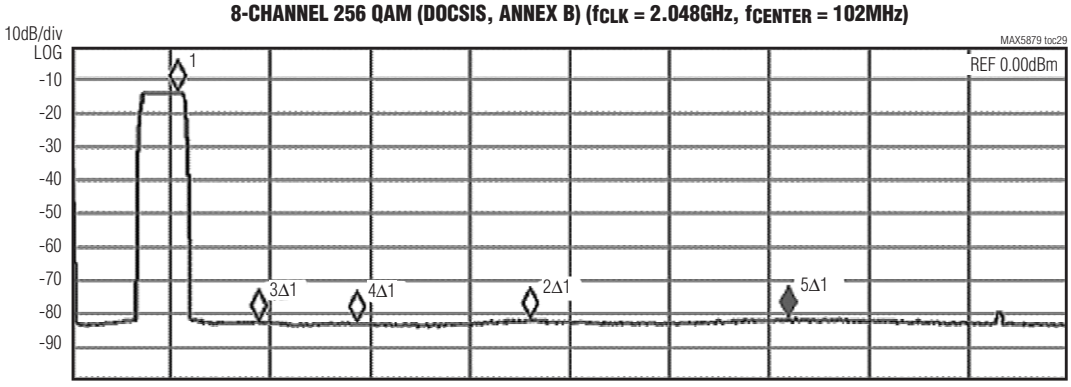
4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	892.1	-14.99dBm
2		(Δ) -243.1	(Δ) -66.47dB
3	HD2	(Δ) -644.6	(Δ) -64.13dB
4		(Δ) -491.7	(Δ) -67.08dB
5		(Δ) -19.8	(Δ) -66.78dB

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz)



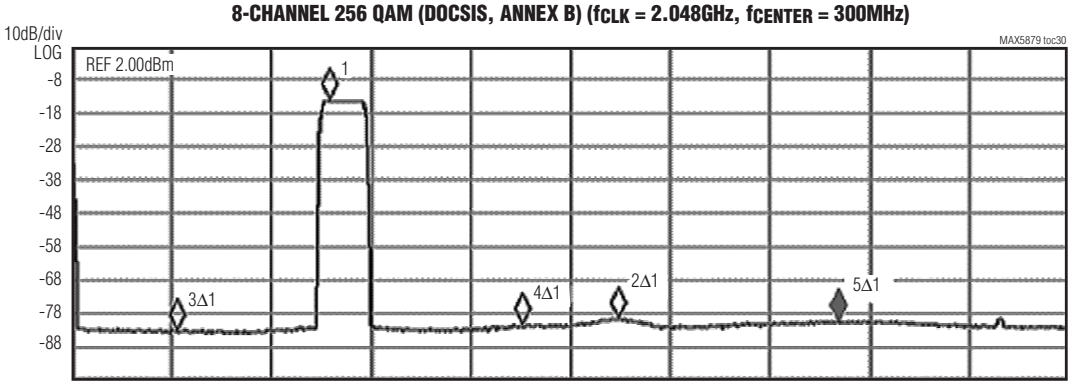
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	117.7	-14.04dBm
2	HD5	(Δ) 389.4	(Δ) -67.86dB
3	HD2	(Δ) 90.2	(Δ) -68.59dB
4		(Δ) 198.0	(Δ) -68.95dB
5		(Δ) 673.2	(Δ) -67.58dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

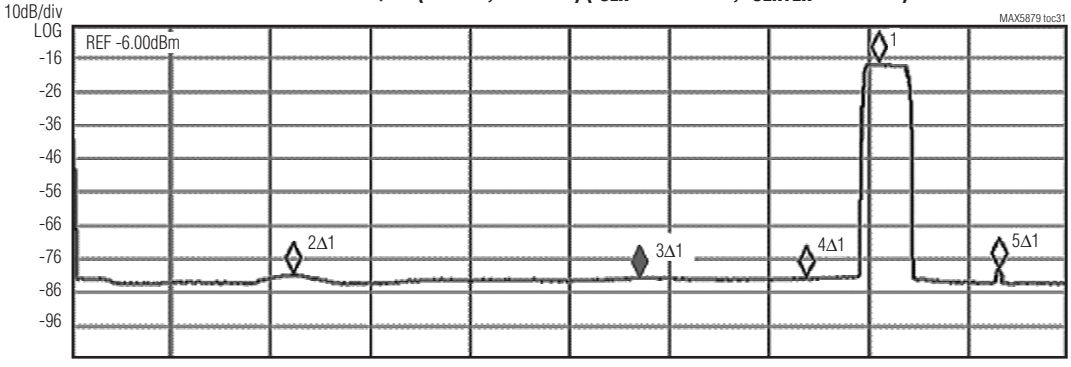
8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	284.9	-14.41dBm
2	HD2	(Δ) 317.9	(Δ) -65.28dB
3		(Δ) -168.3	(Δ) -68.82dB
4		(Δ) 212.3	(Δ) -67.31dB
5	HD3	(Δ) 559.9	(Δ) -66.06dB

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz)



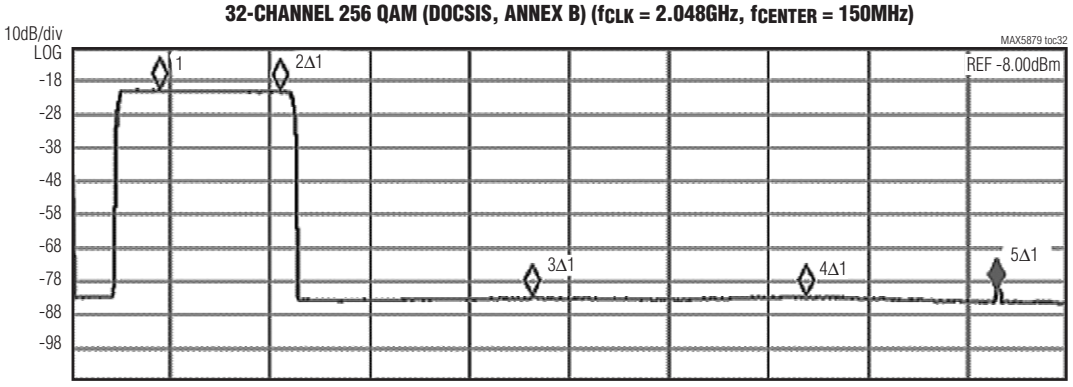
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	891.0	-17.98dBm
2	HD2	(Δ) -654.7	(Δ) -62.80dB
3		(Δ) -264.0	(Δ) -63.69dB
4		(Δ) -79.2	(Δ) -63.80dB
5	f_{CLK}/2	(Δ) 133.1	(Δ) -61.40dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

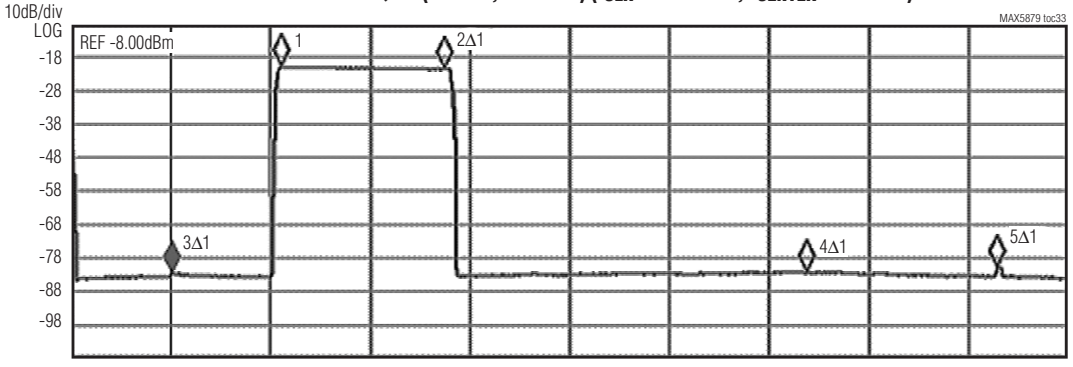
32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 150MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	100.0	-20.87dBm
2	f_{OUT}	(Δ) 132.0	(Δ) -0.21dB
3		(Δ) 410.3	(Δ) -62.01dB
4		(Δ) 712.8	(Δ) -62.00dB
5	f_{CLK}/2	(Δ) 922.9	(Δ) -59.98dB

32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 324MHz)



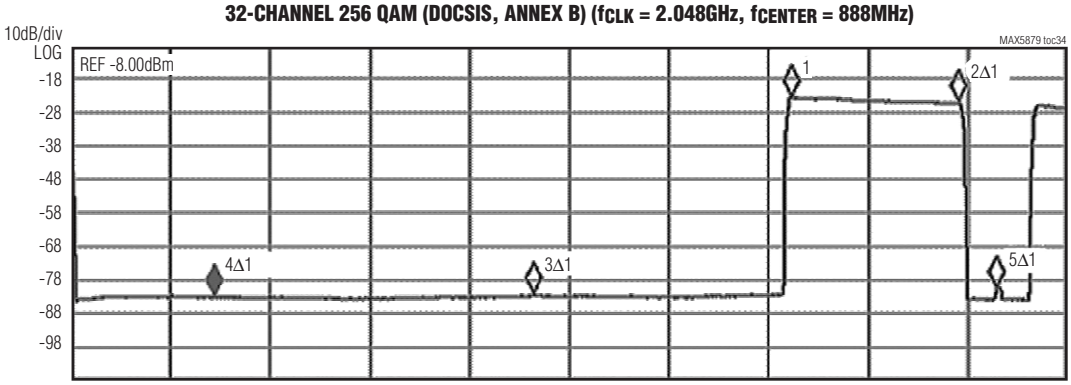
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	232.1	-20.93dBm
2	f_{OUT}	(Δ) 179.3	(Δ) -0.52dB
3		(Δ) -121.0	(Δ) -61.92dB
4		(Δ) 579.7	(Δ) -61.46dB
5	f_{CLK}/2	(Δ) 789.8	(Δ) -60.18dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

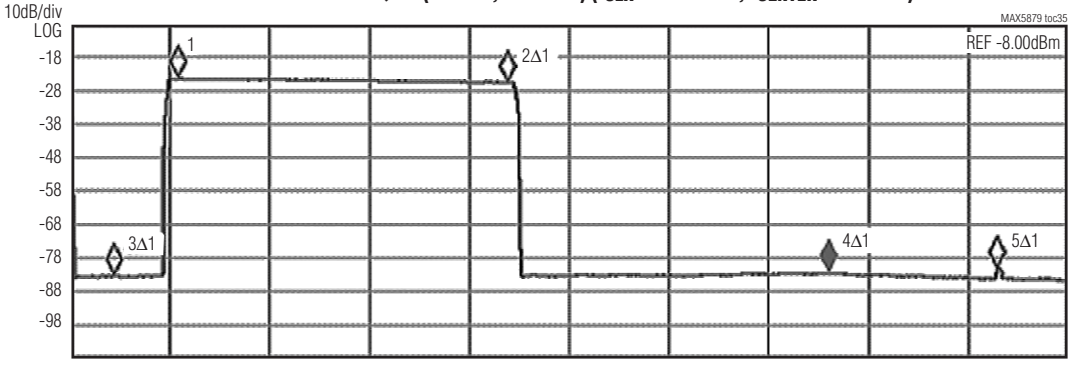
32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 888MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	795.3	-23.65dBm
2	f_{OUT}	(Δ) 183.7	(Δ) -1.65dB
3		(Δ) -284.9	(Δ) -58.79dB
4		(Δ) -636.9	(Δ) -59.45dB
5	f_{CLK}/2	(Δ) 226.6	(Δ) -56.82dB

64-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz)



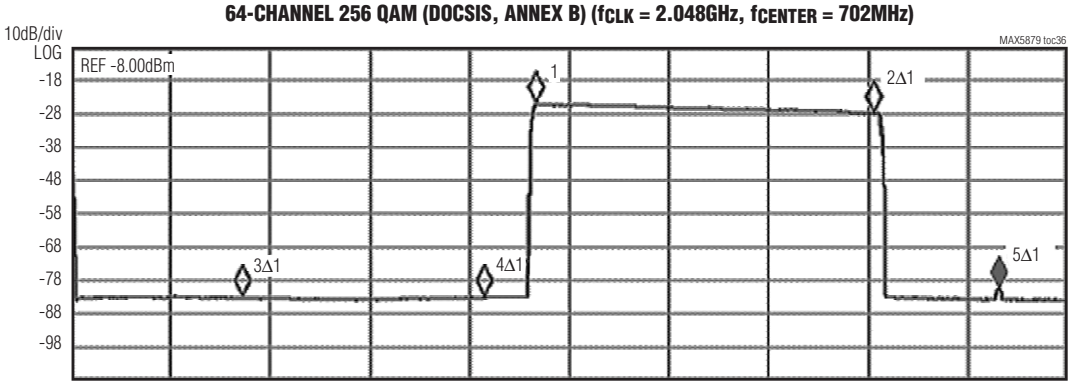
CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	118.8	-24.49dBm
2	f_{OUT}	(Δ) 363.0	(Δ) -1.18dB
3		(Δ) -70.4	(Δ) -58.93dB
4		(Δ) 717.2	(Δ) -58.07dB
5	f_{CLK}/2	(Δ) 903.1	(Δ) -56.87dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode,**R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

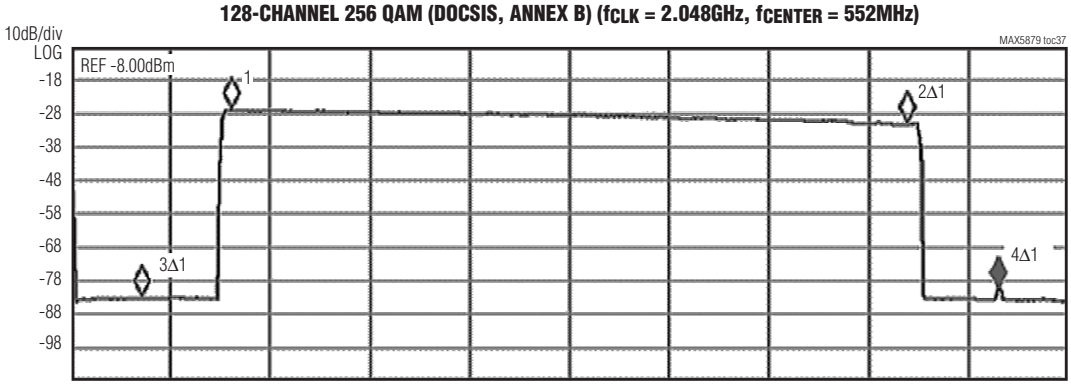
64-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 702MHz)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	513.7	-25.17dBm
2	f_{OUT}	(Δ) 372.9	(Δ) -2.77dB
3		(Δ) -324.5	(Δ) -58.06dB
4		(Δ) -57.2	(Δ) -57.84dB
5	f_{CLK}/2	(Δ) 510.4	(Δ) -55.40dB

128-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 552MHz)



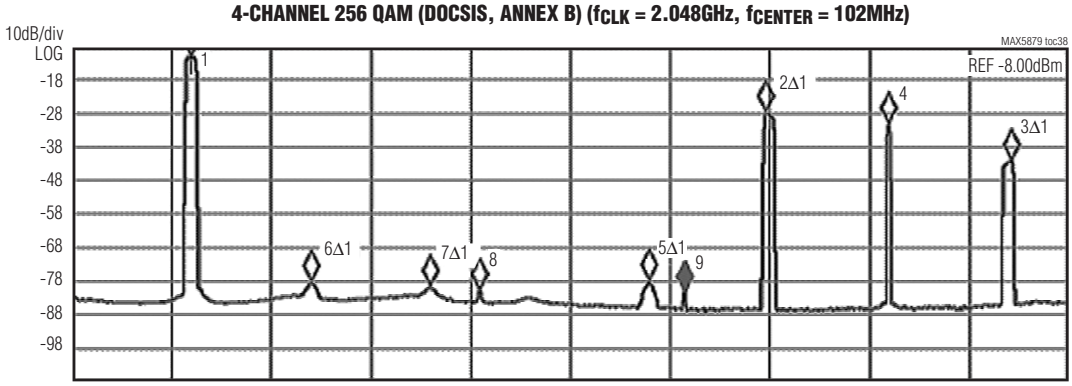
CENTER = 550GHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	177.1	-26.9dBm
2	f_{OUT}	(Δ) 745.8	(Δ) -4.40dB
3		(Δ) -97.9	(Δ) -56.35dB
4	f_{CLK}/2	(Δ) 845.9	(Δ) -53.78dB

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz)



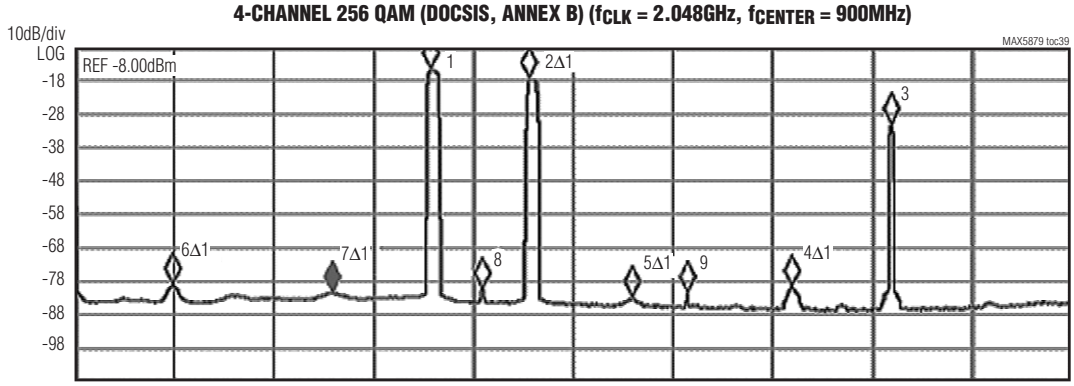
CENTER = 1.25GHz, SPAN = 2.5GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY	POWER
1	f_{OUT}	297.5MHz	-11.19dBm
2	IMAGE, 2ND NYQUIST	(Δ) 1.4425GHz	(Δ) -16.93dB
3	IMAGE, 3RD NYQUIST	(Δ) 2.0575GHz	(Δ) -31.13dB
4	f_{CLK}	2.0475GHz	-31.62dBm
5		(Δ) 1.1491GHz	(Δ) -67.03dB
6		(Δ) 302.5GHz	(Δ) -67.35dB
7		(Δ) 602.5GHz	(Δ) -68.88dB
8	f_{CLK}/2	1.0225GHz	-80.99dBm
9	3 x f_{CLK}/2	1.5350GHz	-81.51dBm

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz)



CENTER = 1.25GHz, SPAN = 2.5GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

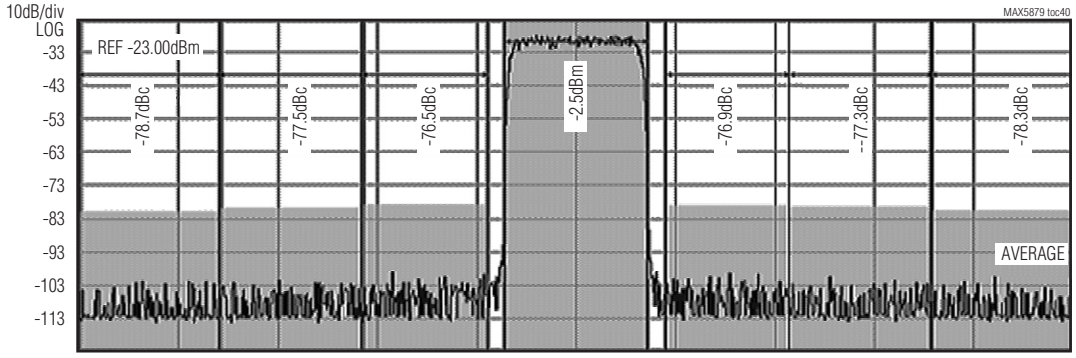
MARKER	SIGNAL	FREQUENCY	POWER
1	f_{OUT}	892.5MHz	-11.19dBm
2	IMAGE, 2ND NYQUIST	(Δ) 247.5MHz	(Δ) -2.72dB
3	f_{CLK}	2.0475GHz	-31.56dBm
4		(Δ) 905.0MHz	(Δ) -64.83dB
5		(Δ) 506.6MHz	(Δ) -68.15dB
6		(Δ) -647.5MHz	(Δ) -64.24dB
7		(Δ) -245.0MHz	(Δ) -66.59dB
8	$f_{CLK}/2$	1.0225GHz	-80.47dBm
9	3 x $f_{CLK}/2$	1.5350GHz	-81.71dBm

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

Typical Operating Characteristics (continued)

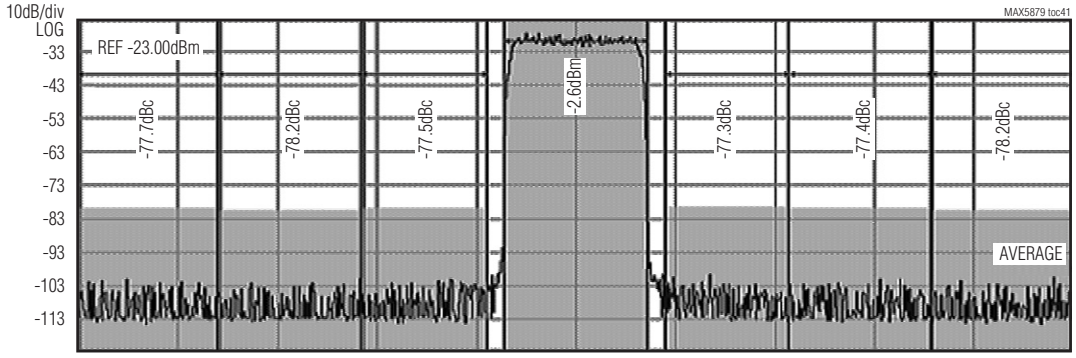
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 98.99MHz)



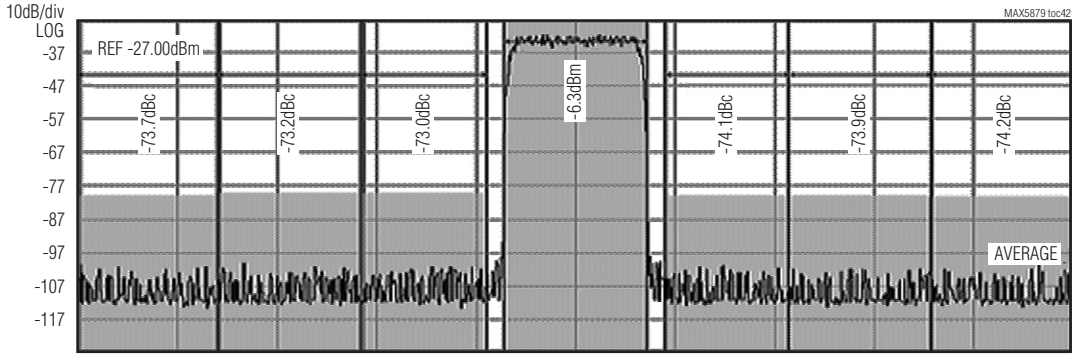
CENTER = 99MHz, SPAN = 42MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 303MHz)



CENTER = 303MHz, SPAN = 42MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

1-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 903MHz)

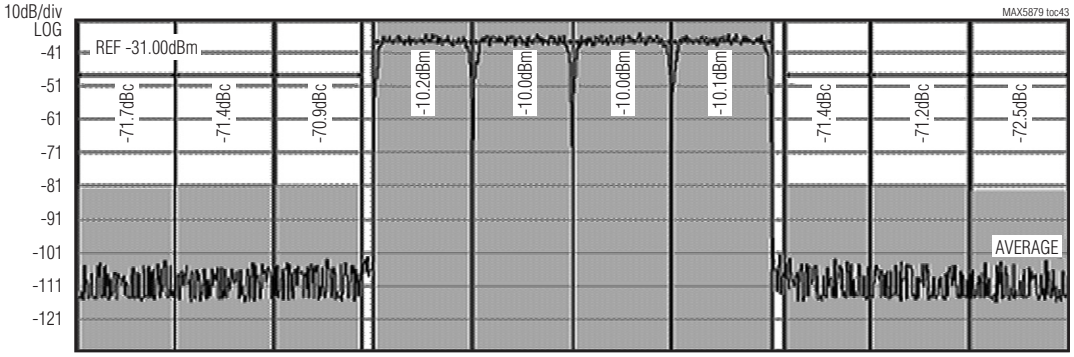


CENTER = 903MHz, SPAN = 42MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

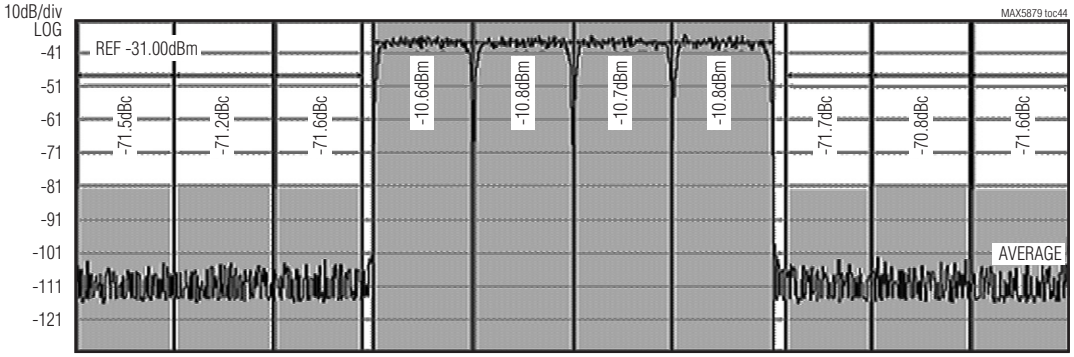
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz)



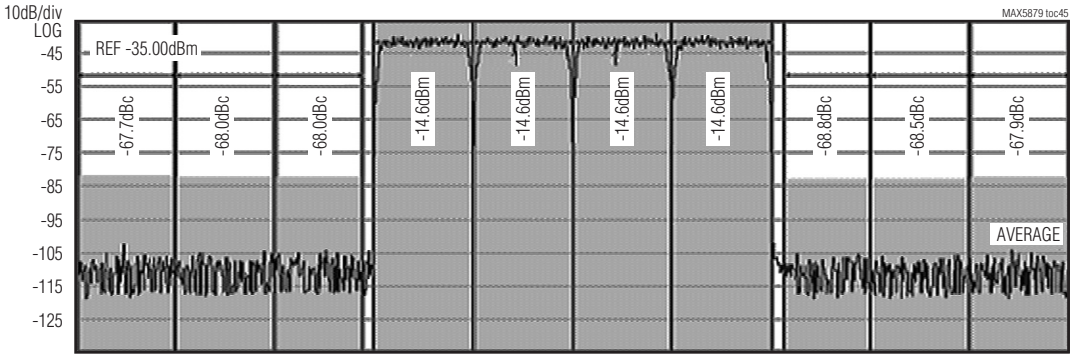
CENTER = 102MHz, SPAN = 60MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz)



CENTER = 300MHz, SPAN = 60MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

4-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz)

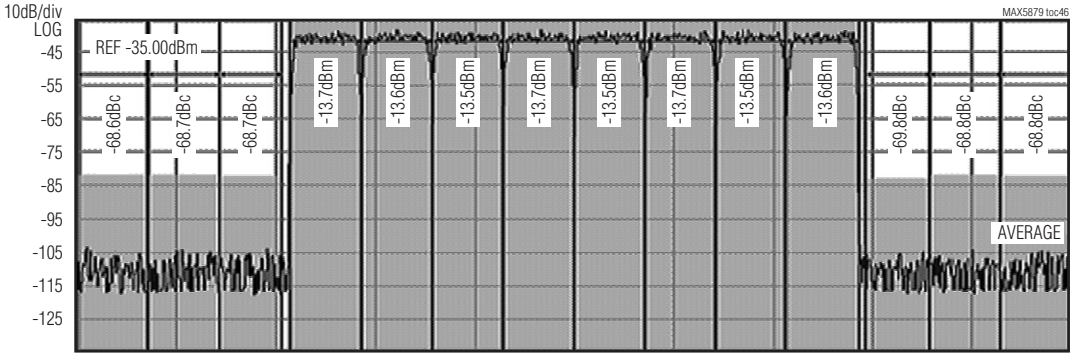


CENTER = 900MHz, SPAN = 60MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

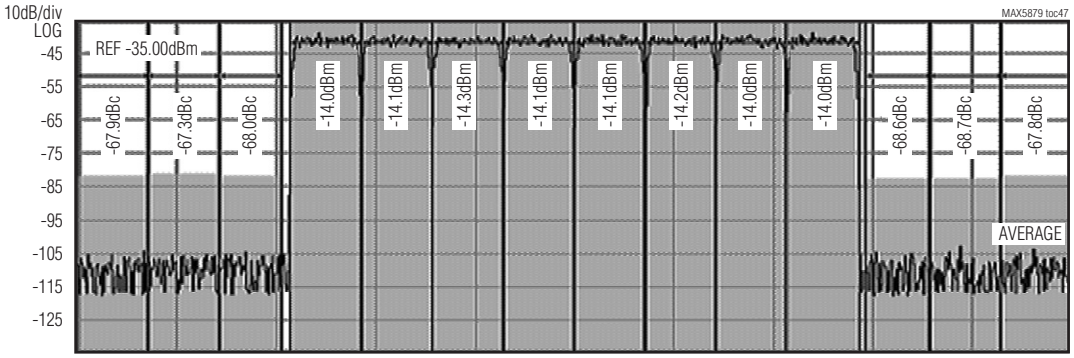
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz)



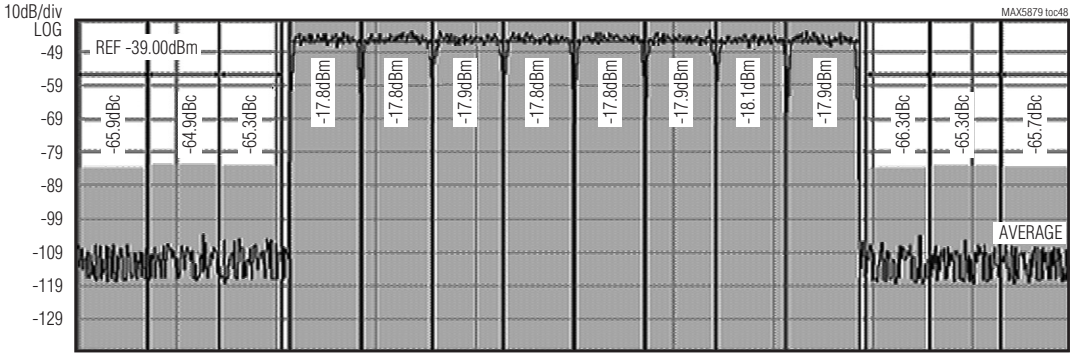
CENTER = 102MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz)



CENTER = 300MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz)



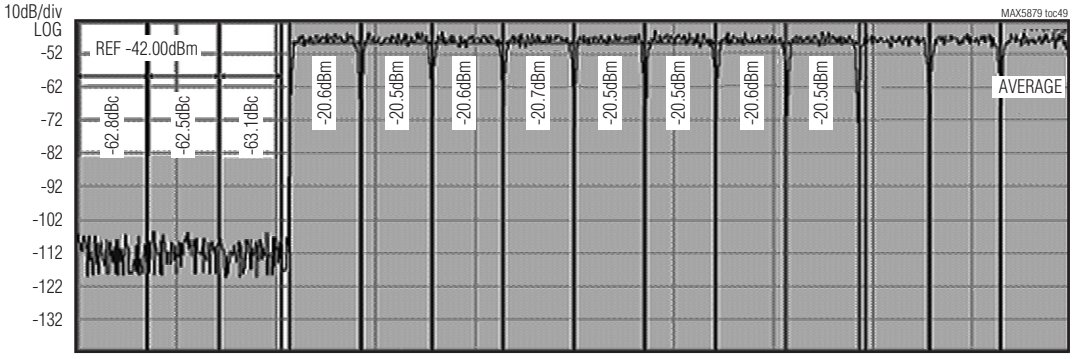
CENTER = 900MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

Typical Operating Characteristics (continued)

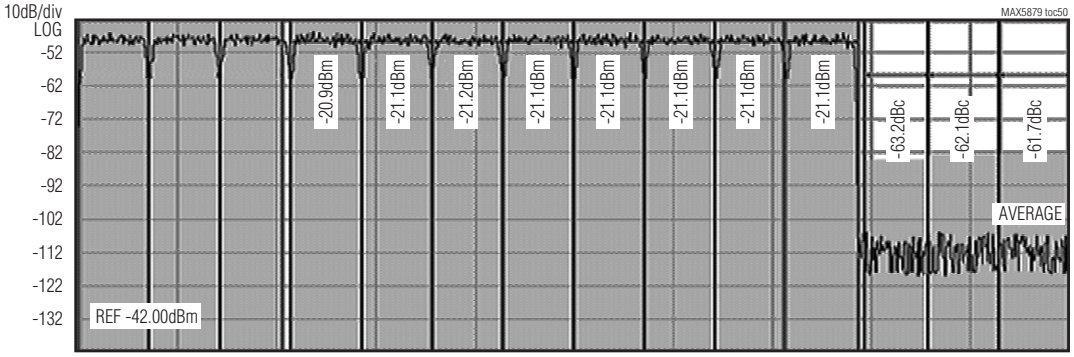
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 150MHz, WORST-CASE SIDE)



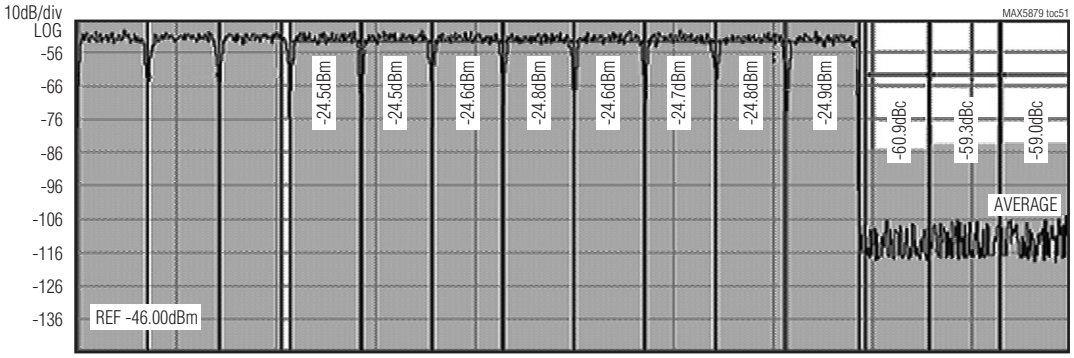
CENTER = 78MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 324MHz, WORST-CASE SIDE)



CENTER = 396MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

32-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 888MHz, WORST-CASE SIDE)

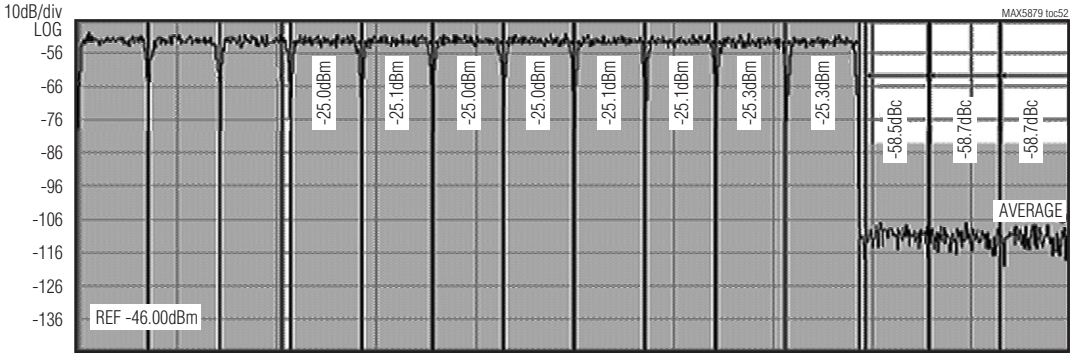


CENTER = 960MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

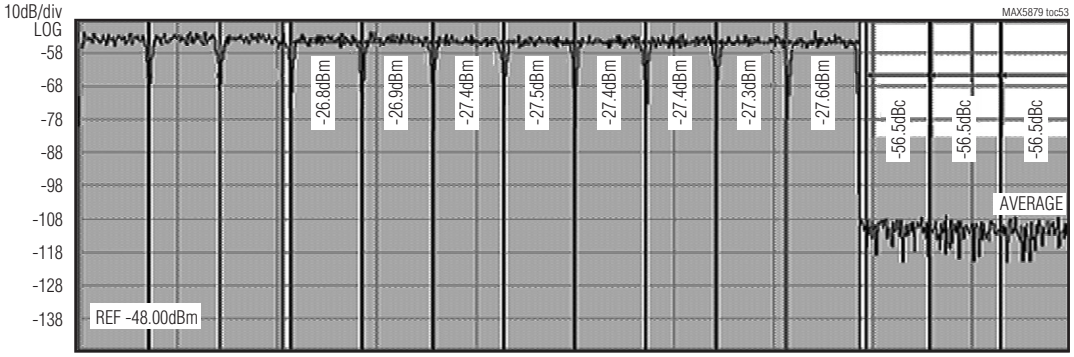
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

64-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz, WORST-CASE SIDE)



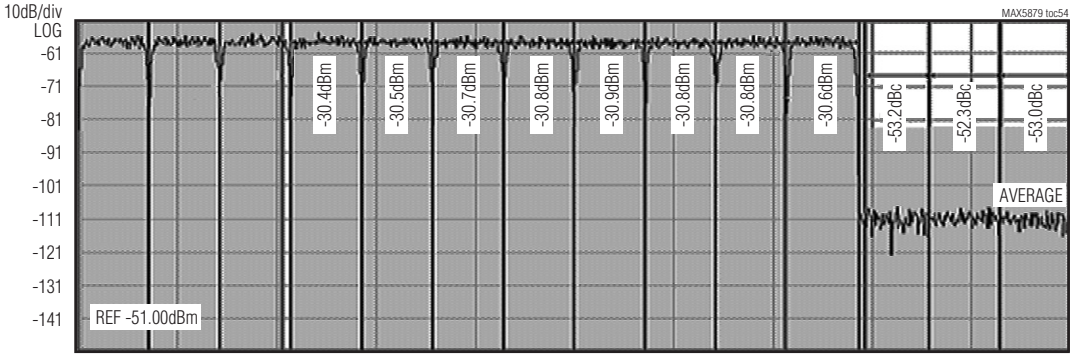
CENTER = 468MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

64-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 702MHz, WORST-CASE SIDE)



CENTER = 870MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

128-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 150MHz, WORST-CASE SIDE)

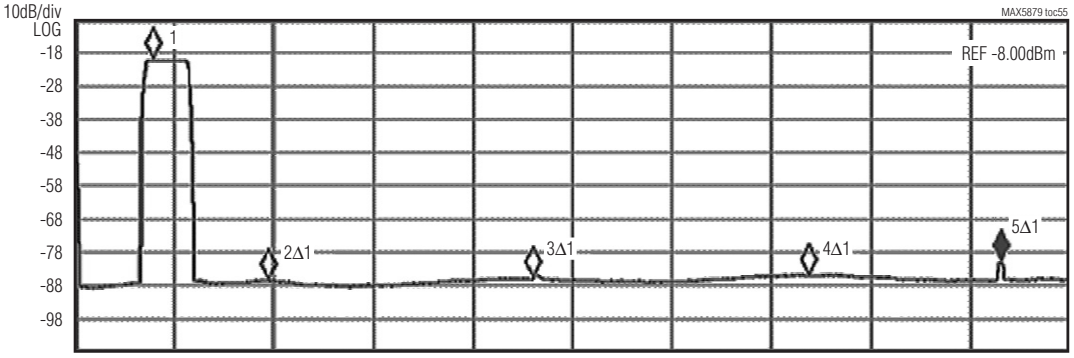


CENTER = 912MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 4kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 1kΩ**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

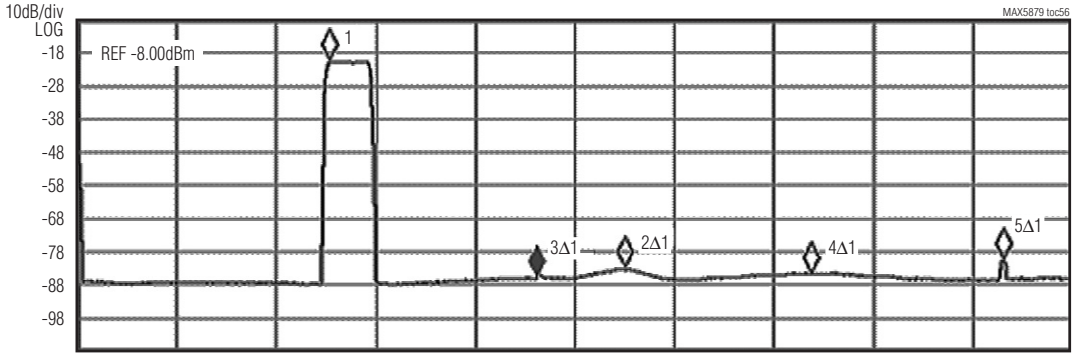
8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	86.9	-20.21dBm
2		(Δ) 126.5	(Δ) -66.33dB
3		(Δ) 420.2	(Δ) -65.75dB
4		(Δ) 724.9	(Δ) -64.88dB
5	f_{CLK}/2	(Δ) 937.2	(Δ) -60.82dB

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

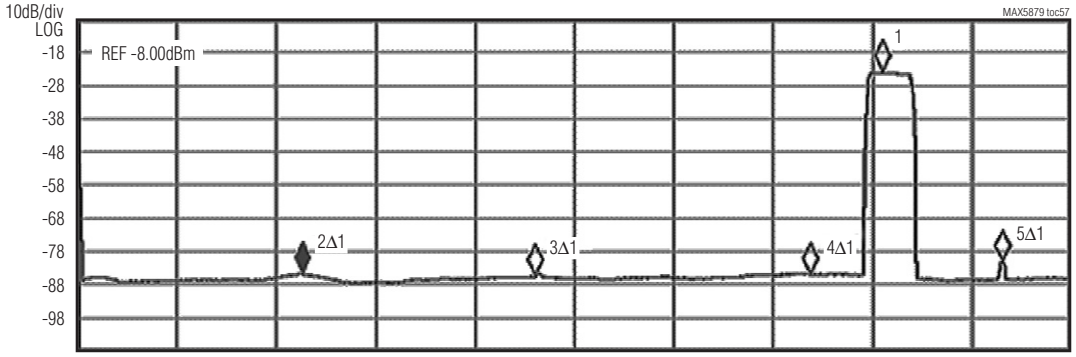
MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	279.6	-20.59dBm
2		(Δ) 325.6	(Δ) -62.61dB
3		(Δ) 228.8	(Δ) -65.38dB
4		(Δ) 532.4	(Δ) -64.16dB
5	f_{CLK}/2	(Δ) 744.7	(Δ) -60.16dB

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 4kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 1kΩ**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

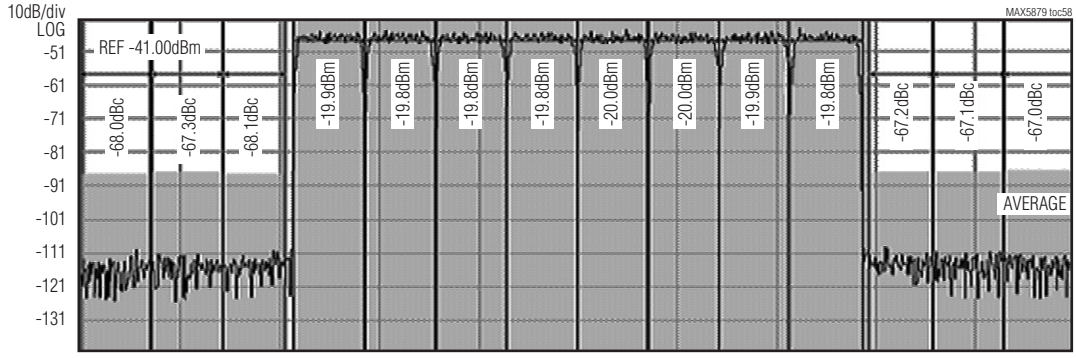
8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)



CENTER = 550MHz, SPAN = 1.1GHz, RBW = 6MHz, VBW = 620kHz, SWEEP = 2s (1001pts)

MARKER	SIGNAL	FREQUENCY (MHz)	POWER
1	f_{OUT}	891.0	-24.04dBm
2		(Δ) -641.3	(Δ) -60.82dB
3		(Δ) -383.9	(Δ) -61.55dB
4		(Δ) -79.2	(Δ) -61.01dB
5	f_{CLK}/2	(Δ) 133.1	(Δ) -57.11dB

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 102MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)

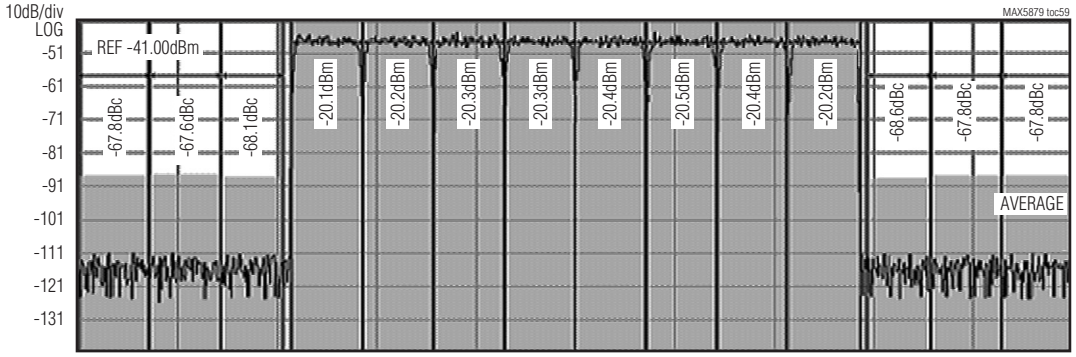


CENTER = 102MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

Typical Operating Characteristics (continued)

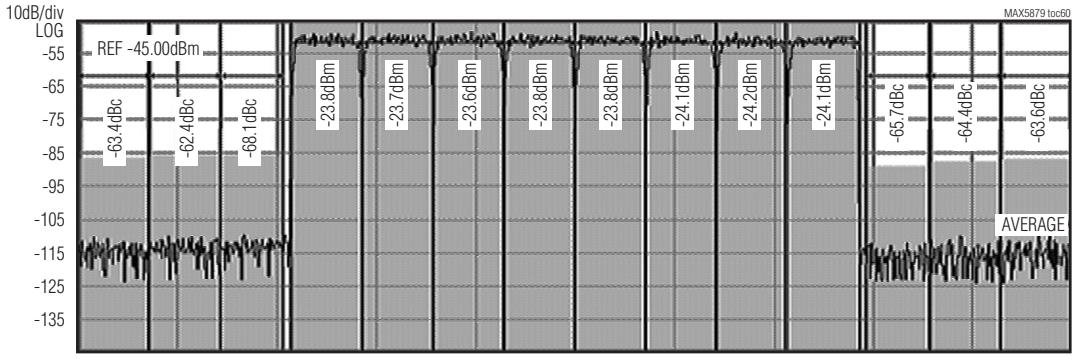
($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 4kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 1kΩ**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 300MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)



CENTER = 300MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

8-CHANNEL 256 QAM (DOCSIS, ANNEX B) (f_{CLK} = 2.048GHz, f_{CENTER} = 900MHz, $I_{FULL-SCALE}$ = 40mA, I_{CONST} = 20mA)



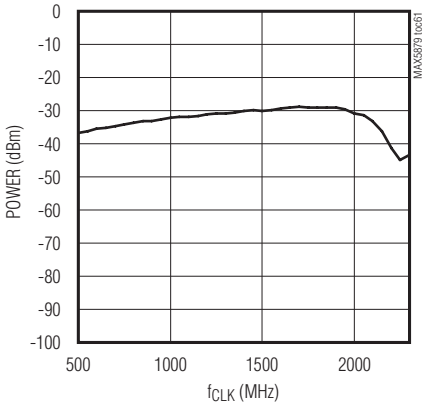
CENTER = 900MHz, SPAN = 84MHz, RBW = 10kHz, VBW = 1kHz, SWEEP = 2s

14-Bit, 2.3Gsps Direct RF Synthesis DAC with Selectable Frequency Response

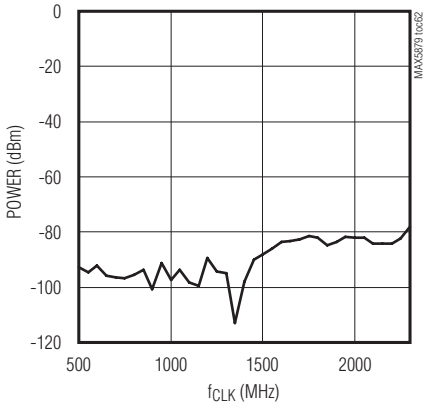
Typical Operating Characteristics (continued)

($V_{AVDD3.3}$ = 3.3V, $V_{DD1.8}$ = V_{AVCLK} = 1.8V, **R_{SET} = 2kΩ**, V_{REFIO} = external 1.25V, V_{DELAY} = $V_{DCLKDIV}$ = 1.8V, V_{DLLOFF} = V_{SE} = 0V, 2:1 mux mode, NRZ mode, **R_{REFRES} = 500Ω**, transformer-coupled differential output, T_A = +25°C, device soldered to the MAX5879 EV kit, unless otherwise noted.)

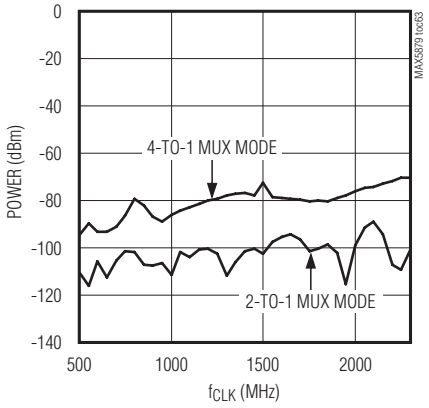
CLOCK FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



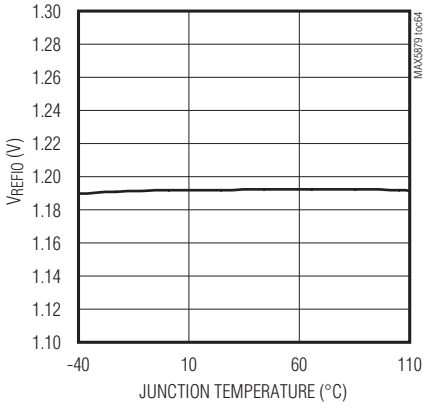
CLOCK/2 FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



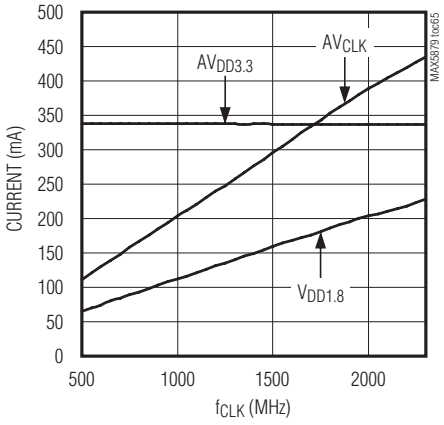
CLOCK/4 FEEDTHROUGH vs. CLOCK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS)



INTERNAL REFERENCE (REFIO) VOLTAGE vs. JUNCTION TEMPERATURE



SUPPLY CURRENT vs. CLK FREQUENCY (f_{OUT} = 100MHz, A_{OUT} = -0.1dBFS, $I_{FULL-SCALE}$ = 80mA)



Ball Configurations

Ball Assignments (DAC Outputs, Power Supplies, Reference, and DAC Clock)

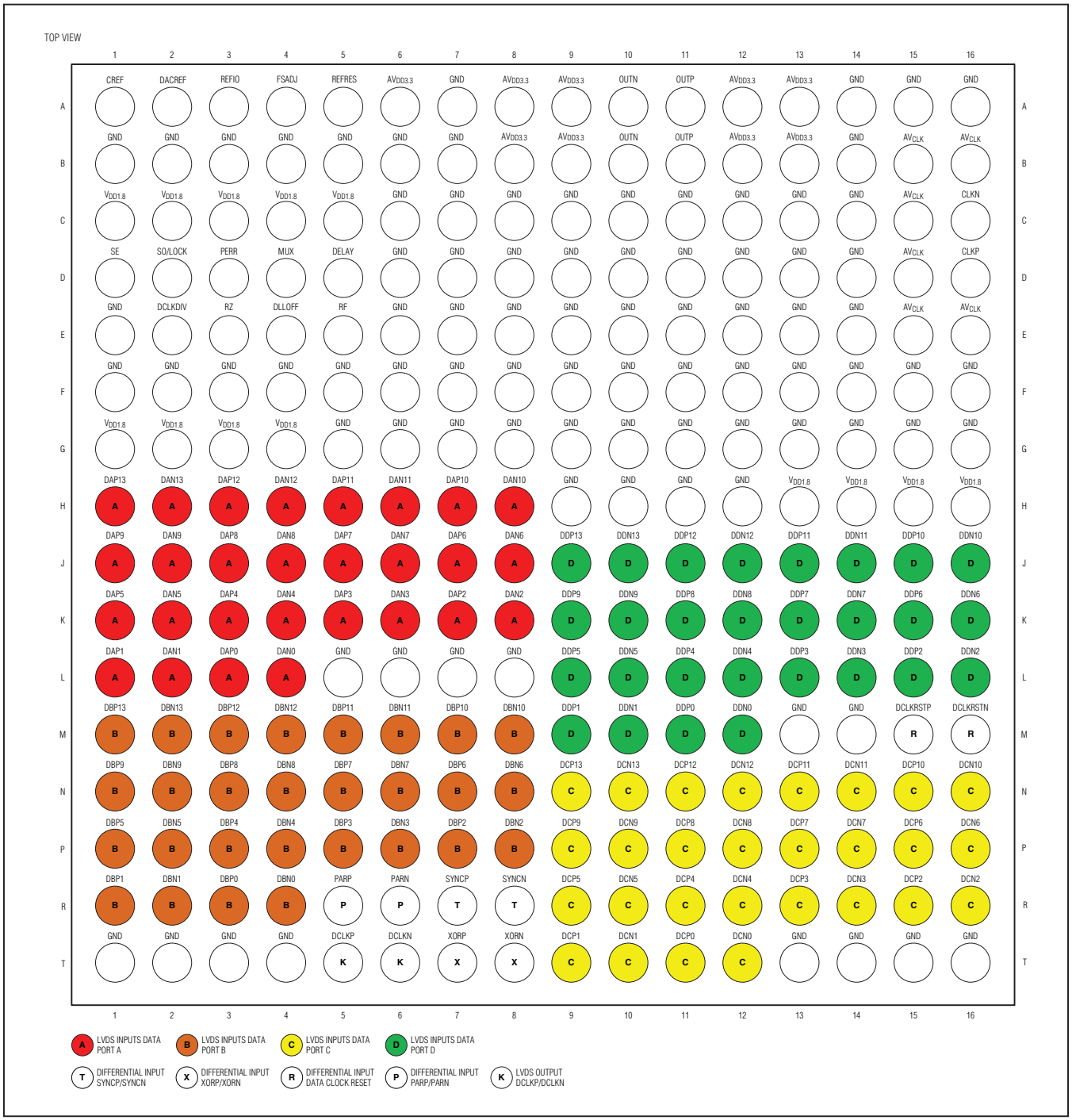
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	CREF R	DACREF R	REFIO R	FSADJ R	REFRES R	$AV_{DD3.3}$ A	GND G	$AV_{DD3.3}$ A	$AV_{DD3.3}$ A	OUTN I	OUTP I	$AV_{DD3.3}$ A	$AV_{DD3.3}$ A	GND G	GND G	GND G
B	GND G	GND G	GND G	GND G	GND G	GND G	GND G	$AV_{DD3.3}$ A	$AV_{DD3.3}$ A	OUTN I	OUTP I	$AV_{DD3.3}$ A	$AV_{DD3.3}$ A	GND G	AV_{CLK} C	AV_{CLK} C
C	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	AV_{CLK} C	CLKN K
D	SE M	SO/LOCK M	PERR M	MUX M	DELAY M	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	AV_{CLK} C	CLKP K
E	GND G	DCLKDIV M	RZ M	DLLOFF M	RF M	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	AV_{CLK} C	AV_{CLK} C
F	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G
G	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G	GND G
H	DAP13	DAN13	DAP12	DAN12	DAP11	DAN11	DAP10	DAN10	GND G	GND G	GND G	GND G	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D	$V_{DD1.8}$ D
J	DAP9	DAN9	DAP8	DAN8	DAP7	DAN7	DAP6	DAN6	DDP13	DDN13	DDP12	DDN12	DDP11	DDN11	DDP10	DDN10
K	DAP5	DAN5	DAP4	DAN4	DAP3	DAN3	DAP2	DAN2	DDP9	DDN9	DDP8	DDN8	DDP7	DDN7	DDP6	DDN6
L	DAP1	DAN1	DAP0	DAN0	GND G	GND G	GND G	GND G	DDP5	DDN5	DDP4	DDN4	DDP3	DDN3	DDP2	DDN2
M	DBP13	DBN13	DBP12	DBN12	DBP11	DBN11	DBP10	DBN10	DDP1	DDN1	DDP0	DDN0	GND G	GND G	DCLKRSTP	DCLKRSTN
N	DBP9	DBN9	DBP8	DBN8	DBP7	DBN7	DBP6	DBN6	DCP13	DCN13	DCP12	DCN12	DCP11	DCN11	DCP10	DCN10
P	DBP5	DBN5	DBP4	DBN4	DBP3	DBN3	DBP2	DBN2	DCP9	DCN9	DCP8	DCN8	DCP7	DCN7	DCP6	DCN6
R	DBP1	DBN1	DBP0	DBN0	PARP	PARN	SYNCP	SYNCN	DCP5	DCN5	DCP4	DCN4	DCP3	DCN3	DCP2	DCN2
T	GND G	GND G	GND G	GND G	DCLKP	DCLKN	XORP	XORN	DCP1	DCN1	DCP0	DCN0	GND G	GND G	GND G	GND G

A $AV_{DD3.3}$ POWER SUPPLY
G GROUND
C AV_{CLK} POWER SUPPLY
K DAC CLOCK
D $V_{DD1.8}$ POWER SUPPLY
R REFERENCE
M MODE CONTROLS, CMOS INPUTS
I ANALOG OUTPUT

Ball Configurations (continued)

Ball Assignments (Data Connections, 4:1 Mux Mode)



Ball Configurations (continued)

Ball Assignments (Data Connections, 2:1 Mux Mode)

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	CREF	DACREF	REFIO	FSADJ	REFRES	$AV_{DD3.3}$	GND	$AV_{DD3.3}$	$AV_{DD3.3}$	OUTN	OUTP	$AV_{DD3.3}$	$AV_{DD3.3}$	GND	GND	GND
B	GND	GND	GND	GND	GND	GND	GND	$AV_{DD3.3}$	$AV_{DD3.3}$	OUTN	OUTP	$AV_{DD3.3}$	$AV_{DD3.3}$	GND	AV_{CLK}	AV_{CLK}
C	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	CLKN
D	SE	SO/LOCK	PERR	MUX	DELAY	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	CLKP
E	GND	DCLKDIV	RZ	DLLOFF	RF	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	AV_{CLK}
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
G	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	DAP13	DAN13	DAP12	DAN12	DAP11	DAN11	DAP10	DAN10	GND	GND	GND	GND	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$
J	DAP9	DAN9	DAP8	DAN8	DAP7	DAN7	DAP6	DAN6	DDP13	DDN13	DDP12	DDN12	DDP11	DDN11	DDP10	DDN10
K	DAP5	DAN5	DAP4	DAN4	DAP3	DAN3	DAP2	DAN2	DDP9	DDN9	DDP8	DDN8	DDP7	DDN7	DDP6	DDN6
L	DAP1	DAN1	DAP0	DAN0	GND	GND	GND	GND	DDP5	DDN5	DDP4	DDN4	DDP3	DDN3	DDP2	DDN2
M	DBP13	DBN13	DBP12	DBN12	DBP11	DBN11	DBP10	DBN10	DDP1	DDN1	DDP0	DDN0	GND	GND	DCLKRSTP	DCLKRSTN
N	DBP9	DBN9	DBP8	DBN8	DBP7	DBN7	DBP6	DBN6	DCP13	DCN13	DCP12	DCN12	DCP11	DCN11	DCP10	DCN10
P	DBP5	DBN5	DBP4	DBN4	DBP3	DBN3	DBP2	DBN2	DCP9	DCN9	DCP8	DCN8	DCP7	DCN7	DCP6	DCN6
R	DBP1	DBN1	DBP0	DBN0	PARP	PARN	SYNCP	SYNCN	DCP5	DCN5	DCP4	DCN4	DCP3	DCN3	DCP2	DCN2
T	GND	GND	GND	GND	DCLKP	DCLKN	XORP	XORN	DCP1	DCN1	DCP0	DCN0	GND	GND	GND	GND

A = UNUSED INPUTS CONNECT TO GROUND
B = LVDS INPUTS DATA PORT B
C = LVDS INPUTS DATA PORT C
D = UNUSED INPUTS CONNECT TO GND
T = DIFFERENTIAL INPUT SYNCP/SYNCN
X = DIFFERENTIAL INPUT XORP/XORN
R = DIFFERENTIAL INPUT DATA CLOCK RESET
P = DIFFERENTIAL INPUT PARP/PARN
K = LVDS OUTPUTS DCLKP/DCLKN

Ball Configurations (continued)

Ball Assignments (Data Connections, RFZ Mode)

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	CREF	DACREF	REFIO	FSADJ	REFRES	$AV_{DD3.3}$	GND	$AV_{DD3.3}$	$AV_{DD3.3}$	OUTN	OUTP	$AV_{DD3.3}$	$AV_{DD3.3}$	GND	GND	GND
B	GND	GND	GND	GND	GND	GND	GND	$AV_{DD3.3}$	$AV_{DD3.3}$	OUTN	OUTP	$AV_{DD3.3}$	$AV_{DD3.3}$	GND	AV_{CLK}	AV_{CLK}
C	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	CLKN
D	SE	SO/LOCK	PERR	MUX	DELAY	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	CLKP
E	GND	DCLKDIV	RZ	DLLOFF	RF	GND	GND	GND	GND	GND	GND	GND	GND	GND	AV_{CLK}	AV_{CLK}
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
G	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	DAP13 A	DAN13 A	DAP12 A	DAN12 A	DAP11 A	DAN11 A	DAP10 A	DAN10 A	GND	GND	GND	GND	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$	$V_{DD1.8}$
J	DAP9 A	DAN9 A	DAP8 A	DAN8 A	DAP7 A	DAN7 A	DAP6 A	DAN6 A	DDP13 D	DDN13 D	DDP12 D	DDN12 D	DDP11 D	DDN11 D	DDP10 D	DDN10 D
K	DAP5 A	DAN5 A	DAP4 A	DAN4 A	DAP3 A	DAN3 A	DAP2 A	DAN2 A	DDP9 D	DDN9 D	DDP8 D	DDN8 D	DDP7 D	DDN7 D	DDP6 D	DDN6 D
L	DAP1 A	DAN1 A	DAP0 A	DAN0 A	GND	GND	GND	GND	DDP5 D	DDN5 D	DDP4 D	DDN4 D	DDP3 D	DDN3 D	DDP2 D	DDN2 D
M	DBP13 B	DBN13 B	DBP12 B	DBN12 B	DBP11 B	DBN11 B	DBP10 B	DBN10 B	DDP1 D	DDN1 D	DDP0 D	DDN0 D	GND	GND	DCLKRSTP R	DCLKRSTN R
N	DBP9 B	DBN9 B	DBP8 B	DBN8 B	DBP7 B	DBN7 B	DBP6 B	DBN6 B	DCP13 C	DCN13 C	DCP12 C	DCN12 C	DCP11 C	DCN11 C	DCP10 C	DCN10 C
P	DBP5 B	DBN5 B	DBP4 B	DBN4 B	DBP3 B	DBN3 B	DBP2 B	DBN2 B	DCP9 C	DCN9 C	DCP8 C	DCN8 C	DCP7 C	DCN7 C	DCP6 C	DCN6 C
R	DBP1 B	DBN1 B	DBP0 B	DBN0 B	PARP P	PARN P	SYNCP T	SYNCN T	DCP5 C	DCN5 C	DCP4 C	DCN4 C	DCP3 C	DCN3 C	DCP2 C	DCN2 C
T	GND	GND	GND	GND	DCLKP K	DCLKN K	XORP X	XORN X	DCP1 C	DCN1 C	DCP0 C	DCN0 C	GND	GND	GND	GND

A LVDS INPUTS DATA PORT B
C LVDS INPUTS DATA PORT C
B UNUSED INPUTS CONNECT TO GROUND
D UNUSED INPUTS CONNECT TO GROUND
T DIFFERENTIAL INPUT SYNCP/SYNCN
X DIFFERENTIAL INPUT XORP/XORN
R DIFFERENTIAL INPUT DATA CLOCK RESET
P DIFFERENTIAL INPUT PARP/PARN
K LVDS OUTPUTS DCLKP/DCLKN

Ball Description

BALL	NAME	FUNCTION
A1	CREF	Noise Bypass Pin. A 1µF capacitor between the CREF and DACREF band limits the phase noise of the DAC.
A2	DACREF	Current-Set Resistor Return Path. For an 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. DACREF is internally connected to GND. **Do not connect to external ground.**
A3	REFIO	Reference Input/Output. Output pin for the internal 1.2V bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
A4	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For an 80mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. See the *Reference System* section for details.
A5	REFRES	Connect a resistor between REFRES and $AV_{DD3.3}$ to set the standing current (I_{CONST}). For 80mA full-scale output current, connect a 500Ω resistor between REFRES and $AV_{DD3.3}$ ($I_{CONST} = I_{FULLSCALE}/2$). See the *Reference System* section for details.
A6, A8, A9, A12, A13, B8, B9, B12, B13	$AV_{DD3.3}$	Analog 3.3V Supply Voltage. Connect 0.1µF bypass capacitors between each $AV_{DD3.3}$ ball and GND.
A7, A14, A15, A16, B1–B7, B14, C6–C14, D6–D14, E1, E6–E14, F1–F16, G5–G16, H9–H12, L5–L8, M13, M14, T1–T4, T13–T16	GND	Analog Ground. Connect to ground plane with minimum inductance.
A10, B10	OUTN	Negative Terminal of Differential DAC Output. OUTN has an internal 25Ω resistor to $AV_{DD3.3}$.
A11, B11	OUTP	Positive Terminal of Differential DAC Output. OUTP has an internal 25Ω resistor to $AV_{DD3.3}$.
B15, B16, C15, D15, E15, E16	AV_{CLK}	Clock 1.8V Supply Voltage. Connect 0.1µF bypass capacitors between each AV_{CLK} ball and GND.
C1–C5, G1–G4, H13–H16	$V_{DD1.8}$	1.8V Supply Voltage. Connect 0.1µF bypass capacitors between each $V_{DD1.8}$ ball and GND.
C16	CLKN	Negative Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.

Ball Description (continued)

BALL	NAME	FUNCTION
D1	SE	Scan Enable Input. During normal operation, SE should be connected to GND. When SE is high (1.8V), the parallel input register is configured as a shift register, allowing the contents of the input register to be shifted out on SO/LOCK. **Note:** Scan mode does not operate in 2:1 or RFZ modes. SE is a 3.3V tolerant, 1.8V CMOS input with an internal pulldown resistor.
D2	SO/LOCK	1.8V CMOS Logic Output SE = High: SO/LOCK is a scan data output. SE = Low: SO/LOCK is a DLL locking indicator output, and logic-high indicates DLL is locked.
D3	PERR	1.8V CMOS Logic-Level Parity Error Output. When a parity error is detected in the DAC input data, this pin is set high for a minimum of 48 LVDS data periods. This can be used to provide failure monitoring for the system. Note that this pin can pulse high when the power is initially applied and before the DLL is locked.
D4	MUX	MUX Mode Selection MUX = 0: Input data format in 2:1 (ports B and C). MUX = 1: Input data format in 4:1 for NRZ, RZ, and RF modes. Input data format 2:1 (ports A and C) for RFZ mode. MUX is a 3.3V tolerant, 1.8V CMOS input with an internal pulldown resistor.
D5	DELAY	Data Clock Mode Control DELAY = 0: No clock delay when DLLOFF = 1. DELAY = 1: One f_{CLK} period delay added to DCLKP/DCLKN when DLLOFF = 1. DLLOFF ≠ 1: DELAY is a 4-level input pin used along with the DLLOFF pin (see Table 1 for details). DELAY is a 3.3V tolerant, 1.8V 4-level-logic input.
D16	CLKP	Positive Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
E2	DCLKDIV	Data Clock Divider Mode Input DCLKDIV = 1: DCLKP/DCLKN is $f_{CLK}/4$ when MUX = 0, $f_{CLK}/8$ when MUX = 1. DCLKDIV = 0: DCLKP/DCLKN is $f_{CLK}/2$ when MUX = 0, $f_{CLK}/4$ when MUX = 1. DCLKDIV is a 3.3V tolerant, 1.8V CMOS input with an internal pulldown resistor.
E3	RZ	Return-to-Zero (RZ) Mode-Select Input RZ = 0 (and RF = 0): NRZ DAC operation. RZ = 1 (and RF = 0): RZ DAC operation. RZ = 1 (and RF = 1, MUX = 1): RFZ DAC operation. RZ is a 3.3V tolerant, 1.8V CMOS input with an internal pulldown resistor.
E4	DLLOFF	Data Clock Mode Control DLLOFF ≠ 1: DLL is enabled as a 4-level-logic input pin used along with the DELAY pin (see Table 1 for details). DLLOFF = 1: DLL is disabled. Reset DLL after a stable clock is applied. Set DLLOFF = 1 to perform the reset. DLLOFF is a 3.3V tolerant, 1.8V 4-level-logic input.

Ball Description (continued)

BALL	NAME	FUNCTION
E5	RF	Radio Frequency (RF) Mode-Select Input RF = 0: NRZ or RZ mode. RF = 1 (and RZ = 0): RF mode. RF = 1 (and RZ = 0, MUX = 1): RFZ mode. RF is a 3.3V tolerant, 1.8V CMOS input with an internal pulldown resistor.
H1, H3, H5, H7, J1, J3, J5, J7, K1, K3, K5, K7, L1, L3	DAP[13:0]	Positive Terminals of the A-Channel LVDS Data Inputs (Offset Binary Format). DAP13 is the MSB. Connect to GND if only using 2:1 mux mode.
H2, H4, H6, H8, J2, J4, J6, J8, K2, K4, K6, K8, L2, L4	DAN[13:0]	Negative Terminals of the A-Channel LVDS Data Inputs. Connect to GND if only using 2:1 mux mode.
J9, J11, J13, J15, K9, K11, K13, K15, L9, L11, L13, L15, M9, M11	DDP[13:0]	Positive Terminals of the D-Channel LVDS Data Inputs (Offset Binary Format). DDP13 is the MSB. Connect to GND if using only 2:1 mux mode or RFZ mode.
J10, J12, J14, J16, K10, K12, K14, K16, L10, L12, L14, L16, M10, M12	DDN[13:0]	Negative Terminals of the D-Channel LVDS Data Inputs. Connect to GND if using only 2:1 MUX mode or RFZ mode.
M1, M3, M5, M7, N1, N3, N5, N7, P1, P3, P5, P7, R1, R3	DBP[13:0]	Positive Terminals of the B-Channel LVDS Data Inputs (Offset Binary Format). DBP13 is the MSB. Connect to GND if only using RFZ mode.
M2, M4, M6, M8, N2, N4, N6, N8, P2, P4, P6, P8, R2, R4	DBN[13:0]	Negative Terminals of the B-Channel LVDS Data Inputs. Connect to GND if only using RFZ mode.
M15	DCLKRSTP	Positive Terminal of the LVDS Input for DCLK Reset
M16	DCLKRSTN	Negative Terminal of the LVDS Input for DCLK Reset
N9, N11, N13, N15, P9, P11, P13, P15, R9, R11, R13, R15, T9, T11	DCP[13:0]	Positive Terminals of the C-Channel LVDS Data Inputs (Offset Binary Format). DCP13 is the MSB.

Ball Description (continued)

BALL	NAME	FUNCTION
N10, N12, N14, N16, P10, P12, P14, P16, R10, R12, R14, R16, T10, T12	DCN[13:0]	Negative Terminals of the C-Channel LVDS Data Inputs
R5	PARP	Positive Terminal of the Parity LVDS Data Input. The parity input data is used internally to provide detection of bit errors between the data source and the DAC and can be used for system monitoring. PARP/PARN should be delayed three DCLKP/DCLKN cycles.
R6	PARN	Negative Terminal of the Parity LVDS Data Input
R7	SYNCP	Positive Terminal of the Synchronization LVDS Data Input. The SYNCP/SYNCN pair should be driven synchronously with the DAC data input pairs and should be a pseudorandom sequence.
R8	SYNCN	Negative Terminal of the Synchronization LVDS Data Input
T5	DCLKP	Positive Terminal of the LVDS Data Clock Output
T6	DCLKN	Negative Terminal of the LVDS Data Clock Output
T7	XORP	Positive Terminal of the XOR LVDS Data Input. The A-, B-, C-, and D-channel data bits are all logically exclusive ORed by the data on the XOR pin internally. This function can be used for whitening spurious signals that can be present in the input data. XORP/XORN should be delayed one DCLKP/DCLKN cycle. To disable the XOR function, drive logic 0 into the XORP/XORN input pair.
T8	XORN	Negative Terminal of the XOR LVDS Data Input

General Description

The MAX5879 is a high-performance, 14-bit, 2.3Gsps multi-Nyquist digital-to-analog converter (DAC). The device accepts a clock signal up to 2.3GHz and provides four selectable frequency-response modes (NRZ, RZ, RF, and RFZ). The high sample rate and selectable response allow digital generation of signals to more than 2GHz output frequency.

The device has four 14-bit, multiplexed, low-voltage differential signaling (LVDS) input ports and includes a DCLK output for synchronization with the data source, as well as SYNC and parity input bits. The data interface operates in either single data-rate or double data-rate mode and in 2:1 or 4:1 multiplexed (mux) mode. The 2:1 mux mode reduces the number of pins from the driving data source (FPGA or ASIC). An integrated delay-locked loop (DLL) circuit is also included to ease data synchronization and timing requirements with the data source. The parity input and parity error flag output can be used to detect bit errors between the data source and the DAC. A DCLK reset circuit is included for aligning the data-capture clocks of multiple DACs.

The device is a current-steering DAC with an integrated, 50Ω differential output termination to ensure optimum dynamic performance. The device produces a user-defined (R_{SET}, R_{REFRES}), full-scale current range up to 80mA, providing high output power.

Operating from 1.8V and 3.3V power supplies, the device dissipates 2.4W at 2.3Gsps. The device is specified over the -40°C to +85°C extended temperature range and is offered in a 256-ball CSBGA package.

Reference System

The device supports operation with the on-chip 1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external low-impedance reference source, or as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, decouple REFIO to DACREF with a 1µF capacitor. Since REFIO has a 10kΩ series resistance, buffer REFIO with an external amplifier to drive external loads.

The device's reference circuit (Figure 1) employs a control amplifier, designed to regulate the full-scale current (I_{OUT}) for the differential current outputs of the DAC. The bandwidth of the control amplifier is typically less than 100kHz. The DAC full-scale output current can be calculated as follows:

$$I_{OUT} = 128 \times I_{REF}$$

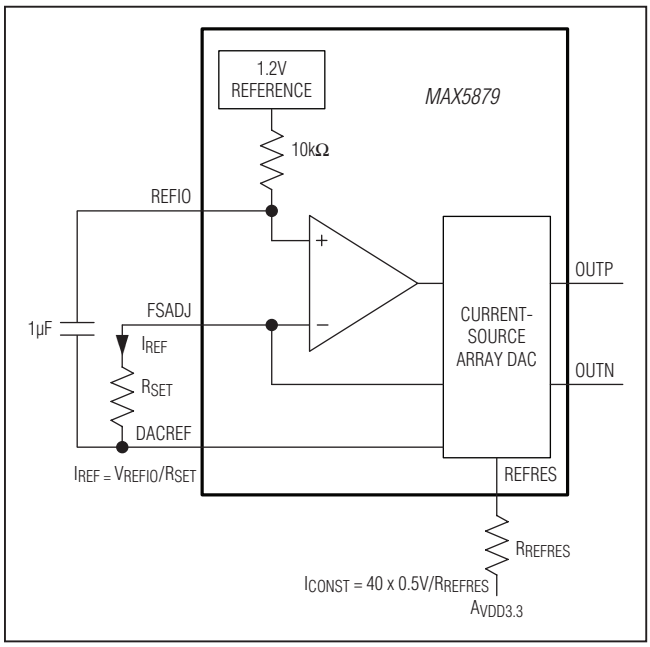


Figure 1. Reference Architecture, Internal Reference Configuration

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO}/R_{SET}$) and I_{OUT} is the full-scale output current of the DAC.

The device also produces a constant standing current at the DAC outputs. This constant current should be set to 1/2 of the full-scale current with a maximum value of 40mA. A resistor connected between REFRES and $AV_{DD3.3}$ (R_{REFRES} in Figure 1) is used to set the value of the constant current (I_{CONST}). The current from REFRES is regulated to produce a 0.5V drop across R_{REFRES} and is scaled by a factor of 40 to produce the constant DAC output current. To determine the required R_{REFRES} value for a specific current, use the following formula:

$$R_{REFRES} = 40 \times 0.5V / I_{CONST}$$

where R_{REFRES} is the required resistor value, and I_{CONST} is 1/2 of the full-scale output current of the DAC.

With an external reference voltage of 1.25V, R_{SET} is typically set to 2kΩ and R_{REFRES} is set to 500Ω, resulting in a full-scale signal current of 80mA and a constant current of 40mA, which produces a maximum continuous-wave (CW) output power of 9dBm. In general, the dynamic performance of the DAC improves with increasing full-scale current. Total power dissipation can be reduced at the expense of dynamic performance by lowering the full-scale and constant-current settings. For example, by reducing the full-scale current to 40mA and the constant current to 20mA, the power dissipation drops by approximately 500mW.

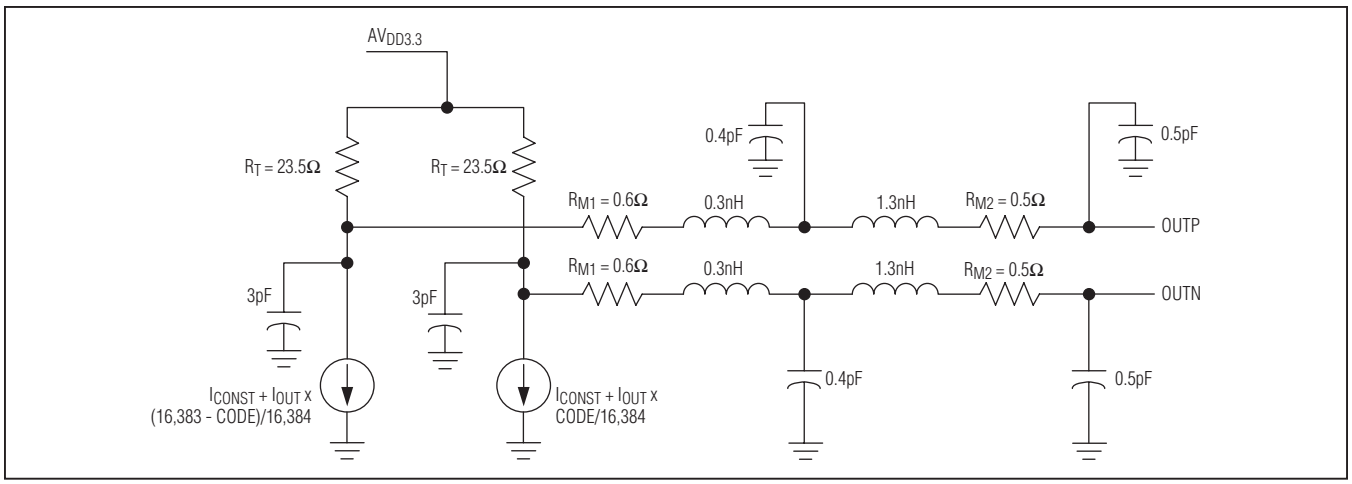


Figure 2. Equivalent Output Circuit

Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to $AV_{DD3.3}$, providing a 50Ω differential output resistance. As mentioned in the *Reference System* section, a constant-current sink is connected to each DAC output. Figure 2 shows an equivalent circuit of the internal output structure of the device. The circuit has some resistive, capacitive, and inductive elements. These elements limit the output bandwidth to 2GHz with a resistive, differential 50Ω load.

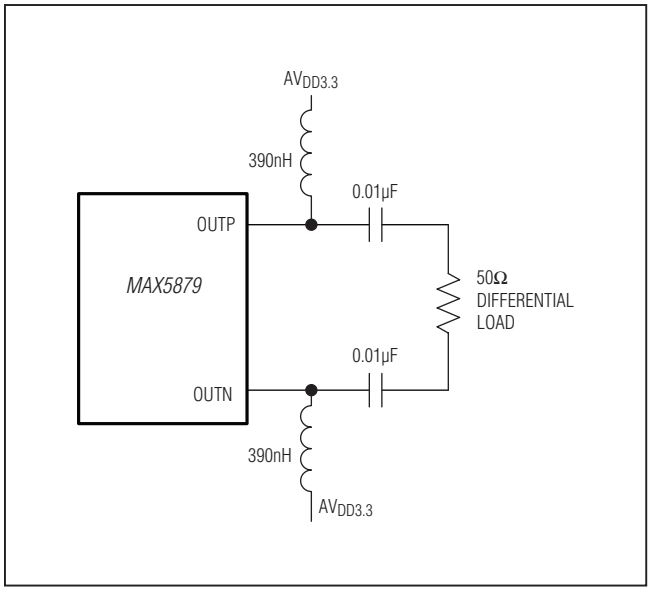


Figure 3. Typical Output Circuit

The outputs need to be pulled up externally to $AV_{DD3.3}$. It is recommended that inductors be used for this purpose, as shown in Figure 3. The use of discrete inductors and capacitors allows for near-perfect symmetry in the output circuit layout. Low-resistance wire-wound inductors and high-Q, low-ESR capacitors are recommended. An external 50Ω differential load is also required to avoid excessive voltage swings at the DAC output pins.

Clock Inputs

The device has a universal, differential clock input (CLKP, CLKN) operating from a separate power supply (AV_{CLK}) to achieve the best possible jitter performance. The two clock inputs should be driven from a differential clock source. A sine-wave or square-wave signal can be used. For the highest speeds and highest performance, a sinusoidal clock should be used. At rates where it is feasible, an LVDS or PECL clock can also be used. The LVDS or PECL clock must be AC-coupled to the device. Each pin is internally DC biased to 1/3 of the supply voltage AV_{CLK}.

The clock input has an internal 100Ω differential termination resistor. For 50Ω (differential) termination, an additional external termination resistor is required between CLKP and CLKN. The balanced input should be AC-coupled unless the common mode of the clock source is within the specifications for the device's clock input. An example of a well-balanced single-ended to differential application circuit using three baluns is shown in Figure 4.

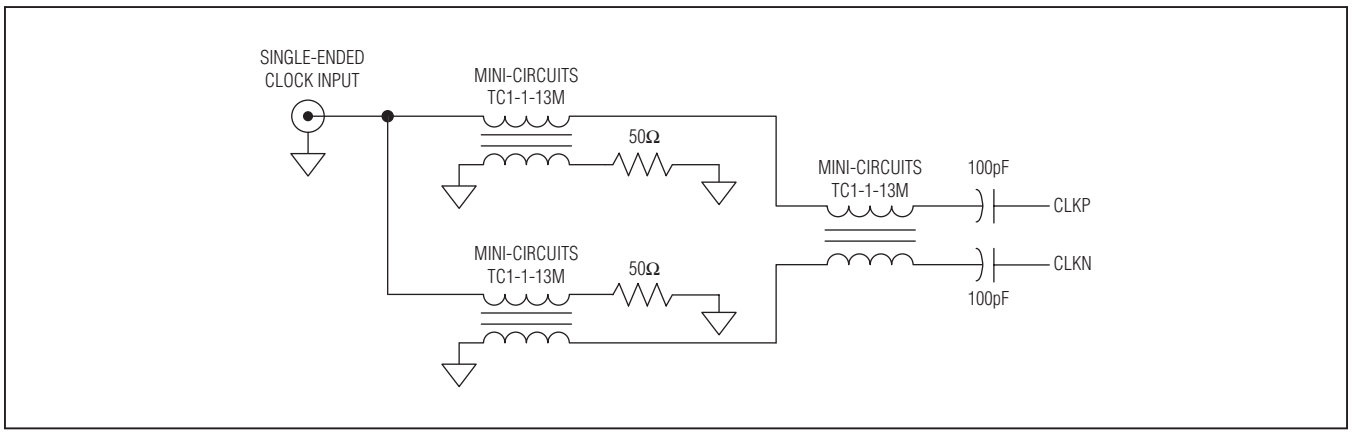


Figure 4. Balanced Clock Interface Circuit

Data Inputs

The device supports both single data-rate (SDR) and double data-rate (DDR) data interfaces. The data inputs (DxP[13:0] and DxN[13:0] (where x = A, B, C, and D), XORP, XORN, PARP, PARN, SYNCP, and SYNCN) all accept LVDS or differential high-speed transceiver logic (DHSTL) signal levels. DCLKRSTP/DCLKRSTN is also a differential input, but requires a higher signal swing than the LVDS signal pairs and does not support DHSTL levels.

The device can accept data in either 2:1 or 4:1 mux modes. The f_{CLK} input clock is divided internally to create the internal clock used to latch input data. The frequency of this internal clock is determined by the mux mode employed and is either $f_{CLK}/2$ when in 2:1 mode (MUX = 0), or $f_{CLK}/4$ when in 4:1 mode (MUX = 1). An additional user-enabled divide-by-2 (DCLKDIV = 1) is available to reduce the DCLKP/DCLKN output frequency, providing a lower frequency reference clock that can be used to synchronize the data source and the device.

The data sequence in 4:1 mux mode is DA1, DB1, DC1, DD1, DA2, DB2, etc. Only ports B and C are used when operating in 2:1 mux mode. The output is updated in the sequence of DB1, DC1, DB2, DC2, etc. The RFZ frequency response mode uses only ports A and C. The data sequence for the RFZ mode is DA1, DC1, DA2, DC2, etc.

When the device is only used in the 2:1 mux or RFZ modes, the unused data inputs (ports A and D for 2:1 mux mode and ports B and D for RFZ mode) should be connected to GND. Note that the scan function does not work in 2:1 or RFZ modes. Alternatively, any unused ports can be simply driven with LVDS logic-low when not in use. The scan feature is then functional when needed, as well as the ability to easily change the operating mode to meet specific signal-generation requirements.

Table 1 shows the supported data rates, port configurations, and DCLKP/DCLKN frequencies for all operating modes.

Figure 5 shows a simplified block diagram for a clocking scheme using an FPGA and the device DLL. The f_{CLK} input clock to the device is divided by two to produce the $f_{CLK}/2$ clock that is equal to the input data rate when operating in 2:1 mux mode. The $f_{CLK}/2$ signal feeds a variable delay line and an optional divide-by-2 block to produce the DCLK signal that is sent to the FPGA. By adjusting the delay of the DCLK signal, the phase of the input data can be adjusted. The device's DLL is used to lock the phase of the incoming data to the internal clock that is used to latch the data. The incoming SYNC signal is used to close the DLL loop and is a replica of the other data lines, but with a pseudorandom data pattern.

The clock-management circuitry (CMC) should not be placed inside the DLL loop and is not needed for clocking the output data and output serializer/deserializer (SerDes) to the DAC. However, it can be used to generate internal clocks, locked to DCLK, for any data FIFO and internal logic. The buffered DCLK without the CMC is used to clock the output SerDes. One output SerDes, with its data wired in such a manner as to reduce its function to that of a simple buffer, is used to match the timing of the SYNC signal to the FPGA output data. This adds between 1ns and 3ns delay on SYNC referenced to the device's DCLK output.

When the device is configured with the optional internal divide-by-2 turned off, the output clock rate must be divided by two (or more) externally for some generations of FPGAs.

Table 1. Data Interface Operating Modes

MUX	DCLKDIV	FREQUENCY-RESPONSE MODE	ACTIVE INPUT PORTS	DCLKP/DCLKN OUTPUT FREQUENCY	MAXIMUM INPUT DATA RATE PER PORT (Msps)
0	0	NRZ, RZ, RF	B, C	$f_{CLK}/2$	1150
0	1	NRZ, RZ, RF	B, C	$f_{CLK}/4$	1150 (DDR)
1	0	NRZ, RZ, RF	A, B, C, D	$f_{CLK}/4$	575
1	0	RFZ	A, C*	$f_{CLK}/4$	575
1	1	NRZ, RZ, RF	A, B, C, D	$f_{CLK}/8$	575 (DDR)
1	1	RFZ	A, C*	$f_{CLK}/8$	575 (DDR)

**Ports B and D are internally zero stuffed. Parity is calculated for A and C ports only.*

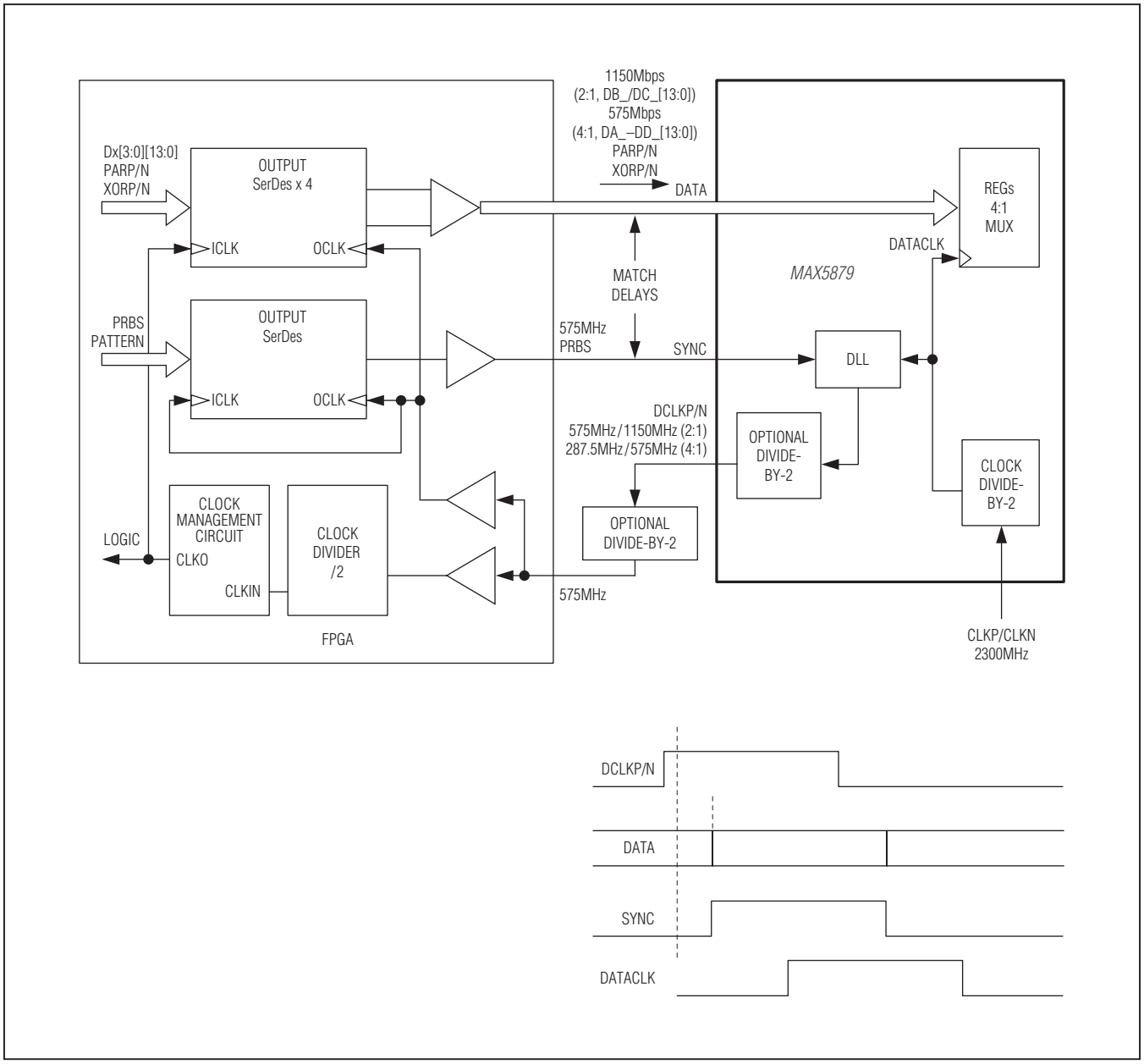


Figure 5. Interfacing the MAX5879 to an FPGA

DAC Impulse/ Frequency-Response Modes

The device has four user-selectable DAC impulse/ frequency-response modes. The four impulse responses are shown in Figure 6. The modes are set using the RZ and RF input pins, as shown in Table 2.

The default operating mode, and typical of most DACs, is NRZ mode. Using this mode, the frequency response of the DAC has the familiar sync shape, with zeroes at every multiple of the DAC update frequency. The theoretical frequency response for the NRZ mode of operation is shown in Figure 7. The amplitude for a specific output frequency, relative to the maximum output power, can be calculated as follows:

$$A_{NRZ} = A_0 \left| \frac{\sin(\pi f_{OUT} T)}{\pi f_{OUT} T} \right|$$

where T is $1/f_{DAC}$.

In RZ mode, the DAC output has a duty cycle determined by the clock input duty cycle. The DAC output is midscale when CLKP/CLKN is a logic-low, and set by the data input when CLKP/CLKN is logic-high. This causes the output amplitude and frequency rolloff of the DAC to be scaled by the duty cycle. The amplitude for a specific output frequency, relative to the maximum output power, can be calculated as follows:

$$A_{RZ} = \frac{A_0}{2} \left| \frac{\sin(\pi f_{OUT} T/2)}{\pi f_{OUT} T/2} \right|$$

where T is $1/f_{DAC}$.

Table 2. Frequency-Response Selection

RZ	RF	OPERATING MODE
0	0	NRZ
1	0	RZ
0	1	RF
1	1	RFZ*

**MUX = 1 only; use channels A and C. Channels B and D are internally zero stuffed. Parity is calculated for the A and C ports only.*

This frequency response is flatter than the NRZ response in the first three Nyquist zones, and particularly in the 2nd and 3rd Nyquist zones, making the DAC usable for outputting wideband signals in these zones. The trade-off when using this mode is lower maximum power in the 1st Nyquist zone. The theoretical frequency response for the RZ mode of operation is shown in Figure 8.

The third mode of operation is called RF mode. This is similar to mixing the DAC output with the DAC update clock. In this mode, the amplitude response is:

$$A_{RF} = A_0 \left| \frac{\sin(\pi f_{OUT} T/2)}{\pi f_{OUT} T/2} \sin(\pi f_{out} T/2) \right|$$

where T is $1/f_{DAC}$.

The theoretical frequency response for the RF mode of operation is shown in Figure 9.

The final mode of operation is called RFZ mode and is a combination of the RF and RZ modes. It is only available in the 4:1 mux input mode. This mode offers a spectral response that is flat over a wider bandwidth than the other modes. Note that f_{DAC} is $f_{CLK}/2$ for the RFZ mode.

$$A_{RFZ} = \frac{A_0}{2} \left| \frac{\sin(\pi f_{OUT} T/4)}{\pi f_{OUT} T/4} \sin(\pi f_{OUT} T/4) \right|$$

where T is $1/f_{DAC}$.

The theoretical frequency response for the RFZ mode of operation is shown in Figure 10.

The achievable output power at any one frequency and in any mode is found by normalizing the output power to the low-frequency NRZ response (0dB in Figure 7).

It is clear that the NRZ mode provides the highest power in the 1st Nyquist zone. The RZ mode provides the flattest frequency response in the 1st and 3rd Nyquist zones, and the RF mode provides superior output power in the 2nd and 3rd Nyquist zones, as well as the flattest gain in the 2nd Nyquist zone. The RFZ mode provides the flattest response across the 3rd through 5th Nyquist zones.

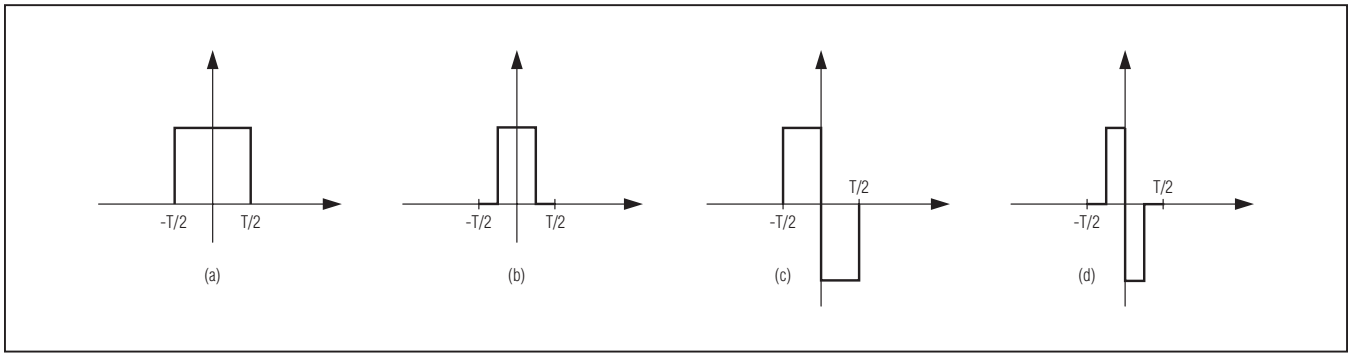


Figure 6. Impulse Responses in (a) NRZ Mode, (b) RZ Mode, (c) RF Mode, and (d) RFZ Mode

Note: *$T = 1/f_{DAC}$*

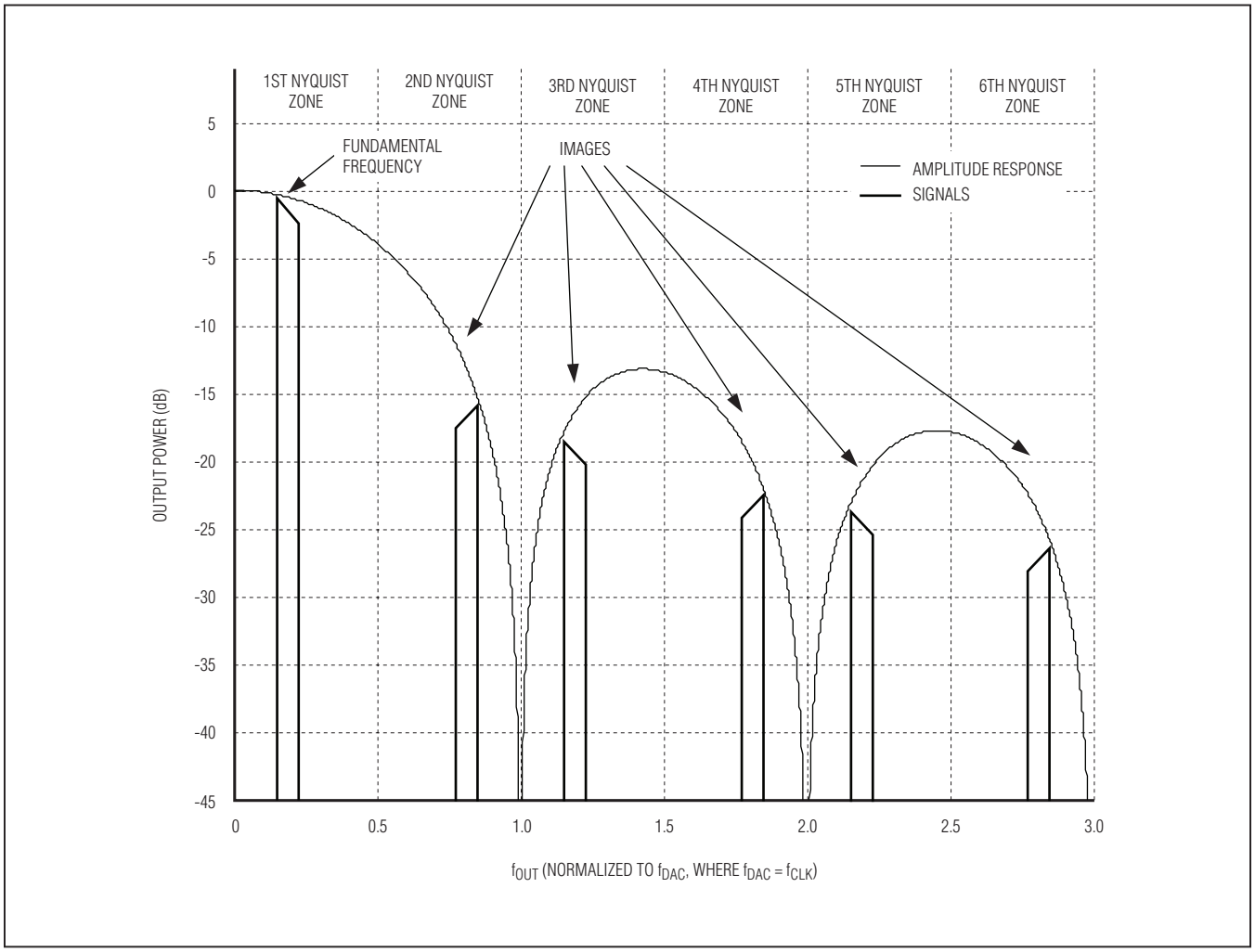


Figure 7. Theoretical Frequency Response (NRZ Mode)

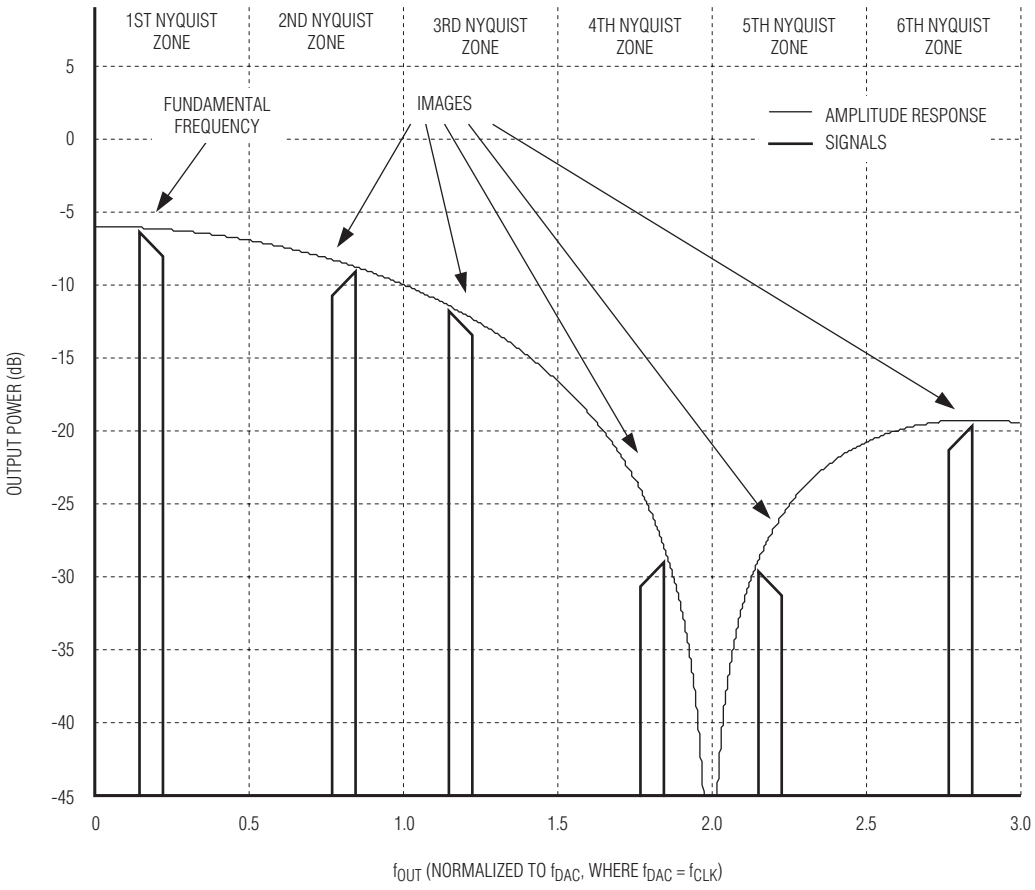


Figure 8. Theoretical Frequency Response (RZ Mode)

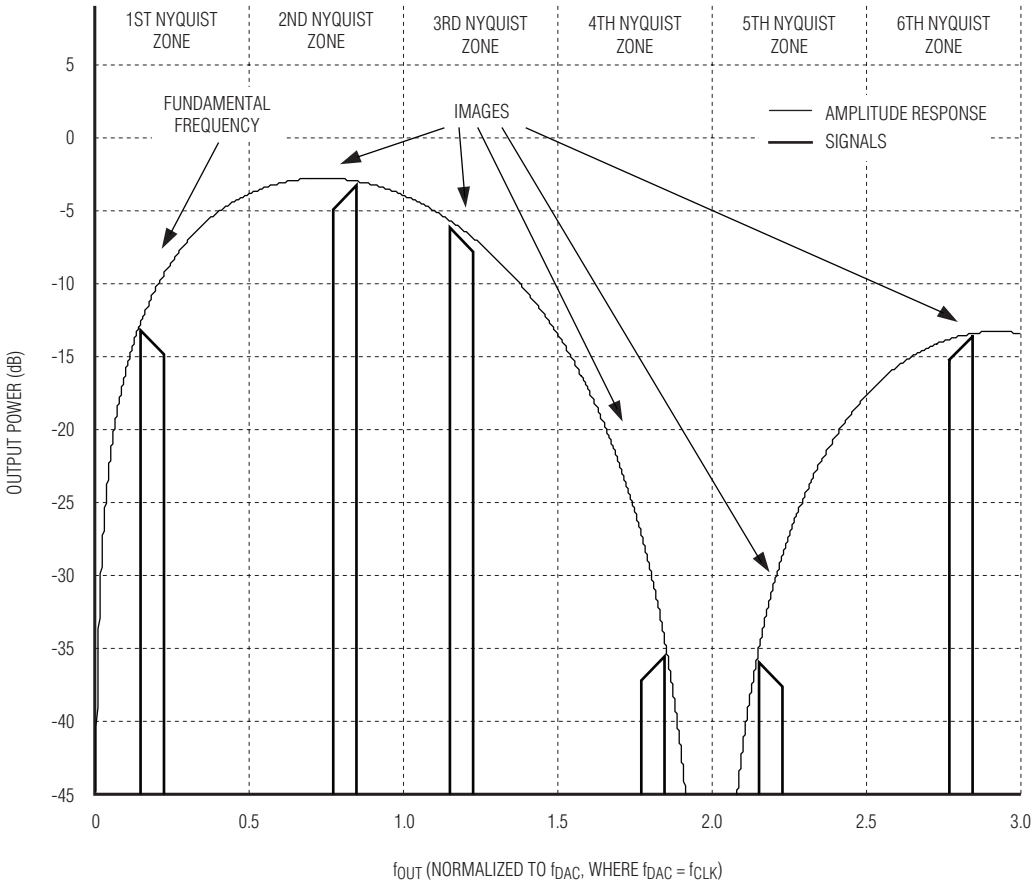


Figure 9. Theoretical Frequency Response (RF Mode)

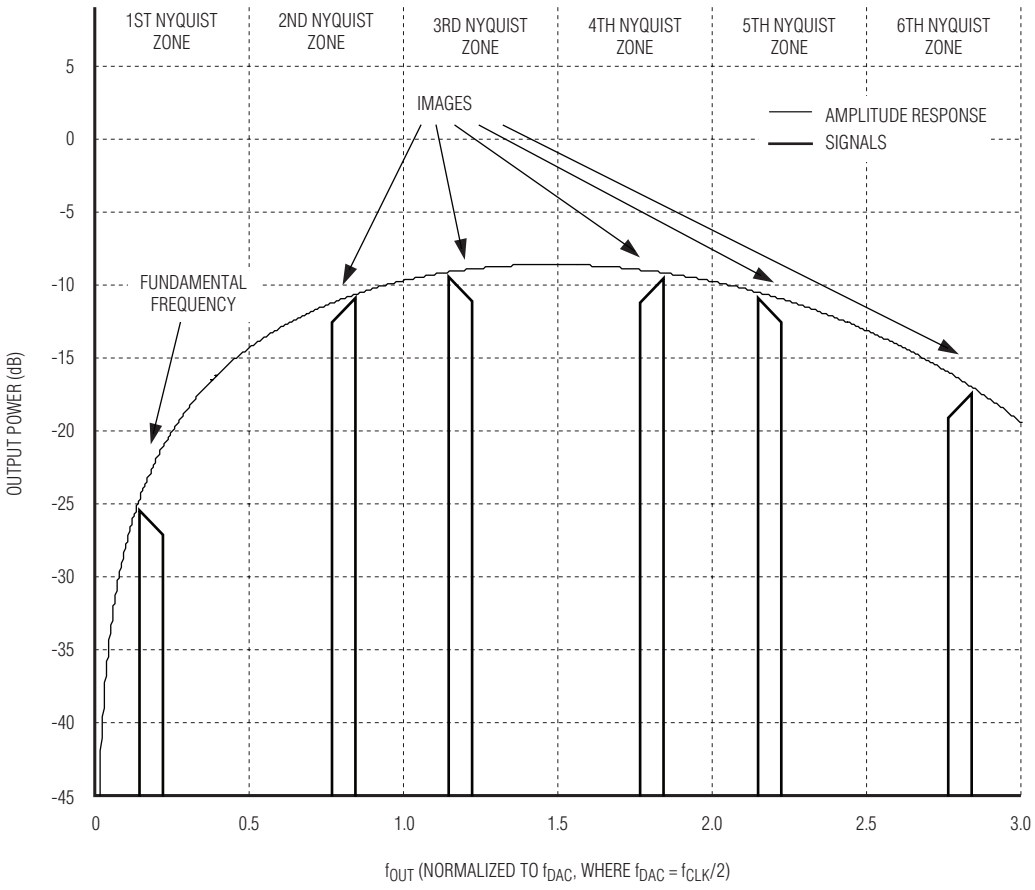


Figure 10. Theoretical Frequency Response (RFZ Mode)

DLL Frequency Selection and 4-Level Input

Two external pins (DLLOFF and DELAY) have 4-level inputs (high, low, open, and resistor to ground) that perform the following functions:

- Turn DLL on or off
- Select operating frequency range of DLL

Table 3 defines the functionality of the DLLOFF and DELAY controls. Figure 11 shows the block diagram of the 4-level input circuitry.

Note: Reset the DLL circuitry at power-up and each time the frequency range is changed. Set DLLOFF = 1 prior to selecting the range to perform the reset.

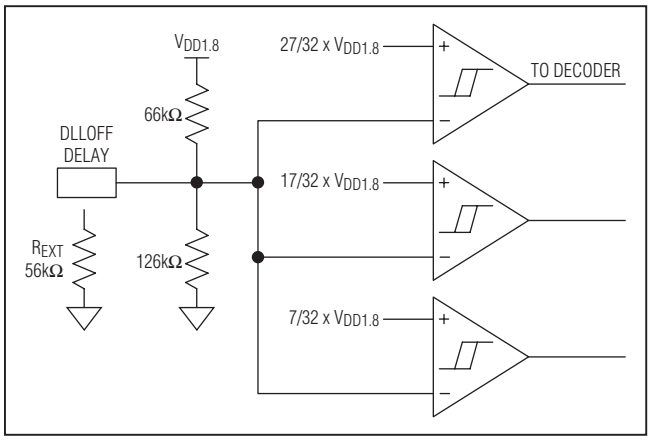


Figure 11. 4-Level Input for DLLOFF and DELAY Pins

XOR and Parity Inputs

The device includes an XOR data function that can be used to whiten the spectral content of the data bits. Figure 12 shows the XOR and parity calculation. The block labeled “parity calculation” returns a 1 when there is an odd number of 1s in the DAC data. The parity is calculated by the device and compared to the received parity from the FPGA. When the received and calculated parity bits do not match, PERR is set high and held for 48 DCLK cycles to make it easier for the FPGA or supervisory microcontroller to monitor asynchronously. Note that the FPGA also XORs the parity bit before sending it to the device. This ensures that corruption of the XOR bit results in detected parity errors.

The XORP/XORN and PARP/PARN signals include pipeline delays internal to the device. These delays must be compensated for in the data source in order for them to align to the data within the device. XORP/XORN requires one DCLK cycle delay and PARP/PARN requires three.

SO/LOCK Signal

The SO/LOCK pin is a dual-mode output signal. When SE is logic-low (0V) the SO/LOCK signal indicates the lock condition of the DLL circuit; SO/LOCK is logic-high (1.8V) when the DLL is locked.

The second function of the SO/LOCK signal is an output of the data input register on the device. Setting SE to logic 1 configures the input data register flip-flops into a 56-bit shift register connected to the SO/LOCK output, as shown in Figure 13. The contents of the shift register are output on the SO/LOCK pin, allowing verification of connectivity in the data interface.

Table 3. Pin Function (DLLOFF, DELAY)

MUX	DLLOFF	DELAY	f_{CLK} (MHz)		f_{DLL} (MHz)		OPERATION
Low	High	High	—	—	—	—	DLL disabled, one f_{CLK} period delay added to the DCLKP/DCLKN outputs
	High	Low	—	—	—	—	DLL disabled, no delay
	Low	High	2150	2300	1075	1150	DLL enabled
	Low	Open	1900	2150	950	1075	DLL enabled
	Open	Low	1650	1900	825	950	DLL enabled
	Open	High	1400	1650	700	825	DLL enabled
	Open	Open	1250	1400	625	700	DLL enabled
	Resistor to ground	Low	1100	1250	550	625	DLL enabled
	Resistor to ground	High	950	1100	475	550	DLL enabled
	Resistor to ground	Open	800	950	400	475	DLL enabled
High	Resistor to ground	Low	2200	2300	550	575	DLL enabled
	Resistor to ground	High	1900	2200	475	550	DLL enabled
	Resistor to ground	Open	1600	1900	400	475	DLL enabled

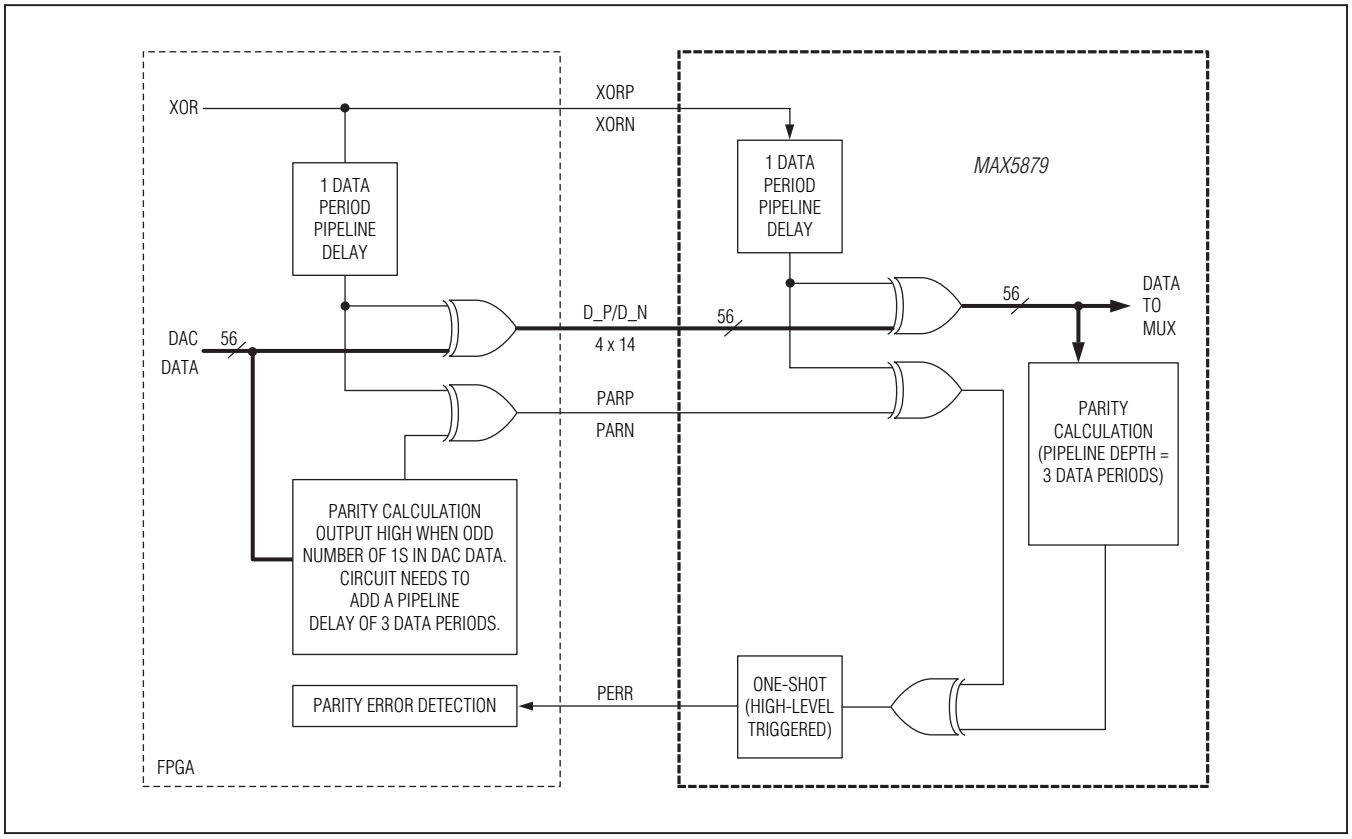


Figure 12. XOR and Parity Functions

Note: *Parity is calculated for the DA, DC, and XOR inputs only for the RFZ mode. Parity is calculated for the DB, DC, and XOR inputs only for the 2:1 mux mode. Parity is calculated for the DA, DB, DC, DD, and XOR inputs for the 4:1 mux mode (excludes RFZ mode).*

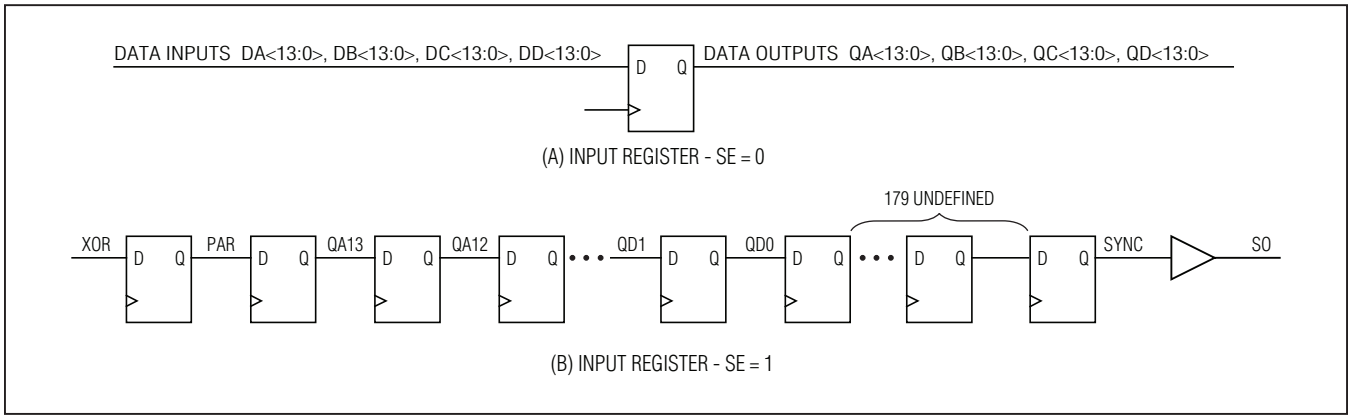


Figure 13. Input Register Flip-Flops in (a) Normal Operation and (b) Scan Mode

Note: *Scan function is not supported in 2:1 mux or RFZ modes.*

A timing diagram for the scan operation is shown in Figure 14. Known input data is applied to the DAC data inputs on the first DCLK pulse, and the input register is loaded in a parallel fashion. Note that the input data needs one clock cycle to propagate before SE can be set to logic-high. When SE is set to logic-high, the input shift register is activated and the serial-data stream is output at the SO/LOCK pin at the input data rate (f_{DATA}). The SCAN sequence outputs a total of 238 bits. The first bit, output immediately upon transitioning SE to the high state, is the SYNC bit. The next 179 bits are undefined. The LVDS input bits are next in the sequence starting with QD0 and continuing through QA13. The final two bits are PAR followed by XOR. SE must be transitioned low to return SO/LOCK to the lock function or to perform another SCAN sequence.

SE and SO/LOCK are a 1.8V CMOS logic interface intended for low-frequency operation. The DAC input clock frequency should be lower than normal when using the scan functionality.

Multiple DAC Synchronization

Multiple analog outputs with accurately known relative phase must be generated in many transmit applications. In a quadrature modulator (Figure 15), the I and Q channels must have a well-defined phase relationship to achieve image rejection. In Figure 15, the delays of DAC1 and DAC2 must be well matched. In transmitters using digital beamforming, accurate control of the relative phase of a large number of D/A converters could be needed.

When using a DAC with multiplexed inputs, such as the MAX5879, or an interpolating DAC with a data clock

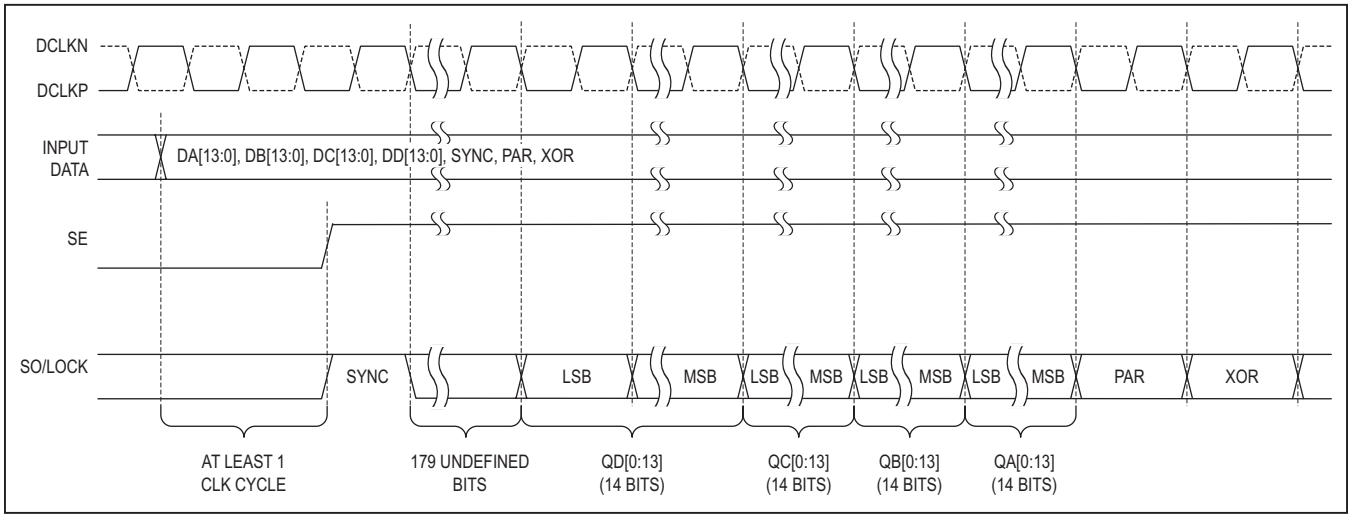


Figure 14. Timing Diagram (Scan Operation)

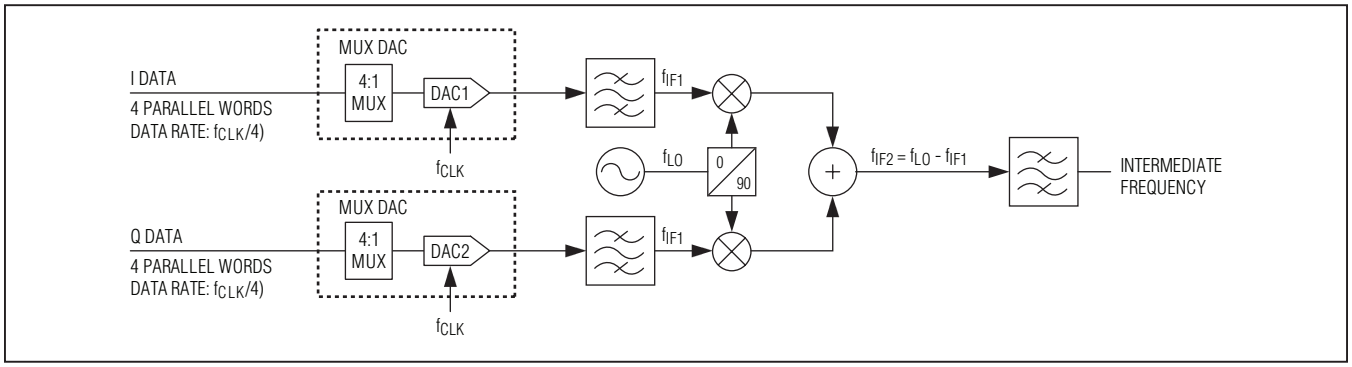


Figure 15. DACs and First Upconversion Stage of I/Q Transmitter Using Mux DACs

output, the input data rate is 1/N times the DAC update rate, and the DAC is latching data on one or both data clock transitions. In the MAX5879, N = 2 or 4, and the input data rate is 1/2 or 1/4 the DAC update rate. The DAC outputs a data clock (DCLK) that is derived from the input clock with a digital clock divider. When the DAC is powered up, the digital clock divider can start up in any one of N states. If multiple DACs are used, the clock dividers of different DACs can start up in different states, hence the DACs latch data at different times. Unless this is detected and corrected, different DACs can output data one or more clock cycles delayed with respect to each other. Resetting the clock divider in each DAC avoids this condition. To ensure a robust system, it is necessary to detect a phase error condition and correct it.

The device implements a reset circuit that allows for resetting the DCLK outputs of multple DACs. The circuit functions by resetting the internal counter used to generate the DCLK signal. Prior to performing a reset, the DLL (if used) should be enabled and locked (LOCK = 1). Then assert DCLKRST for a minimum of 20 and maximum of 40 DAC clock cycles. DCLKRST is then transitioned low and the DCLK output starts after an additional 17 DAC clock cycles. Note that in DDR mode (DCLKDIV = 1), the DCLK output signal of multiple devices can be 180° out of phase.

Applications Information

Output Coupling

The differential voltage between OUTP and OUTN can be converted to a single-ended voltage using a transformer or a differential-amplifier configuration. The DAC outputs should be pulled up to $AV_{DD3.3}$. It is recommended to use bias tees built from discrete inductors and capacitors for the pullups. Two recommended output-circuit configurations are shown in Figure 16. To achieve the maximum bandwidth, minimize the inductance in the ground lead on the secondary side of the transformer. Use a very short trace and multiple vias for the connection to the ground plane.

Grounding, Bypassing, Power-Supply, and Board-Layout Considerations

Grounding and power-supply decoupling can influence the performance of the device. Unwanted digital crosstalk can couple through the input, reference, power supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the device.

Use of a multilayer PCB with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance microstrip lines on the top layer of the board,

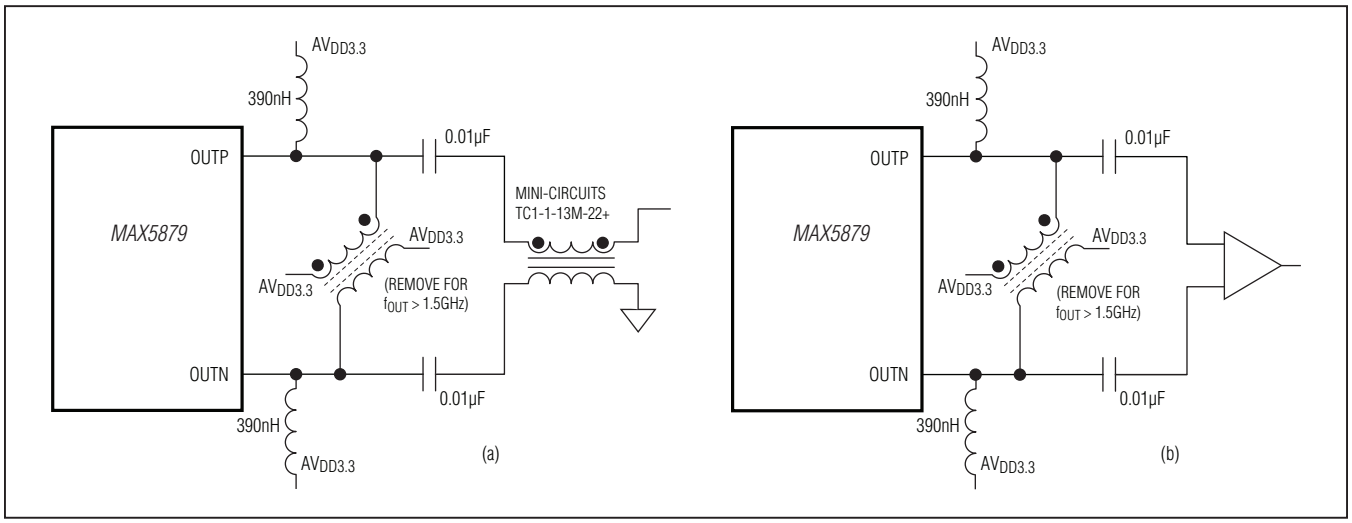


Figure 16. (a) Balun Transformer Output and (b) Amplified Output Configuration

directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top-layer dielectric may be advisable. The data clock (DCLKP, DCLKN) must be routed so its coupling into the clock input and the DAC output is minimized.

Digital input signals should be run as controlled-impedance striplines between ground planes. Digital signals should be kept as far away from sensitive analog inputs, reference input sense lines, common-mode inputs, and clock inputs as practical. It is particularly important to minimize coupling between digital signals and the clock to optimize dynamic performance for high output frequencies. A symmetric design of the clock input and analog output lines is critical to minimize distortion and optimize the DAC's dynamic performance. Digital signal paths should be kept short and run lengths matched to avoid data delay mismatch.

The device supports three separate power-supply inputs for analog 3.3V ($AV_{DD3.3}$), switching ($V_{DD1.8}$), and clock (AV_{CLK}) circuits. Each $AV_{DD3.3}$, $V_{DD1.8}$, and AV_{CLK} input should at least be decoupled with a separate 47nF capacitor as close as possible to the input and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PCB with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network can also improve performance.

Static Performance Parameter Definitions

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the time between the instant that a step is input to the device and the point where the output reaches the corresponding value and stays within the specified accuracy.

Noise Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of the largest distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude, or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD products to any output tone.

Adjacent Channel Power (ACP)

Adjacent channel power is commonly used in combination with DOCSIS-compliant QAM signals. ACP is the ratio in dB between the power in a channel at a specified frequency offset from the edge of the transmitted channel block, and the power in the lowest frequency channel of the transmitted block. ACP provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with wideband code-division multiple access (WCDMA), ACLR reflects the leakage power ratio in dB between the measured powers within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5879EXF+	-40°C to +85°C	256 CSBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
256 CSBGA	X25677+10	21-0474	90-0291

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/11	Initial release	—
1	10/12	Updated the *Electrical Characteristics*, Figures 5, 13, 14 and the *SO/LOCK Signal* section	6, 47, 54, 55