Click here to ask an associate for production status of specific part numbers.

MAX77857

2.5V to 16V Input, 7A Switching Current High-Efficiency Buck-Boost

General Description

The MAX77857 is a high-efficiency, high-performance buck-boost converter targeted for systems requiring a wide input voltage range (2.5V to 16V). It features 7A switching current and can supply up to 6A output current in buck mode and up to 4A in boost mode (Boost Ratio ≤ 1.3). It operates in PWM mode and implements an automatic SKIP mode to improve light-load efficiency.

The default output voltage is 5V when using internal feedback resistors. It can also be configured to any default output voltages between 3V and 15V when using external feedback resistors. The output voltage is adjustable dynamically through the I^2C serial interface (see the *Output Voltage Configuration* section).

The SEL pin allows a single external resistor to program four different I^2C interface slave addresses, four different switching current limit thresholds, and selection between external/internal feedback resistors. The different switching current limit thresholds allow the use of lower profile and smaller external components that are optimized for a particular application. The use of external feedback resistors allows for a wider output voltage range and customizable output voltages at startup.

The I^2C serial interface is optional and allows for dynamically controlling the output voltage, slew rate of the output voltage change, switching-current limit threshold, switching frequency, and forced PWM mode operation. The I^2C-programmed settings have priority over the R_{SEL} decoded settings.

The MAX77857 is available in a 2.83mm x 2.03mm, 35-bump and 31-bump wafer-level package (WLP) and a 3.5mm x 3.5mm, 16-lead Flip Chip QFN package (FC2QFN).

Applications

- USB Power Delivery (USB-PD) OTG
- Qualcomm® Quick Charge™
- USB V_{BUS} Supply and DRP (Dual Role Power) Ports
- DSLR, DSLR Lens
- Display Power
- Up to 3-Cell Li-Ion Battery Applications
- Notebook Computer, Tablet PC

Benefits and Features

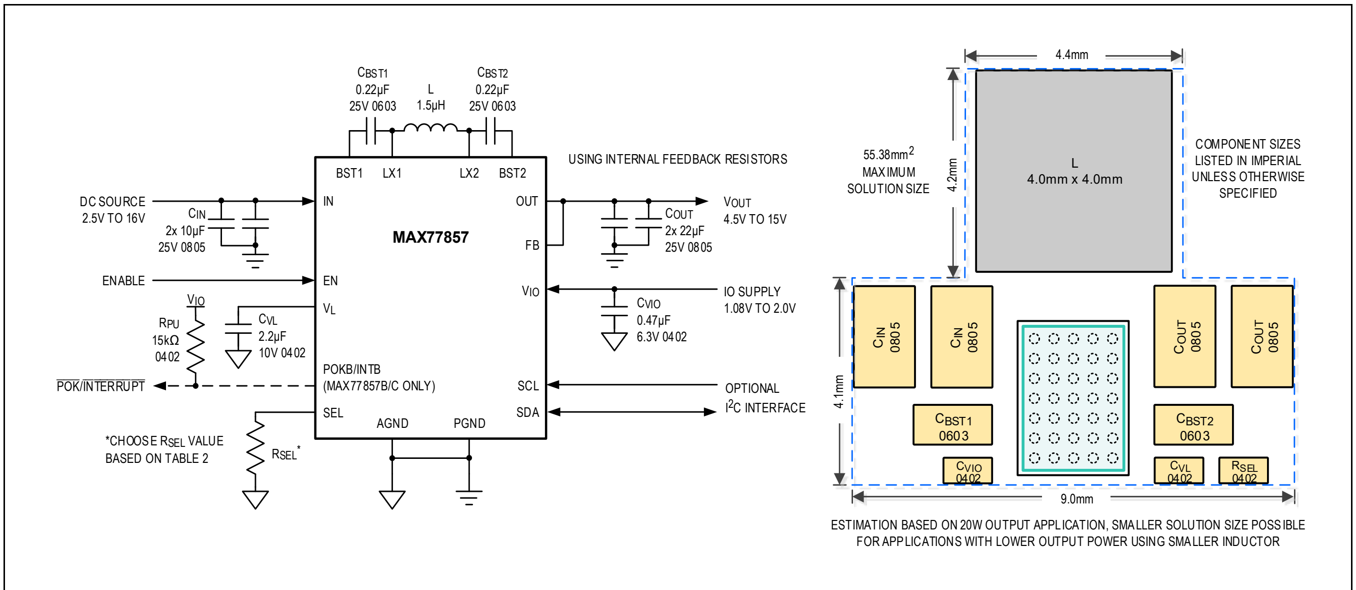
- Wide Input Voltage Range: 2.5V to 16V
- Default Output Voltage
  - 5V with Internal Feedback Resistors
  - 3V to 15V with External Feedback Resistors
- I^2C-Programmable Output Voltage after Startup
  - 4.5V to 15V with Internal Feedback Resistors
  - 3.0V to 15V with External Feedback Resistors, See *Table 1*
- Maximum Output Current
  - Buck Mode: Up to 6A
  - Boost Mode: Up to 4A (Boost Ratio ≤ 1.3)
- 7A Typical Switching Current
- R_{SEL} Configuration
  - I^2C Interface Slave Address
  - Switching Current Limit Threshold
  - Internal/External Feedback Resistors
- I^2C Programming
  - Output Voltage (DVS)
  - Slew Rate of Output Voltage Change
  - Switching Current Limit Threshold
  - Switching Frequency
  - Forced PWM Mode Operation (FPWM)
  - Power-OK (POK) Status and Fault Interrupt Masks
- Soft-Start
- Output Active Discharge
- Open-Drain Power-OK (POK) Monitor and Fault Condition Interrupt (MAX77857B/C Only)
- Protection Features
  - Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Overvoltage Protection (OVP)
  - Thermal Shutdown (THS)
- High Density Interconnect (HDI) PCB not Required (See the *PCB Layout Guideline* section)
- Available in 2.83mm x 2.03mm 35 WLP or 31 WLP or 3.5mm x 3.5mm 16 FC2QFN

***Ordering Information* appears at end of data sheet.**

Qualcomm Quick Charge is a product of Qualcomm Technologies, Inc. and/or its subsidiaries.

19-101423; Rev 2; 8/22

Simplified Application Circuit



Absolute Maximum Ratings

IN, LX1, LX2, OUT, FB to PGND .... -0.3V to +17.6V

BST1, BST2 to AGND .... -0.3V to +20.0V

BST1 to LX1, BST2 to LX2 .... -0.3V to +2.2V

POKB/INTB, SCL, SDA to AGND, PGND .. -0.3V to V_{IO} + 0.3V

V_L, V_{IO}, SEL, EN to AGND, PGND .... -0.3V to +2.0V

PGND to AGND .... -0.3V to +0.3V

Continuous Power Dissipation ....

WLP Package (T_A = +70°C, derate 20.4mW/°C above +70°C (Note 1)) 1633mW

FC2QFN Package (T_A = +70°C, derate 20.7mW/°C above +70°C (Note 1)) 1656mW

Maximum Junction Temperature .... +150°C

Storage Temperature Range .... -65°C to +150°C

Soldering Temperature (reflow) .... +260°C

Note 1: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

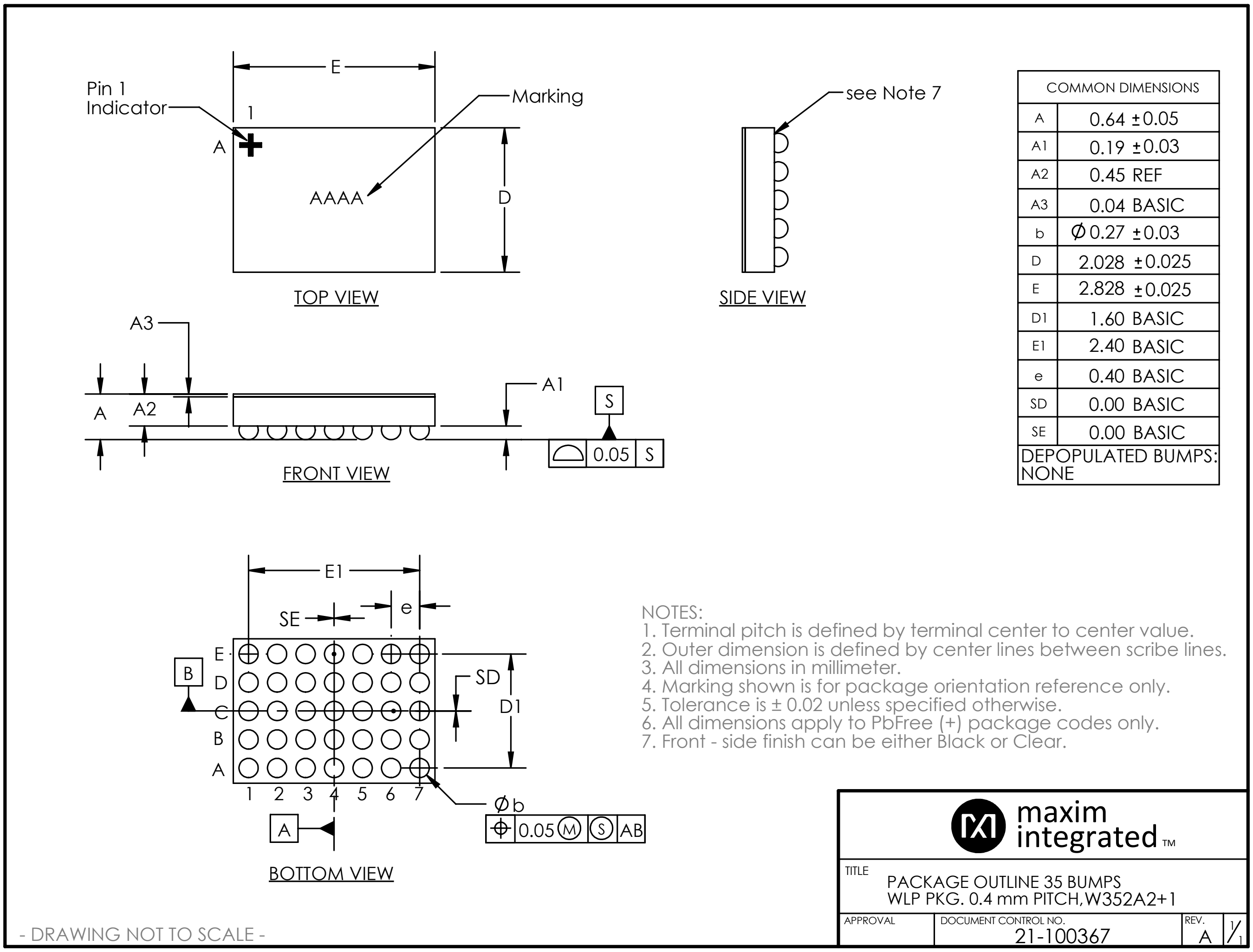
Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE
Input Voltage Range	V_{IN}		2.5V to 16V
Output Voltage Range	V_{OUT}	Internal feedback	4.5V to 15V
		External feedback	3V to 15V
Output Current Range	I_{OUT}	For continuous operation at 6A, the junction temperature (T_J) is limited to +105ºC. If the junction temperature is higher than 105ºC, the expected lifetime at 6A continuous operation is derated	0A to 6A
Junction Temperature Range	T_J		-40°C to +125°C

Package Information

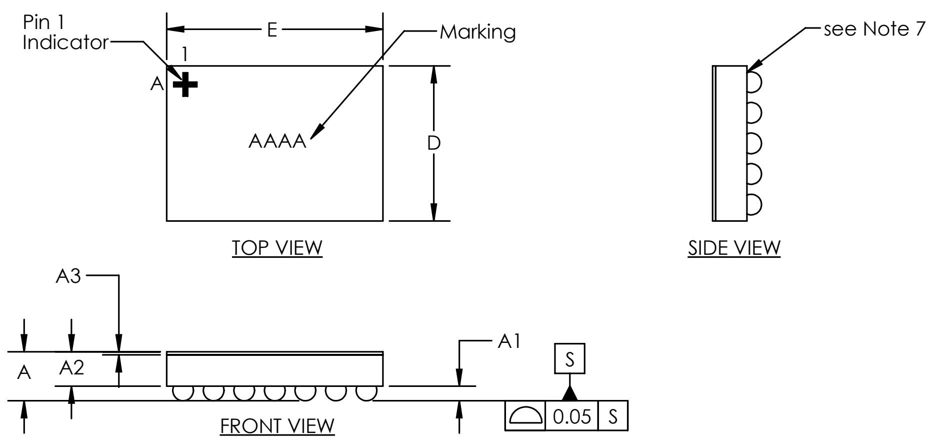
35 WLP

Package Code	W352A2+1
Outline Number	21-100367
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	49°C/W

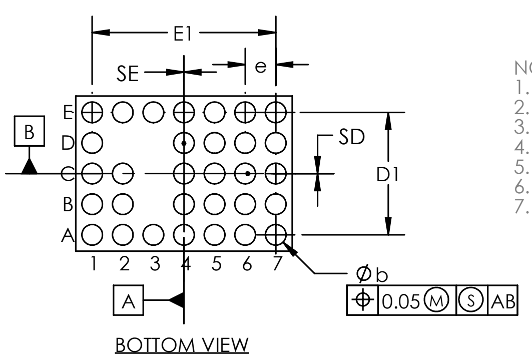


31 WLP

Package Code	W312A2+2
Outline Number	21-100641
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	49°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	2.028 ±0.025
E	2.828 ±0.025
D1	1.60 BASIC
E1	2.40 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: B3, C3, D2, D3	



NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

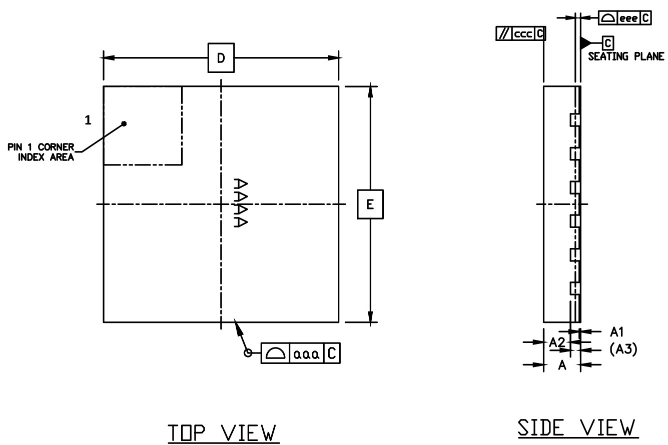
TITLE: PACKAGE OUTLINE 31 BUMPS WLP PKG. 0.4 mm PITCH, W312A2+2

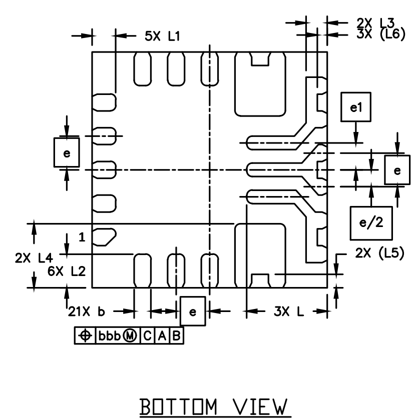
APPROVAL | DOCUMENT CONTROL NO. 21-100641 | REV. B | 1/1

- DRAWING NOT TO SCALE -

16 FC2QFN

Package Code	F163A3F+1
Outline Number	21-100410
Land Pattern Number	90-100141
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	48.3°C/W





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3.5 BSC	
	Y	E		3.5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.4 BSC	
LEAD LENGTH		L	1.1	1.2	1.3
		L1	0.25	0.35	0.45
		L2	0.4	0.5	0.6
		L3	0.22	0.315	0.42
		L4	0.85	0.95	1.05
LEAD EDGE TO PKG		L5		0.2 REF	
		L6		0.15 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTES
1. REFER TO JEDEC MO-220;
2. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET SPECS.
4. FINISH: Cu/EP •Sn8~20s
5. MAXIM PKG CODE : F163A3F+1
6. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.

maxim integrated™

TITLE: PACKAGE OUTLINE, 16L FC2QFN 3.5x3.5x0.55mm

APPROVAL | DOCUMENT CONTROL NO. 21-100410 | REV. B | 1/1

-DRAWING NOT TO SCALE-

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Voltage Range	V_{IN}			2.5		16	V
Input Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		2.3	2.4	2.5	V
Input Undervoltage Lockout (UVLO) Hysteresis	V_{UVLO_HYS}	$V_{UVLO\_R} – V_{UVLO\_F}$			150		mV
Shutdown Supply Current	I_{SHDN}	EN = LOW, T_J = -40°C to +85°C			2	6	µA
Quiescent Supply Current	I_Q	EN = HIGH, R_{SEL} = short to GND, no switching	SKIP mode, T_J = -40°C to +85°C		50	67	µA
			FPWM mode		4		mA
OUTPUT VOLTAGE							
Output Voltage Regulation Range	V_{OUT}	Using internal feedback resistors		4.5		15	V
		Using external feedback resistors		3.0		15	
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 2.5V to 16V, V_{OUT} = 4.5V to 15V, I_{OUT} = 0mA, using internal feedback resistors	SKIP mode	-1.0		+4.5	%
			FPWM mode	-1.0		+2.0	
FB Accuracy	V_{FB_ACC}	VREF[7:0] = 0x3D to 0xCC		-1.0		+2.0	%
V_L INTERNAL SUPPLY							
V_L Regulator Voltage	V_{VL}			1.65	1.8	1.89	V
V_{IO} SUPPLY							
V_{IO} Voltage Range	V_{VIO}			1.08		2.0	V
V_{IO} Valid Threshold	$V_{VIO\_VALID\_R}$	V_{IO} rising		0.965	1.02	1.08	V
	$V_{VIO\_VALID\_F}$	V_{IO} falling		0.85	0.9	0.955	
V_{IO} Bias Current	I_{VIO}	No I^2C interface (SDA and SCL unconnected)				2.0	µA
		$f_{SCL} = f_{SDA}$ = 1MHz			50		
ENABLE							
EN Input LOW Voltage	V_{EN_IL}					0.4	V
EN Input HIGH Voltage	V_{EN_IH}			0.9			V
EN Internal Pulldown Current	I_{EN_PD}	EN = HIGH			0.1		µA
POWER-OK							
POK Output LOW Voltage	V_{POK_OL}	I_{POK} = 1mA				0.3	V
POK Rising Threshold	V_{POK_R}	V_{OUT} rising, expressed as percentage of target V_{OUT} voltage		90	95		%
POK Falling Threshold	V_{POK_F}	V_{OUT} falling, expressed as percentage of target V_{OUT} voltage			85		%
THERMAL PROTECTION							

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Threshold	T_{SHDN_R}	T_J rising (Note 3)		150		˚C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}	$T_{SHDN\_R} – T_{SHDN\_F}$ (Note 3)		20		˚C
BUCK-BOOST REGULATOR						
Switching Frequency	f_{SW}	I_{OUT} = 0mA, FPWM mode; FREQ[1:0] = 00	1.10	1.20	1.30	MHz
		I_{OUT} = 0mA, FPWM mode; FREQ[1:0] = 01	1.38	1.50	1.62	
		I_{OUT} = 0mA, FPWM mode; FREQ[1:0] = 10 (default)	1.66	1.80	1.94	
		I_{OUT} = 0mA, FPWM mode; FREQ[1:0] = 11	1.93	2.10	2.27	
Startup Delay Time	t_{SUDLY}	(Note 2)		100		μs
Soft-Start Time	t_{SS}	Measured from OUT start ramping to stop ramping during startup, C_{OUT} = 44μF, I_{OUT} = 0mA (Note 2)		2.0		ms
Soft-Start Switching Current Limit	I_{LIM_SS}	ILIM[2:0] = 100, 101, 110, or 111 ($I_{LIM} \leq$ 3.8A) (Note 3)		I_{LIM}		A
		ILIM[2:0] = 000, 001, 010, or 011 (I_{LIM} > 3.8A) (Note 3)		3.8		
High-Side Switching Current Limit	I_{LIM}	ILIM[2:0] = 000	6.2	7.0	8.3	A
		ILIM[2:0] = 001 (I^2C only, not available with R_{SEL}) (Note 3)		6.2		
		ILIM[2:0] = 010	4.8	5.6	6.9	
		ILIM[2:0] = 011 (I^2C only, not available with R_{SEL}) (Note 3)		4.6		
		ILIM[2:0] = 100	3.3	3.8	5.1	
		ILIM[2:0] = 101 (I^2C only, not available with R_{SEL}) (Note 3)		2.8		
		ILIM[2:0] = 110	1.5	1.8	2.9	
		ILIM[2:0] = 111 (I^2C only, not available with R_{SEL}) (Note 3)		0.99		
Valley Current Limit	I_{LIM_VALLEY}	ILIM[2:0] = 000 or 001 (Note 3)		2.5		A
		ILIM[2:0] = 010 or 011 (Note 3)		1.8		
		ILIM[2:0] = 100 or 101 (Note 3)		1.0		
		ILIM[2:0] = 110 or 111 (Note 3)		0.3		
Skip Mode Switching Current Limit	I_{LIM_SKIP}	SKIP mode (Note 3)		1.4		A
Line Regulation	$\Delta V/V_{IN}$	V_{IN} = 2.5V to 16V, V_{OUT} = 5V, I_{OUT} = 0mA and 1A, FPWM mode		± 0.3		%/V
Load Regulation	$\Delta V/V_{OUT}$	$V_{IN} \geq$ 4V, V_{OUT} = 5V, I_{OUT} = 0mA to 3A, FPWM mode		± 0.6		%/A
Internal Reference Voltage	V_{REF}	VREF[7:0] = 0x3D, code clamped below this level		0.299		V
		VREF[7:0] = 0x44, default value		0.333		
		VREF[7:0] = 0xCC, code clamped above this level		1.000		

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Reference Voltage Programmable Range	V_{REF}	VREF[7:0] = 0x3D to 0xCC	0.299		1.000	V
Internal Reference DVS Ramp Rate	$\Delta V_{REF}/\Delta t$	SLEW_RATE[1:0] = 00, FREQ[1:0] = 10, or 11		4/3		mV/µs
		SLEW_RATE[1:0] = 00, FREQ[1:0] = 00, or 01		7/6		
		SLEW_RATE[1:0] = 01		2/3		
		SLEW_RATE[1:0] = 10		1/3		
		SLEW_RATE[1:0] = 11, FREQ[1:0] = 10, or 11		17/75		
		SLEW_RATE[1:0] = 11, FREQ[1:0] = 00, or 01		1/6		
FB Input Leakage Current	I_{FB_LK}		-1		+1	µA
High-Side MOSFET On Resistance	R_{DSON_HS}	IN to LX1, LX2 to OUT		20	35	mΩ
Low-Side MOSFET On Resistance	R_{DSON_LS}	LX1 to PGND, LX2 to PGND		22	43	mΩ
Overvoltage-Limit Threshold	V_{OVP}		15.85	16.40	16.95	V
Overvoltage-Release Threshold	V_{OVP_REL}		15.25	15.50	16.20	V
Output Active Discharge Current	I_{DISCHG}	EN = LOW or $V_{IN} < V_{UVLO\_F}$, V_{OUT} = 15V		5		mA

Electrical Characteristics–I²C Serial Interface

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input HIGH Voltage	V_{IH}		0.7 x V_{VIO}			V
SCL, SDA Input LOW Voltage	V_{IL}				0.3 x V_{VIO}	V
SCL, SDA Input Hysteresis	V_{HYS}	Fast mode/Fast-mode plus	0.05 x V_{VIO}			V
		High-speed mode	0.1 x V_{VIO}			
SDA Output LOW Voltage	V_{OL}	I_{SINK} = 2mA (Fast mode/Fast-mode plus) or 3mA (High-speed mode)			0.2 x V_{VIO}	V
SCL, SDA Input Capacitance	C_I				10	pF
SCL, SDA Input Leakage Current	I_{LK}		-10	0.001	+10	µA
TIMING (FAST MODE)						
Clock Frequency	f_{SCL}		0		400	kHz

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between STOP and START Condition	t_{BUSF}		1.3			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.6			µs
SCL LOW Period	t_{LOW}		1.3			µs
SCL HIGH Period	t_{HIGH}		0.6			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.6			µs
DATA Setup Time	T_{SU_DATA}		100			ns
SCL, SDA Receiving Rise Time	t_{R_REV}		20		300	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO} /5.5V)		300	ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				900	ns
Data Valid Acknowledge Time	t_{VD_ACK}				900	ns
Bus Capacitance	C_B	(Note 2)			400	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns
TIMING (FAST-MODE PLUS)						
Clock Frequency	f_{SCL}		0		1000	kHz
Bus Free Time Between STOP and START Condition	t_{BUSF}		0.5			µs
Hold Time (REPEATED) START Condition	t_{HD_START}		0.26			µs
SCL LOW Period	t_{LOW}		0.5			µs
SCL HIGH Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_START}		0.26			µs
DATA Setup Time	T_{SU_DATA}		50			ns
SCL, SDA Receiving Rise Time	t_{R_REV}				120	ns
SCL, SDA Receiving Fall Time	t_{F_REV}		20 x (V_{VIO} /5.5V)		120	ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Data Valid Time	t_{VD_DATA}				450	ns
Data Valid Acknowledge Time	t_{VD_ACK}				450	ns
Bus Capacitance	C_B	(Note 2)			550	pF
Pulse Width of Suppressed Spikes	t_{SP}				140	ns

(V_{IN} = 7.6V, V_{OUT} = 5V, V_{VIO} = 1.8V, R_{SEL} = 536Ω, Typicals are at $T_A \approx T_J$ = +25ºC. Limits are 100% production tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization, unless otherwise noted.)

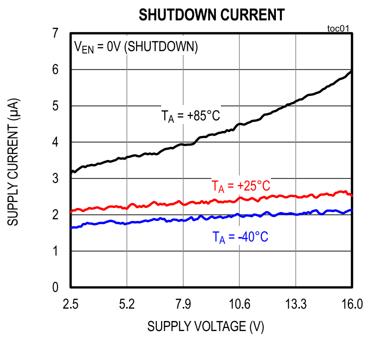
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING (HIGH-SPEED MODE, BUS CAPACITANCE = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Hold Time (REPEATED) START Condition	t_{HD_START}		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Setup Time REPEATED START Condition	t_{SU_START}		160			ns
DATA Hold Time	t_{HD_DATA}				95	ns
DATA Setup Time	T_{SU_DATA}		10			ns
SCL Rise Time	t_{R_SCL}		10		50	ns
SCL Fall Time	t_{F_SCL}		10		50	ns
SDA Rise Time	t_{R_SDA}		10		80	ns
SDA Fall Time	t_{F_SDA}		10		80	ns
Setup Time for STOP Condition	t_{SU_STOP}		160			ns
Bus Capacitance	C_B	(Note 2)			100	pF
Pulse Width of Suppressed Spikes	t_{SP}				30	ns

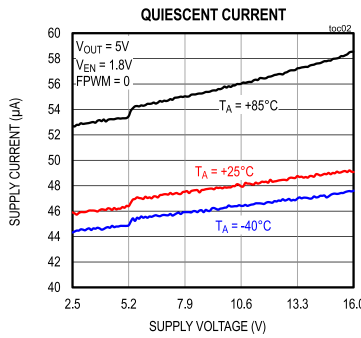
Note 2: Internal design target. Not production tested.

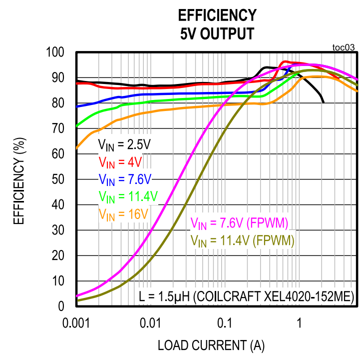
Note 3: Characterized by ATE or bench test. Not production tested.

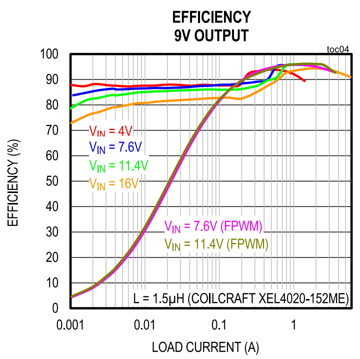
Typical Operating Characteristics

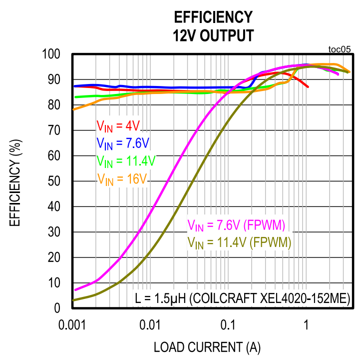
(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4**: Measurement limited by switching current limit. Actual maximum output current depends on system thermal performance.)

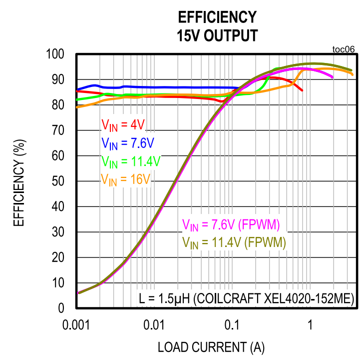


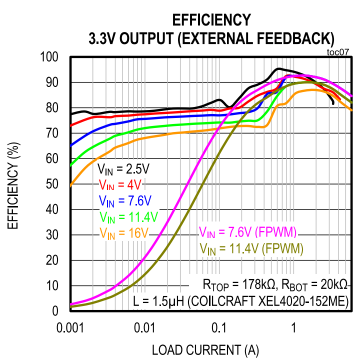


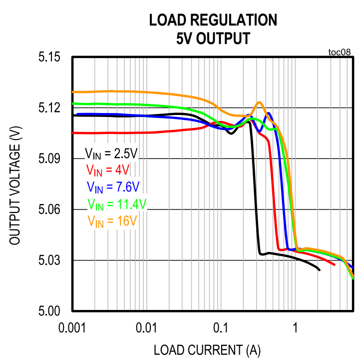


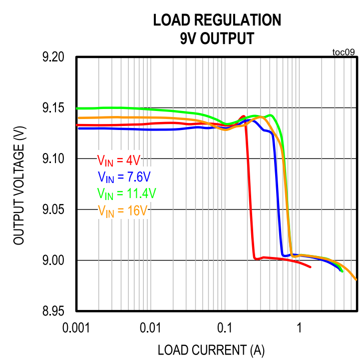












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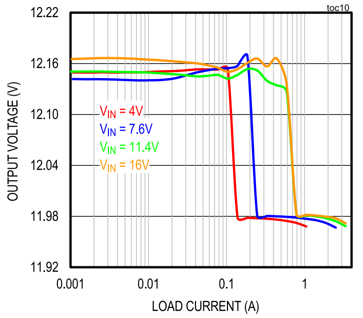
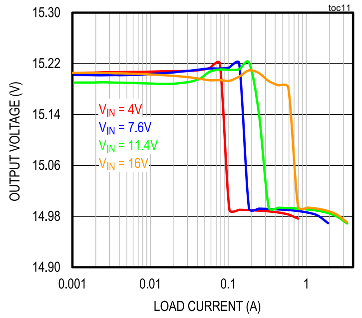
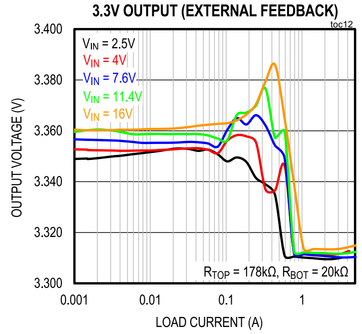
LOAD REGULATION
12V OUTPUT



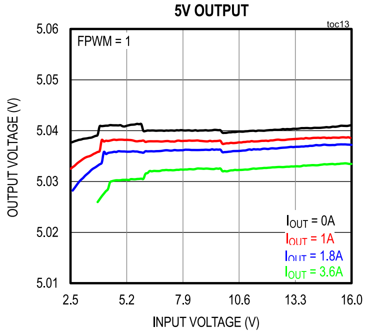
LOAD REGULATION
15V OUTPUT



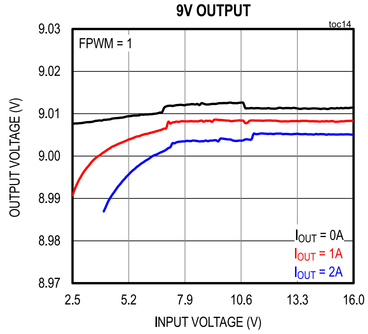
LOAD REGULATION
3.3V OUTPUT (EXTERNAL FEEDBACK)



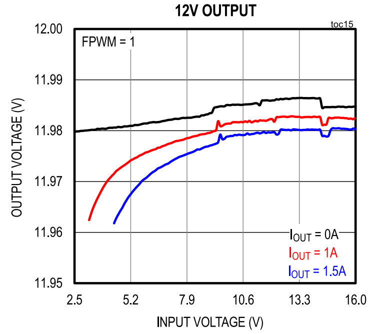
LINE REGULATION
5V OUTPUT



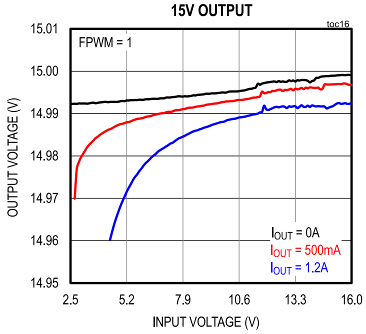
LINE REGULATION
9V OUTPUT



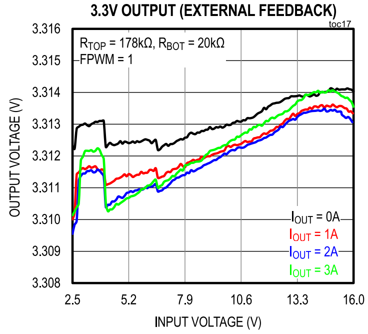
LINE REGULATION
12V OUTPUT



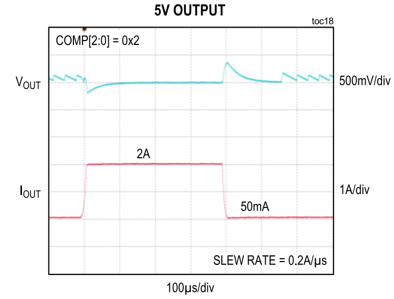
LINE REGULATION
15V OUTPUT



LINE REGULATION
3.3V OUTPUT (EXTERNAL FEEDBACK)

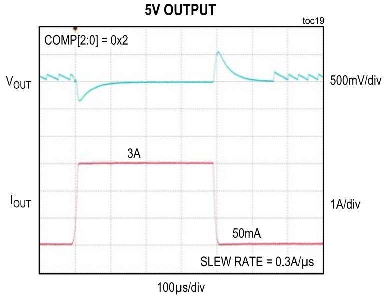


LOAD TRANSIENT RESPONSE
5V OUTPUT

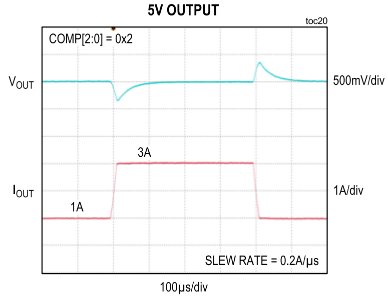


(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4**: Measurement limited by switching current limit. Actual maximum output current depends on system thermal performance.)

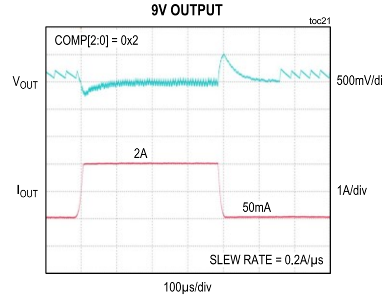
LOAD TRANSIENT RESPONSE
5V OUTPUT



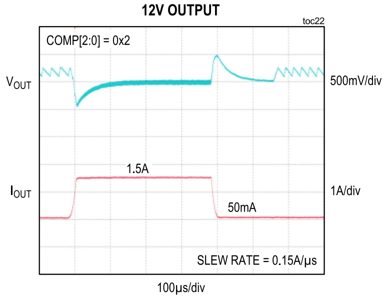
LOAD TRANSIENT RESPONSE
5V OUTPUT



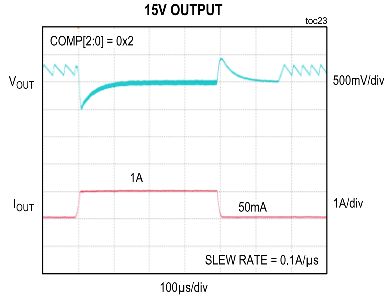
LOAD TRANSIENT RESPONSE
9V OUTPUT



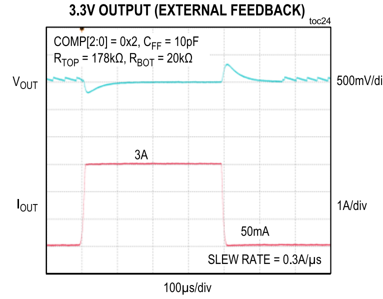
LOAD TRANSIENT RESPONSE
12V OUTPUT



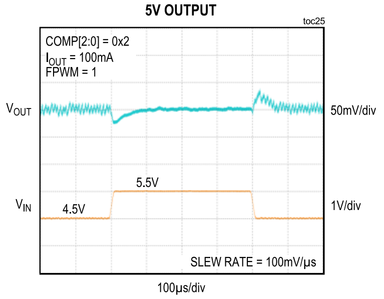
LOAD TRANSIENT RESPONSE
15V OUTPUT



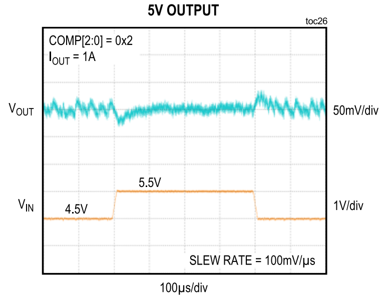
LOAD TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



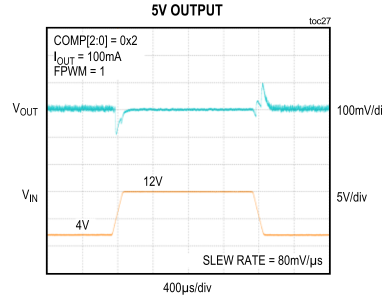
LINE TRANSIENT RESPONSE
5V OUTPUT



LINE TRANSIENT RESPONSE
5V OUTPUT



LINE TRANSIENT RESPONSE
5V OUTPUT



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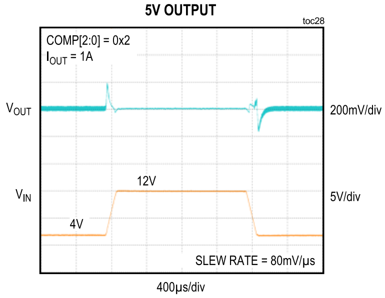
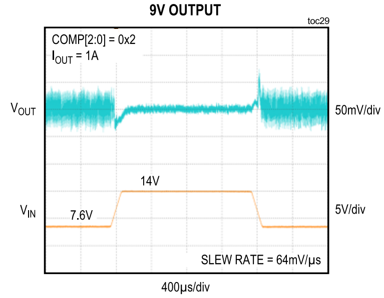
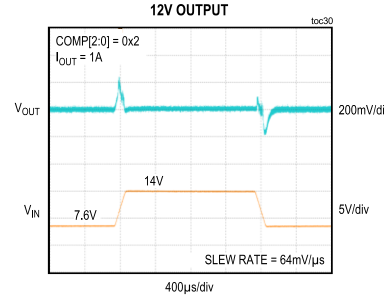
LINE TRANSIENT RESPONSE
5V OUTPUT



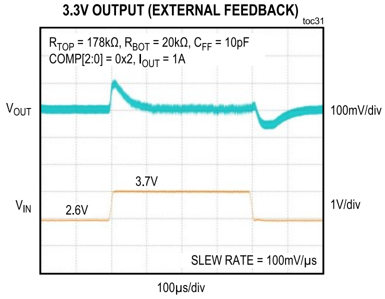
LINE TRANSIENT RESPONSE
9V OUTPUT



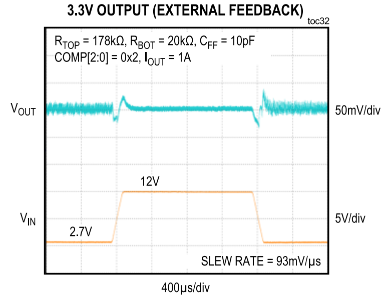
LINE TRANSIENT RESPONSE
12V OUTPUT



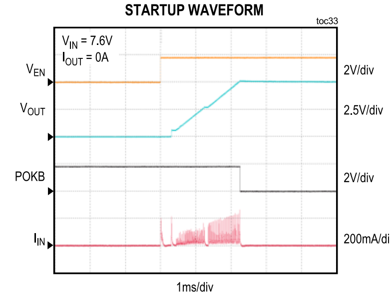
LINE TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



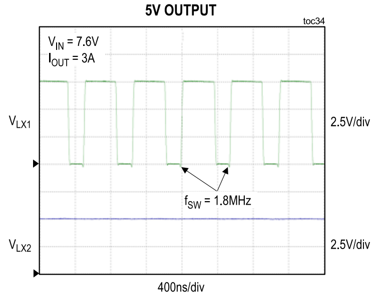
LINE TRANSIENT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



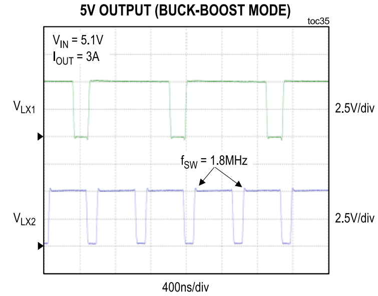
STARTUP WAVEFORM



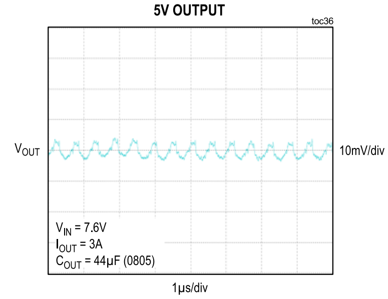
SWITCHING WAVEFORM
5V OUTPUT



SWITCHING WAVEFORM
5V OUTPUT (BUCK-BOOST MODE)



OUTPUT VOLTAGE RIPPLE
5V OUTPUT



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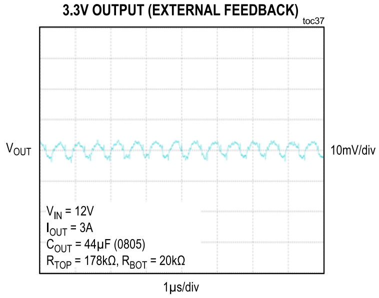
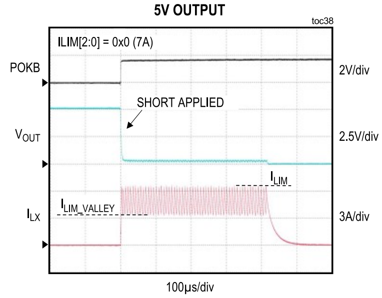
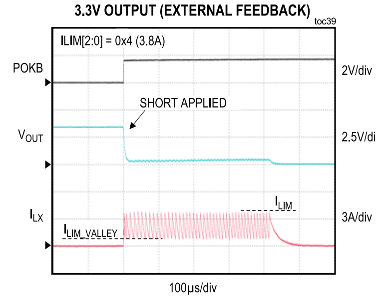
OUTPUT VOLTAGE RIPPLE
3.3V OUTPUT (EXTERNAL FEEDBACK)



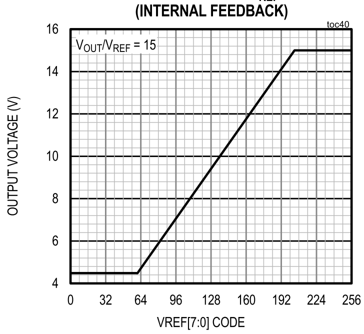
SHORT-CIRCUIT RESPONSE
5V OUTPUT



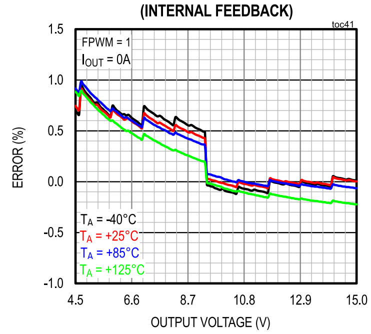
SHORT-CIRCUIT RESPONSE
3.3V OUTPUT (EXTERNAL FEEDBACK)



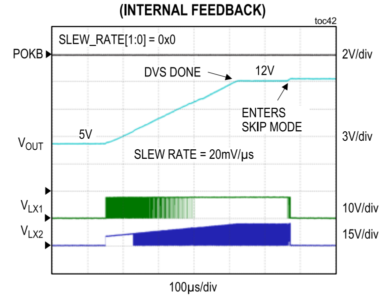
OUTPUT VOLTAGE vs. V_{REF} CODE
(INTERNAL FEEDBACK)



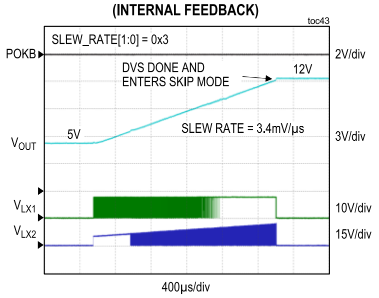
OUTPUT VOLTAGE ACCURACY
(INTERNAL FEEDBACK)



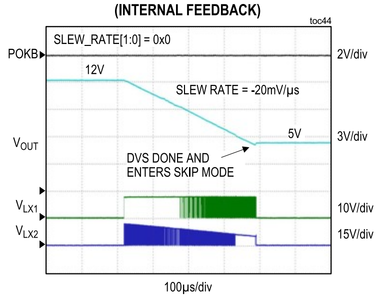
DYNAMIC VOLTAGE SCALING
(INTERNAL FEEDBACK)



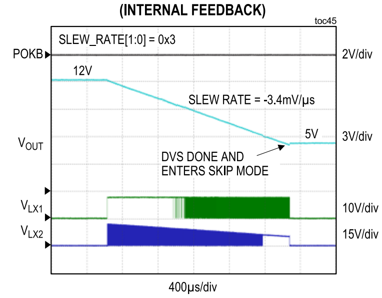
DYNAMIC VOLTAGE SCALING
(INTERNAL FEEDBACK)



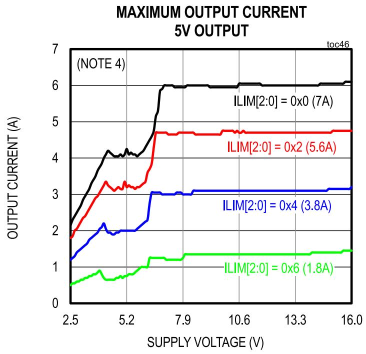
DYNAMIC VOLTAGE SCALING
(INTERNAL FEEDBACK)

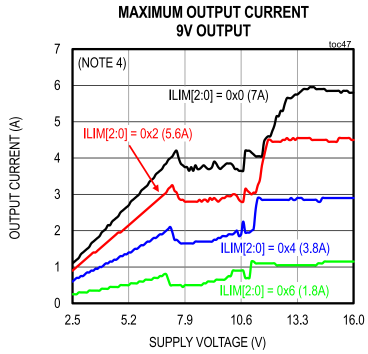


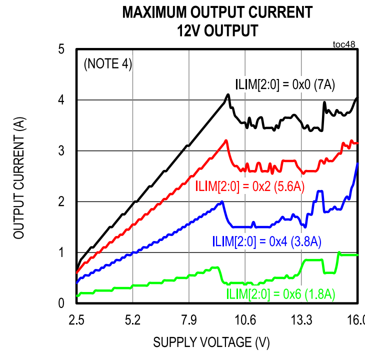
DYNAMIC VOLTAGE SCALING
(INTERNAL FEEDBACK)

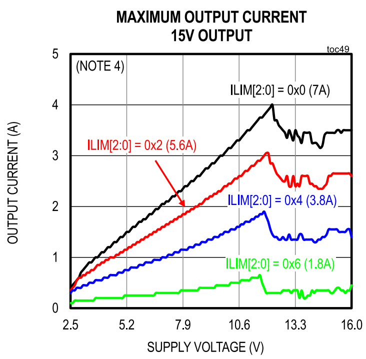


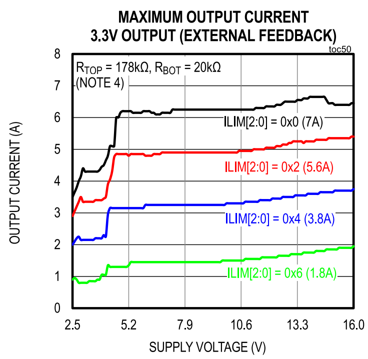
(V_{IN} = 7.6V, V_{OUT} = 5V, L = 1.5µH (Coilcraft XEL4020-152ME), C_{OUT} = 2x 22µF, FPWM = 0, ILIM[2:0] = 0x0 (7A), f_{SW} = 1.8MHz, internal feedback configuration, T_A = +25°C, unless otherwise noted. **Note 4**: Measurement limited by switching current limit. Actual maximum output current depends on system thermal performance.)





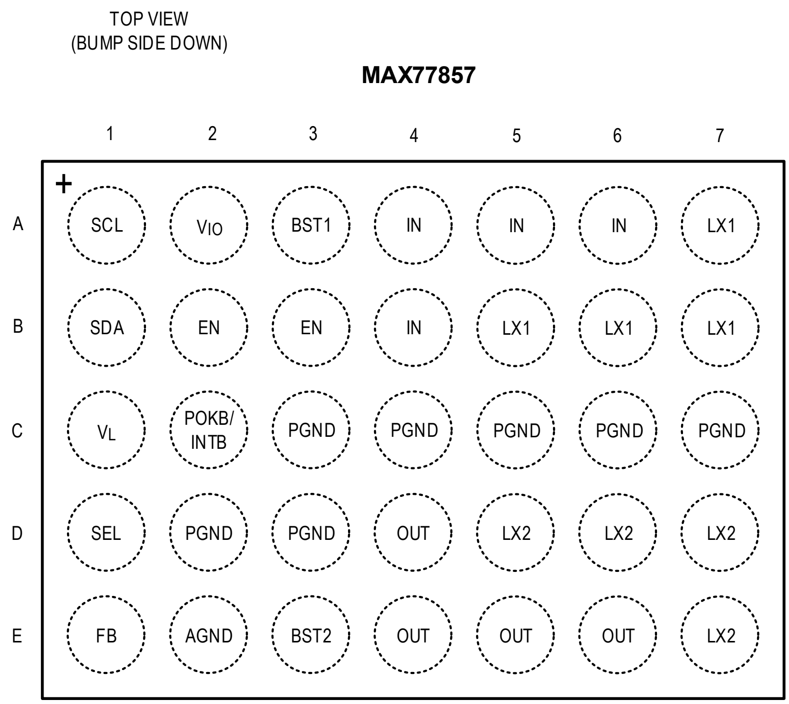






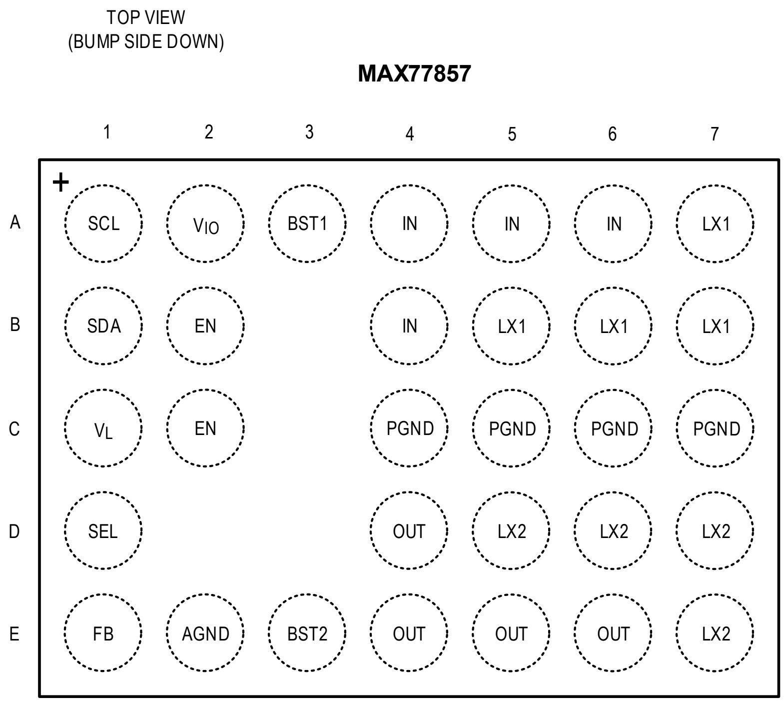
Pin Configurations

35 WLP



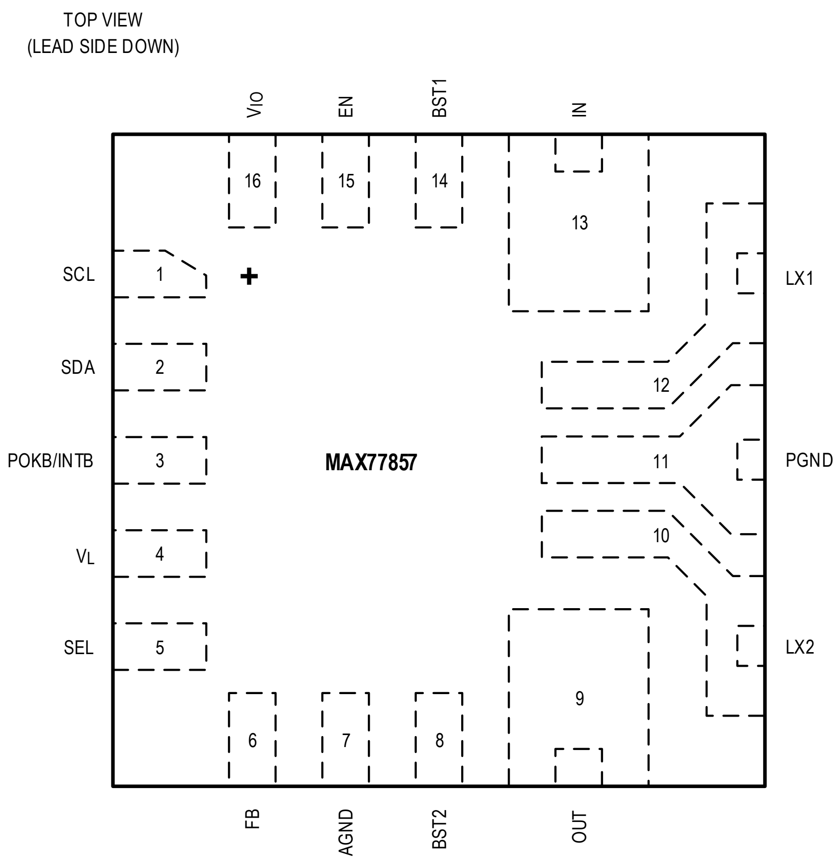
35 WLP
(2.83mm x 2.03mm, 0.4mm PITCH)

31 WLP



31 WLP
(2.83mm x 2.03mm, 0.4mm PITCH)

16 FC2QFN



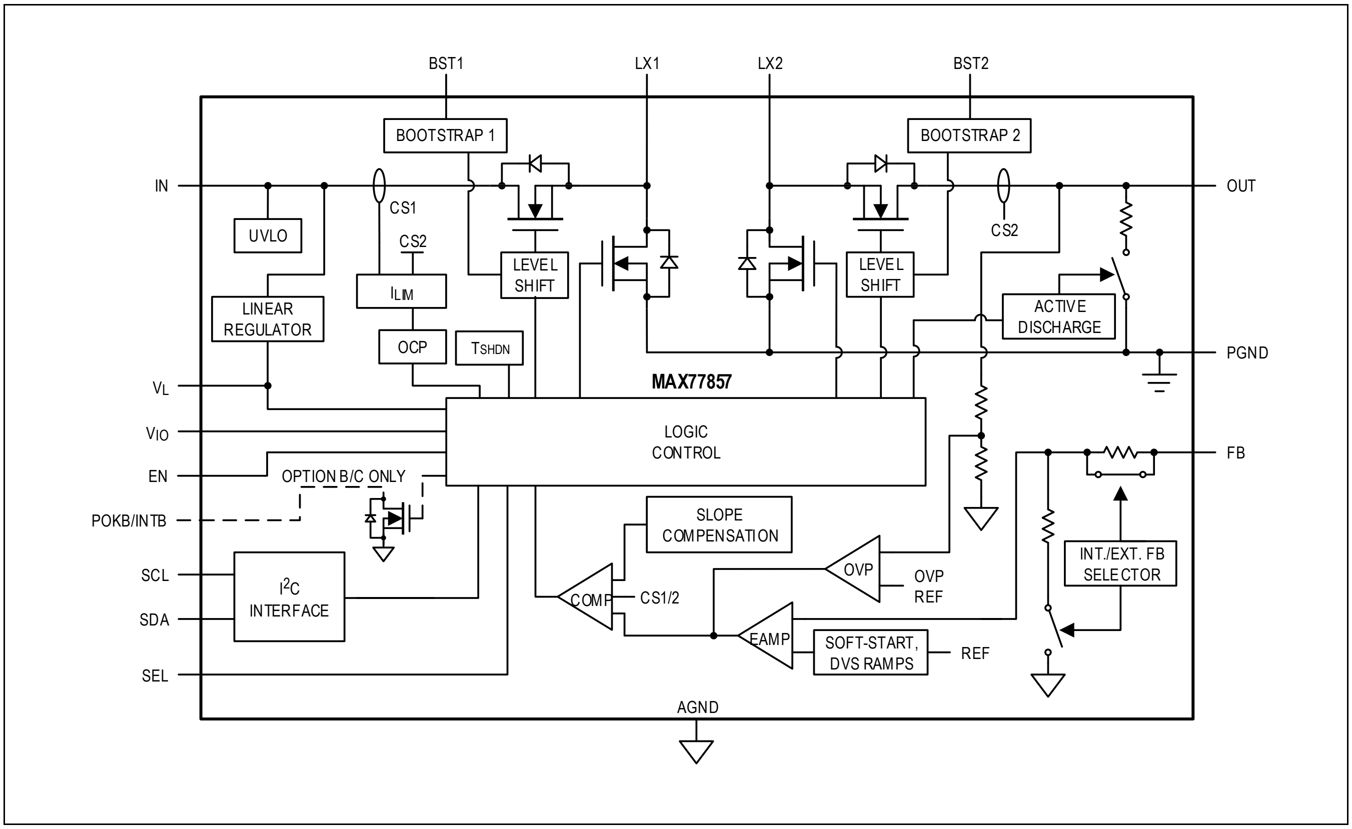
16 FC2QFN
(3.5mm x 3.5mm, 0.5mm PITCH)

Pin Descriptions

PIN			NAME	FUNCTION	Type
35 WLP	31 WLP	16 FC2QFN			
A1	A1	1	SCL	I2C Serial Interface Clock (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor when using the I2C Serial Interface or connect to AGND when the I2C Serial Interface is not in use.	Digital Input
B1	B1	2	SDA	I2C Serial Interface Data (High-Z in OFF State). Connect to V_{IO} with a 1.5kΩ to 2.2kΩ pullup resistor when using the I2C Serial Interface or connect to AGND when the I2C Serial Interface is not in use.	Digital I/O
C2		3	POKB/INTB	Buck-Boost Output Power-OK Monitor or Fault Interrupt Active-Low Open-Drain Output. Connect to V_{IO} with a 15kΩ pullup	Digital Output

				resistor. See the *Power-OK Monitor and Fault Interrupts* section for more details. Do not connect to this pin if not in use.	
C1	C1	4	V_L	Low-Voltage Internal Supply. Powered from IN. Bypass to AGND with a 10V 2.2μF ceramic capacitor. Do not load this pin externally except for usage stated in the *Non-I²C and Standalone Operation* section.	Analog
D1	D1	5	SEL	Configuration Selection. Connect a resistor between SEL and AGND. See *Table 2* for resistor values and configurations.	Analog
E1	E1	6	FB	**Using Internal Feedback Resistors:** Output Voltage Sense Input. Connect to the output at the point-of-load (close to output capacitor). **Using External Feedback Resistors:** Output Voltage Feedback Input. Connect to the center tap of an external resistor divider from OUT to AGND to set the output voltage. See the *Output Voltage Configuration* section for more details.	Analog
E2	E2	7	AGND	Analog Ground. Connect to PGND on the PCB. See the *PCB Layout Guideline* section for more details.	Ground
E3	E3	8	BST2	LX2 High-Side FET Driver Supply. Connect a 25V 0.22μF ceramic capacitor between BST2 and LX2.	Power Input
D4, E4, E5, E6	D4, E4, E5, E6	9	OUT	Buck-Boost Output. Bypass to PGND with two 25V 22μF ceramic capacitors as close as possible.	Power Output
D5, D6, D7, E7	D5, D6, D7, E7	10	LX2	Buck-Boost Switching Node 2	Power
C3, C4, C5, C6, C7, D2, D3	C4, C5, C6, C7	11	PGND	Power Ground. Connect to AGND on the PCB. See the *PCB Layout Guidelines* section for more details.	Ground
A7, B5, B6, B7	A7, B5, B6, B7	12	LX1	Buck-Boost Switching Node 1	Power
A4, A5, A6, B4	A4, A5, A6, B4	13	IN	Buck-Boost Input. Bypass to PGND with two 25V 10μF ceramic capacitors as close as possible.	Power Input
A3	A3	14	BST1	LX1 High-Side FET Driver Supply. Connect a 25V 0.22μF ceramic capacitor between BST1 and LX1.	Power Input
B2, B3	B2, C2	15	EN	Active-High Buck-Boost Enable Input. Compatible with the V_{IO} voltage domain. Pulldown internally with 0.1μA current source. See the *Non-I²C and Standalone Operation* section for more information if application desires to control EN with IN (i.e., start up MAX77857 whenever IN's voltage is valid).	Digital Input
A2	A2	16	V_{IO}	IO Voltage Supply. Bypass to AGND with a 6.3V 0.47μF ceramic capacitor. Registers are held in reset and regulator remains disabled when this pin's voltage is invalid.	Power Input

Functional Diagrams



Detailed Description

General Description

The MAX77857 is a high-efficiency, high-performance buck-boost converter targeted for systems requiring a wide input voltage range (2.5V to 16V). The IC can supply up to 6A of output current in buck mode and up to 4A in boost mode (boost ratio ≤ 1.3). The IC allows systems to change the output voltage and load current capacity dynamically through the I^2C serial interface. The IC supports the standard 5V/3A USB V_{BUS} requirement as well as USB PD requirements. Systems equipped with MAX77857 can provide fast-charging peripheral devices with higher output voltage, minimizing power loss across cable/connector and reducing charging time.

The IC operates either in SKIP mode or in forced-PWM (FPWM) mode, depending on the operating conditions, to optimize the efficiency. The default output voltage is 5V when using internal feedback resistors. The IC can also be configured to any default output voltages between 3V and 15V when using external feedback resistors. The output voltage is adjustable dynamically (DVS) between 4.5V and 15V in 73.5mV steps when using internal feedback resistors, or between 3V to 15V when using external feedback resistors (with step-size dependent on the external feedback resistor ratio), by programming the internal reference voltage through the I^2C serial interface. See the *Output Voltage Configuration* section for more information.

The SEL pin allows a single external resistor, R_{SEL}, to connect to AGND to program the following:

- I^2C Interface Slave Address (4 options)
- Switching Current Limit Threshold (4 options)
- Feedback Resistor Selection (Internal or external)

The different I^2C interface slave addresses accommodate multiple devices in a system with a limited I^2C bus. The different switching current limit thresholds allow the use of lower profile and smaller external components optimized for a particular application. The use of external feedback resistors allows for a wider output voltage range and customizable output voltages at startup. See the *SEL Pin Configuration* section for more information.

An optional I^2C serial interface allows dynamic control of the following:

- Output Voltage (using Internal Reference Voltage)
- Slew Rate of Output Voltage Change (4 options)
- Switching Current Limit Threshold (8 options)
- Switching Frequency (4 options)
- Forced-PWM Mode Operation
- Power-OK (POK) Status and Fault Interrupts
- Internal Compensation

The different switching frequencies provide options to improve the EMI performance by avoiding EMI sensitive frequency bands. The I^2C-programmed settings have priority over the R_{SEL} decoded settings.

Start-Up

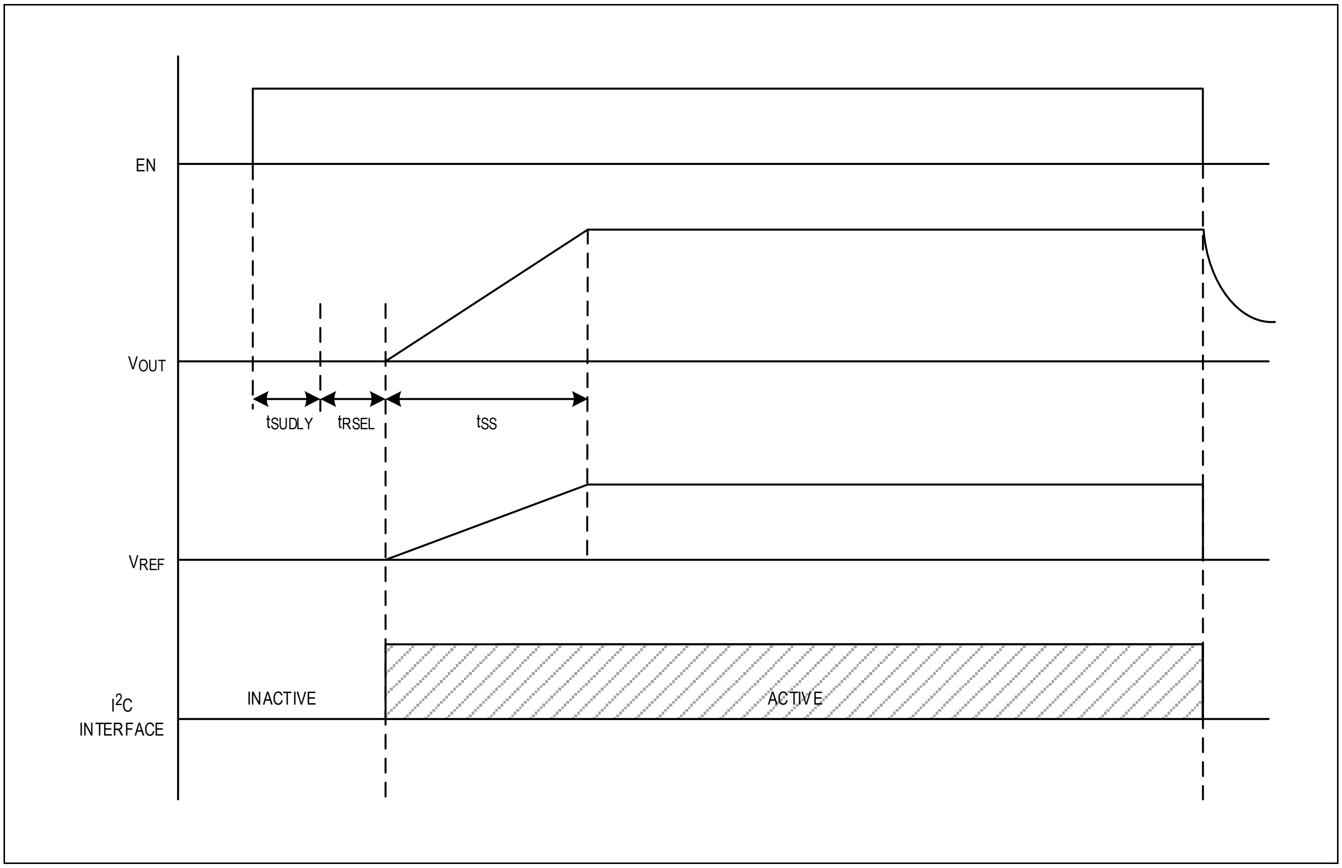


Figure 1. Start-Up Waveform

The start-up behavior is depicted in *Figure 1*. When input voltage V_{IN} is above UVLO threshold V_{UVLO_R} and EN pin is at logic HIGH, the IC starts up by first turning on the internal bias circuitry (V_L), which takes typically 100µs (t_{SUDLY}) to settle. The IC then senses the SEL pin resistance to set the I2C interface slave address, switching current limit threshold, and the use of internal or external feedback resistors. The R_{SEL} reading takes typically 200µs (t_{RSEL}) to complete. See the *SEL Pin Configuration* section for more information. Next, the IC checks if the V_{IO} voltage is valid. If so, it activates the I2C interface and begins the buck-boost soft-start process (see the *Soft-Start* section).

When EN toggles to logic HIGH, if output-active discharge is still active from a previous shutdown event, the IC waits for active discharge to finish before it initiates the startup sequence.

It is possible to use the internal regulator V_L to provide power to the V_{IO} pin, or to use V_{IN} to control the EN pin. See the *Non-I2C and Standalone Configuration* section for more details.

Soft-Start

The IC features soft-start to avoid a large amount of input current drawn from the system supply during startup. The default soft-start time (t_{SS}) is 2ms typical. During soft-start, the internal reference voltage (V_{REF}) slowly ramps up to the target value. The switching current limit threshold during soft-start is reduced to 3.8A if the I_{LIM} setting is set to be higher than such value (through R_{SEL}). If the I_{LIM} setting is set to be 3.8A or lower, then the same switching current limit threshold applies during soft-start. After soft-start finishes, the normal switching current limit threshold applies.

For the MAX77857C, if V_{OUT} does not reach POK level (typically 95% of the V_{OUT} target) after soft-start timer (t_{SS}) expires, the IC latches off. This behavior does not apply to the MAX77857A/B. See the *Immediate Shutdown and Latch-Off Condition* section for more information.

Shutdown

Pull the EN pin to logic LOW to shut down the IC. In a shutdown event, the IC stops switching, resets all registers, and activates the output-active discharge until the output voltage (V_{OUT}) drops below about 2.5V or after 500ms, whichever occurs sooner.

Immediate Latch-Off Conditions

The IC has a latch-off feature to protect itself under certain fault conditions by shutting down the buck-boost regulator.

Immediate Shutdown Conditions:

- IN UVLO: V_{IN} < Input UVLO Falling Threshold (V_{UVLO_F})
- V_{IO} UVLO: V_{VIO} < V_{IO} Valid Falling Threshold ($V_{VIO\_VALID\_F}$)

Latch-Off Conditions:

- Thermal Shutdown: T_J > Thermal-Shutdown Rising Threshold (T_{SHDN_R}) (See the *Thermal Shutdown (THS)* section)
- OCP/HARDSHORT: I_{LIM} Timer > 427µs (See the *Overcurrent Protection (OCP)* section)
- Start-Up (MAX77857C Only): V_{OUT} < POK Level after Soft-Start Timer (t_{SS}) Expires (See the *Soft-Start* section)

The events in this category are associated with potentially hazardous system states. Under immediate shutdown conditions, the IC shuts down the buck-boost regulator output and the I^2C serial communication bus and resets all registers, until the system recovers from these fault conditions. Under latch-off conditions, the IC shuts down the buck-boost regulator output only, while keeping the I^2C serial communication bus active and preserving the state of the registers. To recover from latch-off, the fault condition needs to be removed from the system, and a power-cycling EN or IN pin is required. Active discharge is engaged when the buck-boost regulator is shut down from all fault conditions except for thermal shutdown. See the *Output Active Discharge* section for more information.

Output Active Discharge

The IC includes an internal switch that provides a path to discharge the energy stored in the output capacitor to PGND. Output active discharge is activated whenever the buck-boost regulator is disabled (by a shutdown event or by any conditions described in the *Immediate Shutdown and Latch-Off Conditions* section, except for thermal shutdown). The amount of discharge current is 5mA typical when V_{OUT} is at 15V, and it decreases as V_{OUT} decreases during the discharge. When the active discharge is enabled, the EN pin control signal is ignored. After V_{OUT} has dropped below 2.5V (typical) or the 600ms timer has expired, whichever occurs sooner, active discharge is disabled. When the buck-boost regulator is operating, the internal discharging switch is disconnected from the output.

Buck-Boost Regulator

The MAX77857 buck-boost regulator utilizes a four-switch H-bridge configuration and contains buck, boost, or 3-phase operating modes. This topology maintains output voltage regulation over the input voltage range. The buck-boost regulator is ideal in up to 3-cell Li-ion battery-powered applications, providing 3V to 15V of output voltage range. High switching frequency and a unique control algorithm allow for the smallest solution size, low output noise, and the highest efficiency across a wide input voltage and output current range.

Buck-Boost Control Scheme

The buck-boost regulator operates using a fixed-frequency pulse-width modulated (PWM) control scheme with current-mode compensation. The buck-boost utilizes an H-bridge topology using a single inductor. The default switching frequency is 1.8MHz. The bitfield FREQ[1:0] sets the switching frequency. The different switching frequencies provide options to avoid EMI-sensitive frequency bands and improve EMI performance.

The H-bridge topology has three switching phases, as shown in *Figure 2*:

- Φ1 switch phase (HS1 = ON, LS2 = ON) stores energy in the inductor and ramps up inductor current at a rate proportional to input voltage divided by inductance: V_{IN}/L.
- Φ2 switch phase (HS1 = ON, HS2 = ON) ramps inductor current up (in buck mode) or down (in boost mode) at a rate proportional to the differential voltage across the inductor: $(V_{IN} - V_{OUT})/L$
- Φ3 switch phase (LS1 = ON, HS2 = ON) releases energy from the inductor and ramps down inductor current at a rate proportional to output voltage divided by inductance: $-V_{OUT}/L$.

Boost mode operation ($V_{IN} < V_{OUT}$) utilizes Φ1 and Φ2 within a single clock period. See the representation of the inductor current waveform for boost mode operation in *Figure 2*. Buck mode operation ($V_{IN} > V_{OUT}$) utilizes Φ2 and Φ3 within a single clock period. See the representation of the inductor current waveform for buck mode operation in *Figure 2*. 3-Phase mode operation ($V_{IN} \approx V_{OUT}$) utilizes Φ1, Φ2, and Φ3 within a single clock period. See the representation of the inductor current waveform for 3-phase mode operation in *Figure 2*.

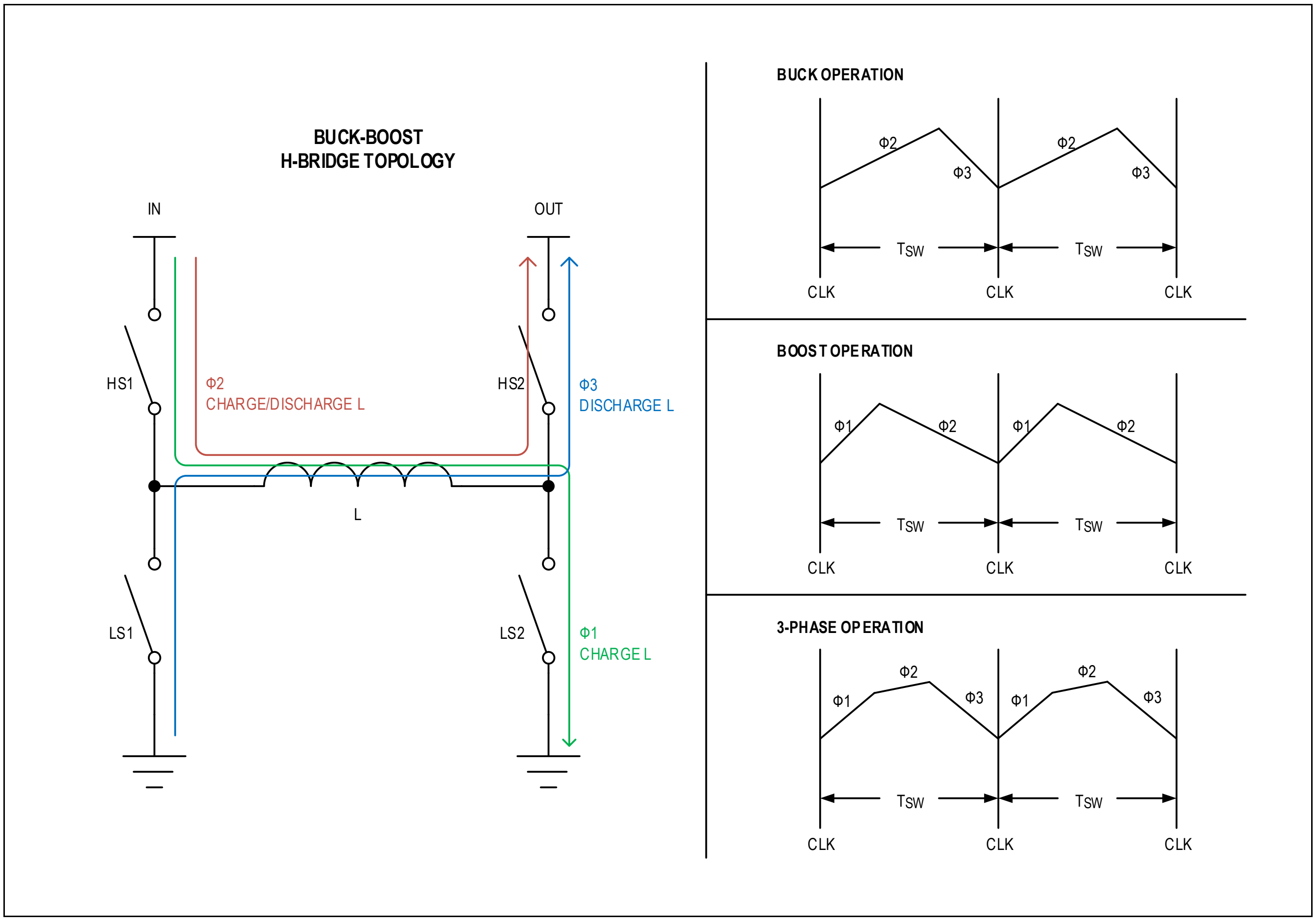


Figure 2. Buck-Boost H-Bridge Topology

SKIP Mode and Forced-PWM (FPWM) Mode

The IC automatically enters SKIP mode operation at no load or light load conditions to improve efficiency. In SKIP mode, output voltage V_{OUT} is regulated between SKIP mode upper threshold (V_{SKIP_UPPER}) and lower threshold (V_{SKIP_LOWER}), which are typically 3% and 1% above output voltage target (V_{TARGET}), respectively. The IC automatically transitions from SKIP mode to PWM mode depending on output load condition and input/output voltage ratio.

Another way to enable PWM mode operation is by writing 1 to the FPWM[0] bitfield through the I2C serial interface. This forces PWM mode operation regardless of output load current. Forced-PWM (FPWM) mode benefits applications where the lowest output ripple is required, whereas SKIP mode helps maximize the buck-boost regulator's efficiency at light loads.

Regardless of the FPWM[0] bitfield setting, the IC enters FPWM mode when V_{OUT} is changed to a different V_{TARGET} (DVS) to speed up the transition time. During DVS events that transition from a higher V_{OUT} to a lower one, the IC enters FPWM mode when V_{OUT} falls below V_{SKIP_LOWER} of the old V_{TARGET} and stays in FPWM mode until V_{OUT} falls below V_{SKIP_UPPER} of the new V_{TARGET}. Then V_{OUT} naturally drops based on the output load condition until it falls to V_{SKIP_LOWER}, at which the SKIP mode switching cycle resumes. *Figure 3* depicts such operation during DVS.

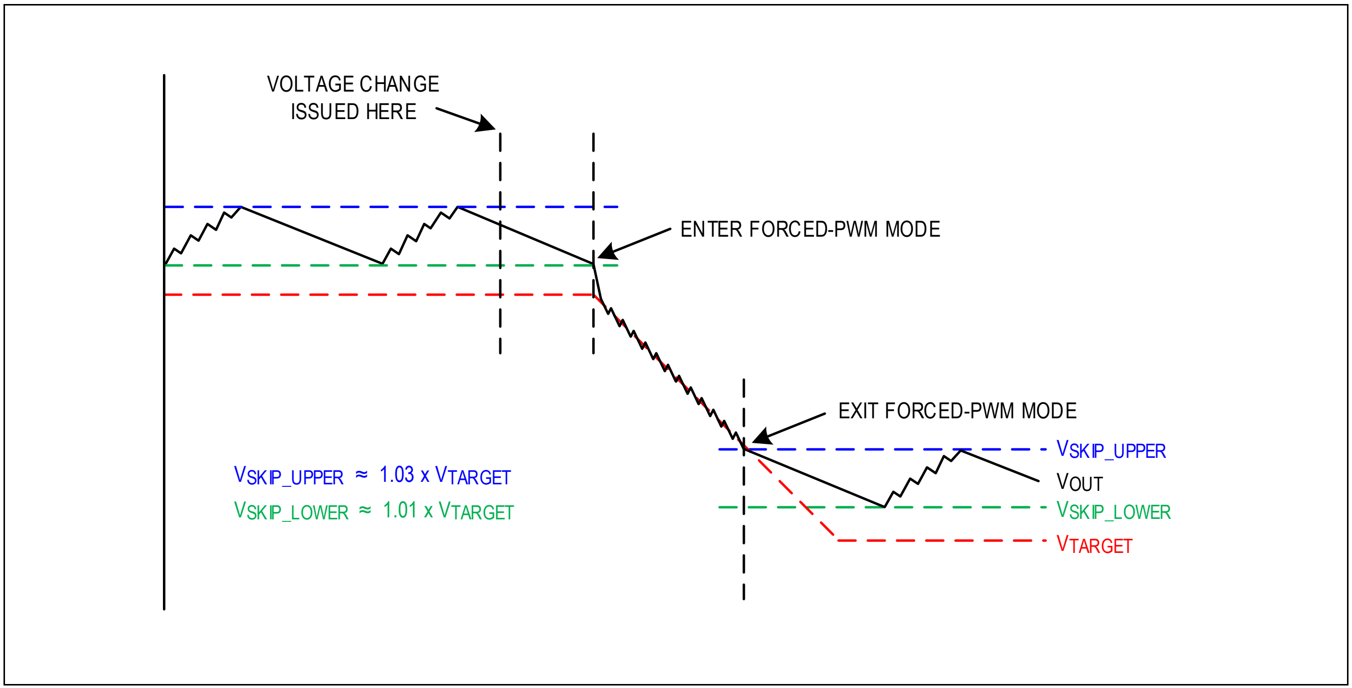


Figure 3. SKIP Mode Threshold and FPWM Mode Operation During DVS

Output Voltage Configuration

The IC supports a wide output voltage range between 4.5V and 15V when using internal feedback resistors, and between 3.0V and 15V when using external feedback resistors. The use of internal feedback resistors provides benefits of fewer external components and less overall solution size, while the use of external feedback resistors allows for wider output voltage range and customizable output voltage V_{OUT} at startup without using the I2C serial interface. The selection between using internal or external feedback resistors is configurable by R_{SEL}. See the *SEL Pin Configuration* section for more information.

Internal Feedback Resistor Configuration

When using internal feedback resistors, the V_{OUT} range is between 4.5V and 15V in 73.5mV steps. The default V_{OUT} is 5V (V_{REF} = 0.333V). Use the appropriate R_{SEL} value to configure the IC for using internal feedback resistors, and connect the FB pin directly to the OUT pin at the local output capacitor.

External Feedback Resistor Configuration

When using external feedback resistors, the V_{OUT} range is between 3.0V and 15V. The actual output voltage range and step size depend on the external feedback resistor ratio. Use the appropriate R_{SEL} value to configure the IC for using external feedback resistors, and connect a resistor divider between OUT, FB, and AGND as shown in *Figure 4*. It is also recommended to add a 10pF feedforward capacitor (C_{FF}) in parallel with the top feedback resistor (R_{TOP}). Choose R_{TOP} (from OUT to FB) between 150kΩ and 330kΩ. Resistors with 1% tolerance (or better) are highly recommended to keep the accuracy of V_{OUT}. Calculate the value of R_{BOT} (from FB to AGND) for the desired V_{OUT} at startup with the following equation:

$$R_{BOT} = \frac{R_{TOP} \times V_{REF}}{V_{OUT} - V_{REF}}, V_{OUT} \leq V_{OVP}$$

where V_{REF} is the default internal reference voltage.

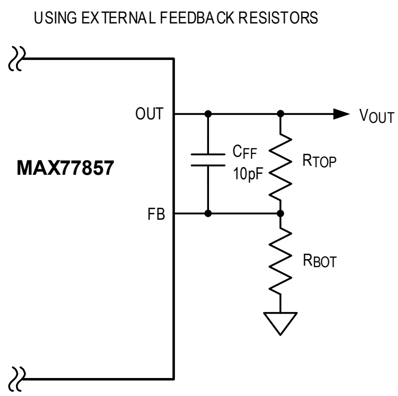


Figure 4. Connecting External Feedback Resistors to MAX77857

With default V_{REF} of 0.333V, *Table 1* lists the recommended external feedback resistor values (in E192 series) for common startup output voltages.

Table 1. Feedback Resistor Value Recommendations

DEFAULT V_{REF} (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	STARTUP V_{OUT} (V)	PROGRAMMABLE V_{OUT} RANGE (V)	V_{OUT} STEP SIZE (mV)
0.333	160	20	3	3.0 to 9.0	44.1
	178	20	3.3	3.0 to 9.9	48.5
	Internal Feedback Resistors		5	4.5 to 15	73.5
	312	12	9	8.1 to 15	132.3
	232	6.65	12	10.7 to 15	175.8
	234	5.3	15	13.5 to 15	221.2

Dynamic Voltage Scaling (DVS)

V_{OUT} is dynamically adjustable by programming V_{REF} through the I^2C serial interface. The bitfield VREF[7:0] sets the V_{REF}. V_{REF} ranges between 0.299V and 1V in 4.9mV steps. When using internal feedback resistors, V_{OUT} ranges between 4.5V and 15V in 73.5mV steps, and it can be calculated with the following equation:

$$V_{OUT} = V_{REF} \times 15$$

When using external feedback resistors, the V_{OUT} range and step size vary based on the external feedback resistor values. The V_{OUT} step size can be calculated with the following equation:

$$V_{OUT\_STEP} = \left(\frac{4.9mV}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP})$$

To calculate the V_{OUT} range, use the following equation and plug in the minimum V_{REF} of 0.299V and maximum V_{REF} of 1V:

$$V_{OUT} = \left(\frac{V_{REF}}{R_{BOT}}\right) \times (R_{BOT} + R_{TOP}), V_{OUT} \leq V_{OVP}$$

Note that V_{OUT} cannot exceed output voltage range, or it triggers overvoltage protection. See the *Overvoltage Protection (OVP)* section for more information.

The bitfield SLEW_RATE[1:0] sets the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$), with the default value of 4/3mV/μs. The actual V_{OUT} DVS ramp rate ($\Delta V_{OUT}/\Delta t$) can be calculated from the V_{REF} DVS ramp rate ($\Delta V_{REF}/\Delta t$) using the above equations for external feedback resistors. For example, if using internal feedback resistors, the default $\Delta V_{REF}/\Delta t$ of 4/3mV/μs corresponds to the $\Delta V_{OUT}/\Delta t$ of 20mV/μs.

SEL Pin Configuration

The SEL pin allows a single resistor (R_{SEL}) connecting the SEL pin to AGND to configure high side switching current limit threshold (I_{LIM}), I^2C serial interface slave address, and the use of internal or external feedback resistors. Resistors with 1% tolerance (or better) should be used for R_{SEL}. *Table 2* lists nominal R_{SEL} values with corresponding settings.

Table 2. MAX77857 R_{SEL} Selection Table

R_{SEL} (Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C SLAVE ADDRESS (7-BIT)	R_{SEL} (Ω)	FEEDBACK RESISTOR SELECTION	TYPICAL I_{LIM} (A)	I^2C SLAVE ADDRESS (7-BIT)
SHORT TO GND	Internal feedback resistors	7.0	110 0110 (0x66)	3740	External feedback resistors	7.0	110 0110 (0x66)
200			110 0111 (0x67)	8060			110 0111 (0x67)
309			110 1110 (0x6E)	12400			110 1110 (0x6E)
422			110 1111 (0x6F)	16900			110 1111 (0x6F)
536		5.6	110 0110 (0x66)	21500		5.6	110 0110 (0x66)
649			110 0111 (0x67)	26100			110 0111 (0x67)
768			110 1110 (0x6E)	30900			110 1110 (0x6E)
909			110 1111 (0x6F)	36500			110 1111 (0x6F)
1050		3.8	110 0110 (0x66)	42200		3.8	110 0110 (0x66)
1210			110 0111 (0x67)	48700			110 0111 (0x67)
1400			110 1110 (0x6E)	56200			110 1110 (0x6E)
1620			110 1111 (0x6F)	64900			110 1111 (0x6F)
1870		1.8	110 0110 (0x66)	75000		1.8	110 0110 (0x66)
2150			110 0111 (0x67)	86600			110 0111 (0x67)
2490			110 1110 (0x6E)	100000			110 1110 (0x6E)
2870			110 1111 (0x6F)	OPEN			110 1111 (0x6F)

Internal Compensation Options

For designs looking to optimize its performance, the COMP[2:0] bitfield for internal compensation adjustment is available through the I^2C serial interface. For those systems that do not utilize the I^2C serial interface, stability can still be optimized by adjusting output capacitance. In general, performance can be further optimized by lowering the COMP[2:0] bitfield value or by adding additional output capacitance.

Power-OK Monitor and Fault Interrupts (MAX77857B/C Only)

The IC features a power-OK (POK) monitor and fault interrupt functionalities. The status of POK and fault interrupts are stored in register 0x10 (INT_SRC), which can be accessed through the I^2C serial interface.

The POK bit in the INT_SRC register is active-high (so the POKB/INTB pin is active-low), and it is constantly updated based on the actual V_{OUT} level while the buck-boost regulator is enabled. The POK bit is logic LOW when V_{OUT} falls below 85% (typical) of the target voltage, and it is logic HIGH when V_{OUT} rises above 95% (typical) of the target voltage. During a soft-start or V_{OUT} DVS event, V_{OUT} sensing for POK is temporarily disabled, and the POK bit holds the value prior to the soft-start or V_{OUT} DVS event. V_{OUT} sensing for POK resumes after soft-start or DVS finishes.

The fault interrupt bits in the INT_SRC register are active-high (so POKB/INTB pin is active-low). Any of the following fault conditions triggers the interrupt by setting the corresponding fault interrupt bit to 1 in the INT_SRC register. The interrupts can only be reset by power cycling the IN or EN pins.

- OVP: The IC activates overvoltage protection. (See the *Overvoltage Protection (OVP)* section.)
- HARDSHORT: The IC is latched off by output hard-short event. (See the *Overcurrent Protection (OCP)* section.)
- THS: The IC is latched off by a thermal shutdown event. (See the *Thermal Shutdown (THS)* section.)
- OCP: The IC is latched off by overcurrent protection. (See the *Overcurrent Protection (OCP)* section.)

The IC also features an active-low, open-drain POKB/INTB digital output pin to reflect the status of POK and/or fault interrupts. Connect POKB/INTB pin with a 15kΩ pullup resistor to V_{IO}. The signal on POKB/INTB is logical NOR of all unmasked POK and fault interrupt bitfields in INT_SRC register. This pin is logic LOW when V_{OUT} is above the POK threshold (POK unmasked) or when there is an unmasked interrupt event. *Table 3* shows the truth table of POKB/INTB pin, with all bits unmasked (INT_MASK = 0x00).

The connection of individual POK and fault interrupt bitfield in the INT_SRC register to the POKB/INTB pin can be masked by writing 1 to the corresponding mask bitfield in register 0x11 (INT_MASK). For example, when the POK_M bitfield in INT_MASK register is 1, any activities on the POK bitfield in the INT_SRC register do not affect the POKB/INTB pin.

Table 3. POKB/INTB Pin Truth Table

POK	OVP	HARDSHORT	THS	OCP	POKB/INTB
0	0	0	0	0	HIGH
1	X	X	X	X	LOW
X	1	X	X	X	LOW
X	X	1	X	X	LOW
X	X	X	1	X	LOW
X	X	X	X	1	LOW

**With all POK/fault interrupt bits unmasked (INT_MASK = 0x00)*

When intending to use the POKB/INTB pin for POK, it is recommended to mask all fault interrupt bits (and unmask POK bit) by writing 0x0F to the INT_MASK register (default). On the other hand, when intending to use this pin for fault interrupts, it is recommended to mask the POK bit (and unmask all fault interrupt bits) by writing 0x10 to the INT_MASK register. See the *Register Map* for more details.

Protection Features

Undervoltage Lockout (UVLO)

The IC's undervoltage lockout feature prevents operation in abnormal input conditions when input voltage V_{IN} falls below IN UVLO falling threshold (V_{UVLO_F}) or when V_{IO} voltage (V_{VIO}) falls below V_{IO} valid falling threshold ($V_{VIO\_VALID\_F}$). Regardless of EN pin status, the IC becomes disabled and all registers reset until V_{IN} rises above IN UVLO rising threshold (V_{UVLO_R}) and V_{IO} rises above V_{IO} valid rising threshold ($V_{VIO\_VALID\_R}$).

Overvoltage Protection (OVP)

The IC's overvoltage protection feature ensures that the output voltage V_{OUT} never exceeds the overvoltage limit threshold (V_{OVP}, 16.4V typical). In this fault condition, V_{OUT} rises to V_{OVP}. The IC detects overvoltage, sets OVP[0] interrupt bit in INT_SRC register (address 0x10), and activates overvoltage protection by disabling high-side MOSFETs and enabling low-side MOSFETs until V_{OUT} drops below the overvoltage release threshold (V_{OVP_REL}, 15.5V typical). As a result, V_{OUT} regulates between V_{OVP} and V_{OVP_REL}.

Overcurrent Protection (OCP)

The IC features a robust switching current limit scheme that protects the IC and inductor during overload and fast transient conditions. The current sensing circuit takes current information from the high-side MOSFETs to determine the peak switching current ($R_{DS(ON)}$ x I_L).

The IC provides eight different cycle-by-cycle current limit thresholds (I_{LIM}) for the high-side MOSFET to support different output current levels. The bitfield ILIM[2:0] or R_{SEL} resistor value sets the I_{LIM}. Note that while all eight options are programmable through the I^2C serial interface, only four options are selectable through R_{SEL}. When the I_{LIM} setting from the I^2C serial interface and the one from R_{SEL} differs, the I^2C setting has priority over R_{SEL}.

When inductor current (I_L) reaches the programmed current limit level (I_{LIM}), the IC enters the OCP state. The inductor charging phase terminates, and the discharging phase (Φ3) begins for the rest of the switching period. The charging phase begins again at the next clock cycle. If during the OCP state V_{OUT} drops below 70% of the target, then the IC enters the HARD-SHORT state. Like the OCP state, the inductor charging phase terminates and the discharging phase (Φ3) begins. But unlike the OCP state, the discharging phase does not terminate until the inductor current has dropped below the valley current limit threshold (I_{LIM_VALLEY}), and then the inductor charging phase follows. As a result, the effective switching frequency in the HARD-SHORT state differs from normal switching frequency set in the FREQ[1:0] register bitfield. See *Table 4* for available I_{LIM} options and their corresponding I_{LIM_VALLEY} values.

Table 4. MAX77857 Switching Current Limit Options

<table>
<tr><th>ILIM[2:0] BITFIELD VALUE</th><th>NORMAL CURRENT LIMIT (I_{LIM})</th><th>VALLEY CURRENT LIMIT (I_{LIM_VALLEY})</th><th>SOFT-START CURRENT LIMIT (I_{LIM_SS})</th><th>SKIP MODE CURRENT LIMIT (I_{LIM_SKIP})</th></tr>
<tr><td>000 (0x0)</td><td>7.0A</td><td rowspan="2">2.5A</td><td rowspan="5">3.8A</td><td rowspan="8">1.4A</td></tr>
<tr><td>001 (0x1)</td><td>6.2A</td></tr>
<tr><td>010 (0x2)</td><td>5.6A</td><td rowspan="2">1.8A</td></tr>
<tr><td>011 (0x3)</td><td>4.6A</td></tr>
<tr><td>100 (0x4)</td><td>3.8A</td><td rowspan="2">1.0A</td></tr>
<tr><td>101 (0x5)</td><td>2.8A</td><td>2.8A</td></tr>
<tr><td>110 (0x6)</td><td>1.8A</td><td rowspan="2">0.3A</td><td>1.8A</td></tr>
<tr><td>111 (0x7)</td><td>0.99A</td><td>0.99A</td></tr>
</table>

The IC also includes a 427μs I_{LIM} timer to latch off the buck-boost regulator. This timer is activated in the HARD-SHORT state for the MAX77857A/B and the MAX77857C (boost mode in WLP package), and in both OCP and HARD-SHORT states for the MAX77857C (buck mode in WLP package, all modes in FC2QFN package). When this timer expires after 427μs (e.g., when I_L has reached I_{LIM} continuously for 427μs), the IC latches off the buck-boost regulator. If the latch-off occurs in the OCP state, then the OCP[0] interrupt bit is set. If latch-off occurs in the HARD-SHORT state, then both OCP[0] and HARDSHORT[0] interrupt bits are set. *Figure 5* and *Figure 6* depict the behavior during OCP and HARD-SHORT states in each MAX77857 IC version. See the *Immediate Shutdown and Latch-Off Conditions* section for information about latch-off. If prior to latch-off, the overcurrent event disappears and I_L no longer reaches I_{LIM}, the IC resets the timer.

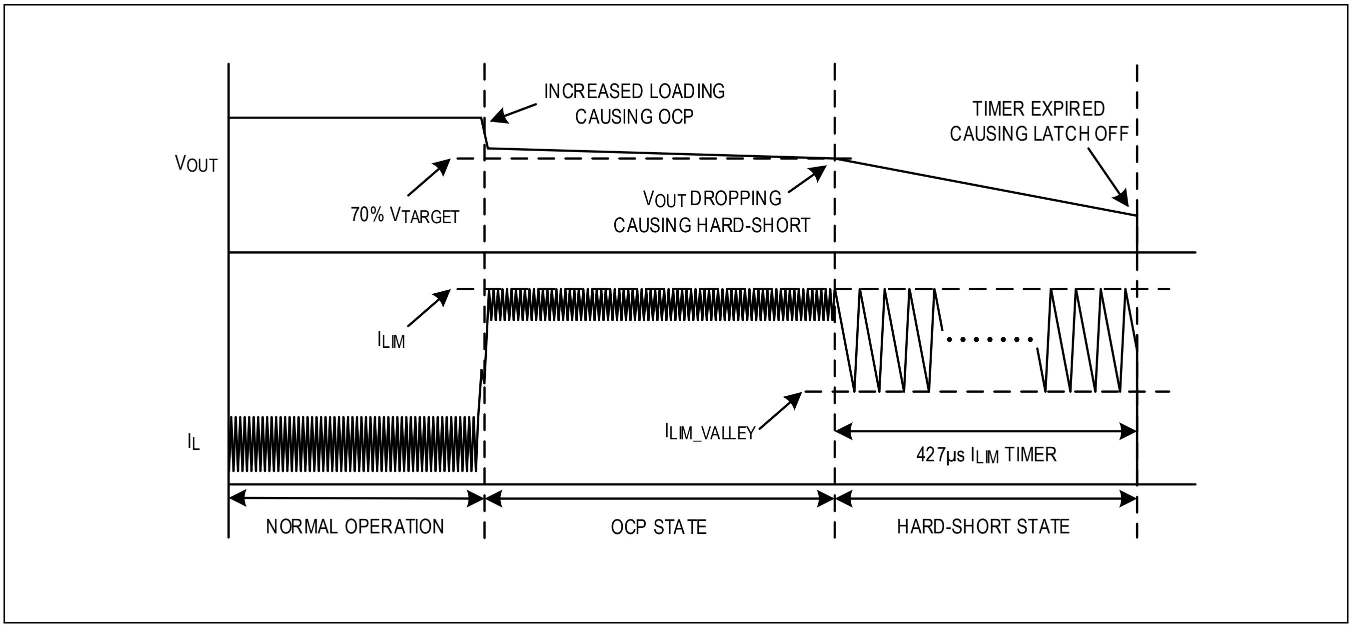


Figure 5. MAX77857A/B and MAX77857C (Boost Mode in WLP Package) Overcurrent and Output Hard-Short Behavior

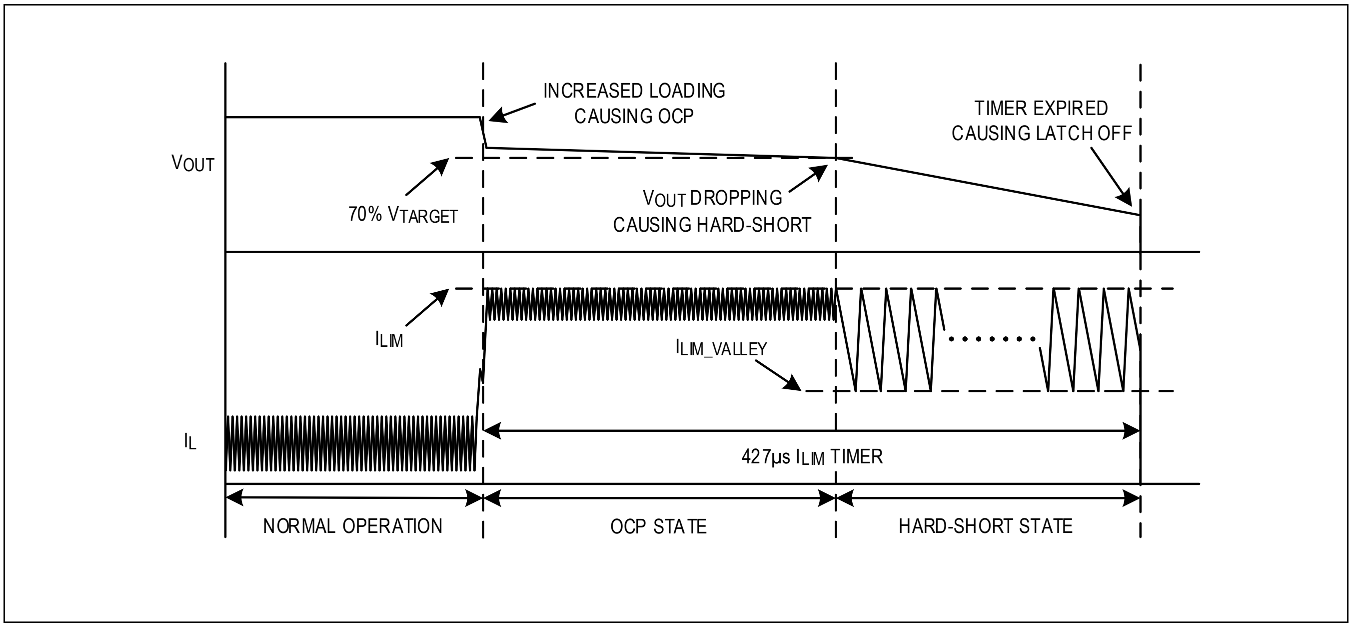


Figure 6. MAX77857C (Buck Mode in WLP Package, All Modes in FC2QFN Package) Overcurrent and Output Hard-Short Behavior

Thermal Shutdown (THS)

The IC contains an internal thermal protection circuit that monitors die temperature. *Figure 7* depicts the thermal shutdown behavior. The IC enters thermal shutdown (THS) when junction temperature (T_J) exceeds thermal shutdown rising threshold (T_{SHDN_R}, 150ºC typ). In THS, the IC is latched off and THS[0] interrupt bit is set. Unlike other latch-off events, output active discharge is not activated. Power cycling the EN or IN pins resets the THS[0] interrupt bit and is required to recover from thermal shutdown. See the *Immediate Shutdown and Latch-Off Conditions* section for more information.

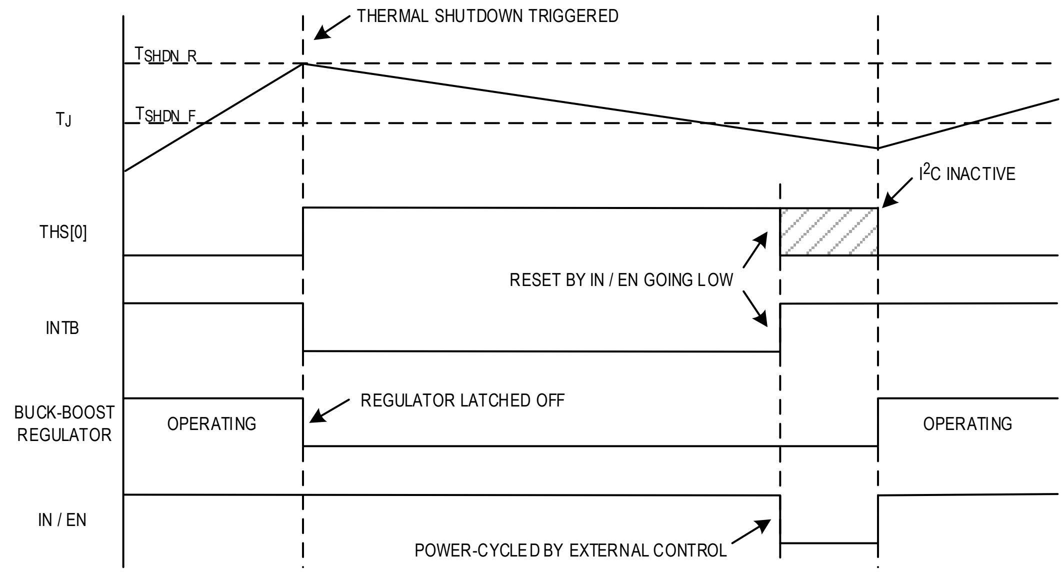


Figure 7. Thermal Shutdown Recovery

Detailed Description–I2C Serial Interface

General Description

The I2C-compatible 2-wire serial interface is used for setting output voltage and other functions. See the *Register Map* for available settings.

The I2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I2C bus is a multi-master bus. The maximum number of devices that can be attached to the bus is only limited by bus capacitance.

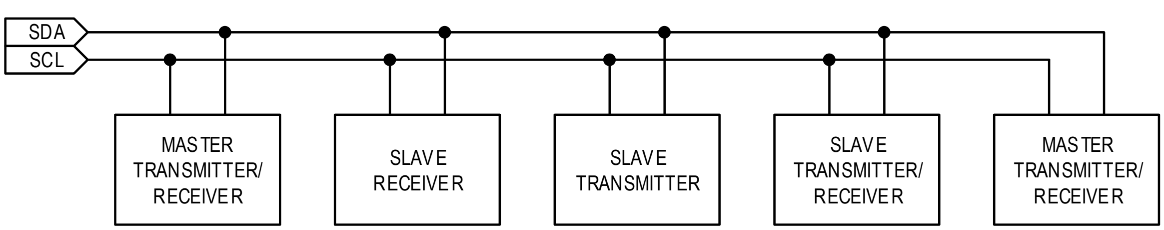


Figure 8. Functional Logic Diagram for the Communications Controller

Figure 8 shows an example of a typical I2C bus system. A device on the I2C bus that sends data to the bus is called a “transmitter.” A device that receives data from the bus is called a "receiver.” A device that initiates a data transfer and generates SCL clock signals to control the data transfer is called a “master.” Any device being addressed by the master is called a “slave.” The MAX77857 is a slave on the I2C bus, and it can be both a transmitter and a receiver.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on the SDA must remain stable during the HIGH portion of the SCL clock pulse. Changes in the SDA while the SCL is HIGH are control signals (START and STOP conditions).

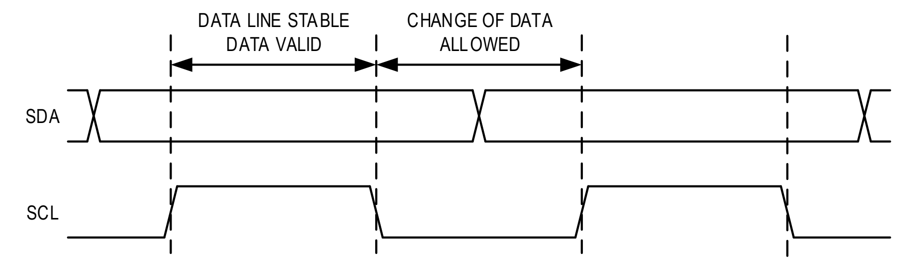


Figure 9. I²C Bit Transfer

START and STOP Conditions

When the I2C serial interface is inactive, the SDA and SCL idle HIGH. A master device initiates communication by issuing a START condition (S). A START condition (S) is a HIGH-to-LOW transition on the SDA while the SCL is HIGH. A STOP condition (P) is a LOW-to-HIGH transition on the SDA while the SCL is HIGH.

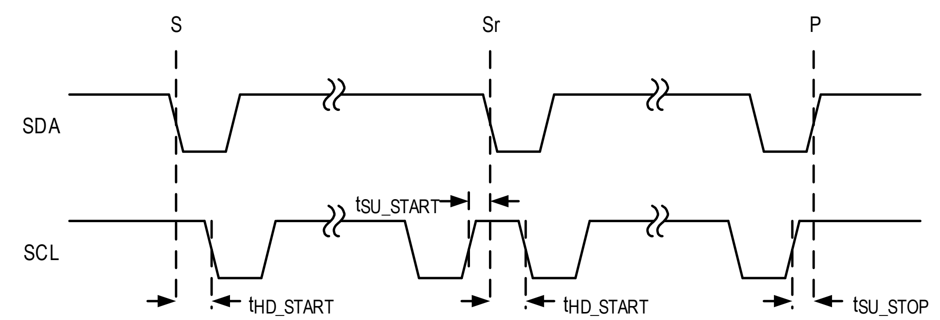


Figure 10. START and STOP Conditions

A START condition (S) from the master device signals the beginning of a transmission. The master terminates transmission by issuing a NOT-ACKNOWLEDGE (nA) followed by a STOP condition (P).

A STOP condition (P) frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP condition (P) in order to maintain control of the bus. In general, a REPEATED START (Sr) command is functionally equivalent to a regular START condition (S).

When a STOP condition (P) or incorrect address is detected, the MAX77857 internally disconnects the SCL from the I2C serial interface until the next START condition (S), minimizing digital noise and feed-through.

Acknowledge Bit

Both the I^2C bus master device and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull the SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it LOW during the HIGH portion of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows the SDA to be pulled HIGH before the rising edge of the acknowledge-related clock pulse and leaves it HIGH during the HIGH portion of the clock pulse.

Monitoring the acknowledge bits allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication later.

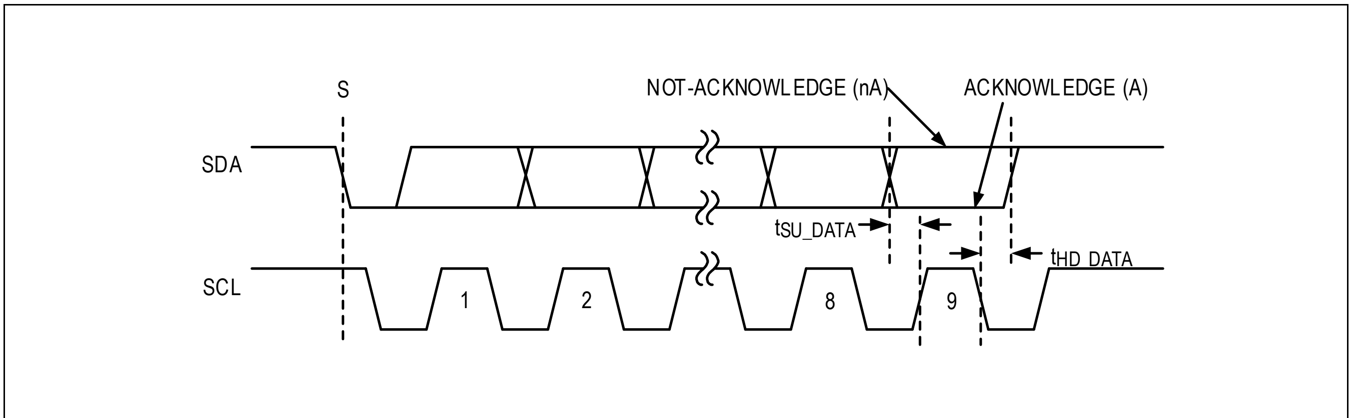


Figure 11. Acknowledge Bit

Slave Address

Table 5 shows the available I^2C slave addresses of the MAX77857. The MAX77857 supports up to four different slave addresses through R_{SEL} programming for when multiple devices in the same I^2C bus line need to be used or when there is a conflict between the slave addresses in the system. See *Table 2* for available R_{SEL} values and the corresponding I^2C slave addresses.

Table 5. MAX77857 I^2C Slave Addresses

7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
110 0110 (0x66)	1100 1100 (0xCC)	1100 1101 (0xCD)
110 0111 (0x67)	1100 1110 (0xCE)	1100 1111 (0xCF)
110 1110 (0x6E)	1101 1100 (0xDC)	1101 1101 (0xDD)
110 1111 (0x6F)	1101 1110 (0xDE)	1101 1111 (0xDF)

Figure 12 shows the 7-bit slave address at 0x66.

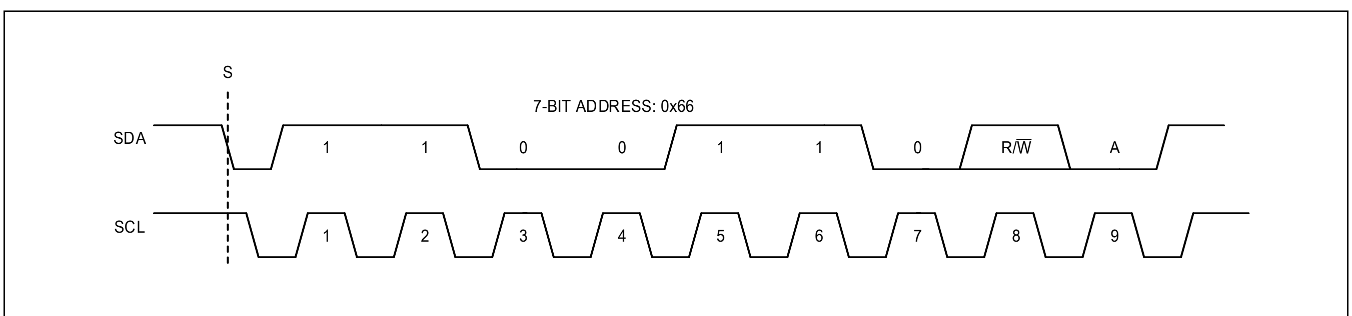


Figure 12. Slave Address Byte Example

Clock Stretching

In general, the clock signal generation for the I^2C bus is the responsibility of the master device. The I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77857 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77857 does not implement the I^2C specification "General Call Address." The MAX77857 does not issue an ACKNOWLEDGE (A) if it detects the "General Call Address" (0000 0000).

Communication Speed

The MAX77857 supports the following communication speeds:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast-mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speed, the pullup resistance must be decreased to maintain a reasonable time constant. In general, for a bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. The major considerations with respect to the MAX77857 are as follows:

- The master device shall use current source pullups to shorten the signal rise times.
- The slave device must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition (P), the MAX77857 inputs filters are set to standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters to high-speed mode, use the protocol described in the *Engage in High-Speed Mode* section.

Communication Protocols

The MAX77857 supports both writing to and reading from its registers.

Writing to a Single Register

Figure 13 shows the protocol for writing to a single register. This protocol is the same as the “Write Byte” protocol in the SMBus specification.

The “Write Byte” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

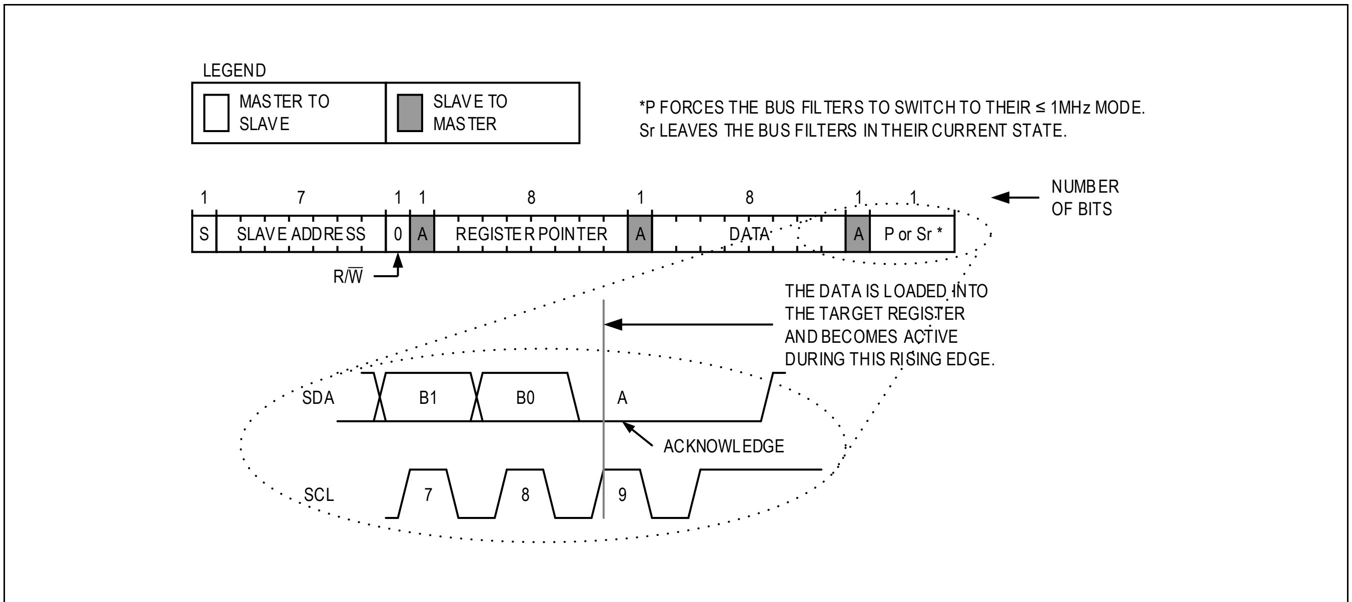


Figure 13. Writing to a Single Register

Writing to Sequential Registers

Figure 14 shows the protocol for writing to sequential registers. This protocol is similar to the "Write Byte" protocol, except the master device continues to write after the slave device receives the first byte of data. When the master is done writing data, it issues a STOP condition (P) or REPEATED START condition (Sr).

The "Writing to Sequential Registers" protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of the SCL, the data byte is loaded into its target register and the data becomes active.
8. Step 6 to step 7 are repeated as many times as the master requires.
9. During the last acknowledge-related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

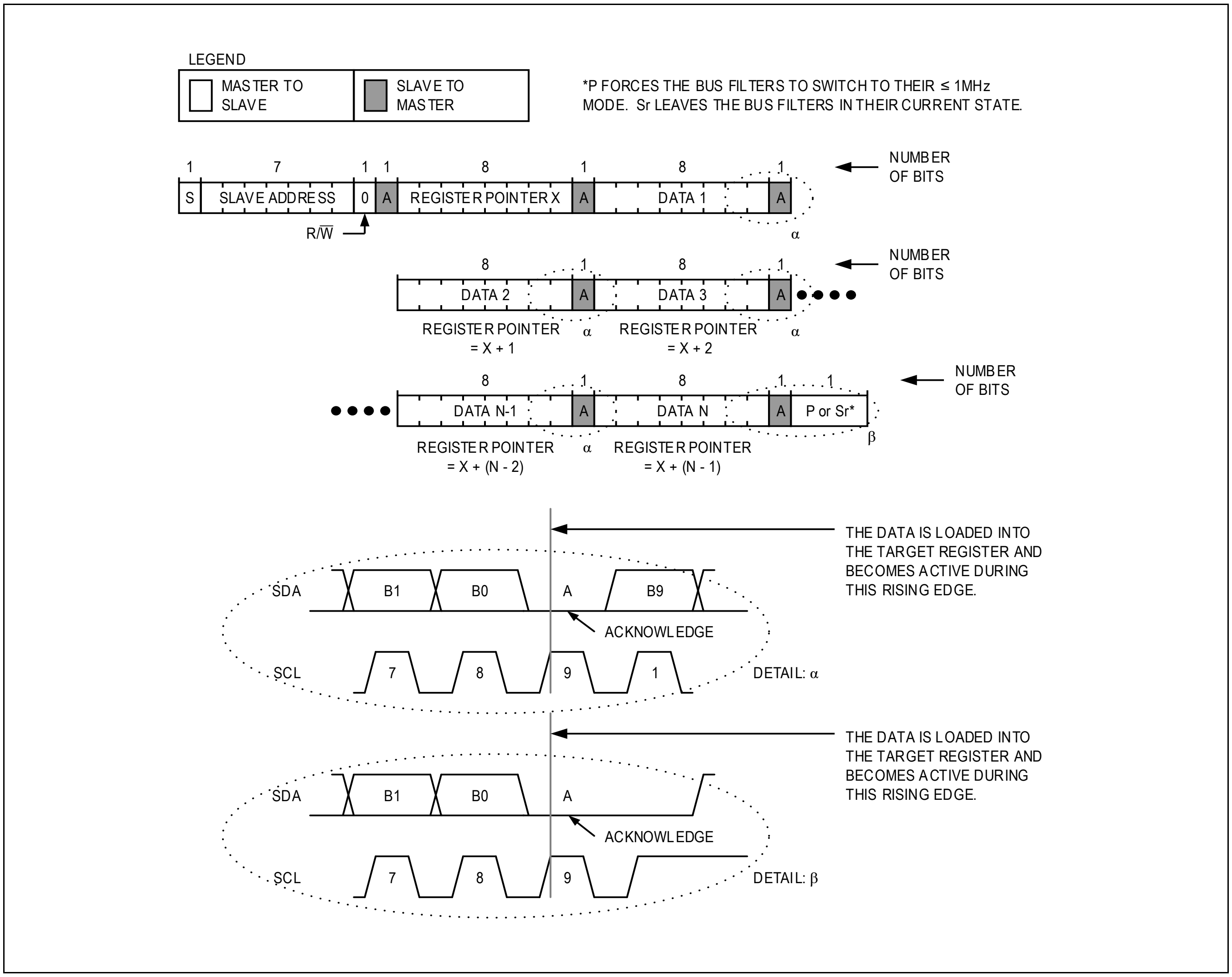


Figure 14. Writing to Sequential Registers

Reading from a Single Register

Figure 15 shows the protocol for reading from a single register. This protocol is the same as the “Read Byte” protocol in the SMBus specification.

The “Read Byte” protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW
9. The addressed slave places 8 bits of data from the location specified by the register pointer on the bus.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

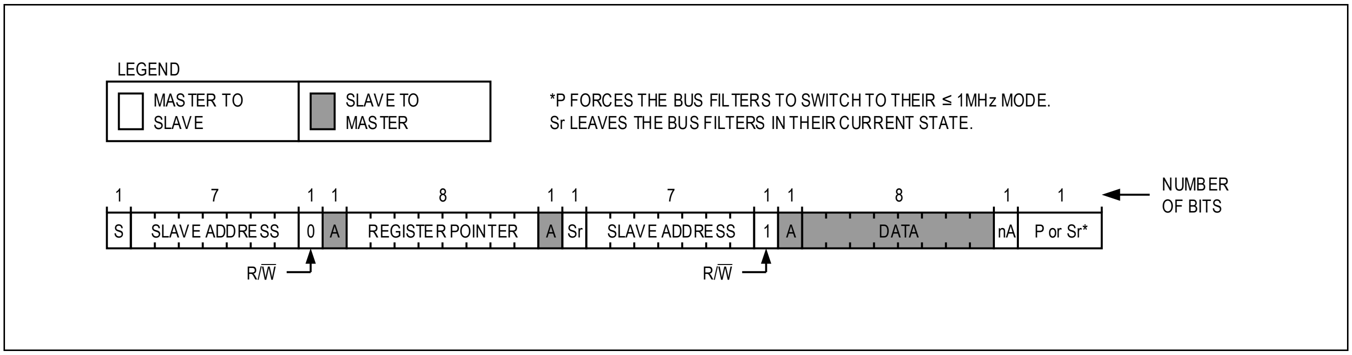


Figure 15. Reading to a Single Register

Reading from Sequential Registers

Figure 16 shows the protocol for reading from sequential registers. This protocol is similar to the "Read Byte" protocol, except the master device issues an ACKNOWLEDGE (A) to signal the slave device that it wants more data. When the master device has all the data it requires, it issues a NOT-ACKNOWLEDGE (nA) and a STOP condition (P) to end the transmission.

The "Continuous Read from Sequential Registers" protocol is as follows:

1. The master sends a START condition (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling the SDA LOW.
9. The addressed slave places 8 bits of data from the location specified by the register pointer on the bus.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 and 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START condition (Sr) leaves the bus input filters in their current state.

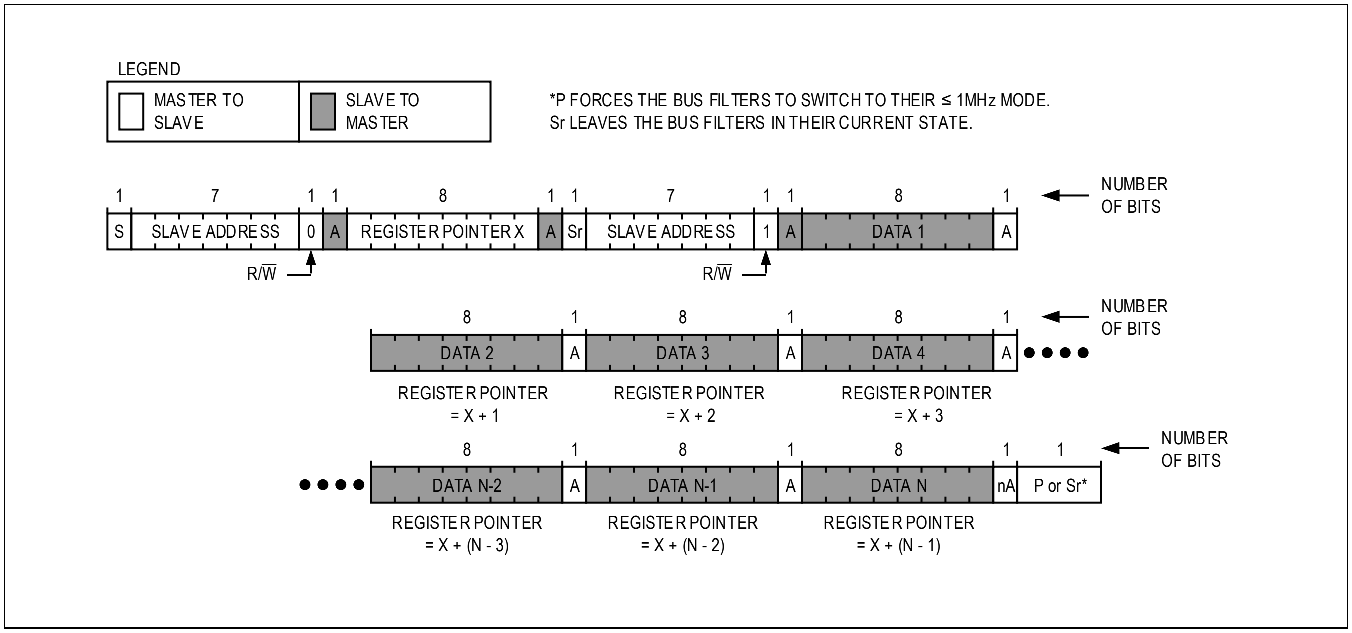


Figure 16. Reading from Sequential Registers

Engage in High-Speed Mode

Figure 17 shows the protocol for engaging in high-speed mode operation, which allows the bus to operate at speeds up to 3.4MHz.

The protocol to engage in high-speed mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START condition (S).
3. The master sends the 8-bit master code 0000 1xx0, where 'xx' are don't care bits.
4. The addressed slave issues a NOT-ACKNOWLEDGE (nA).
5. The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a STOP condition (P) is issued. Issuing a STOP condition (P) ensures that the bus input filters are set for 1MHz or slower operation.

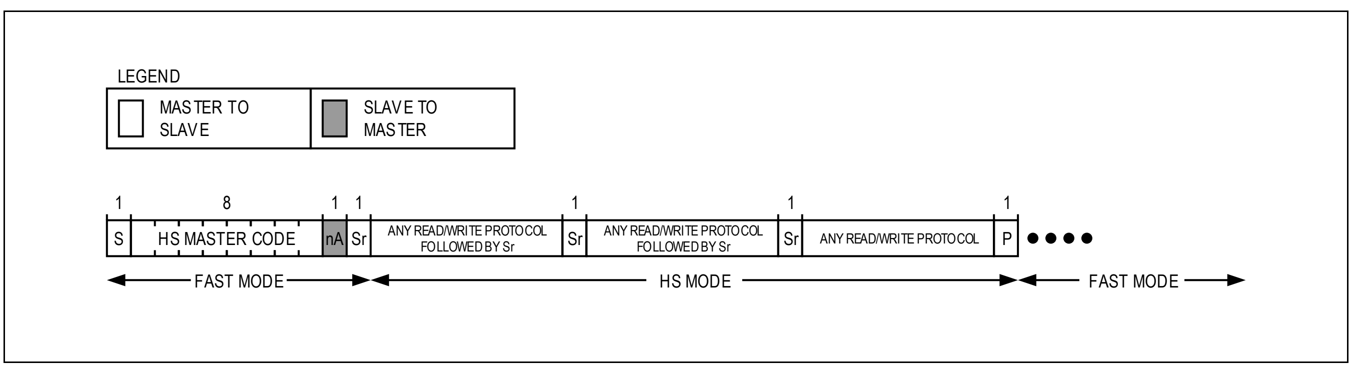


Figure 17. Engage in High-Speed Mode Protocol

High-Speed Mode Extension

The MAX77857 supports the high-speed mode extension feature. This feature keeps the IC in high-speed mode operation even after receiving a STOP condition (P). This eliminates the need for the master device to re-issue the command for engaging in high-speed mode when the master device wants to stay in high-speed mode for multiple read/write cycles.

Figure 18 shows the I2C mode transition state diagram. Write 1 to the HS_EXT[0] bitfield to enable the high-speed mode extension when the MAX77857 is in low-speed mode. Enabling the high-speed mode extension when the MAX77857 is in high-speed mode is not supported.

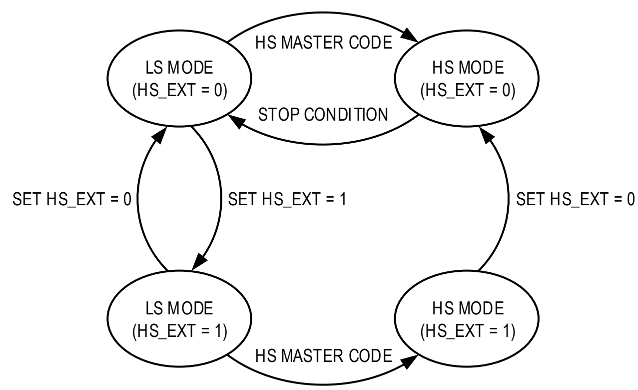


Figure 18. I²C Operating Mode State Diagram

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x10	INT_SRC[7:0]	RSVD	RSVD	RSVD	POK	OVP	HARDSHORT	THS	OCP
0x11	INT_MASK[7:0]	RSVD	RSVD	RSVD	POK_M	OVP_M	HARDSHORT_M	THS_M	OCP_M
0x12	REG_CONT1[7:0]	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
0x13	REG_CONT2[7:0]	VREF[7:0]							
0x14	REG_CONT3[7:0]	RSVD	RSVD	FPWM	RSVD	RSVD[1:0]		SLEW_RATE[1:0]	
0x15	I2C_CNFG[7:0]	RSVD	RSVD[2:0]			RSVD	RSVD	RSVD	HS_EXT

Register Details

INT_SRC (0x10)

POK and Interrupt Source Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	POK	OVP	HARDSHORT	THS	OCP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Reads back 0.	N/A
RSVD	6	Reserved. Reads back 0.	N/A
RSVD	5	Reserved. Reads back 0.	N/A
POK	4	Power-OK Status	0: Output voltage is below POK threshold. 1: Output voltage is above POK threshold.
OVP	3	Overvoltage Protection Interrupt	0: Output overvoltage has NOT been detected. 1: Output overvoltage has been detected.
HARDSHORT	2	Ouput Hard Short Interrupt	0: Buck-Boost regulator has NOT been latched off due to output hardshort. 1: Buck-Boost regulator has been latched off due to output hardshort.
THS	1	Thermal Shutdown Interrupt	0: Buck-Boost regulator has NOT been latched off due to thermal shutdown. 1: Buck-Boost regulator has been latched off due to thermal shutdown.
OCP	0	Overcurrent Protection Interrupt	0: Buck-Boost regulator has NOT been latched off due to overcurrent. 1: Buck-Boost regulator has been latched off due to overcurrent.

INT_MASK (0x11)

POK and Interrupt Mask Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	POK_M	OVP_M	HARDSHORT_M	THS_M	OCP_M
Reset	0b0	0b0	0b0	0b0	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	N/A

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	6	Reserved	N/A
RSVD	5	Reserved	N/A
POK_M	4	Power-OK Status Mask	0: Power-OK status is NOT masked (Default). 1: Power-OK status is masked.
OVP_M	3	Overvoltage Protection Interrupt Mask	0: Overvoltage protection interrupt is NOT masked. 1: Overvoltage protection interrupt is masked (Default).
HARDSHORT_M	2	Ouput Hard Short Interrupt Mask	0: Ouput hard short interrupt is NOT masked. 1: Ouput hard short interrupt is masked (Default).
THS_M	1	Thermal Shutdown Interrupt Mask	0: Thermal shutdown interrupt is NOT masked. 1: Thermal shutdown interrupt is masked (Default).
OCP_M	0	Overcurrent Protection Interrupt Mask	0: Overcurrent protection interrupt is NOT masked. 1: Overcurrent protection interrupt is masked (Default).

REG_CONT1 (0x12)

Control Register 1

BIT	7	6	5	4	3	2	1	0
Field	COMP[2:0]			FREQ[1:0]		ILIM[2:0]		
Reset	0b010			0b10		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
COMP	7:5	Internal Compensation R_C Option (Bandwidth)	000: R_C = 30kΩ, Buck mode R_C = 20kΩ, Boost mode 001: R_C = 45kΩ, Buck mode R_C = 30kΩ, Boost mode 010: R_C = 60kΩ, Buck mode R_C = 45kΩ, Boost mode (Default) 011: R_C = 70kΩ, Buck mode R_C = 50kΩ, Boost mode 100: R_C = 80kΩ, Buck mode R_C = 55kΩ, Boost mode 101: R_C = 90kΩ, Buck mode R_C = 60kΩ, Boost mode 110: R_C = 110kΩ, Buck mode R_C = 75kΩ, Boost mode 111: R_C = 150kΩ, Buck mode R_C = 100kΩ, Boost mode
FREQ	4:3	Switching Frequency	00: 1.2MHz 01: 1.5MHz 10: 1.8MHz (Default) 11: 2.1MHz
ILIM	2:0	High-Side Switching Current Limit	000: 7.0A 001: 6.2A 010: 5.6A 011: 4.6A 100: 3.8A 101: 2.8A 110: 1.8A 111: 0.99A

REG_CONT2 (0x13)

Control Register 2

BIT	7	6	5	4	3	2	1	0
Field	VREF[7:0]							
Reset	0x44							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VREF	7:0	Internal Reference Voltage	0x00–0x3C: 0.299V 0x3D–0xCC: 4.9mV/LSB in a linear transfer function between 0.299V (0x3D) and 1.000V (0xCC) 0xCD–0xFF: 1.000V Default: 0x44: 0.333V

REG_CONT3 (0x14)

Control Register 3

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	FPWM	RSVD	RSVD[1:0]		SLEW_RATE[1:0]	
Reset	0b0	0b0	0b0	0b0	0b11		0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	N/A
RSVD	6	Reserved	N/A
FPWM	5	Forced-PWM Mode	0: Forced-PWM mode is disabled (Default). 1: Forced-PWM mode is enabled.
RSVD	4	Reserved	N/A
RSVD	3:2	Reserved	N/A
SLEW_RATE	1:0	Internal Reference DVS Ramp Rate. See the *Output Voltage Configuration* section for equations to convert V_{REF} DVS ramp rate to V_{OUT} DVS ramp rate.	00: 7/6mV/μs (FREQ = 00 or 01) 4/3mV/μs (FREQ = 10 or 11) (Default) 01: 2/3mV/μs 10: 1/3mV/μs 11: 1/6mV/μs (FREQ = 00 or 01) 17/75mV/μs (FREQ = 10 or 11)

I2C_CNFG (0x15)

I^2C Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD[2:0]			RSVD	RSVD	RSVD	HS_EXT
Reset	0b0	0b000			0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved	N/A
RSVD	6:4	Reserved	N/A
RSVD	3	Reserved	N/A
RSVD	2	Reserved	N/A
RSVD	1	Reserved	N/A
HS_EXT	0	I^2C High-Speed Mode Extension Control	0: I^2C high-speed mode extension is disabled (Default). 1: I^2C high-speed mode extension is enabled.

Applications Information

Software (I^2C) Control

Control the IC using software commands sent over the I^2C serial interface.

Assert V_{IO} valid and connect SDA and SCL to a serial host to enable the serial bus and full software control of the IC. When using software, the serial host can accomplish the following:

- Monitor overvoltage protection interrupt using the OVP[0] bitfield.
- Monitor overcurrent protection interrupt using the OCP[0] bitfield.
- Monitor output hard-short interrupt using the HARDSHORT[0] bitfield.
- Monitor thermal shutdown interrupt using the THS[0] bitfield.
- Change POK and fault interrupt mask using the OVP_M[0], OCP_M[0], HARDSHORT_M[0], and THS_M[0] bitfields.
- Change target output voltage (V_{OUT}) by setting internal reference voltage (V_{REF}) using the VREF[7:0] bitfield.
- Change slew-rate of output voltage change ($\Delta V_{OUT}/\Delta t$) using the SLEW_RATE[1:0] bitfield.
- Change regulation mode (SKIP, FPWM) dynamically using the FPWM[0] bitfield.
- Change switching current limit threshold (I_{LIM}) using the ILIM[2:0] bitfield.
- Change switching frequency using the FREQ[1:0] bitfield.
- Change internal compensation option using the COMP[2:0] bitfield.

The configuration registers reset when V_{IO} becomes invalid, when IN falls below UVLO falling threshold (V_{UVLO_F}), or when EN is logic LOW. See the *Detailed Description–I^2C Serial Interface* section and *Register Map* for more information.

Non-I^2C and Standalone Operation

The MAX77857 can operate without I^2C software control. The switching current limit can be configured by a resistor (R_{SEL}) connecting the SEL pin to AGND. The output voltage can be configured by external feedback resistors. See the *SEL Pin Configuration* section and the *Output Voltage Configuration* section for more information. If the I^2C serial interface is not in use, connect the SCL and SDA pins to V_L to avoid unwanted behavior.

Moreover, the IC is capable of standalone operation, in which the IC starts up whenever V_{IN} is valid, and it does not require a separate supply for the V_{IO} pin. This is useful for systems without a host controller, or the IC is the only power supply in the system. To configure the IC for standalone operation, connect a 510kΩ from the IN pin to the EN pin. The IC clamps the voltage at the EN pin internally to make sure it does not exceed the absolute maximum rating. If the system does not have a separate supply to power the V_{IO} pin, connect the V_{IO} pin to V_L so V_{IO} can be supplied by the internal regulator. Connections for standalone operation are shown in Figure 19.

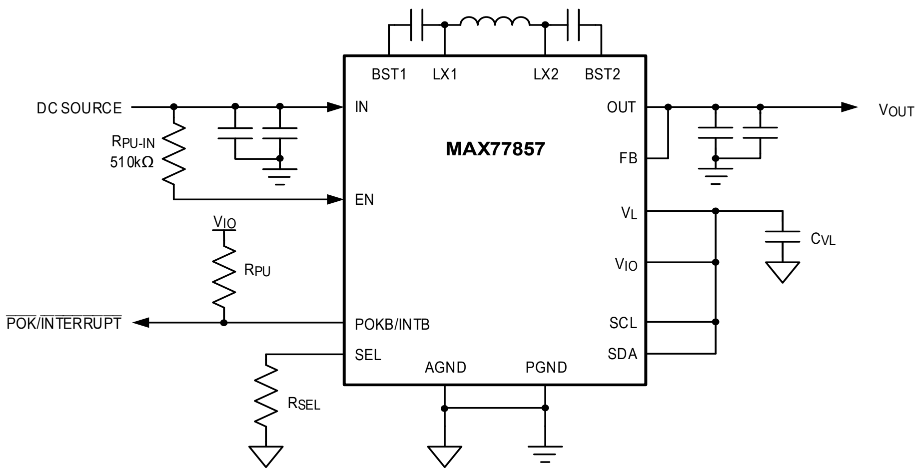


Figure 19. Connections for Standalone Operation

Inductor Selection

An inductor with a saturation current rating (I_{SAT}) greater than or equal to the typical high-side switching current limit threshold (I_{LIM}) setting is recommended. In general, inductors with lower saturation current and higher DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the RMS current rating (I_{RMS}) of the inductor (the current at which the temperature rises appreciably) based on the expected load current.

The chosen inductor value should ensure that the peak-inductor ripple current (I_{PEAK}) is below the I_{LIM} setting so that the converter can maintain regulation. A 1.5μH inductor is recommended throughout the operating range of the converter. See Table 6 for recommended inductors.

Table 6. Inductor Recommendations

VENDOR	PART NUMBER	NOMINAL INDUCTANCE (μH)	TYPICAL DCR (mΩ)	I_{SAT} (A)	I_{RMS} (A)	DIMENSIONS L x W x H (mm)	I_{LIM} SETUP
Sumida	CDMT40D20HF-1R5NC	1.5	19.5	7.1	7.5	4.0 x 4.0 x 2.1	ILIM[2:0] = 000 (7.00A)
Coilcraft	XEL4020-152MEC	1.5	21.45	7.4	7.5	4.0 x 4.0 x 2.1	ILIM[2:0] = 000 (7.00A)
TDK	VLS3012HBX-1R0M	1.0	39	6.11	5.13	3.0 x 3.0 x 1.2	ILIM[2:0] = 100 (3.80A)
Samsung	CIGT252010EH1R0MNE	1.0	26	5	4.3	2.5 x 2.0 x 1.0	ILIM[2:0] = 100 (3.80A)
Cyntec	HTEH16080H-1R0MSR	1.0	95	2.1	1.8	1.6 x 0.8 x 0.8	ILIM[2:0] = 110 (1.72A)
Murata	DFE18SBN1R0ME0L	1.0	120 (max)	1.9	1.8	1.6 x 0.8 x 0.8	ILIM[2:0] = 111 (0.98A)

Input Capacitor Selection

For most applications, bypass the IN pin with two 25V 10μF nominal ceramic input capacitors (C_{IN}) that maintain 1μF or higher effective capacitance at its working voltage. Effective C_{IN} is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter but increase inrush current from voltage supply when connected. C_{IN} reduces the current peaks drawn from the input power source and reduces switching noise in the system. The ESR/ESL of C_{IN} and its series PCB trace should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to the converter's switching frequency.

Pay special attention to capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{IN}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the converter. Choose effective C_{OUT} to be 8.2µF minimum. Effective C_{OUT} is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. For most applications, two 25V 22µF capacitors are recommended for C_{OUT}.

Pay special attention to capacitor's voltage rating, initial tolerance, variation with temperature, and DC bias characteristic when selecting C_{OUT}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Other Required Component Selection

Table 7 illustrates the requirements for other required components.

Table 7. Other Component Selection Requirements

SYMBOL	COMPONENT DESCRIPTION	PARAMETER	MIN	TYP	MAX	UNITS
C_{BST}	High-Side FET Driver Bootstrap Capacitor	Suggested Capacitance		0.22		µF
C_{VL}	V_L Regulator Bypass Capacitor	Effective Capacitance	0.5		3	µF
		Equivalent Series Resistance (ESR)			100	mΩ
C_{VIO}	V_{IO} Regulator Bypass Capacitor	Effective Capacitance	0.3		1.5	µF
		Equivalent Series Resistance (ESR)			100	mΩ
R_{SEL}	SEL Pin Resistor	Acceptable Tolerance	-1		+1	%
R_{PU}	POKB/INTB Pullup Resistor	Suggested Resistance		15		kΩ

PCB Layout Guidelines

Careful circuit board layout is critical to achieving low switching power losses and clean, stable operation. For WLP package, if POK or fault interrupt functionality is desired, then a high-density interconnect (HDI) PCB is required to route to the POKB/INTB pin. Otherwise, HDI PCB is recommended but not required. *Figure 20*, *Figure 21*, and *Figure 22* show example non-HDI and HDI PCB layouts for the MAX77857 WLP package. HDI PCB is not required for the FC2QFN package. *Figure 23* shows an example layout for the MAX77857 FC2QFN package.

When designing the PCB, follow these guidelines:

- Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN pin and OUT pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
- Place the inductor next to the LX bumps (as close as possible) and make the traces between the LX bumps and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer (as in the examples), make sure to include enough vias to minimize trace

impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.

- Route LX nodes to its corresponding bootstrap capacitor (C_{BST}) as short as possible. Prioritize C_{BST} placement to reduce trace length to the IC.
- Connect the inner PGND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create PGND islands, as PGND islands risk interrupting the hot loops. Connect the AGND and AGND island to the low-impedance ground plane on the PCB (the same net as PGND).
- Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
- Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

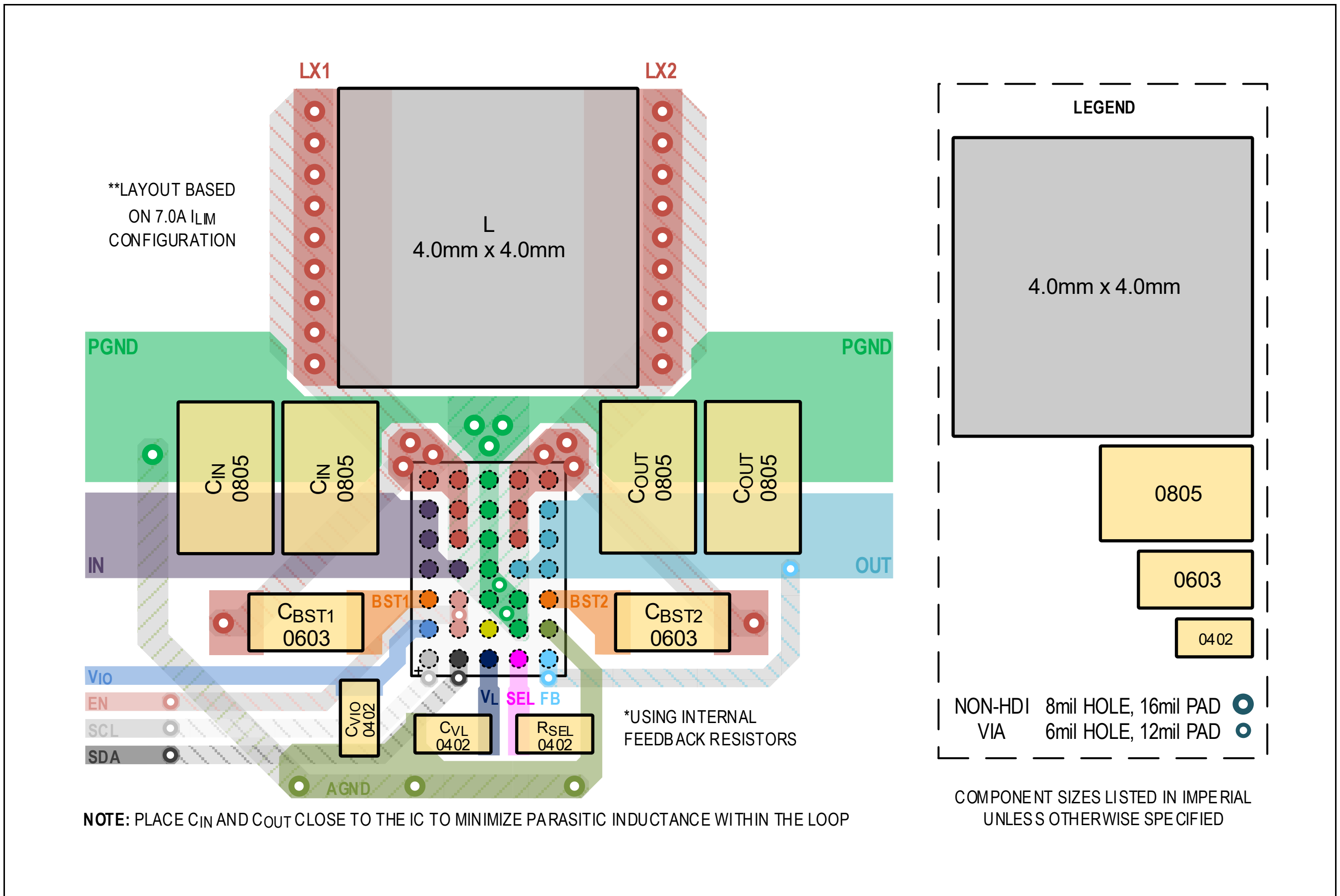


Figure 20. Non-HDI PCB Layout Recommendation for 35 WLP Package with 4mm x 4mm Inductor

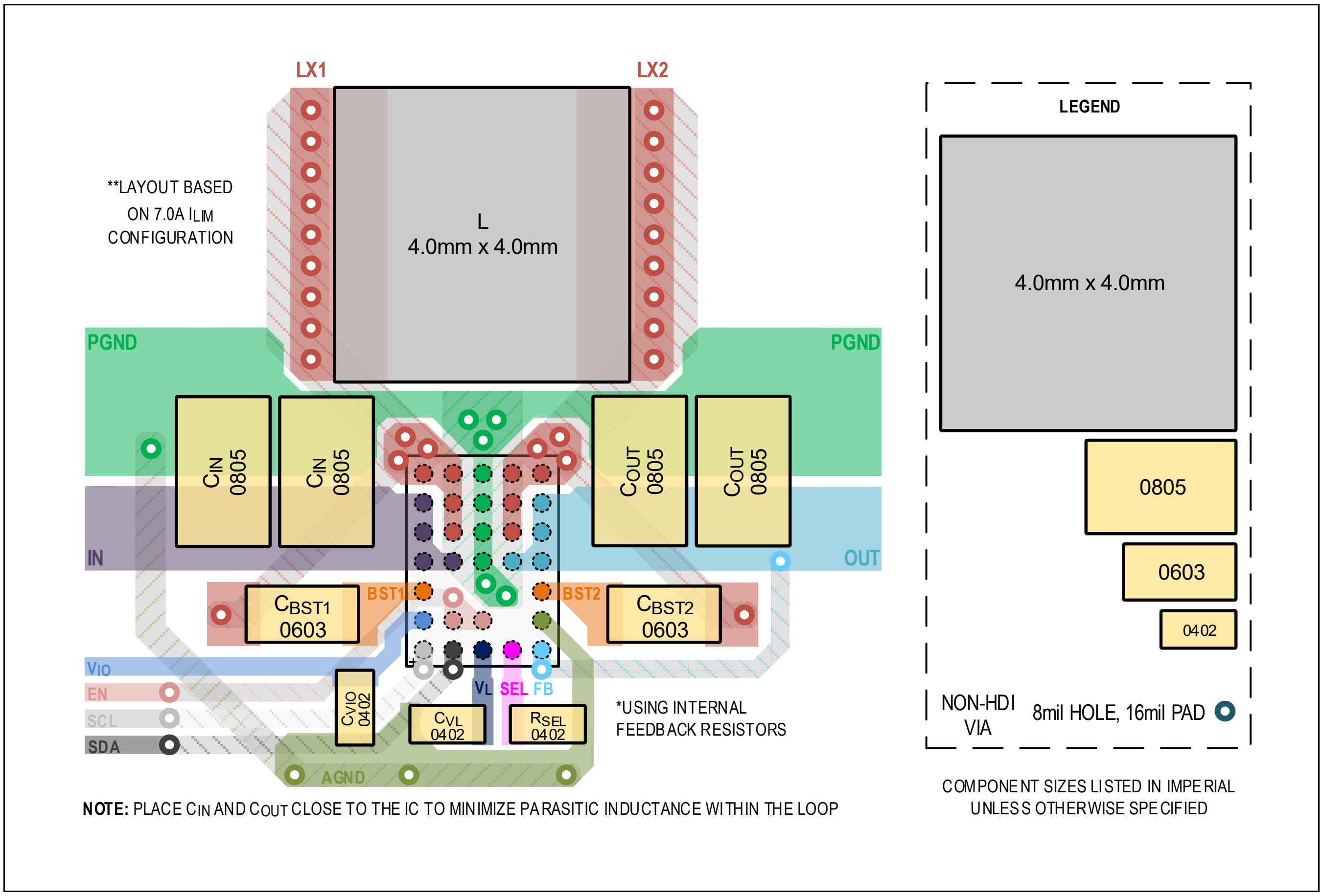


Figure 21. Non-HDI PCB Layout Recommendation for 31 WLP Package with 4mm x 4mm Inductor

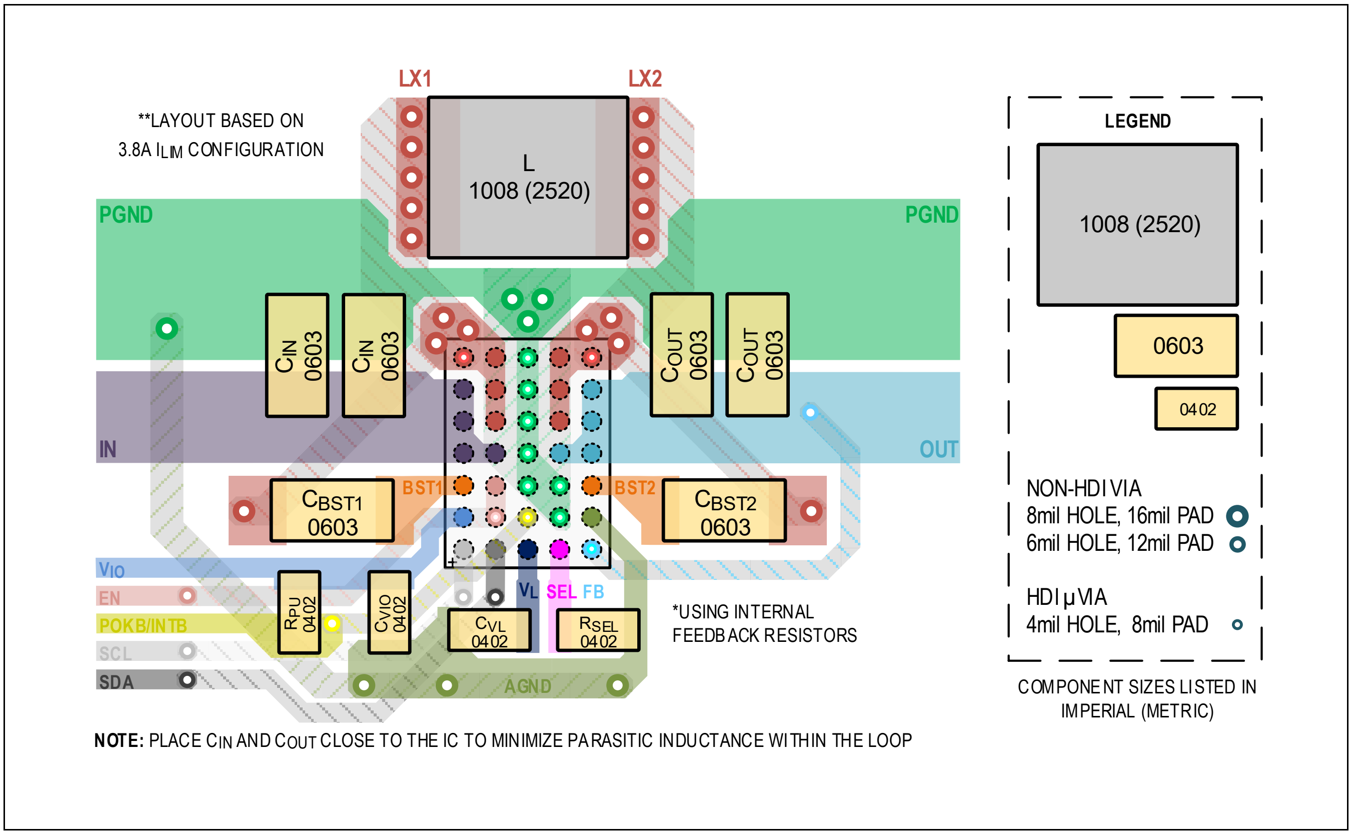


Figure 22. HDI PCB Layout Recommendation for 35 WLP Package with POKB/INTB and 2520 Inductor

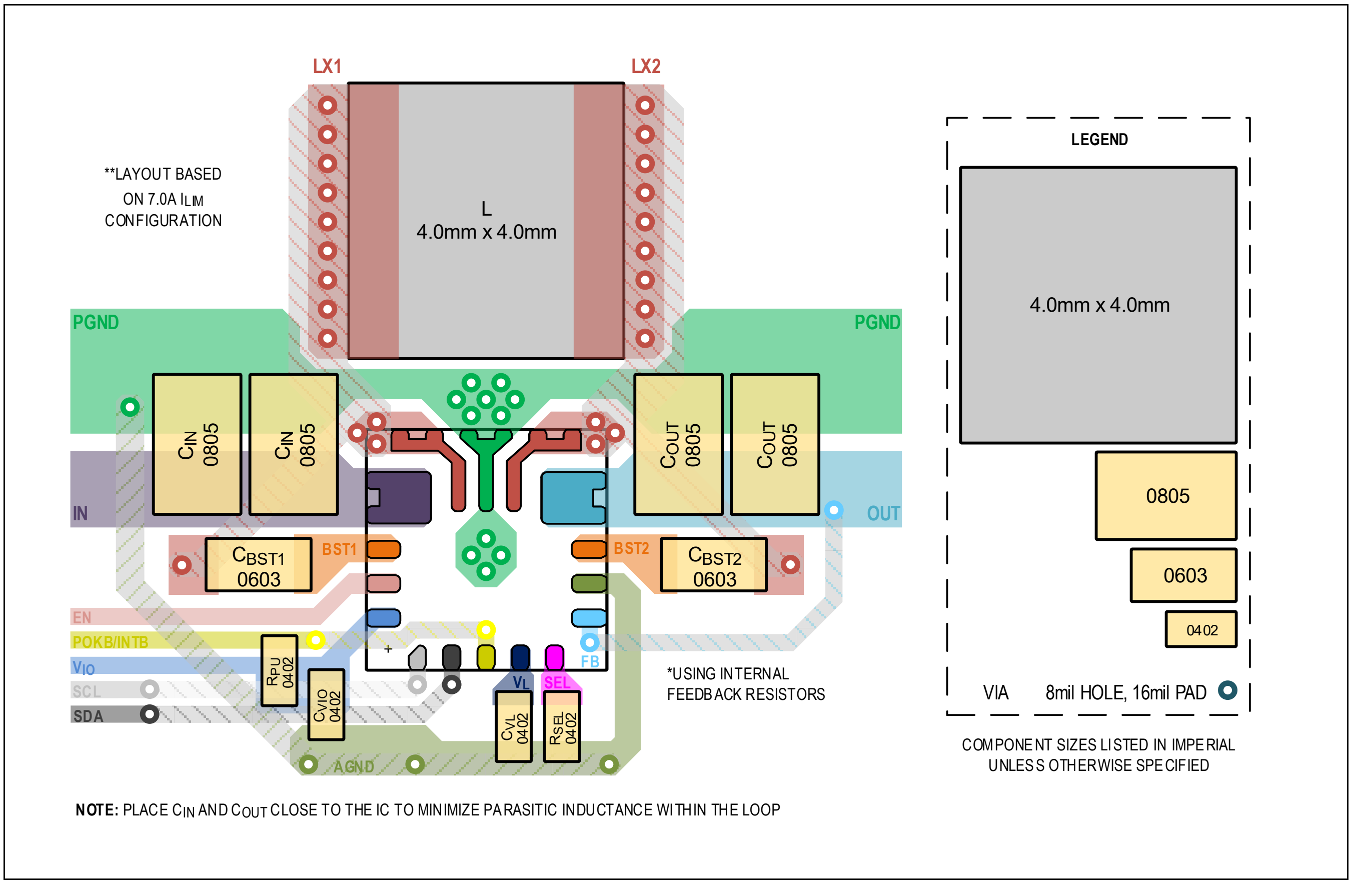
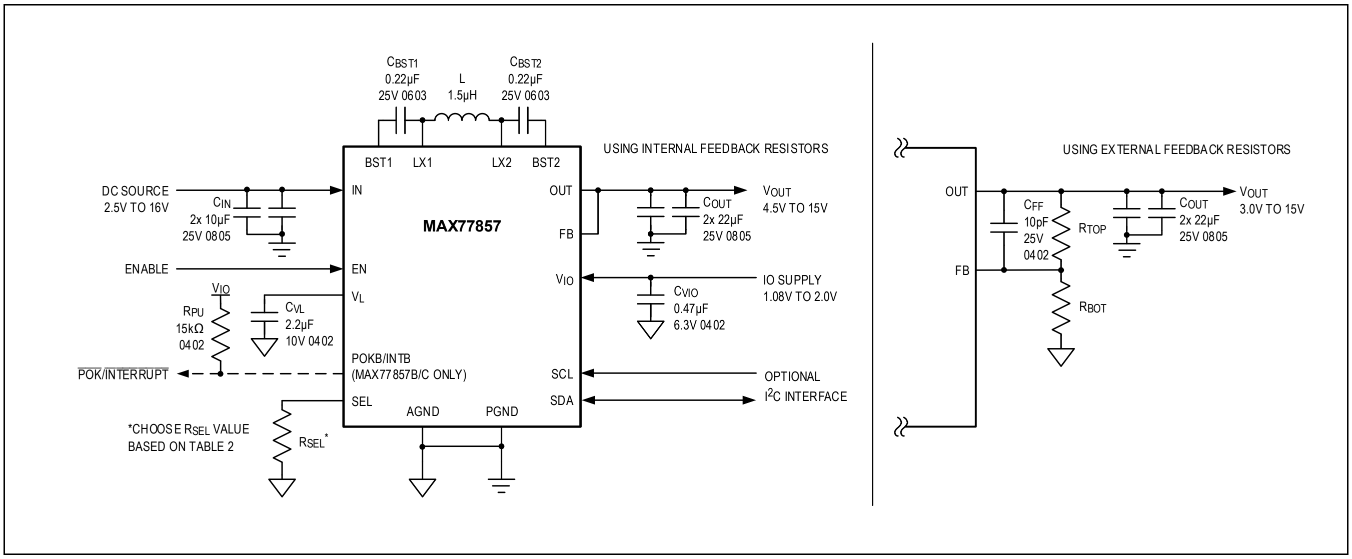


Figure 23. PCB Layout Recommendation for 16 FC2QFN Package with 4mm x 4mm Inductor

Typical Application Circuit



Ordering Information

PART NUMBER	DEFAULT SWITCHING FREQUENCY	DEFAULT OUTPUT VOLTAGE	POKB/INTB	STARTUP/I_{LIM} LATCH-OFF	PIN-PACKAGE
MAX77857AEWQ+T			No	No	31 WLP
MAX77857BEWB+T			Yes	No	35 WLP
MAX77857CEWB+T	1.8MHz	5V	Yes	Yes	35 WLP
MAX77857BEFE+T*			Yes	No	16 FC2QFN
MAX77857CEFE+T*			Yes	Yes	16 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*
For other switching frequency options, contact sales representatives for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/22	Release for Market Intro	—
1	3/22	Updated the Ordering Information table	52
2	8/22	Updated Electrical Characteristics, Start-Up, Overcurrent Protection (OCP), and PCB Layout Guidelines sections, added Figure 23	7, 24, 31, 32, 47, 51