19-2484; Rev 0; 7/02

MAXIM

# ECL/PECL Dual Differential 2:1 Multiplexer



## General Description

The MAX9384 fully differential dual 2:1 multiplexer (mux) features extremely low propagation delay (560ps max) and output-to-output skew (40ps max). The device is ideal for clock and data multiplexing applications. The two 2:1 muxes are controlled individually or simultaneously through mux select inputs COM_SEL, SEL0, and SEL1. The mux select inputs are compatible with ECL/PECL logic, and are referenced to on-chip outputs $V_{BB0}$ and $V_{BB1}$, nominally $V_{CC}$ - 1.33V.

The differential inputs D, $\overline{D}$ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip supply output $V_{BB}$ as a reference voltage. All the differential inputs have bias and clamp circuits that force the outputs to a low default when the inputs are left open or at $V_{EE}$. The single-ended mux select inputs have pulldowns to $V_{EE}$, providing low default inputs when the select inputs are left open.

The device operates with a wide supply range ($V_{CC}$ - $V_{EE}$) of +3.0V to +5.5V for PECL or -3.0V to -5.5V for ECL, and is pin compatible with the MC100LVEL56 and MC100EL56. The MAX9384 is offered in a 20-pin wide SO package, and is specified for operation from -40°C to +85°C.

## Applications

High-Speed Telecom, Datacom Applications

Central-Office Backplane Clock Distribution

Access Multiplexers (DSLAM/DLC)

***Functional Diagram appears at end of data sheet.***

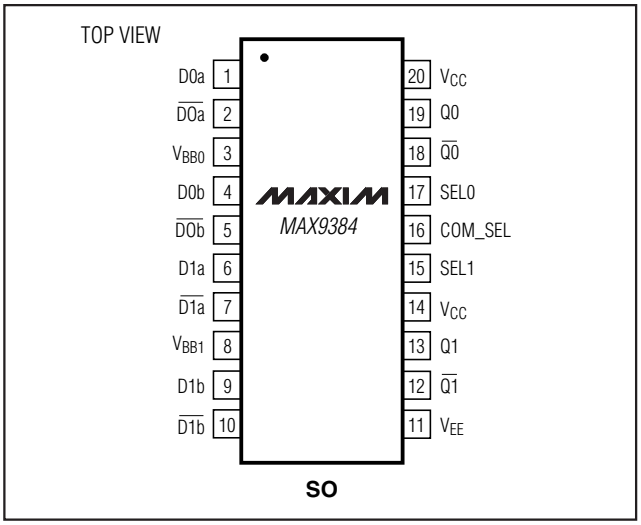
## Features

- **40psP-P Deterministic Jitter**
- **440ps Differential Propagation Delay**
- **12ps Output-to-Output Skew**
- **Individual and Common Select**
- **+3.0V to +5.5V Supplies for Differential LVPECL/PECL**
- **-3.0V to -5.5V Supplies for Differential LVECL/ECL**
- **Outputs Low for Inputs Open or at $V_{EE}$**
- **>2kV ESD Protection (Human Body Model)**
- **Pin Compatible with MC100LVEL56 and MC100EL56**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX9384EWP | -40°C to +85°C | 20 Wide SO |

## Pin Configuration



# ECL/PECL Dual Differential 2:1 Multiplexer

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ - $V_{EE}$ .....-0.3V to 6.0V
Inputs (D_, $\overline{D}$_, SEL_, COM_SEL) to $V_{EE}$....-0.3V to ($V_{CC}$ + 0.3V)
D_ to $\overline{D}$_ .....±3.0V
Continuous Output Current .....50mA
Surge Output Current.....100mA
$V_{BB}$ Sink/Source Current .....±0.65mA
Junction-to-Ambient Thermal Resistance in Still Air
20-Lead Wide SO .....+100°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow
20-Lead Wide SO .....+58°C/W
Junction-to-Case Thermal Resistance
20-Lead Wide SO .....+20°C/W
Continuous Power Dissipation ($T_A$ = +70°C)
20-Lead Wide SO
(derate 10mW/°C above +70°C).....800mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model
(D_, $\overline{D}$_, Q_, $\overline{Q}$_, SEL_, COM_SEL) .....≥ 2kV
Soldering Temperature (10s).....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ - $V_{EE}$ = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V. Typical values are at $V_{CC}$ - $V_{EE}$ = 3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **SINGLE-ENDED INPUT SEL_, COM_SEL** | | | | | | | | | | | | |
| Input High Voltage | $V_{IH}$ | Internally referenced to $V_{BB}$, Figure 1 | $V_{CC}$ - 1.165 | | $V_{CC}$ | $V_{CC}$ - 1.165 | | $V_{CC}$ | $V_{CC}$ - 1.165 | | $V_{CC}$ | V |
| Input Low Voltage | $V_{IL}$ | Internally referenced to $V_{BB}$, Figure 1 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | V |
| Input Current | $I_{IN}$ | $V_{IH}$, $V_{IL}$ | -10 | | +50 | -10 | | +50 | -10 | | +50 | µA |
| **DIFFERENTIAL INPUT (D_, $\overline{D}$_)** | | | | | | | | | | | | |
| Single-Ended Input High Voltage | $V_{IH}$ | $V_{BB}$ connected to the unused input, Figure 1 | $V_{CC}$ - 1.165 | | $V_{CC}$ | $V_{CC}$ - 1.165 | | $V_{CC}$ | $V_{CC}$ - 1.165 | | $V_{CC}$ | V |
| Single-Ended Input Low Voltage | $V_{IL}$ | $V_{BB}$ connected to the unused input, Figure 1 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | $V_{CC}$ - 1.810 | | $V_{CC}$ - 1.475 | V |
| High Voltage of Differential Input | $V_{IHD}$ | Figure 1 | $V_{EE}$ + 1.3 | | $V_{CC}$ | $V_{EE}$ + 1.2 | | $V_{CC}$ | $V_{EE}$ + 1.2 | | $V_{CC}$ | V |
| Low Voltage of Differential Input | $V_{ILD}$ | Figure 1 | $V_{EE}$ | | $V_{CC}$ - 0.095 | $V_{EE}$ | | $V_{CC}$ - 0.095 | $V_{EE}$ | | $V_{CC}$ - 0.095 | V |
| Differential Input Voltage | $V_{IHD}$ - $V_{ILD}$ | Figure 1 | 0.095 | | 3.0 | 0.095 | | 3.0 | 0.095 | | 3.0 | V |
| Input Current | $I_{IN}$ | $V_{IH}$, $V_{IL}$, $V_{IHD}$, $V_{ILD}$ | -100 | | +100 | -100 | | +100 | -100 | | +100 | µA |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC}$ - $V_{EE}$ = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V. Typical values are at $V_{CC}$ - $V_{EE}$ = 3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT (Q_, $\overline{Q\_}$)** | | | | | | | | | | | | |
| Single-Ended Output High Voltage | $V_{OH}$ | Figure 2 | $V_{CC}$ - 1.085 | $V_{CC}$ - 0.998 | $V_{CC}$ - 0.880 | $V_{CC}$ - 1.025 | $V_{CC}$ - 0.947 | $V_{CC}$ - 0.880 | $V_{CC}$ - 1.025 | $V_{CC}$ - 0.929 | $V_{CC}$ - 0.880 | V |
| Single-Ended Output Low Voltage | $V_{OL}$ | Figure 2 | $V_{CC}$ - 1.830 | $V_{CC}$ - 1.707 | $V_{CC}$ - 1.555 | $V_{CC}$ - 1.810 | $V_{CC}$ - 1.685 | $V_{CC}$ - 1.620 | $V_{CC}$ - 1.810 | $V_{CC}$ - 1.690 | $V_{CC}$ - 1.620 | V |
| Differential Output Voltage | $V_{OH}$ - $V_{OL}$ | Figure 2 | 600 | | | 640 | | | 660 | | | mV |
| **REFERENCE OUTPUT ($V_{BB}$)** | | | | | | | | | | | | |
| Reference Voltage Output | $V_{BB}$ | $I_{BB}$ = ±0.5mA (Note 4) | $V_{CC}$ - 1.38 | $V_{CC}$ - 1.322 | $V_{CC}$ - 1.26 | $V_{CC}$ - 1.38 | $V_{CC}$ - 1.330 | $V_{CC}$ - 1.26 | $V_{CC}$ - 1.38 | $V_{CC}$ - 1.335 | $V_{CC}$ - 1.26 | V |
| **SUPPLY** | | | | | | | | | | | | |
| Supply Current | $I_{EE}$ | (Note 5) | | 15 | 24 | | 17 | 24 | | 19 | 24 | mA |

# ECL/PECL Dual Differential 2:1 Multiplexer

## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ - $V_{EE}$ = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V, $V_{IHD}$ - $V_{ILD}$ = 0.15V to 1V, $f_{IN} \le$ 500MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at $V_{CC}$ - $V_{EE}$ = 3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, unless otherwise noted.) (Note 6)

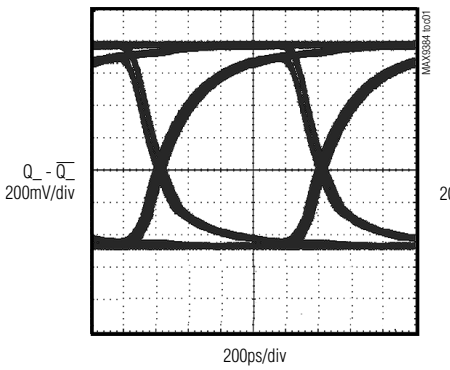
| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Differential Input-to-Output Delay | $t_{PLHD}$, $t_{PHLD}$ | Figure 2 | 340 | | 540 | 350 | | 550 | 360 | | 560 | ps |
| Single-Ended Input-to-Output Delay | $t_{PLH1}$, $t_{PHL1}$ | Figure 3 (Note 7) | 290 | | 540 | 310 | | 560 | 330 | | 580 | ps |
| SEL_ and COM_SEL to Output Delay | $t_{PLH2}$, $t_{PHL2}$ | Figure 4 (Note 7) | 310 | | 730 | 320 | | 740 | 330 | | 750 | ps |
| Output-to-Output Skew | $t_{SKOO}$ | (Note 8) | | 12 | 40 | | 12 | 40 | | 12 | 40 | ps |
| Added Random Jitter | $t_{RJ}$ | $f_{IN}$ = 500MHz (Note 9) | | 0.3 | 0.8 | | 0.4 | 0.8 | | 0.5 | 0.8 | $ps_{(RMS)}$ |
| Added Deterministic Jitter | $t_{DJ}$ | 1.0Gbps $2^{23}$ - 1 PRBS pattern (Note 9) | | 40 | 70 | | 40 | 70 | | 40 | 70 | $ps_{(P-P)}$ |
| Switching Frequency | $f_{MAX}$ | $V_{OH}$ - $V_{OL}$ ≥ 300mV, Figure 2 | 1.5 | | | 1.5 | | | 1.5 | | | GHz |
| Output Rise and Fall Time (20% to 80%) | $t_R$, $t_F$ | Figure 2 | 200 | 310 | 440 | 200 | 310 | 440 | 200 | 310 | 440 | ps |

**Note 1:** Measurements are made with the device in thermal equilibrium.
**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.
**Note 3:** DC parameters production tested at $T_A$ = +25°C and guaranteed by design over the full operating temperature range.
**Note 4:** Use $V_{BB}$ only for inputs that are on the same device as the $V_{BB}$ reference.
**Note 5:** All pins open except $V_{CC}$ and $V_{EE}$.
**Note 6:** Guaranteed by design and characterization. Limits are set at ±6 sigma.
**Note 7:** Test conditions are $V_{IH}$ = $V_{CC}$ - 1.11V and $V_{IL}$ = $V_{CC}$ - 1.53V.
**Note 8:** Measured between outputs of the same part at the signal crossing points for a same-edge transition. Differential input signal.
**Note 9:** Device jitter added to the input signal. Differential input signal.

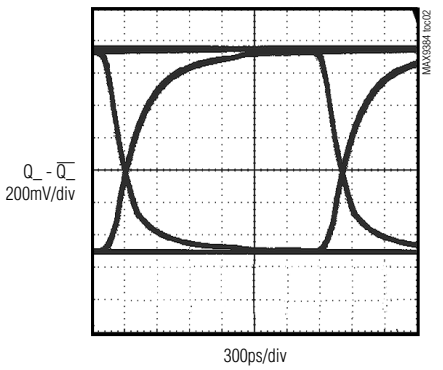
## Typical Operating Characteristics

($V_{CC}$ - $V_{EE}$ = 3.3V, $V_{IHD}$ = $V_{CC}$ - 1V, $V_{ILD}$ = $V_{CC}$ - 1.5V, COM_SEL = low, SEL_ = low, outputs loaded with 50Ω ±1% to $V_{CC}$ - 2V, $f_{IN}$ = 500MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.)

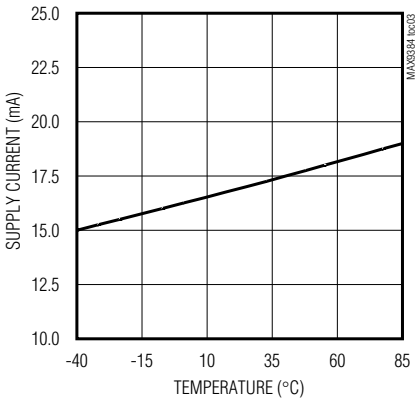
**DIFFERENTIAL OUTPUT EYE PATTERN AT 1Gbps, PRBS $2^{23}$ - 1, NRZ DATA PATTERN**



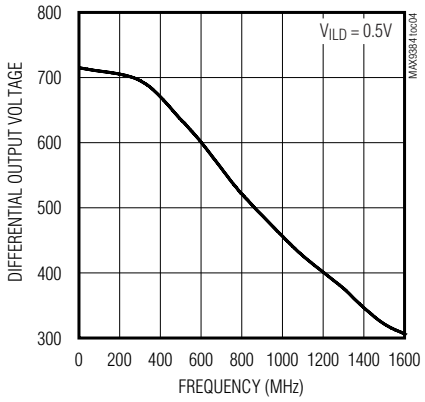

**DIFFERENTIAL OUTPUT EYE PATTERN AT 500Mbps, PRBS $2^{23}$ - 1, NRZ DATA PATTERN**



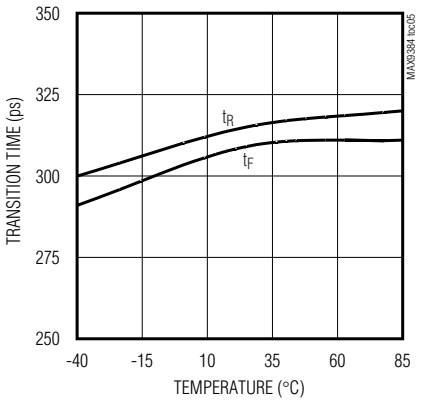

**SUPPLY CURRENT ($I_{EE}$) vs. TEMPERATURE**



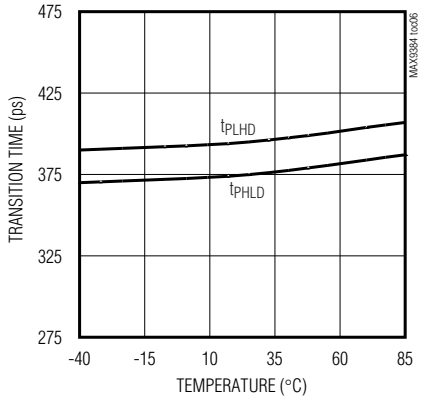

**OUTPUT AMPLITUDE ($V_{OH}$ - $V_{OL}$) vs. FREQUENCY**




**TRANSITION TIME vs. TEMPERATURE**




**DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE**



# ECL/PECL Dual Differential 2:1 Multiplexer

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | D0a | Noninverting Differential Input **a** for MUX 0. Internal 120kΩ pulldown to $V_{EE}$. |
| 2 | $\overline{D0a}$ | Inverting Differential Input **a** for MUX 0. Internal 120kΩ pulldown to $V_{EE}$ and 120kΩ pullup to $V_{CC}$. |
| 3 | $V_{BB0}$ | Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass $V_{BB0}$ to $V_{CC}$ with a 0.01µF ceramic capacitor. Otherwise leave open. $V_{BB0}$ is internally connected to $V_{BB1}$. |
| 4 | D0b | Noninverting Differential Input **b** for MUX 0. Internal 120kΩ pulldown to $V_{EE}$. |
| 5 | $\overline{D0b}$ | Inverting Differential Input **b** for MUX 0. Internal 120kΩ pulldown to $V_{EE}$ and 120kΩ pullup to $V_{CC}$. |
| 6 | D1a | Noninverting Differential Input **a** for MUX 1. Internal 120kΩ pulldown to $V_{EE}$. |
| 7 | $\overline{D1a}$ | Inverting Differential Input **a** for MUX 1. Internal 120kΩ pulldown to $V_{EE}$ and 120kΩ pullup to $V_{CC}$. |
| 8 | $V_{BB1}$ | Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass $V_{BB1}$ to $V_{CC}$ with a 0.01µF ceramic capacitor. Otherwise leave open. $V_{BB1}$ is internally connected to $V_{BB0}$. |
| 9 | D1b | Noninverting Differential Input **b** for MUX 1. Internal 120kΩ pulldown to $V_{EE}$. |
| 10 | $\overline{D1b}$ | Inverting Differential Input **b** for MUX 1. Internal 120kΩ pulldown to $V_{EE}$ and 120kΩ pullup to $V_{CC}$. |
| 11 | $V_{EE}$ | Negative Supply Voltage |
| 12 | $\overline{Q1}$ | Inverting Output for MUX 1. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 13 | Q1 | Noninverting Output for MUX 1. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 14, 20 | $V_{CC}$ | Positive Supply Voltage. Bypass each $V_{CC}$ to $V_{EE}$ with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device. |
| 15 | SEL1 | Select Logic Input for MUX 1. Internal 210kΩ pulldown to $V_{EE}$. |
| 16 | COM_SEL | Common Select Logic Input. Internal 210kΩ pulldown to $V_{EE}$. |
| 17 | SEL0 | Select Logic Input for MUX 0. Internal 210kΩ pulldown to $V_{EE}$. |
| 18 | $\overline{Q0}$ | Inverting Output for MUX 0. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |
| 19 | Q0 | Noninverting Output for MUX 0. Typically terminate with 50Ω resistor to $V_{CC}$ - 2V. |

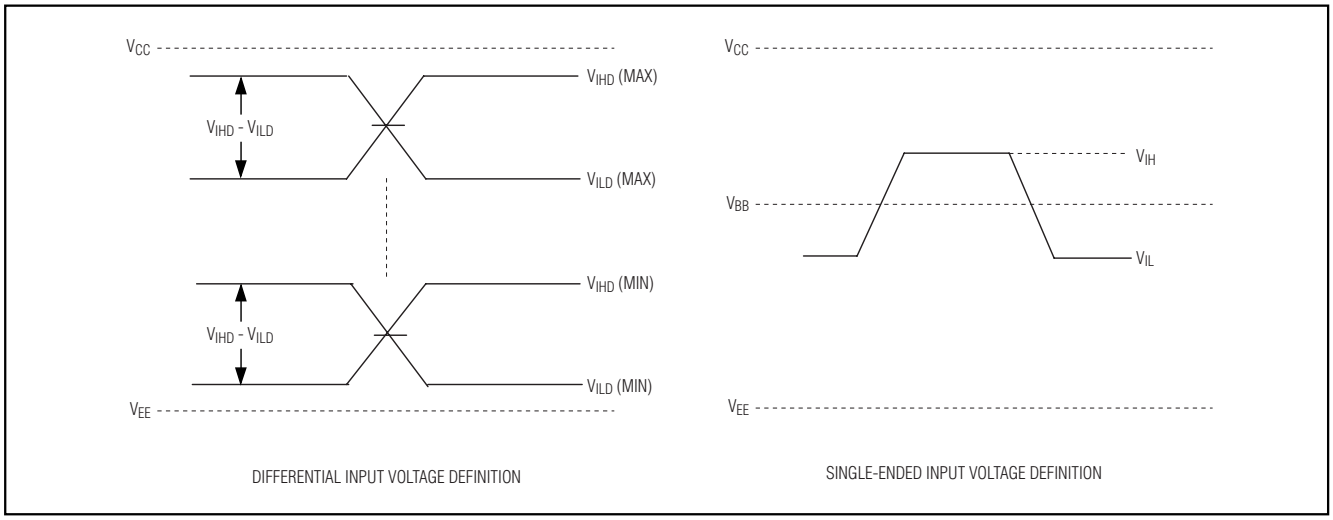



*Figure 1. Input Definitions*

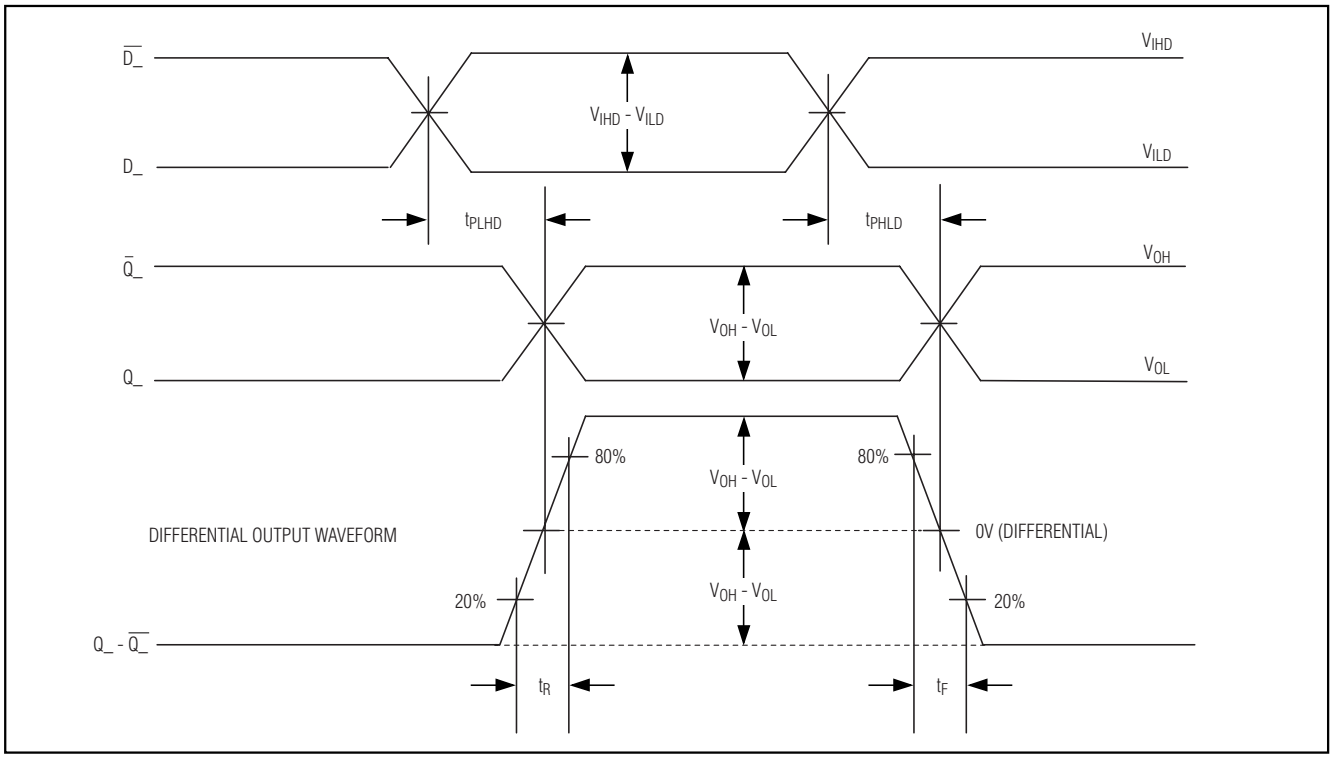



*Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram*

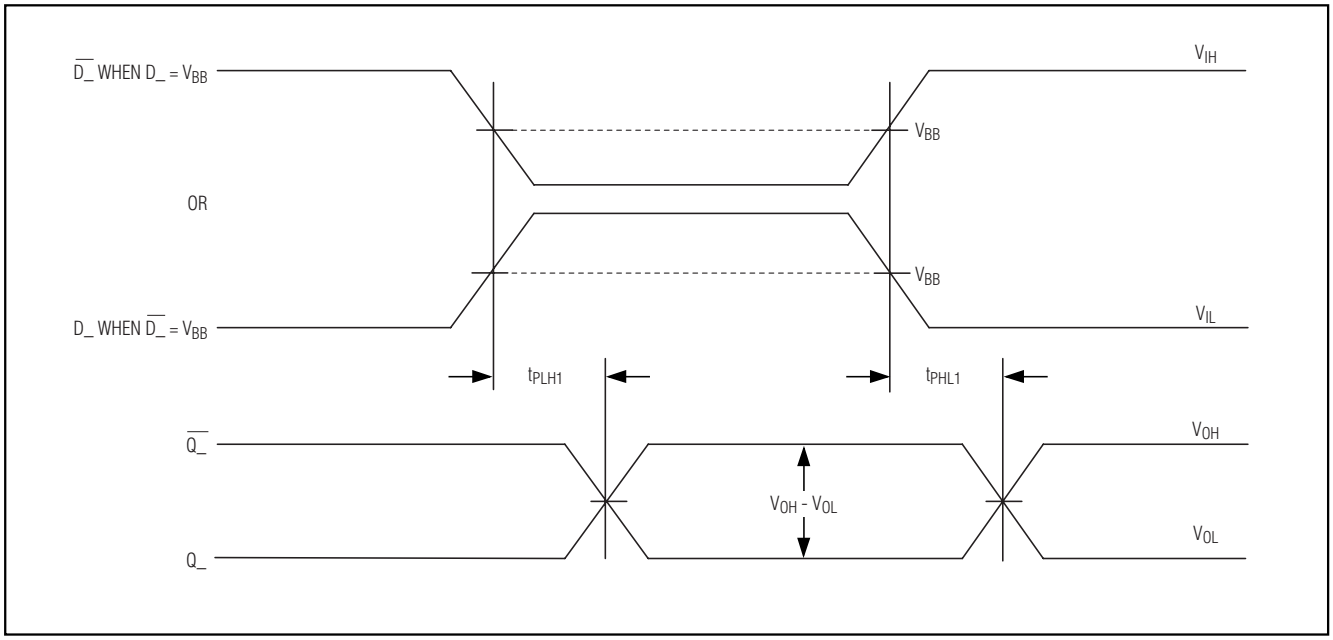



*Figure 3. Single-Ended Input-to-Output Propagation Delay Timing Delay*

# ECL/PECL Dual Differential 2:1 Multiplexer

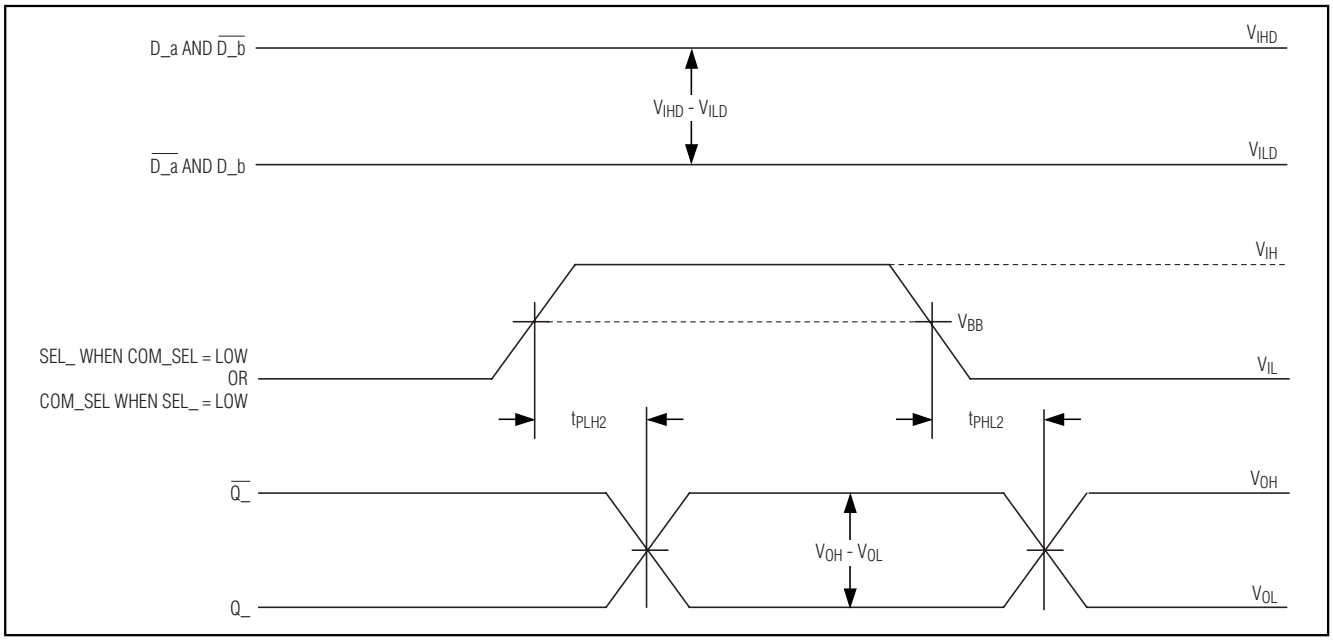



*Figure 4. Select Inputs (COM_SEL, SEL_) to Output (Q_, $\overline{Q\_}$) Delay Timing Diagram*

## Detailed Description

The MAX9384 dual differential 2:1 multiplexer features extremely low propagation delay (560ps max) and output-to-output skew (40ps max). These features make the device ideal for clock and data multiplexing applications.

The two differential muxes are controlled individually or simultaneously through select control inputs, SEL0, SEL1, and COM_SEL (see Table 1). The select control inputs are referenced to $V_{BB}$ (nominally $V_{CC}$ - 1.33V) and are internally pulled down to $V_{EE}$ through 210kΩ resistors. By default, the select inputs are low when left open.

The differential inputs D_, $\overline{D\_}$ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference voltage $V_{BB}$. The reference output voltage, pins $V_{BB0}$ and $V_{BB1}$, provides the input reference voltage for single-ended operation for each mux. A single-ended input of at least $V_{BB\_}$ ±95mV or a differential input of at least 95mV switches the outputs to the $V_{OH}$ and $V_{OL}$ levels specified in the *DC Electrical Characteristics*. The maximum magnitude of the differential input from D_ to $\overline{D\_}$ is ±3.0V. Specifications for the high and low voltages of a differential input ($V_{IHD}$ and $V_{ILD}$) and the differential input voltage ($V_{IHD}$ - $V_{ILD}$) apply simultaneously.

The device operates over a wide supply range ($V_{CC}$ - $V_{EE}$) of +3.0V to +5.5V for PECL or -3.0V to -5.5V for ECL, and is pin compatible with the MC100LVEL56 and MC100EL56.

### Table 1. Input Select Truth Table

| CONTROL INPUT | | DATA INPUT |
|---|---|---|
| COM_SEL | SEL_ | D_ , $\overline{D\_}$ |
| L or open | L or open | b* |
| | H | a |
| H | X | a |

**Default input when COM_SEL and SEL_ are left open.*

### Single-Ended Operation

A single-ended input can be driven to $V_{CC}$ and $V_{EE}$ or by a single-ended LVPECL/LVECL signal. D_, $\overline{D\_}$ are differential inputs but can be configured to accept single-ended inputs. This is accomplished by connecting the on-chip reference voltage, $V_{BB\_}$, to an unused complementary input as a reference. For example, the differential D0a, $\overline{D0a}$ input is converted to a noninverting, single-ended input by connecting $V_{BB0}$ to $\overline{D0a}$ and connecting the single-ended input to D0a. Similarly, an inverting input is obtained by connecting $V_{BB0}$ to D0a and connecting the single-ended input to $\overline{D0a}$.

When using the $V_{BB\_}$ reference output, bypass it with a 0.01µF ceramic capacitor to $V_{CC}$. If not used, leave it open. The $V_{BB\_}$ reference can source or sink 0.5mA, which is sufficient to drive two inputs.

## Applications Information

### Output Termination

Terminate the outputs through 50Ω to $V_{CC}$ - 2V or use equivalent Thevenin terminations. Terminate each Q_ and $\overline{Q}$_ output with identical termination on each for minimal distortion. When a single-ended signal is taken from the differential output, terminate both Q_ and $\overline{Q}$_. Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

### Supply Bypassing

Bypass each $V_{CC}$ to $V_{EE}$ with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close to the device as possible, with the 0.01µF capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. When using the $V_{BB0}$ or $V_{BB1}$ reference outputs, bypass each one with a 0.01µF ceramic capacitor to $V_{CC}$. If the $V_{BB0}$ or $V_{BB1}$ reference outputs are not used, they can be left open.

### Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

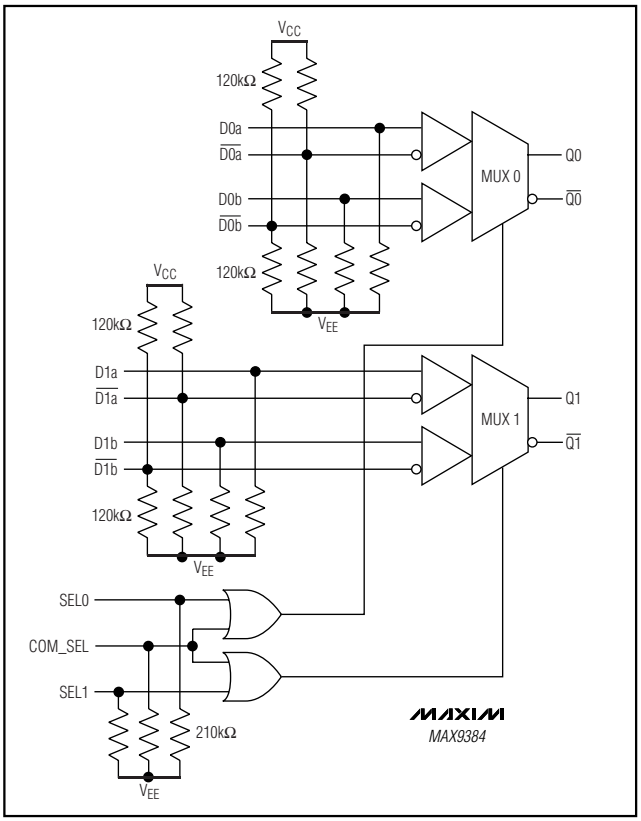
Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

## Chip Information

TRANSISTOR COUNT: 485

PROCESS: Bipolar

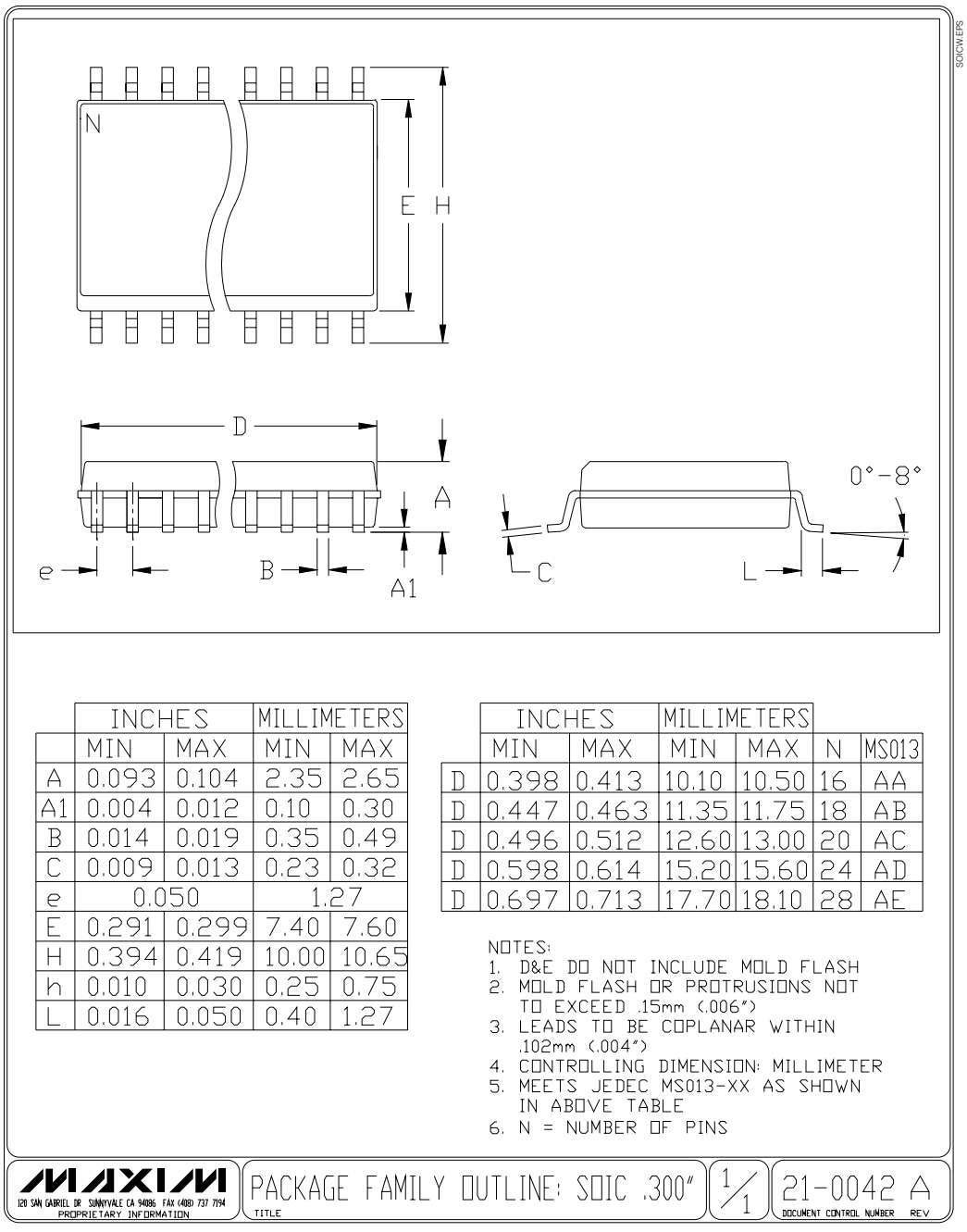
## Functional Diagram



# ECL/PECL Dual Differential 2:1 Multiplexer

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| e | 0.050 | | 1.27 | |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| h | 0.010 | 0.030 | 0.25 | 0.75 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS013 |
| D | 0.398 | 0.413 | 10.10 | 10.50 | 16 | AA |
| D | 0.447 | 0.463 | 11.35 | 11.75 | 18 | AB |
| D | 0.496 | 0.512 | 12.60 | 13.00 | 20 | AC |
| D | 0.598 | 0.614 | 15.20 | 15.60 | 24 | AD |
| D | 0.697 | 0.713 | 17.70 | 18.10 | 28 | AE |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .300" (TITLE) | 1/1 | 21-0042 A (DOCUMENT CONTROL NUMBER REV)